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PCI Development Kit, Cyclone II Edition

Getting Started User Guide



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Development Kit Version 1.0.0 PCI Development Kit, Cyclone II Edition Getting Started User Guide Altera Corporation May 2005



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About This User Guide

Revision History

The table below displays the revision history for the chapters in this User Guide.

Chapter	Date	Version	Changes Made
All	May 2005	1.0.0	First publication

How to Contact Altera

For the most up-to-date information about Altera[®] products, go to the Altera world-wide web site at www.altera.com. For technical support on this product, go to www.altera.com/mysupport. For additional information about Altera products, consult the sources shown below.

Information Type	USA & Canada	All Other Locations
Technical support	www.altera.com/mysupport/	www.altera.com/mysupport/
	(800) 800-EPLD (3753) (7:00 a.m. to 5:00 p.m. Pacific Time)	+1 408-544-8767 7:00 a.m. to 5:00 p.m. (GMT -8:00) Pacific Time
Product literature	www.altera.com	www.altera.com
Altera literature services	literature@altera.com	literature@altera.com
Non-technical customer service	(800) 767-3753	+ 1 408-544-7000 7:00 a.m. to 5:00 p.m. (GMT -8:00) Pacific Time
FTP site	ftp.altera.com	ftp.altera.com

Typographic Conventions

This document uses the typographic conventions shown below.

Visual Cue	Meaning
Bold Type with Initial Capital Letters	Command names, dialog box titles, checkbox options, and dialog box options are shown in bold, initial capital letters. Example: Save As dialog box.
bold type	External timing parameters, directory names, project names, disk drive names, filenames, filename extensions, and software utility names are shown in bold type. Examples: f _{MAX} , \qdesigns directory, d: drive, chiptrip.gdf file.
Italic Type with Initial Capital Letters	Document titles are shown in italic type with initial capital letters. Example: AN 75: High-Speed Board Design.
Italic type	Internal timing parameters and variables are shown in italic type. Examples: $t_{P A}$, $n + 1$.
	Variable names are enclosed in angle brackets (< >) and shown in italic type. Example: <i><file name="">, <project name="">.pof</project></file></i> file.
Initial Capital Letters	Keyboard keys and menu names are shown with initial capital letters. Examples: Delete key, the Options menu.
"Subheading Title"	References to sections within a document and titles of on-line help topics are shown in quotation marks. Example: "Typographic Conventions."
Courier type	Signal and port names are shown in lowercase Courier type. Examples: data1, tdi, input. Active-low signals are denoted by suffix n, e.g., resetn.
	Anything that must be typed exactly as it appears is shown in Courier type. For example: c:\qdesigns\tutorial\chiptrip.gdf. Also, sections of an actual file, such as a Report File, references to parts of files (e.g., the AHDL keyword SUBDESIGN), as well as logic function names (e.g., TRI) are shown in Courier.
1., 2., 3., and a., b., c., etc.	Numbered steps are used in a list of items when the sequence of the items is important, such as the steps listed in a procedure.
••	Bullets are used in a list of items when the sequence of the items is not important.
\checkmark	The checkmark indicates a procedure that consists of one step only.
	The hand points to information that requires special attention.
+	The angled arrow indicates you should press the Enter key.
••••	The feet direct you to more information on a particular topic.



1. About This Kit

Introduction

The PCI Development Kit, Cyclone[™] II Edition provides everything you need to develop and test a complete PCI system based on the Cyclone II device and using Altera® PCI MegaCore® functions.

This chapter briefly describes the kit's features and documentation including:

- The Cyclone II EP2C35 PCI development board
- Quartus® II Software, Development Kit Edition (DKE)
- PCI-to-DDR2 reference design
- MegaCore IP Library CD-ROM

Kit Features The PCI Development Kit, Cyclone II Edition, features:

The Cyclone II EP2C35 PCI Development Board—a prototyping platform that allows you to develop and prototype high-speed PCI and PCI-X bus interfaces, DDR2 SDRAM, and the 10/100 Ethernet interface.

For specific information about board components and interfaces, refer to the *Cyclone II EP2C35 PCI Development Board Reference Manual*.

- PCI-to-DDR2 Reference Design—This design is a 64-bit, 66-MHz, hardware verified, open-source PCI-to-DDR2 SDRAM memory reference design that uses the Altera pci_mt64 and DDR & DDR2 SDRAM Controller MegaCore functions. The design is useful for a variety of hardware applications and lets you quickly begin prototyping and verification.
- Cyclone II PCI Development Kit Application & Drivers—This open-source Windows application is an interactive platform you can use to perform PCI transactions. You can also use the kit's application as a starting point for developing your own custom software.
- PLD Applications PCI-X CORE CD-ROM—PLD Applications' PCI-X IP core is a versatile integrated solution to interface any user application or system to 32- and 64-bit PCI-X buses. The core is fully customizable; most of its features can be enabled or disabled to suit

specific design requirements. This IP core includes a complete set of tools, including reference designs and applications targeted to the Cyclone II EP2C35 PCI development board.

- Jungo WinDriver Development Toolkit—Jungo's WinDriver is a driver development toolkit that automates and simplifies the development of user mode Windows device drivers for PCI buses. WinDriver is designed to enable development of high performance, high quality user-mode device drivers, and does not require DDK knowledge or kernel-level development.
- Quartus II Software, Development Kit Edition (DKE), version 5.0—The Quartus II software provides a comprehensive environment for system-on-a-programmable-chip (SOPC) design. The Quartus II software integrates into nearly any design environment, with interfaces to industry-standard EDA tools. The kit includes:
 - The SOPC Builder system development tool
 - A one-year Quartus II DKE software license, Windows platform only
 - The Quartus II DKE software license allows you to use the product for 12 months. After 12 months, the Quartus II DKE software license expires and you must purchase another Quartus II license to continue using the Quartus II software. For more information, refer to the Altera web site at www.altera.com.
- MegaCore IP Library CD-ROM, version 5.0—This CD-ROM contains Altera IP MegaCore functions. You can evaluate the MegaCore functions using the OpenCore[®] Plus feature, which allows you to:
 - Simulate the behavior of a MegaCore function within your system
 - Verify the functionality of your design, as well as quickly and easily evaluate its size and speed
 - Generate time-limited device programming files for designs that include MegaCore functions
 - Program a device and verify your design in hardware

You only need to purchase a license for a MegaCore function when you are completely satisfied with its functionality and performance, and want to take your design to production.

The OpenCore Plus hardware evaluation feature is an evaluation tool for prototyping only. You must purchase a license to use an Altera IP function in production designs.

Documentation

The PCI Development Kit, Cyclone II Edition contains the following documents:

- Readme file—Contains special instructions for the kit and last minute additions to the documentation.
- PCI Development Kit, Cyclone II Edition Getting Started User Guide— Describes how to start using the kit (this document).
- Cyclone II EP2C35 PCI Development Board Reference Manual—Provides specific information about the board's components and interfaces, steps for using the board, and pin-outs and signal specifications
- AN 390: PCI-to-DDR2 SDRAM Reference Design—Describes the reference design that is included with the kit. The design is a typical PCI implementation of the user application that interfaces to the DDR2 Controller MegaCore function.



2. Getting Started

Introduction	The PCI Development Kit, Cyclone [™] II Edition is a complete PCI and PCI-X prototyping and testing kit, based on the Cyclone II device. With this kit, you can perform various PCI transactions between the board and the host PC, as well as configure the board with either the factory-programmed or user-programmable design.
	In addition to providing a PCI/PCI-X form factor development board, the kit also includes all of the hardware and software development tools, as well as the documentation and accessories you need to begin developing PCI systems using the Cyclone II device.
	This user guide familiarizes you with the contents of the kit and walks you through setting up a PCI development environment.
	In this guide, you will do the following:
	 Inspect the contents of the kit Install the development tools software Set up licensing Connect the cables to the board and your PC Test the board using the factory-programmed design Install the board in your PC Perform example PCI transactions Configure the Cyclone II device Use the board as a prototyping platform
Before You Begin	Before using the kit or installing the software, be sure to check the kit's contents and inspect the board to verify that you received all of the items listed below. If any of the items are missing, contact Altera [®] before you proceed. You should also verify that your computer's hardware and

software meet the kit's system requirements.

PCI Development Kit, Cyclone II Edition Contents

The PCI Development Kit, Cyclone II Edition contains the following items:

- Cyclone II EP2C35 PCI development board with an EP2C35F672 Cyclone II device (ordering code: PCI-DEVKIT-2C35)
- PCI Development Kit, Cyclone II Edition CD-ROM, version 1.0.0
 - PCI-to-DDR2 reference design
 - Cyclone II PCI development kit application and device driver
 - Board manufacturing files
- Quartus[®] II Software Development Kit Edition (DKE), version 5.0
- Jungo WinDriver Development Toolkit

The Jungo CD-ROM provides a free 30-day evaluation of Jungo's Driver Development Toolkit. For more information on the driver, refer to the documentation on the CD-ROM.

- PLD Applications PCI-X CORE CD-ROM
- MegaCore[®] IP Library CD-ROM, version 5.0, which contains the PCI Compiler and DDR & DDR2 Controller Compiler
- USB-Blaster[™] download cable and USB cable
- Power supply and three separate adapter cables for North America/Japan, Europe, and the United Kingdom

Inspect the Board

Place the board on an anti-static surface and inspect it to ensure that it has not been damaged during shipment. Verify that all components are on the board and appear intact.



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Without proper anti-static handling, the Cyclone II EP2C35 PCI development board can be damaged.



Refer to the *Cyclone II EP2C35 PCI Development Board Reference Manual* (available on the *PCI Development Kit, Cyclone II Edition CD-ROM*) for information on the board's components.

Hardware Requirements

The Cyclone II EP2C35 PCI development board is initially configured for installation in a conventional PCI slot.

You can use the Cyclone II EP2C35 PCI development board in either a 3.3- or 5.0-V PCI system and in either a 32- or 64-bit PCI bus slot. To use the board with the kit's demo application, you need a PC with an available PCI or PCI-X bus slot.

Software Requirements

To use the kit's demo application, you must have Windows XP, SP1.

You should install the following software before you begin developing designs for the kit:

- The Quartus II software version 5.0. See "Installing the Quartus II Software & MegaCore Functions" on page 2–5.
- Internet Explorer 5.0 or later to use Quartus II Help. You need a web browser to register the Quartus II software and request license files.

You need your network identification card (NIC) ID for licensing the Quartus II software.

Your NIC ID is a 12-digit hexadecimal number that identifies your computer to the computer that serves Quartus II licenses. Networked (or floating-node) licensing requires a NIC ID or server host ID. When obtaining a license file for network licensing, you should use the NIC ID from the PC that will issue the Quartus II licenses to distributed users over a network. You can find the NIC ID for your card by typing ipconfig /all at a command prompt. Your NIC ID is the number on the physical address line, without the dashes.

Quartus II System Requirements

To use the *PCI Development Kit, Cyclone II Edition CD-ROM* with the Quartus II software provided with the kit, your system must meet the Quartus II software minimum requirements.



Refer to the *Quartus II Installation & Licensing Manual for PCs* for system requirements.

Software Installation

The instructions in this section explain how to install the following:

- PCI Development Kit, Cyclone II Edition CD-ROM
- The Quartus II Software, Development Kit Edition, including MegaCore functions from the MegaCore IP Library CD-ROM

Installing the PCI Development Kit, Cyclone II Edition CD-ROM Contents

The *PCI Development Kit, Cyclone II Edition CD-ROM* contains the following items:

- PCI Development Kit, Cyclone II Edition application and drivers
- PCI-to-DDR2 reference design and configuration files
- PCI Development Kit, Cyclone II Edition Getting Started User Guide (this document)
- Cyclone II EP2C35 PCI Development Board Reference Manual
- Before you can compile the PCI-to-DDR2 reference design, you must install the MegaCore IP Library CD-ROM.
- AN 390: PCI-to-DDR2 SDRAM Reference Design
- Board manufacturing files

To install the *PCI Development Kit, Cyclone II Edition CD-ROM,* perform the following steps:

- Insert the PCI Development Kit, Cyclone II Edition CD-ROM into your CD-ROM drive and double click the cycloneii_pci_kit-v1.0.0.exe file.
- 2. Follow the online instructions to complete the installation process.

The installation program copies the PCI development kit files to your hard-disk, installs the software driver and application, and creates an icon in **Programs > Altera > MegaCore > PCI Development Kit, Cyclone II Edition v1.0.0** (Windows Start menu), which you can use to launch the Windows development kit application and view the kit's documentation.

When the installation is complete, the PCI Development Kit, Cyclone II Edition installation program creates the directory structure shown in Figure 2–1, where *<path>* is the PCI Development Kit, Cyclone II Edition CD-ROM installation directory.





Table 2–1 lists the file directory names and a description of their contents.

Table 2–1. Installed File Directory Names & Description of Contents					
Directory Name	Description of Contents				
bin	Contains the kit's demo application and device driver.				
board_manufacturing	Contains the board design and production test files. You can use the board design files as a starting point for creating your own board.				
configuration_files	Contains the configuration files for the Cyclone II EP2C35 PCI development board.				
doc	Contains the documentation related to the development kit.				
reference_design	Contains the PCI-to-DDR2 reference design files including open-source HDL, Quartus II synthesis and simulation files.				
software	Contains the source code for the kit's demo application and device driver.				

Installing the Quartus II Software & MegaCore Functions

Refer to *Installing the Quartus II Software in the Quartus II Installation & Licensing Manual for PCs* for software installation instructions. After installing the software, request and install a license to enable it. Refer to "Setting Up Licensing" for more information.

During the installation of the Quartus II software, you are given the option to install the MegaCore IP Library. When prompted to do so, choose to install the MegaCore IP Library and follow the on-screen instructions.

Setting Up Licensing

This section describes the software licensing procedures.

Licensing the PCI Development Kit, Cyclone II Edition

Before using the Quartus II software, you must obtain a license file from the Altera web site at **www.altera.com** and install the license file on your PC.

The Quartus II DKE software license allows you to use the product for 12 months. After 12 months, you must purchase a Fixed PC or FloatNet subscription.

To obtain a license, follow these steps:

- If you have a Fixed PC or FloatNet Quartus II subscription, you can use that software instead of the Quartus II DKE software. If you intend to use your existing licensed software, you can skip the instructions below to obtain the license for the Quartus II Software Development Kit Edition included in your development kit.
- 1. Select the Licensing link at the top-right corner on the home page of the Altera Web site at **www.altera.com**.
- 2. Click Cyclone II Development Kits.
- 3. Follow the instructions to request your license. Altera will e-mail you a license file that enables the software. You need your network identification card (NIC) ID and the kit serial number to license the Quartus II software.
 - Your network interface card (NIC) ID is a 12-character hexadecimal number that uniquely identifies your computer. You can find the NIC ID for your card by typing ipconfig /all at a command prompt. Your NIC ID is the number on the physical address line.

The kit serial number is an 11-digit code of the form 2C35PCXXXX where the X's represent decimal numbers. This serial number is located in three places: on the external shipping box, internal box, and Quartus II CD- ROM jacket. Refer to the serial number sticker in Figure 2–2.

Figure 2–2. Serial Number Example



The serial number is the bottom-most number, which is 2C35PCXXXXX in the above example.

- 4. After receiving your license that Altera e-mails you, close the following software applications if they are open:
 - Quartus II software
 - MAX+PLUS II software
 - LeonardoSpectrum synthesis tool
 - Synplify synthesis software
 - ModelSim simulator software
 - Precision RTL synthesis software
- 5. To install your license, refer to *Specifying the License File* in the *Quartus II Design Software Installation & Licensing for PCs* manual, which is included in the *PCI Development Kit, Cyclone II Edition*.

Licensing MegaCore Functions

You only need to purchase a license for a MegaCore function when you are completely satisfied with its functionality and performance, and want to take your design to production.

The OpenCore Plus hardware evaluation feature is an evaluation tool for prototyping only. You must purchase a license to use an Altera IP function in production designs.

For details on licensing the OpenCore Plus hardware feature, refer to the application note, *AN 320: OpenCore Plus Evaluation of Megafunctions*.

Install the Board in Your PC

You must install the Cyclone II EP2C35 PCI development board (see Figure 2–3) in your PC after you have installed the *PCI Development Kit, Cyclone II Edition CD-ROM*. To install the board in your PC, turn off your PC and install the board in an available PCI slot.

Ensure that the EPCS64 device select switch (J3) is in the *Up* position (i.e., toward the component side of the board). If the switch is not in the *Up* position, your board will not function properly.

When you power-up the PC, the Cyclone II device is configured with the default, factory-programmed design stored in flash memory. After the device is configured, the user LEDs (D1-D8) blink and the CONF DONE LED (D10) illuminates. This is a power-up indication that the board is functional and the Cyclone II device has been successfully configured.





To install the kit's driver, perform the following steps in the **Found New Hardware Wizard**:

- 1. Turn on Install the software automatically (recommended).
- 2. Click Next to go to the Completing the Found New Hardware Wizard window.
- 3. Click Finish to complete the driver installation.

This section explains how to use the kit's demo application to perform the following PCI transactions:

- PCI target write (Demo tab)
- PCI master write (Demo tab)
- Latency timer configuration register & PCI Master write (Debug tab)
- PCI master loop (Debug tab)
- Address offset and target loop (Debug tab)

PCI Target Write Transaction (Demo Tab)

In this example, the data source is the system and the destination is the PCI board. You can verify the setup in the **Command Information** section of the kit's demo application.

- Run the development kit's application by choosing Programs > Altera > Megacore > PCI Development Kit, Cyclone II Edition v1.0.0 > Cyclone II PCI Kit (Windows Start menu). The kit application opens to the Demo tab with a PCI target write transaction selected for one iteration of 2,048 bytes of random data. Leave the kit application running for the remaining examples.
- 2. Select Target Write from the Commands box.
- 3. Keep the following default values in the Address/Size box:
 - Transfer Length: 2048
 - Iterations: 1
- 4. Click **Execute** to begin operation.
- 5. Review the results in the Display Window.
- 6. In the Data Type list, select Inc Packet.
- 7. Click Execute.

Perform PCI Transactions with the Kit's Demo Application 8. Review the transaction's speed from the performance meter and the transaction's results from the **Display Window** (see Figure 2–4).

Figure 2–4. PCI Target Write Transaction (Demo Tab)

	O Master Read	C Master Write	Command Information PCI Data Command: Write Source: System
	C Target Read	 Target Write 	Destination: PCI Card
Address / Size Transfer L 2048	ength Iterations	Data Type	
)isplay Window			
Result of Tuesday, A	Target Write opera	tion Addres	64.6
Carget Per	formance Register: cycles	I⊄ Hex Ci I⊄ ASCII	Code
54 MBytes	/ second		
504 CIOCK 54 MBytes Address	Hex Data	ASCII Data	
Address 0x0000000 0x0000008 0x0000010 0x0000018 0x0000018	Hex Data 00000002 0000001 0000004 0000003 0000006 0000000 0000008 00000007 0000000a 00000009	ASCII Data	Speed (MB/S)

PCI Master Write Transaction (Demo Tab)

In this example, the data source is the PCI board and the destination is the system memory. You can verify this setup in the **Command Information** section of the kit's application.

- 1. Ensure that the **Demo** tab is active.
- 2. Select Master Write from the Commands box.
- 3. Specify the following settings in the Address/Size box:
 - Transfer Length: 4096
 - Iterations: 2
- 4. Click Execute.
- 5. Review the transaction's speed from the performance meter and the transaction's results from the **Display Window** (see Figure 2–5).

Figure 2–5. PCI Master Write Transaction (Demo Tab)

Altera Cyclone II PCI Development Ki	Application	4	
e Edit Help			
Demo Debug			
Commands		Command Information	
C Master Read	Master Write	Command: Write Source: PCI Card	
C. Target Board	C. Target I (like	Destination Costs	
() Taiyetheau	C Talget write	Destination: Syste	m
Address / Size			
Transfer Length Iterations	Data Type		
4096 2	Inc Packet 🔄		
Display Window			
Result of Master Write ope	aration 🔺 🔽 Add	ess 452.1	
Tuesday, April 26, 2005 at	16:35:48 🗖 🔽 Hex	Code	
Master Performance Registe	er: 🔽 ASC	l code	
452 MBytes / Second			
Address Hex Data	ASCII Data		
0x0000000 00000002 000000	01	Speed (MB/S)	
0x0000008 0000004 000000 0x0000010 0000006 000000	03		
0x0000018 0000008 00000	07 Exec	ute	
0x0000028 000000c 00000	оь 🗹 🗖		
۳			

Latency Timer Configuration Register (Debug Tab)

In this example, the data source is the PCI board and the destination is the system memory, employing a user-configured value for the latency timer. You can verify this setup in the Command Information section of the kit's application.

- 1. Click the **Debug** tab.
- 2. Select Master Write from the Commands box.
- 3. Keep the Address Offset setting of 0x0000000.
- 4. Keep the following values in the Address/Size box:
 - Transfer Length: 4,096
 - Iterations: 2
- 5. In the Configuration Registers list, select Lat Timer.

- The **Lat Timer** is the default value with which the system programmed the latency timer. You can return the setting to its default value after running this example.
- 6. Under Value, type 0x08 (Register Update box).
- 7. Click Write.
- 8. Click Execute.
- 9. Review the results in the **Display Window**. Compare the results with Figure 2–5, which uses the default **Lat Timer** setting of 0x40. See Figure 2–6.
- 10. Change the latency timer register back to the default value.

Figure 2–6. Latency Timer Configuration Register & PCI Master Write (Debug Tab)

Commands — C Mast C Targe	er Read ⓒ Mas et Read ⓒ Targ	ter Write jet Write	C Maste	er Loop et Loop	- Command Information - PCI Command: Write	Data Source: PCI Card Destination: System
Address / Size					Configuration Begisters	
Address Offset 0x0000000 Display Window Result of Tuesday, A	Transfer Length 4096 Master Write oper pril 26, 2005 at	Iterations 2 cation 16:38:14	Data Typ Random	Packet Address Hex Code	Lat Timer Hdr Type BIST BAR0 BAR1 BAR2 BAR3 BIR4	0x08 0x00 0x00 0xfeb00000 0xf0000008 0x0000000 0x0000000 0x0000000 0x0000000 0x0000000 0x0000000 0x0000000 v
Master Per 291 clock 111 MBytes	formance Register cycles > / Second	*:		ASCII code	DMA Registers Dma_csr Dma_par Dma_bcr	0x0019 0x151e0878 0x0000000
Address	Hex Data	ASCII D	ata		Dma_isr	0x00
0x00000000 0x0000008 0x00000010 0x0000018 0x0000020	00000002 000000 00000004 000000 00000006 000000 00000008 000000 0000000a 000000)1)3)5)7)9 	· · · · · · · · · · · · · · · · · · ·	Europa	Register Update Offset 0x0d Bytes 0x01	C Configuration C BAR0 (DMA)

PCI Master Loop (Debug Tab)

In this example, a PCI master read is followed by a PCI master write transaction. The kit's application verifies that the data read and written by the master is the same.

- 1. Ensure that the **Debug** tab is active.
- 2. Select Master Loop from the Commands box.
- 3. Keep the Address Offset setting of 0x0000000.
- 4. Specify the following settings in the Address/Size box:
 - Transfer Length: 4096
 - Iterations: 2
- 5. In the Data Type list, select AA55 Packet.
- 6. Click Execute.
- 7. Review the results in the **Display Window** (see Figure 2–7).

Figure 2–7. PCI Master Loop (Debug Tab)

Commands	Master Loop Target Loop	Command Information	Data
C Master Read C Master Write		PCI	Source: System
C Target Read C Target Write		Command: Read/Write	Destination: PCI Card
Address / Size Address / Size Address Offset Transfer Length Iterations (0x0000000 4096 2 Display Window Result of Master Read operation Master Performance Register: 513 clock cycles S3 MBytes / Second Result of Master Vite operation Master Performance Register: 72 clock cycles 452 MBytes / Second	Data Type Ad55 Packet Address V Address V Address V Address V Address V Address V Address	Configuration Registers Vend ID Dev ID Command Status Rev ID Prog If Sub Class Dua_csr Dma_csr Dma_bcr Dma_isr - Register Update	0x1172 0x0009 0x0117 0x0420 0x01 0x00 0x00 0x0019 0x0019 0x0019 0x0019 0x0010e2980 0x000 0x00
Address Sent Data Received Dat.	a	Offset 0x0d	Configuration BAR0 (DMA) Read Write
Dx0000000 aa55aa55 .U.U aa55aa55 .U.	U V Execute	Bytes 0x01	

Address Offset & Target Loop (Debug Tab)

In this example, a target loop/target write transaction is followed by a target read. The address offset changes the transaction's starting address.

- 1. Ensure that the **Debug** tab is active.
- 2. Select **Target Loop** from the **Commands** box.
- 3. In the Address Offset box, type 0x0000028.
- 4. Keep the following values in the Address/Size box:
 - Transfer Length: 4096
 - Iterations: 2
- 5. In the **Data Type** list, select **Inc Packet**.
- 6. Click Execute.
- 7. Review the starting address of the data transaction in the **Display Window** (Figure 2–8).

Figure 2–8. Address Offset & Target Loop (Debug Tab)

Edit Help		
emo Debug		
Commands C Master Read C Master Write C Target Read C Target Write	C Master Loop	Command Information PCI Command: Write/Read Destination: System
Address / Size Address / Size Address Offset Transfer Length Iterations [0x000028] 4096 [2] Display Window Result of Target Write operation Target Performance Register: 54 MBytes / Second Result of Target Read operation Target Performance Register: 1752 clock cycles 54 MBytes / Second	Data Type Inc Packet	Configuration Registers Vend ID 0x1072 Dev ID 0x0009 Command 0x0117 Status 0x0420 Rev ID 0x01 Prog If 0x00 Sub Class 0x00 DMA Registers DMA Registers Dma_par 0x0f0e2980 Dma_isr 0x00
Address Sent Data Received Data	Execute	Register Update Configuration Offset 0x0d C Configuration Bytes 0x01 C BAR0 (DMA) Value 0x40 Read Write

Configuring the Cyclone II Device

The on-board Cyclone II device can be configured in one of two ways:

- Serial flash configuration
- JTAG configuration

Serial Flash Configuration

The Cyclone II FPGAs use SRAM cells to store configuration data. Because SRAM memory is volatile, configuration data must be downloaded to the Cyclone FPGAs each time power is applied to the board.

The board has a non-volatile configuration scheme that automatically configures the Cyclone II device with either a user-programmable or factory-programmed default design. A switch (J3) is used to select either the user-programmable or the factory-programmed EPCS64 device.

If the switch (J3) is not in the *Down* position (toward the back of the board), you will erase the factory-programmed default design. Refer to "Restoring the Factory-Programmed Design" on page 2–18.

Configuration via User-Programmable Flash Memory

Upon power-up, the configuration circuit (comprised of the selected EPCS64 device) configures the Cyclone II device. If the switch (J3) is set for user configuration (*Down* position), the circuit attempts to load the user design. If the load is not successful, the CONF_DONE LED (D10) does not illuminate and the Cyclone II device is not configured. If the load is successful, the CONF_DONE LED illuminates.

Configuration via Factory-Programmed Design

Assuming the board is installed in a PCI slot, when the factoryprogrammed design is loaded into the Cyclone II device, the user LEDs blink and the CONF_DONE LED illuminates. To select the factory default design, set the switch (J3) to the *Up* position.

JTAG Configuration

The Cyclone II device can be configured after power is applied to the board. The JTAG interface permits the Quartus II software to load the Cyclone II device with a user design through the Altera USB-Blaster download cable. The user design remains in the Cyclone II device until power is removed from the board.