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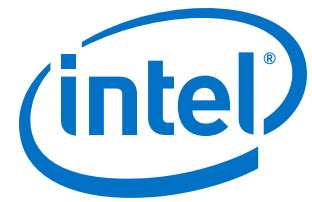

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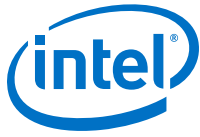
Intel® Stratix® 10 GX Transceiver Signal Integrity Development Kit User Guide

UG-20047
2017.10.11

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Contents

1 Overview

1.1 General Board Description

The Intel® Intel Stratix® 10 GX Transceiver Signal Integrity Development Kit is a complete design environment that includes both hardware and software you need to develop Intel Stratix 10 GX FPGA designs.

The following list describes what you can accomplish with the kit:

- Evaluate transceiver performance up to 17.4 Gbps for L-Tile and 28.3 Gbps for H-Tile version.
- Generate and check pseudo-random binary sequence (PRBS) patterns
- Dynamically change differential output voltage (VOD) pre-emphasis and equalization settings to optimize transceiver performance for your channel
- Perform jitter analysis
- Verify physical medium attachment (PMA) compliance to PCI Express* (PCIe*), 1G/10G/40G/100G Ethernet and other major standards.

Related Links

Stratix 10 Support

1.2 Recommended Operating Conditions

The recommended operating conditions for this development kit are:

- Recommended ambient operating temperature range: 0C to 45C
- Maximum ICC load current: 130 A
- Maximum ICC load transient percentage: 30%
- FPGA maximum power supported by the supplied heatsink/fan: 200 W

1.3 Handling the Development Board

When handling the board, it is important to observe static discharge precautions.

Caution: Without proper anti-static handling, the board can be damaged. Therefore, use anti-static handling precautions when touching the board.

Caution: This development kit should not be operated in a Vibration Environment.

2 Getting Started

2.1 Installing the Quartus Prime software

The Intel Quartus® Prime design software is a multiplatform design environment that easily adapts to your specific needs in all phases of FPGA, CPLD, and SoC designs. The Intel Quartus Prime software delivers the highest performance and productivity for Intel FPGAs, CPLDs, and SoCs.

Design software must enable dramatically increased design productivity in order to take advantage of devices with multi-million logic elements with increased capabilities that provide designers with an ideal platform to meet next-generation design opportunities.

The new Intel Quartus Prime Design Suite® design software includes everything needed to design for Intel FPGAs, SoCs and CPLDs from design entry and synthesis to optimization, verification and simulation. The Intel Quartus Prime Design Suite software includes an additional Spectra-Q® engine that is optimized for Intel Stratix 10 and future devices. The Spectra-Q engine enables new levels of design productivity for next generation programmable devices with a set of faster and more scalable algorithms, a hierarchical database infrastructure and a unified compiler technology.

Intel Quartus Prime Pro Edition

The Intel Quartus Prime Design Suite software is available in three editions based on specific design requirements: Pro, Standard, and Lite Edition.

The Intel Quartus Prime Pro Edition is optimized to support the advanced features in Intel's next generation FPGAs and SoCs and requires a paid license.

Included in the Intel Quartus Prime Pro Edition are the Intel Quartus Prime software, Nios® II EDS and the MegaCore IP Library.

To install Intel's development tools, download the Intel Quartus Prime Pro Edition software from the Quartus Prime Pro Edition page in the Download Center of Intel's website.

2.2 Installing the Development Board

To install the Intel Stratix 10 GX Transceiver Signal Integrity Development Board, perform the following steps:

1. Download the development kit installer from the Stratix 10 GX Transceiver Signal Integrity Development Kit link on the Intel website.

2. Unzip the Intel Stratix 10 Transceiver Signal Integrity Development Kit installer package.

3. The installer package creates the development kit directory structure shown in the figure below.

Figure 1.   Development Kit Directory Structure
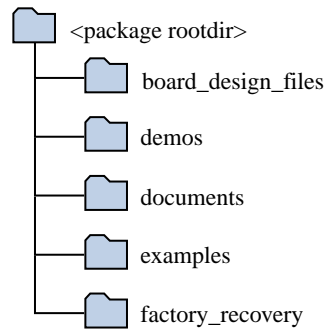
The table below lists the file directory names and a description of their contents

Table 1.   Installed Development Kit Directory Structure

File Directory Name	Description of Directory Contents
board_design_files	Contains schematics, layout, assembly and bill of material board design files. Use these files as a starting point for a new prototype board design
demos	Contains demonstration applications when available
documents	Contains the development kit documentation
examples	Contains the sample design files for the development kit
factory_recovery	Contains the original data programmed onto the board before shipment. Use this data to restore the board with its original factory contents.

2.3 Installing the Intel FPGA Download Cable Driver

The Intel Stratix 10 GX Transceiver Signal Integrity Development Kit includes embedded Intel FPGA Download Cable circuits for FPGA and MAX® V programming. However, for the host computer and board to communicate, you must install the Intel FPGA Download Cable driver on the host computer.

Installation instructions for the Intel FPGA Download Cable driver for your operating system are available on the Intel website.

On the Intel website, navigate to the Cable and Adapter Drivers Information link to locate the table entry for your configuration and click the link to access the instructions.
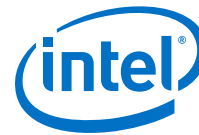
3 Development Board Setup

The instructions in this chapter explain how to setup the Intel Stratix 10 GX Transceiver Signal Integrity Development Board.

3.1 Setting up the Development Board

To prepare and apply power to the board, perform the following steps:

1. The Intel Stratix 10 GX transceiver signal integrity development kit ships with its board switches preconfigured to support the design examples in the kit. If you suspect your board might not be correctly configured with the default settings, follow the instructions in the Factory Default Switch and Jumper Settings on page 8 to return the board to its factory settings before proceeding.

2. The development kit ships with design examples stored in the flash device. The POWER-ON slide switch (SW7) is provided to turn the board **ON** or **OFF**.

    Caution: When the power cord is plugged into connector **J103** of the Intel Stratix 10 transceiver signal integrity development kit, 12V_IN and 3.3V_STBY are present on to the board with switch **SW7** in the '**OFF**' position. These voltages are restricted to a small area of the board. When switch **SW7** is placed to '**ON**' position, all voltages planes have power at this point.

3. Set the POWER-ON switch **SW7** to the **ON** position. When power is supplied to the board, three green LEDs (**D29**, **D31** and **D32**) illuminate and an amber LED (**D36**) extinguishes indicating that the board has power. If the amber LED (**D36**) illuminates, it indicates that one or more power supply is incorrect.

4. **RESET** button (S12) is connected to the MAX V CPLD (MAX_RESETn pin) that is used for AvST configuration. When this button is pressed, the MAX V CPLD initiates a reloading of the stored image from the flash memory using AvST configuration mode. The image loaded right after power cycle or MAX V reset depends on FACTORY_LOAD settings.

    *   **OFF(1)** - factory load

    *   **ON (0)** - user defined load #1

    Page selection can be changed by the PGMSEL button (S10) when the board is powered on, and PGM_CONFIG (S11) is used to reconfigure FPGA with corresponding page which is indicated by PGM_LED0, PGM_LED1 or PGM_LED2.

    Caution: Use only the supplied power supply. Power regulation circuits on the board can get damaged by power supplies with greater voltage.

The MAX V CPLD device on the board contains a parallel flash loader II (PFL II) megafunction. After a POWER-ON or RESET (reconfiguration) event, the MAX V CPLD configures the Intel Stratix 10 FPGA in AvST mode with either factory design or user design depending on the setting of FACTORY_LOAD.

The development kit includes a MAX V CPLD design which contains the PFL II megafunction. The design resides in the `<package dir>\examples\max5` directory. When configuration is complete, **LED D25** (`CONF_DONE`) illumintes signaling that the Intel Stratix 10 GX FPGA device is configured successfully. If the configuration fails, the **LED D23** (`ERROR`) illuminates.

3.2 Factory Default Switch and Jumper Settings

This section shows the factory switch settings for the Intel Stratix 10 GX transceiver signal integrity development kit.

Table 2.   Factory Default Switch Settings

Switch	Board Label	Default Position	Function
SW10	`MSEL1`	2-3 Closed	MSEL setting=0
	`MSEL2`	5-6 Closed	MSEL setting=0
SW11	`MSEL0`	2-3 Closed	MSEL setting=0
SW3-1	Intel Stratix 10	OPEN/OFF	Enable Intel Stratix 10 in JTAG Chain
SW3-2	`MAX V`	OPEN/OFF	Enable MAX V in JTAG chain
SW3-3	`FMC A`	CLOSE/ON	Bypass FMC A in JTAG chain
SW3-4	`FMC B`	CLOSE/ON	Bypass FMC B in JTAG chain
S15-1	`OFF = OSC`	OPEN/OFF	Select Si570 clock source for U3
S15-2	`ON = SMA`	OPEN/OFF	Select Si570 clock source for U4
SW1-1	`S0`	OPEN/OFF	Frequency Select
SW1-2	`S1`	CLOSE/ON	Frequency Select
SW1-3	`SS0`	OPEN/OFF	Spread Spectrum Select
SW1-4	`SS1`	OPEN/OFF	Spread Spectrum Select
SW2-1	`OFF=ISOLATE`	CLOSE/ON	U15 (LTC2987) is enabled in I^{2}C topology
SW2-2	`ON=FULL CHAIN`	CLOSE/ON	U15 (LTC2987) is enabled in I^{2}C topology
S1-1	`OFF=ISOLATE`	CLOSE/ON	U5 and U6 (Si5341) is enabled in I^{2}C topology
S1-2	`ON=FULL CHAIN`	CLOSE/ON	U5 and U6 (Si5341) is enabled in I^{2}C topology
S14-1	`VCCT`	OPEN/OFF	Enable on-board `VCCT` regulator
S14-2	`VCCH`	OPEN/OFF	Enable on-board `VCCH` regulator
SW9-1	`VCCRR`	OPEN/OFF	Enable on-board `VCCRR` regulator
SW9-2	`VCCRL`	OPEN/OFF	Enable on-board `VCCRL` regulator

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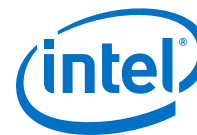
Switch	Board Label	Default Position	Function
SW9-3	`VCCERAM`	OPEN/OFF	Enable on-board `VCCERAM` regulator
SW9-4	`VCC`	OPEN/OFF	Enable on-board `VCC` regulator
SW8-1	`MAX10_DIPSWITCH`	OPEN/OFF	Power Intel MAX 10 user DIP Switch
SW8-2	`FAN_ON`	OPEN/OFF	FAN is not full speed
SW8-3	`PWR_MGMT_SEL`	OPEN/OFF	Select Linear Tech PWR MGMT solution
SW8-4	`MAX10_BOOTSEL`	OPEN/OFF	Power Intel MAX 10 boot select
SW6-1	`FACTORY_LOAD`	OPEN/OFF	Factory Load Control
SW6-2	`MAX5_SWITCH2`	OPEN/OFF	MAX V user DIPSwitch
SW6-3	`MAX5_SWITCH0`	OPEN/OFF	MAX V user DIPSwitch
SW6-4	`MAX5_SWITCH1`	OPEN/OFF	MAX V user DIPSwitch
SW4-1	`S10_UNLOCK`	OPEN/OFF	Stratix 10 User DIPSwitch
SW4-2	`USER_DIP6`	OPEN/OFF	Stratix 10 User DIPSwitch
SW4-3	`USER_DIP5`	OPEN/OFF	Stratix 10 User DIPSwitch
SW4-4	`USER_DIP4`	OPEN/OFF	Stratix 10 User DIPSwitch
SW5-1	`USER_DIP3`	OPEN/OFF	Stratix 10 User DIPSwitch
SW5-2	`USER_DIP2`	OPEN/OFF	Stratix 10 User DIPSwitch
SW5-3	`USER_DIP1`	OPEN/OFF	Stratix 10 User DIPSwitch
SW5-4	`USER_DIP0`	OPEN/OFF	Stratix 10 User DIPSwitch
SW7	`SW7`	OFF	On-board power switch

Figure 2.   Default Switch Settings

Board size = 10" x11"

4 Board Components

4.1 Board Overview

This section provides an overview of the Intel Stratix 10 GX transceiver signal integrity development board including a block diagram of the board.

Figure 3. **Stratix 10 GX Transceiver Signal Integrity Development Kit User Guide Block Diagram**
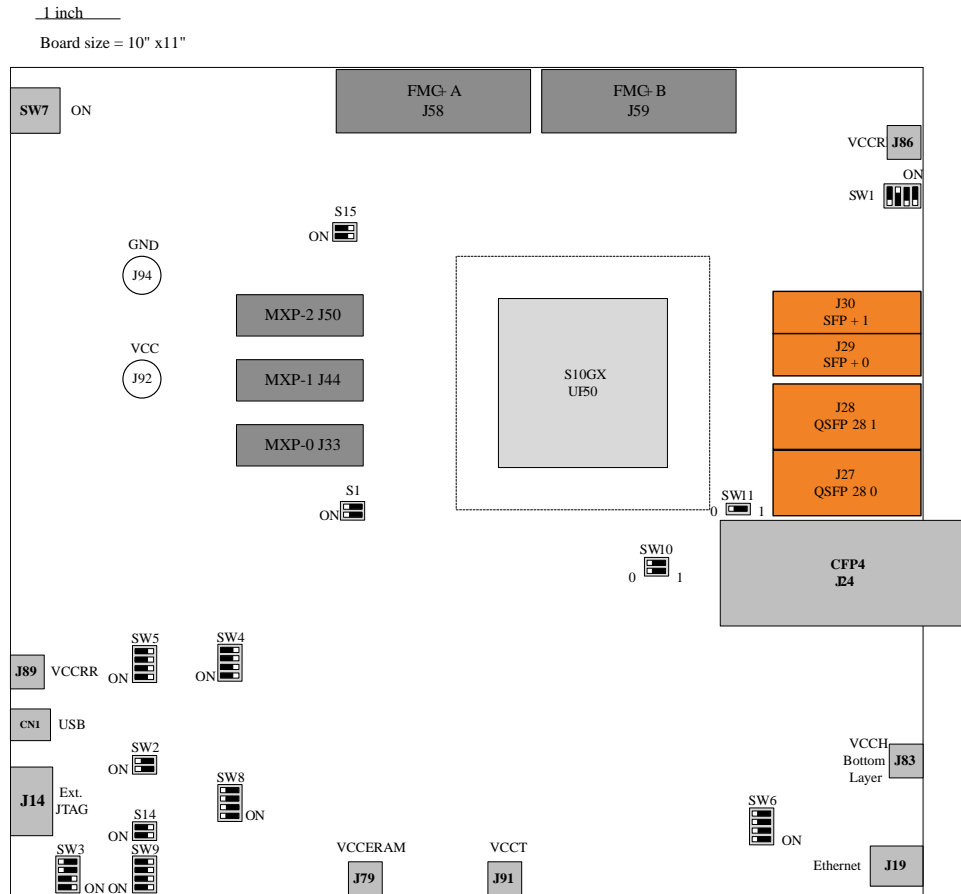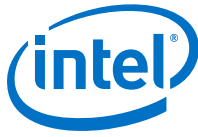
Intel Stratix 10 GX Transceiver Signal Integrity Development Board Components

Table 3. **Board Components Table**

Board Reference	Type	Description
Featured Devices		
U43	FPGA	Intel Stratix 10 GX 280 F2397 FPGA
U20	CPLD	System MAX V CPLD (5M2210ZF256)
U97	FPGA	USB Intel MAX 10 FPGA (10M04SCU169)
U98	FPGA	PWR Intel MAX 10 FPGA (10M16SAU169)
General User Input and Output		
D12-D19	User LEDs (Green)	User LEDs (Green)
D20-D25	MAX V LEDs (Green)	MAX V LEDs (Green)
S2-S13	User Push Buttons	User Push Buttons
SW4-SW5	User DIP Switches	User DIP
SW6	MAX V DIP Switch	MAX V DIP Switch
J20	LCD Display Header	Connector for 16 Character x2 line LCD
Configuration, Status and Setup Elements		
J14	Intel FPGA Download Cable Programming Header	Header to interface external Intel FPGA Download Cable direct to FPGA (through USB Intel MAX 10)
D1-D2	Green LEDs	JTAG Transmit-Receive Activity
D3-D4	Green LEDs	System Console Transmit-Receive Activity
D36	Amber LEDs	System Power error indicator
D5-D6	Green LEDs	FMC cards present indicator
D7-D11	Ethernet LEDs	Ethernet LEDs (TX/RX/LINK)
Clock Circuits		
X2	50-MHz Oscillator	This 50-MHz oscillator is the clock source to clock buffer SL18860DC that provides three 50 MHz outputs to the FPGA and the MAX V CPLD
X1		This 50-MHz oscillator provides clock to the PWR Intel MAX 10 FPGA
SW1	Spread Spectrum/Frequency Selection Switch	SW1 selects frequency and spread spectrum percentages of clock buffer outputs ICS557-03.
Y1	Transceiver Dedicated Reference Clock/ Programmable Oscillator	Feeds REFCLKs on left side of the Intel Stratix 10 GX FPGA device and an LVDS trigger output at board reference J4/J5. The external input is available at board reference J2 and J3. The default frequency is 644.53125 MHz.

continued...

Board Reference	Type	Description
Y2		Feeds `REFCLK`s on right side of the Intel Stratix 10 GX FPGA device and an LVDS trigger output at board reference J8/J9. The external input is available at board reference J6 and J7. The default frequency is 706.25 MHz.
U3, U4, U5	Transceiver Dedicated Reference Clock/ Programmable PLL	Feeds `REFCLK`s on left side of the Intel Stratix 10 GX FPGA device and an LVDS trigger output at board reference J10/J11. The default frequencies are 625 MHz, 614.4 MHz, 100 MHz.
U6		Feeds `REFCLK`s on right side of the Intel Stratix 10 GX FPGA device and an LVDS trigger output at board reference J12/J13. The default frequencies are 625 MHz, 644.53125 MHz, 125 MHz.
J61, J63	External core clock input	SMA external input at `CLKIN_3C0`
J62, J64	External core clock output	SMA external output at `PLL_3C_CLKOUT0`
J65-J66		SMA external input bank at 1C
J67-J68	External transceiver clock input	SMA external input bank at 1M
J69-J70		SMA external input bank at 4C
J71-J72		SMA external input bank at 4K
X4	100-MHz Oscillator	This 100-MHz oscillator provides clock to the MAX V CPLD
Transceiver Interfaces		
J33, J44, J50	MXP connector	17 Gbps/28 Gbps, 4 channels MXP connectors
J31-J32 J34-J43 J45-J49 J51-J57	2.4 mm RF connector	17 Gbps/ 28 Gbps, 6 channels 2.4 mm RF connectors
J29-J30	SFP+ optical transceiver interface	17 Gbps/28 Gbps, 2 channels connected to SFP+ modules
J27-J28	QSFP28 optical transceiver interface	17 Gbps/28 Gbps, 8 channels connected to QSFP28 modules
J24	CFP4 optical transceiver interface	17 Gbps/ 28 Gbps, 4 channels connected to CFP4 module
J58-J59	FMC+ connector	17 Gbps/28 Gbps, 34 channels connected to FMC+ connectors
Memory Devices		
U21-U22	Flash Memory	Two 1-Gbit Micron PC28F00AP30BF CFI Flash device
Communication Ports		

continued...

Board Reference	Type	Description
J19	Gigabit Ethernet Port	RJ-45 connector which provides a 10/100/1000 Ethernet connection through a Marvell 88E1111 PHY
CN1	USB Type-B connector	Connects a type-B USB cable
Power Supply		
U15	LTM2987	Linear Technology power monitor device
U63-U64 U66-U67	LTM4677 3x LTM4650	Power regulators for VCC rail
U68	LTM4620	Power regulators for VCCERAM rail
U69	LTM4620	Power regulators for VCCH rail
U70	LTM4620	Power regulators for VCCRL rail
U71	LTM4620	Power regulators for VCCRR rail
U74	EN63A0	Power regulators for FMCA_VADJ rail
U78	EN63A0	Power regulators for FMCB_VADJ rail
U79	EN6337	Power regulators for 2.5V rail
U82	LTM4630A	Power regulators for 3.3V rail

4.2 Stratix 10 GX FPGA

The development board features the Intel Stratix 10 GX FPGA (1SG280UF50).

Intel Stratix 10 GX FPGA I/O Usage Summary

Table 4.   Stratix 10 GX FPGA Pin Table

Signal Name/Function	I/O Count	Description
Configuration		
S10_JTAG_TCK/TDO/TDI/TMS	4	JTAG Configuration Pins
FPGA_MSEL[2:0]	2	Configuration input pins to set configuration scheme
FPGA_CONF_DONE	1	Configuration done pin
FPGA_nSTATUS	1	Configuration status pin
FPGA_INIT_DONE	1	Configuration pin to signify user mode
FPGAMSEL0	1	Configuration input pins to set configuration scheme and Chip select pin to EPCQL device
FPGA_nCONFIG	1	Configuration input pin to reset FPGA
FPGA_OSC_CLK_1	1	125 MHz Clock
FPGA_AS_CLK	1	Configuration Clock for AS configuration schemes
CPU_RESETn	1	Global reset signal

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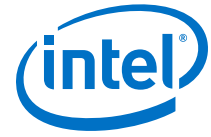
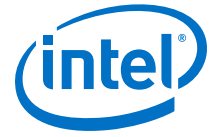| Signal Name/Function	I/O Count	Description
FPGA_CONFIG_D[31:0]	32	Configuration input pin that enables all IOs
FPGA_AS_DATA[3:0]	4	EPCQL data bus
FPGA_AVST_READY	1	SDM ready for AvST configuration scheme
FPGA_AVST_VALID	1	Data valid for AvST configuration scheme
FPGA_AVST_CLK	1	Configuration clock for AvST configuration scheme
FPGA_PR_DONE	1	Partial reconfiguration done pin
FPGA_PR_REQUEST	1	Partial reconfiguration request pin
FPGA_PR_ERROR	1	Partial reconfiguration error pin
NPERSTL, NPERSTR	4	Reset pin for PCIe HIP
FPGA_SDM10	1	SDM IO 10
FPGA_CvP_DONE	1	CvP configuration done pin
FPGA_SEU_ERR	1	SEU error indicate pin
VCC_SDA/VCC_SCL	2	SmartVID PMBus
VCC_ALERTn	1	SmartVID PMBus
Transceivers		
SFP0_TX_DS	1	SFP+ 0 TX disable control Pin
SFP0_RS[1:0]	2	SFP+ 0 Rate Select Control Pin
SFP0_MOD_ABS	1	SFP+ 0 Module Absent Status Pin
SFP0_RX_LOS	1	SFP+ 0
SFP0_TX_FLT	1	SFP+ 0 Transmitter Fault Status Pin
SFP0_SCL	1	SFP+ 0 Management Data Clock
SFP0_SDA	1	SFP+ 0 Management Data I/O Bi-Directional Data
SFP1_TX_DIS	1	SFP+ 1 TX disable control pin
SFP1_RS[1:0]	2	SFP+ 1 Rate Select Control Pin
SFP1_MOD_ABS	1	SFP+ 1 Module Absent Status Pin
SFP1_RX_LOS	1	SFP+ 1
SFP1_TX_FLT	1	SFP+ 1 Transmitter Fault Status Pin
SFP1_SCL	1	SFP+ 1 Management Data Clock
SFP1_SDA	1	SFP+ 1 Management Data I/O Bi-Directional Data
CFP4_MOD_LOPWR	1	CFP4 Module Low Power Mode
CFP4_MOD_RSTn	1	CFP4 Module Reset
CFP4_GLB_ALRMN	1	CFP4 Program Alarm bits

continued...

Signal Name/Function	I/O Count	Description
CFP4_PRTADR[2:0]	3	CFP4 MDIO Physical Port Address
CFP4_TX_DIS	1	CFP4 Transmitter Disable
CFP4_RX_LOS	1	CFP4 Receiver loss of signal
CFP4_MOD_ABS	1	CFP4 Module Absent
CFP4_MDC	1	CFP4 Management Data Clock
CFP4_MDIO	1	CFP4 Management Data I/O Bi-Directional Data
eQSFP_modselL0	1	QSFP28 0 model select
eQSFP_resetL0	1	QSFP28 0 Module Reset
eQSFP_LPmode0	1	QSFP28 0 Module Low Power Mode
eQSFP_modprsL0	1	QSFP28 0 Module Present
eQSFP_intl0	1	QSFP28 0 Module Interrupt
eQSFP_scl0	1	QSFP28 0 Management Data Clock
eQSFP_sda0	1	QSFP28 0 Management Data I/O Bi-Directional Data
eQSFP_modselL1	1	QSFP28 1 model select
eQSFP_resetL1	1	QSFP28 1 Module Reset
eQSFP_LPmode1	1	QSFP28 1 Module Low Power Mode
eQSFP_modprsL1	1	QSFP28 1 Module Present
eQSFP_intl1	1	QSFP28 1 Module Interrupt
eQSFP_scl1	1	QSFP28 1 Management Data Clock
eQSFP_sda1	1	QSFP28 1 Management Data I/O Bi-Directional Data
FALAp/n[33:0]	68	FMC A LA bank GPIOs
FAHAp/n[23:0]	48	FMC A HA bank GPIOs
FAHBp/n[21:0]	44	FMC A HB bank GPIOs
RZQ_2M	1	RZQ pin for bank 2M
RZQ_3K	1	RZQ pin for bank 3K
EXTA_SDA1V8	1	FMC A I^{2}C bus
EXTA_SCL1V8	1	FMC A I^{2}C bus
FAPRSNT1V8_N	1	FMC A present indicator
FACLKBIR1V8	1	FMC A clock direction control
FBLAp/n[33:0]	68	FMC B LA bank GPIOs
EXTB_SDA1V8	1	FMC B I^{2}C bus
EXTB_SCL1V8	1	FMC I^{2}C bus
FBPRSTN1V8_N	1	FMC B present indicator

continued...

Signal Name/Function	I/O Count	Description
USB		
USB_FULL	1	USB FIFO is full
USB_EMPTY	1	USB FIFO is empty
USB_RESETn	1	USB Reset
USB_OEn	1	USB Output Enable
USB_RDn	1	USB Read
USB_WRn	1	USB Write
USB_DATA[7:0]	8	USB Data Bus
USB_ADDR[1:0]	2	USB Address Bus
USB_SCL	1	USB Serial Clock
USB_SDA	1	USB Serial Data
Flash Memory		
FM_D[31:0]	32	Flash Data Bus
FM_A[26:1]	26	Flash Address Bus
FLASH_WEn	1	Flash Write Enable Strobe
FLASH_CEn0	1	Flash Chip Enable
FLASH_CEn1	1	Flash Chip Enable
FLASH_OEn	1	Flash Output Enable
FLASH_RDYBSYn0	1	Flash ready or busy
FLASH_RDYBSYn1	1	Flash ready or busy
FLASH_RESETn	1	Flash reset
FLASH_CLK	1	Flash clock
FLASH_ADVn	1	Flash address valid
MAX V CPLD		
MAX5_OEn	1	Output Enable
MAX5_CSn	1	Chip Select
MAX5_WEn	1	Write Enable
MAX5_CLK	1	Clock
MAX5_BEn[3:0]	4	Byte Enable
Switches, Buttons, LED		
USER_LED[7:0]	8	Light Emitting Diodes
USER_PB[7:0]	8	Push Buttons
USER_DIP[6:0]	7	DIP Switches
USER_IO[9:0]	10	Input/Output

continued...

Signal Name/Function	I/O Count	Description
S10_UNLOCK	1	FPGA Unlock Switch
Ethernet		
ENET_SGMII_TX_P/N	2	Ethernet SGMII Transmit Data
ENET_SGMII_RX_P/N	2	Ethernet SGMII Receive Data
ENET_RSTn	1	Reset
ENET_INTn	1	Interrupt
ENET_MDIO	1	Ethernet Management Data I/O
ENET_MDC	1	Ethernet Management Data Clock
Other Bus		
SPARE[20:1]	20	Spare bus between Intel Stratix 10 and MAX V
I2C_1V8_SCL	1	Intel Stratix 10 I^{2}C bus
I2C_1V8_SDA	1	Intel Stratix 10 I^{2}C bus
Temperature		
OVERTEMPn	1	Intel Stratix 10 over temperature indicator
TEMP_ALERTn	1	Intel Stratix 10 temperature alert indicator
Global Clocks		
CLK_50M_S10	1	50 MHz Global Clock Input
CLK_S10BOT_100M_p/n	2	100 MHz differential core clock for bottom banks
CLKIN_SMA_3C_p/n	2	Global Clock input from SMA
CLKOUT_SMA_3C_p/n	2	Dedicated Clock output to SMA
USB_FPGA_CLK	1	USB FPGA Clock
CLK_S10TOP_ADJ_p/n	2	Adjustable differential core clock for top banks
CLK_S10TOP_125M_p/n	2	125 MHz differential core clock for top banks
FACLKM2Cp/n0	2	FMC A clock input 0
FACLKM2Cp/n1	2	FMC A clock input 1
FBCLKM2Cp/n0	2	FMC B clock input 0
FBCLKM2Cp/n1	2	FMC B clock input 1
FACLKBIDIRp/n2	2	FMC A bidirectional clock 2
FACLKBIDIRp/n3	2	FMC A bidirectional clock 3
Transceiver Clocks		
		continued...

Signal Name/Function	I/O Count	Description
CLK_CFP4_644_p/n	2	Differential top REFCLK input to the transceiver bank 1C
CLKIN_SMA_1C_p/n	2	Differential bottom REFCLK input to the transceiver bank 1C
CLK_QSFP0_644MT_p/n	2	Differential top REFCLK input to the transceiver bank 1D
CLK_QSFP0_644MB_p/n	2	Differential bottomREFCLK input to the transceiver bank 1D
CLK_GXBL1E_614MT_p/n	2	Differential top REFCLK input to the transceiver bank 1E
CLK_GXBL1E_614MB_p/n	2	Differential bottom REFCLK input to the transceiver bank 1E
CLK_GXBL1F_625M_p/n	2	Differential top REFCLK input to the transceiver bank 1F
CLK_SFP_644M_p/n	2	Differential top REFCLK input to the transceiver bank 1K
CLK_GXBL1K_614M_p/n	2	Differential bottom REFCLK input to the transceiver bank 1K
CLK_GXBK1L_625M_p/n	2	Differential top REFCLK input to the transceiver bank 1L
FBGBTCLKM2_Cp/n0	2	Differential top REFCLK input to the transceiver bank 1M
CLKIN_SMA_1M_p/n	2	Differential bottomREFCLK input to the transceiver bank 1M
CLK_FMCB_644M_p/n	2	Differential top REFCLK input to the transceiver bank 1N
FBGBTCLKM2_Cp/n1	2	Differential bottom REFCLK input to the transceiver bank 1N
CLK_SMA_706M_p/n	2	Differential top REFCLK input to the transceiver bank 4C
CLKIN_SMA_4C_p/n	2	Differential bottomREFCLK input to the transceiver bank 4C
CLK_MXP1_706M_p/n	2	Differential top REFCLK input to the transceiver bank 4D
CLK_GXBR4D_644M_p/n	2	Differential bottom REFCLK input to the transceiver bank 4D
CLK_MXP2_706M_p/n	2	Differential top REFCLK input to the transceiver bank 4E
CLK_GXBR4E_644M_p/n	2	Differential bottom REFCLK input to the transceiver bank 4E
CLK_MXP3_706M_p/n	2	Differential top REFCLK input to the transceiver bank 4F
CLK_GXB4F_644M_p/n	2	Differential bottomREFCLK input to the transceiver bank 4F
FAGBTCLKM2_Cp/n0	2	Differential top REFCLK input to the transceiver bank 4K

continued...

Signal Name/Function	I/O Count	Description
`CLKIN_SMA_4K_p/n`	2	Differential bottom `REFCLK` input to the transceiver bank 4K
`FAGBTCLKM2_Cp/n1`	2	Differential top `REFCLK` input to the transceiver bank 4L
`CLK_GXBR4L_644M_p/n`	2	Differential bottom `REFCLK` input to the transceiver bank 4L
`FAGBTCLKM2_Cp/n2`	2	Differential top `REFCLK` input to the transceiver bank 4M
`CLK_GXBR4M_625M_p/n`	2	Differential bottom`REFCLK` input to the transceiver bank 4M
`FAGBTCLKM2_Cp/n3`	2	Differential top `REFCLK` input to the transceiver bank 4N
`CLK_FMCA_706M_p/n`	2	Differential bottom`REFCLK` input to the transceiver bank 4N

4.3 MAX V CPLD System Controller

The Intel Stratix 10 GX transceiver signal integrity development kit consists of a MAX V CPLD (5M2210Z-F256), 256-pin FineLine BGA package. MAX V CPLD devices provide programmable solutions for applications such as FPGA reconfiguration from flash memory, I^2C chain to manage power consumption, core temperature, fan speed, clock frequency and remote update system. MAX V devices feature on-chip flash storage, internal oscillator and memory functionality. With up to 50% lower total power versus other CPLDs and requiring as few as one power supply, MAX V CPLDs can help you meet your low power design requirements.

The following list summarizes the features of MAX V CPLD devices:

- 2210 Logic Elements (LEs)
- 8192 bits of User Flash Memory
- 4 global clocks
- 1 internal oscillator
- 271 maximum user I/O pins
- Low-cost, low power and non-volatile CPLD architecture
- Fast propagation delays and clock-to-output times
- Single 1.8V external supply for device core
- Bus-friendly architecture including programmable slew rate, drive strength, bus-hold and programmable pull-up resistors

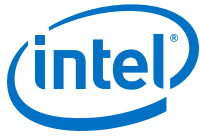The table below lists the MAX V CPLD I/O signals.

Table 5. **MAX V CPLD I/O Signals**

Signal Name	Description
`FA_A[26:1]`	Flash Address Bus
`FM_D[31:0]`	Flash Data Bus
	continued...

Signal Name	Description
FLASH_CLK	Flash Clock
FLASH_RESETn	Flash Reset
FLASH_CEn[1:0]	Flash Chip Enable
FLASH_OEn	Flash Output Enable
FLASH_WEn	Flash Write Enable
FLASH_ADVn	Flash Address Valid
FLASH_RDYBSYn[1:0]	Flash Chip Ready/Busy
FPGA_CONFIG_D[31:0]	FPGA AvST configuration data bus
FPGA_INIT_DONE	FPGA initialization complete
FPGA_nSTATUS	FPGA status
FPGA_CONF_DONE	FPGA configuration complete
FPGA_nCONFIG	FPGA configuration control pin reset to FPGA
FPGA_ASCLK	FPGA AS configuration clock
FPGA_SEU_ERR	FPGA configuration SEU error
FPGA_CvP_DONE	FPGA CvP configuration done
FPGA_SDM	FPGA SDM IO10
FPGA_PR_REQUEST	FPGA partial reconfiguration request
FPGA_PR_DONE	FPGA partial reconfiguration done
FPGA_PR_ERROR	FPGA partial reconfiguration error
FPGA_MSEL[2:0]	FPGA configuration mode setting bits
FPGA_AVST_CLK	FPGA AvST configuration clock
FPGA_AVST_VALID	FPGA AvST configuration data valid
FPGA_AVST_READY	FPGA ready to receive data
I2C_1V8_SCL	MAX V I^{2}C bus
I2C_1V8_SDA	MAX V I^{2}C bus
FAPRSNT1V8_N	FMC A present indicator
FBPRSNT1V8_N	FMC B present indicator
SI5341_1_ENn	SI5341 1 ENABLE
SI5341_1_INTn	SI5341 1 interrupt indicators
SI5341_1_RSTn	SI5341 1 reset
SI5341_1_LOLn	SI5341 1 loss of clock indicators
SI5341_2_ENn	SI5341 2 ENABLE
SI5341_2_INTn	SI5341 2 interrupt indicators
SI5341_2_RSTn	SI5341 2 reset

continued...

Signal Name	Description
SI5341_2_LOLn	SI5341 2 loss of clock indicators
EN_MASTER[1:0]	ENABLE specific I2C buffer
TEMP_ALERTn	FPGA temperature alert input
OVERTEMPn	FPGA over temperature input
OVERTEMP	Over temperature fan control
FAN_RPM	Fan speed control
USB_CFG[14:0]	Bus between USB Intel MAX 10 and MAX V
USB_MAX5_CLK	Clock from USB PHY chip
MAX_OSC_CLK_1	25MHz / 100 MHz / 125 MHz clock input
MAX5_JTAG_TCK	MAX V Test Clock
MAX5_JTAG_TMS	MAX V Test Mode Select
MAX5_JTAG_TDI	MAX V Test Data Input
MAX5_JTAG_TDO	MAX V Test Data Output
FACTORY_LOAD	Factory image for configuration
MAX5_SWITCH [2:0]	System MAX V user DIP switch
PGM_SEL	Flash Memory program select pushbutton
PGM_CONFIG	Flash Memory program configuration pushbutton
MAX_RESETn	System MAX V reset pushbutton
CPU_RESETn	CPU reset pushbutton
PGM_LED[2:0]	Flash image program select indicators
MAXV_ERROR	Intel Stratix 10 configuration error indicator LED
MAXV_LOAD	Intel Stratix 10 configuration active indicator LED
MAXV_CONF_DONE	Intel Stratix 10 configuration done indicator LED
MAX5_BE_n[3:0]	Intel Stratix 10 and MAX V data path, byte enable
MAX5_OEn	Intel Stratix 10 and MAX V data path, output enable
MAX5_CSn	Intel Stratix 10 and MAX V data path, chip select
MAX5_WEn	Intel Stratix 10 and MAX V data path, write enable
MAX5_CLK	Intel Stratix 10 and MAX V data path, clock
SPARE[20:1]	Spare bus between MAX V and Intel Stratix 10
CLK_50M_MAX5	50 MHz clock input
FPGA_ASDATA[3:0]	Intel Stratix 10 AS configuration data
CLK_CONFIG	100 MHz clock input

Figure 4.   I2C Block Diagram
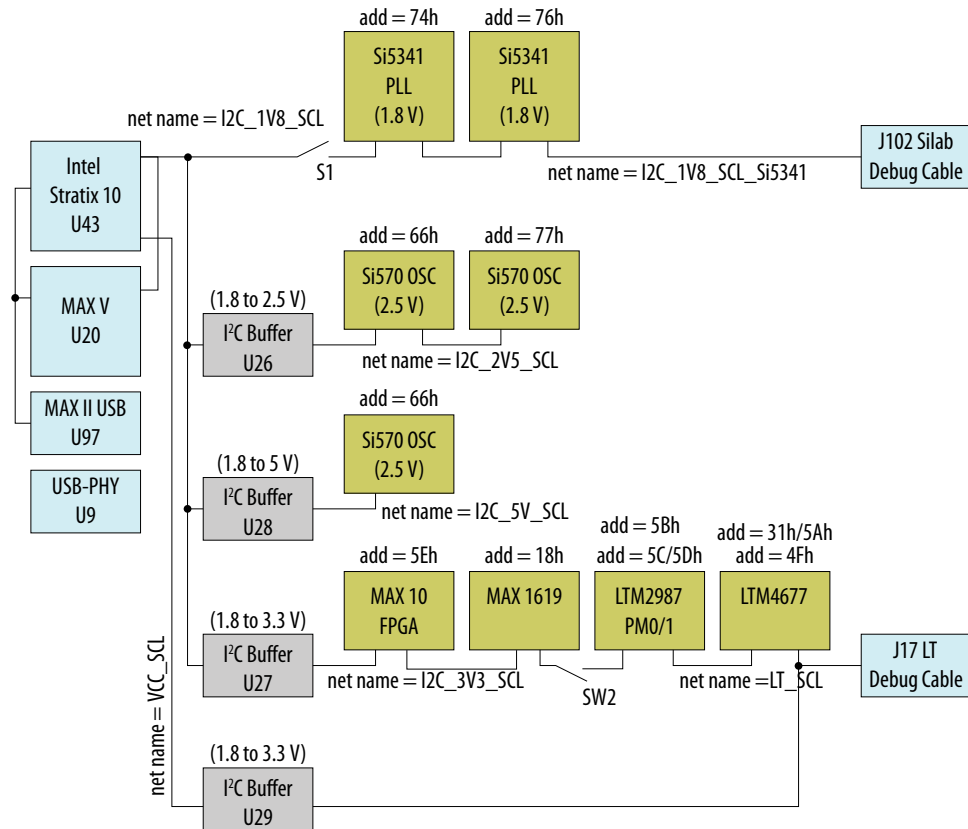
4.4 FPGA Configuration

This section describes the FPGA, flash memory and MAX V CPLD System Controller device programming methods supported by the Intel Stratix 10 GX tranceiver signal integrity development kit.

Three configuration methods except AS mode are mostly used on the Intel Stratix 10 transceiver signal integrity development kit.

- Embedded USB-Blaster is the default method for configuring the FPGA at any time using the Intel Quartus Prime Programmer in JTAG mode with the supplied USB cable.

- MAX V configures the FPGA device via AvST mode using stored images from CFI flash devices either at power-up or pressing the `MAX_RESETn`/`PGM_CONFIG` push button.

- JTAG external header for debugging. Intel recommends that you use lower JTAG clock frequency value such as 16 MHz.
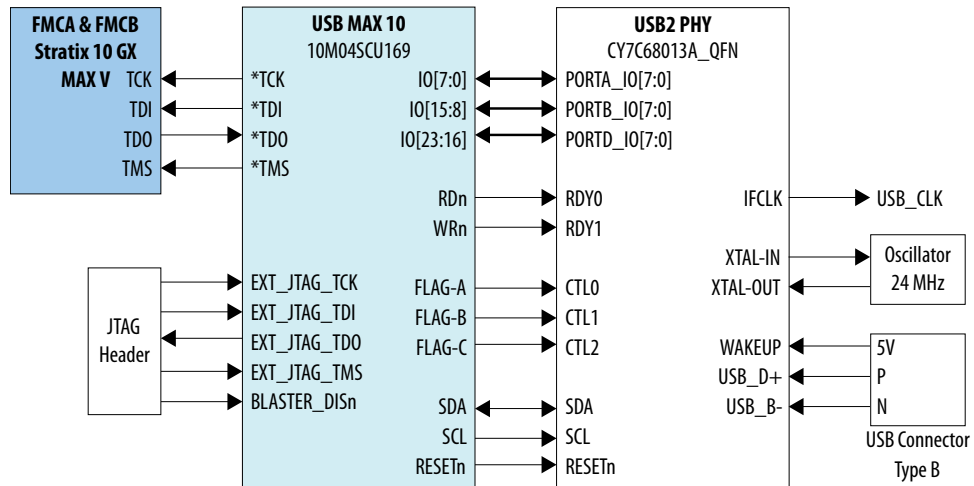
4.4.1 FPGA Programming over Embedded USB-Blaster

Embedded USB-Blaster is the default method for configuring the Intel Stratix 10 GX FPGA using the Intel Quartus Prime Programmer in the JTAG mode with the supplied USB cable.

The figure below shows the conceptual block diagram for the embedded USB-Blaster.

Figure 5.   USB-Blaster II Block Diagram

The embedded USB-Blaster core for USB-based configuration of the Intel Stratix 10 GX FPGA device is implemented using a Type-B USB connector, a CY7C68013A USB2 PHY device, and an Intel Intel MAX 10 10M04SCU169 FPGA. This will allow configuration of the Intel Stratix 10 GX FPGA device using a USB cable directly connected to a computer running Intel Quartus Prime software without requiring the external USB-Blaster dongle. This design will convert USB data to interface with the Intel Stratix 10 GX FPGA's dedicated JTAG port. Four LEDs are provided to indicate USB Blaster activity. The embedded USB Blaster is automatically disabled when an external USB Blaster dongle is connected to the JTAG header.

4.4.2 FPGA Programming from Flash Memory

The figure below shows a detailed schematic block diagram for the MAX V + Flash AvSTx32 mode configuration implementation.

Note: Typical JTAG clock frequency for CFI Flash programming via PFL II core is 16 MHz. You may try it with a lower frequency such as 6 MHz if it fails with 16 MHz.
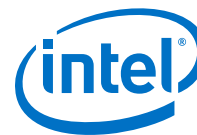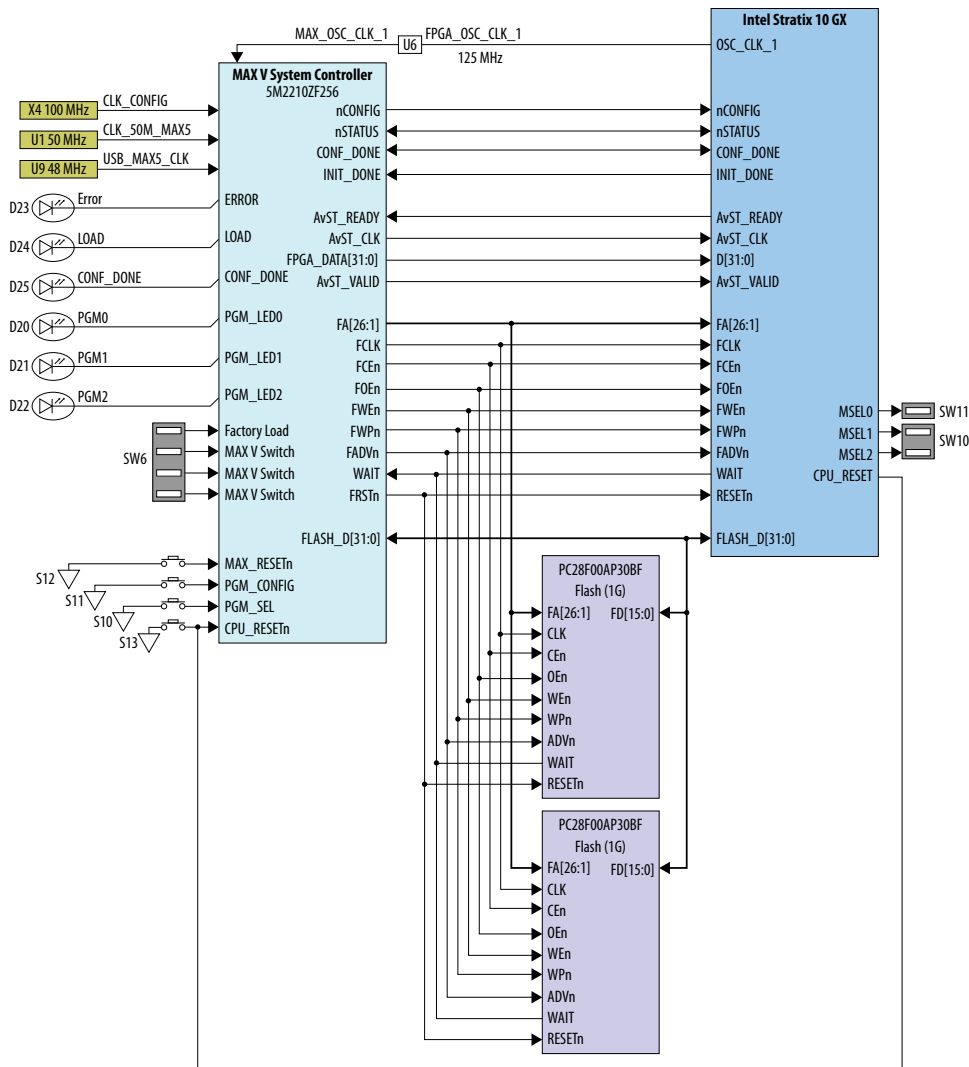
Figure 6. **MAX V + Flash AvSTx32 Configuration Block Diagram**

Once the FPGA is successfully initialized and in user mode, the CPLD will tri-state its Flash interface signals to avoid contention with the FPGA. The PGMSEL dipswitch (S10) is provided to select between two POF files (FACTORY and USER) stored on the Flash.

The Parallel Flash Loader II (PFL II) Megafunction is used to implement the AvSTx32 configuration in the MAX V CPLD. The PFL II Megafunction reads data from the flash and converts it to AvST format. This data is written into the Intel Stratix 10 GX FPGA device through dedicated AvST CLK and FPGA Config Data [31:0] pins at corresponding clock rate, such as 25 MHz, 50 MHz and 100 MHz.

Implementation will be done using an Intel MAX V 5M2210ZF256FBGA CPLD acting as the AvST download controller and two 1G Flash devices. The Flash will be Numonyx 1.8V core, 1.8V I/O 1Gigabit CFI NOR-type device (P/N: PC28F00AP30BF). The MAX V CPLD shares the CFI Flash interface with the Intel Stratix 10 GX FPGA. No arbitration is needed between MAX V CPLD and Intel Stratix 10 GX FPGA to access the Flash as the CPLD only has access prior to FPGA initialization.