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Transceiver Signal Integrity Development Kit, Stratix V GT Edition User Guide



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The Altera® Stratix® V GT Transceiver Signal Integrity Development Kit is a complete design environment that includes both the hardware and software you need to develop Stratix V GT FPGA designs. The one-year license for the Quartus® II software provides everything you need to begin developing custom Stratix V GT FPGA designs. The following list describes what you can accomplish with the kit:


- Evaluate transceiver performance from 600 Mbps up to 12.5 Mbps.
- Evaluate transceiver performance up to 28 Gbps for the GT channels.
- Generate and check pseudo-random binary sequence (PRBS) patterns.
- Dynamically change differential output voltage (V_{OD}) pre-emphasis, and equalization settings to optimize transceiver performance for your channel.
- Perform jitter analysis.
- Verify physical medium attachment (PMA) compliance to PCI Express®(PCIe®), Gbps Ethernet (GbE), XAUI, CEI-6G, Serial RapidIO®, high-definition serial digital interface (HD-SDI), and other major standards.

Kit Features

This section briefly describes the Transceiver Signal Integrity Development Kit, Stratix V GT Edition contents.

Hardware

The Transceiver Signal Integrity Development Kit, Stratix V GT Edition includes the following hardware:

- Stratix V GT development board—A development platform that allows you to develop and prototype hardware designs running on the Stratix V GT FPGA.
 -  For detailed information about the board components and interfaces, refer to the *Transceiver Signal Integrity Development Kit, Stratix V GT Edition Reference Manual*.
- Power supply and cables—The kit includes the following items:
 - Power supply and AC adapters for North America/Japan, Europe, and the United Kingdom
 - USB type A to B cable
 - Ethernet cable

Software

The software for this kit, described in the following sections, is available on the Altera website for immediate downloading. You can also request to have Altera mail the software to you on DVDs.

Quartus II Software

Your kit includes a license for the Development Kit Edition (DKE) of the Quartus II software (Windows platform only). For one year, this license entitles you to most of the features of the Subscription Edition (excluding the IP Base Suite).



After the year, your DKE license will no longer be valid and you will not be permitted to use this version of the Quartus II software. To continue using the Quartus II software, you should download the free Quartus II Web edition or purchase a subscription to Quartus II software. For more information, refer to the [Design Software](#) page of the Altera website.

The Quartus II Development Kit Edition (DKE) software includes the following items:

- Quartus II Software—The Quartus II software, including the Qsys system integration tool, provides a comprehensive environment for network on a chip (NoC) design. The Quartus II software integrates into nearly any design environment and provides interfaces to industry-standard EDA tools.
- MegaCore[®] IP Library—A library that contains Altera IP MegaCore functions. You can evaluate MegaCore functions by using the OpenCore Plus feature to do the following:
 - Simulate behavior of a MegaCore function within your system.
 - Verify functionality of your design, and quickly and easily evaluate its size and speed.
 - Generate time-limited device programming files for designs that include MegaCore functions.
 - Program a device and verify your design in hardware.



The OpenCore Plus hardware evaluation feature is an evaluation tool for prototyping only. You must purchase a license to use a MegaCore function in production.



For more information about OpenCore Plus, refer to [AN 320: OpenCore Plus Evaluation of Megafunctions](#).

- Nios[®] II Embedded Design Suite (EDS)—A full-featured set of tools that allows you to develop embedded software for the Nios II processor, which you can include in your Altera FPGA designs.

Transceiver Signal Integrity Development Kit, Stratix V GT Edition Installer

The license-free Transceiver Signal Integrity Development Kit, Stratix V GT Edition installer includes all the documentation and design examples for the kit.



For information on installing the Development Kit Installer, refer to [“Installing the Development Kit”](#) on page 3-3.

The remaining chapters in this user guide lead you through the following board setup steps:

- Inspecting the contents of the kit
- Installing the design and kit software
- Setting up, powering up, and verifying correct operation of the development board
- Configuring the Stratix V GT FPGA
- Running the Board Test System designs

 For complete information about the development board, refer to the *Transceiver Signal Integrity Development Kit, Stratix V GT Edition Reference Manual*.

Before You Begin

Before using the kit or installing the software, check the kit contents and inspect the board to verify that you received all of the items listed in “[Kit Features](#)” on page 1–1. If any of the items are missing, contact Altera before you proceed.

Inspect the Board

To inspect the board, perform the following steps:

1. Place the board on an anti-static surface and inspect it to ensure that it has not been damaged during shipment.



Without proper anti-static handling, you can damage the board.

2. Verify that all components are on the board and appear intact.
3. For proper Stratix V GT device cooling, install the heatsink/fan included with the kit using the provided heatsink/fan installation tool.

 For more information about power consumption and thermal modeling, refer to *AN 358: Thermal Management for FPGAs*.

References

Use the following links to check the Altera website for other related information:

- For the latest board design files and reference designs, refer to the [Transceiver Signal Integrity Development Kit, Stratix V GT Edition](#) page.
- For the Stratix V GT device documentation, refer to the [Literature: Stratix V Devices](#) page.
- To purchase devices from the eStore, refer to the [Devices](#) page.

- For Stratix V GT OrCAD symbols, refer to the [Capture CIS Symbols](#) page.
- For Nios II 32-bit embedded processor solutions, refer to the [Embedded Processing](#) page.

This chapter explains how to install the following software:

- Quartus II Subscription Edition Software
- Transceiver Signal Integrity Development Kit, Stratix V GT Edition
- USB-Blaster™ driver

Installing the Quartus II Subscription Edition Software

The Quartus II Subscription Edition Software provides the necessary tools used for developing hardware and software for Altera devices. Included in the Quartus II Subscription Edition Software are the Quartus II software, the Nios II EDS, and the MegaCore IP Library. The Quartus II software (including Qsys) and the Nios II EDS are the primary FPGA development tools used to create the reference designs in this kit. To install the Altera development tools, perform the following steps:

1. Download the Quartus II Subscription Edition Software from the [Quartus II Subscription Edition Software](#) page of the Altera website. Alternatively, you can request a DVD from the [Altera IP and Software DVD Request Form](#) page of the Altera website.
2. Follow the on-screen instructions to complete the installation process.



If you have difficulty installing the Quartus II software, refer to the [Altera Software Installation and Licensing Manual](#).

Licensing Considerations

Purchasing this kit entitles you to a one-year license for the Development Kit Edition (DKE) of the Quartus II software.



After the year, your DKE license will no longer be valid and you will not be permitted to use this version of the Quartus II software. To continue using the Quartus II software, you should download the free Quartus II Web edition or purchase a subscription to Quartus II software.

Before using the Quartus II software, you must activate your license, identify specific users and computers, and obtain and install a license file.

If you already have a licensed version of the subscription edition, you can use that license file with this kit. If not, you need to obtain and install a license file. To begin, go to the [Self Service Licensing Center](#) page of the Altera website, log into or create your myAltera account, and take the following actions:

1. On the [Activate Products](#) page, enter the serial number provided with your development kit in the **License Activation Code** box.



 Your serial number is printed on the development kit box below the bottom bar code. The number is 10 or 11 alphanumeric characters and does not contain hyphens. [Figure 3-1](#) shows *3S150SPXXXX* as an example serial number.


Figure 3-1. Locating Your Serial Number



2. Consult the Activate Products table, to determine how to proceed.
 - a. If the administrator listed for your product is someone other than you, skip the remaining steps and contact your administrator to become a licensed user.
 - b. If the administrator listed for your product is you, proceed to step 3.
 - c. If the administrator listed for your product is *Stocking*, activate the product, making you the administrator, and proceed to step 3.
3. Use the [Create New License](#) page to license your product for a specific user (you) on specific computers. The [Manage Computers](#) and [Manage Users](#) pages allow you to add users and computers not already present in the licensing system.

 To license the Quartus II software, you need your computer's network interface card (NIC) ID, a number that uniquely identifies your computer. On the computer you use to run the Quartus II software, type `ipconfig /all` at a command prompt to determine the NIC ID. Your NIC ID is the 12-digit hexadecimal number on the **Physical Address** line.

4. When licensing is complete, Altera emails a **license.dat** file to you. Store the file on your computer and use the **License Setup** page of the **Options** dialog box in the Quartus_II software to enable the software.

 For complete licensing details, refer to the [Altera Software Installation and Licensing Manual](#).

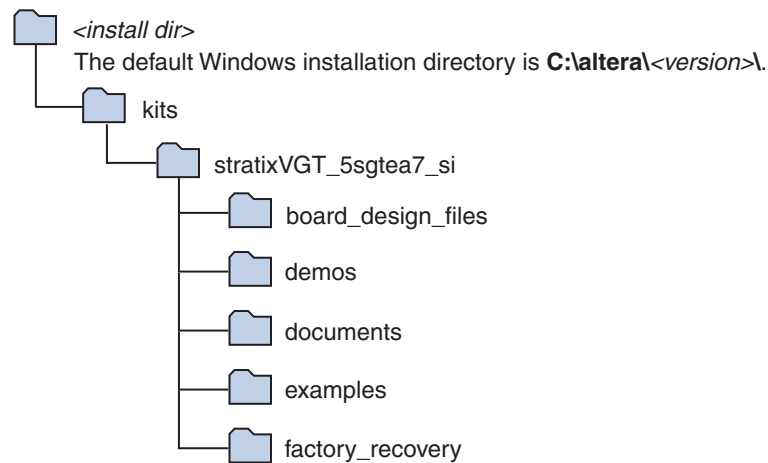
Installing the Development Kit

To install the Transceiver Signal Integrity Development Kit, Stratix V GT Edition, perform the following steps:

1. Download the Transceiver Signal Integrity Development Kit, Stratix V GT Edition installer from the [Transceiver Signal Integrity Development Kit, Stratix V GT Edition](#) page of the Altera website. Alternatively, you can request a development kit DVD from the [Altera Kit Installations DVD Request Form](#) page of the Altera website.
2. Run the Transceiver Signal Integrity Development Kit, Stratix V GT Edition installer.
3. Follow the on-screen instructions to complete the installation process. Be sure that the installation directory you choose is in the same relative location to the Quartus II software installation.

The installation program creates the Transceiver Signal Integrity Development Kit, Stratix V GT Edition directory structure shown in [Figure 3-2](#).

Figure 3-2. Transceiver Signal Integrity Development Kit, Stratix V GT Edition Installed Directory Structure (1)



Note to Figure 3-2:

(1) Early-release versions might have slightly different directory names.

[Table 3-1](#) lists the file directory names and a description of their contents.

Table 3-1. Installed Directory Contents


| Directory Name | Description of Contents |
|---------------------------|--|
| board_design_files | Contains schematic, layout, assembly, and bill of material board design files. Use these files as a starting point for a new prototype board design. |
| demos | Contains demonstration applications when available. |
| documents | Contains the kit documentation. |

Table 3-1. Installed Directory Contents

| Directory Name | Description of Contents |
|-------------------------|--|
| examples | Contains the sample design files for the Transceiver Signal Integrity Development Kit, Stratix V GT Edition. |
| factory_recovery | Contains the original data programmed onto the board before shipment. Use this data to restore the board with its original factory contents. |

Installing the USB-Blaster Driver

The Stratix V GT development board includes integrated USB-Blaster circuitry for FPGA programming. However, for the host computer and board to communicate, you must install the USB-Blaster driver on the host computer.

-  Installation instructions for the USB-Blaster driver for your operating system are available on the Altera website. On the [Altera Programming Cable Driver Information](#) page of the Altera website, locate the table entry for your configuration and click the link to access the instructions.

The instructions in this chapter explain how to set up the Stratix V GT development board.

Setting Up the Board

To prepare and apply power to the board, perform the following steps:

1. The Stratix V GT development board ships with its board switches preconfigured to support the design examples in the kit. If you suspect your board might not be currently configured with the default settings, follow the instructions in “[Factory Default Switch Jumper Settings](#)” on page 4-2 to return the board to its factory settings before proceeding.
2. The development board ships with design examples stored in the flash memory device. Verify the PGMSEL jumper (J28) is set to the jump pins 2-3 position to load the design stored in the factory portion of flash memory. [Figure 4-1](#) shows the switch location on the Stratix V GT development board. Connect the 120 W, 20 VDC @ 6.32 A power supply (model # LTE120E-SW-3XX) to the DC Power Jack (J1) on the FPGA board and plug the cord into a power outlet.



Use only the supplied power supply. Power regulation circuitry on the board can be damaged by power supplies with greater voltage.

3. Set the POWER switch (SW1) to the on position. When power is supplied to the board, the blue LED (D3) illuminates indicating that the board has power.

The MAX II device on the board contains (among other things) a parallel flash loader (PFL) megafunction. When the board powers up, the PFL reads a design from flash memory and configures the FPGA. The PGMSEL jumper (J28) controls which design to load: When pins are in the 2-3 position, the PFL loads the design from the factory portion of flash memory. When pins are in the 1-2 position, the PFL loads the design from the user portion of flash memory.



The kit includes a MAX II design which contains the MAX II PFL megafunction. The design resides in the `<install_dir>\kits\stratixVGT_5sgtea7_si\examples\max2` directory.

When configuration is complete, one of two LEDs illuminate, (D10 for `FACTORY_IMAGE` or D11 for `USER_IMAGE`) signaling that the Stratix V GT device configured successfully. If either configuration fails, the red `CONFIG_ERR` LED (D9) illuminates.



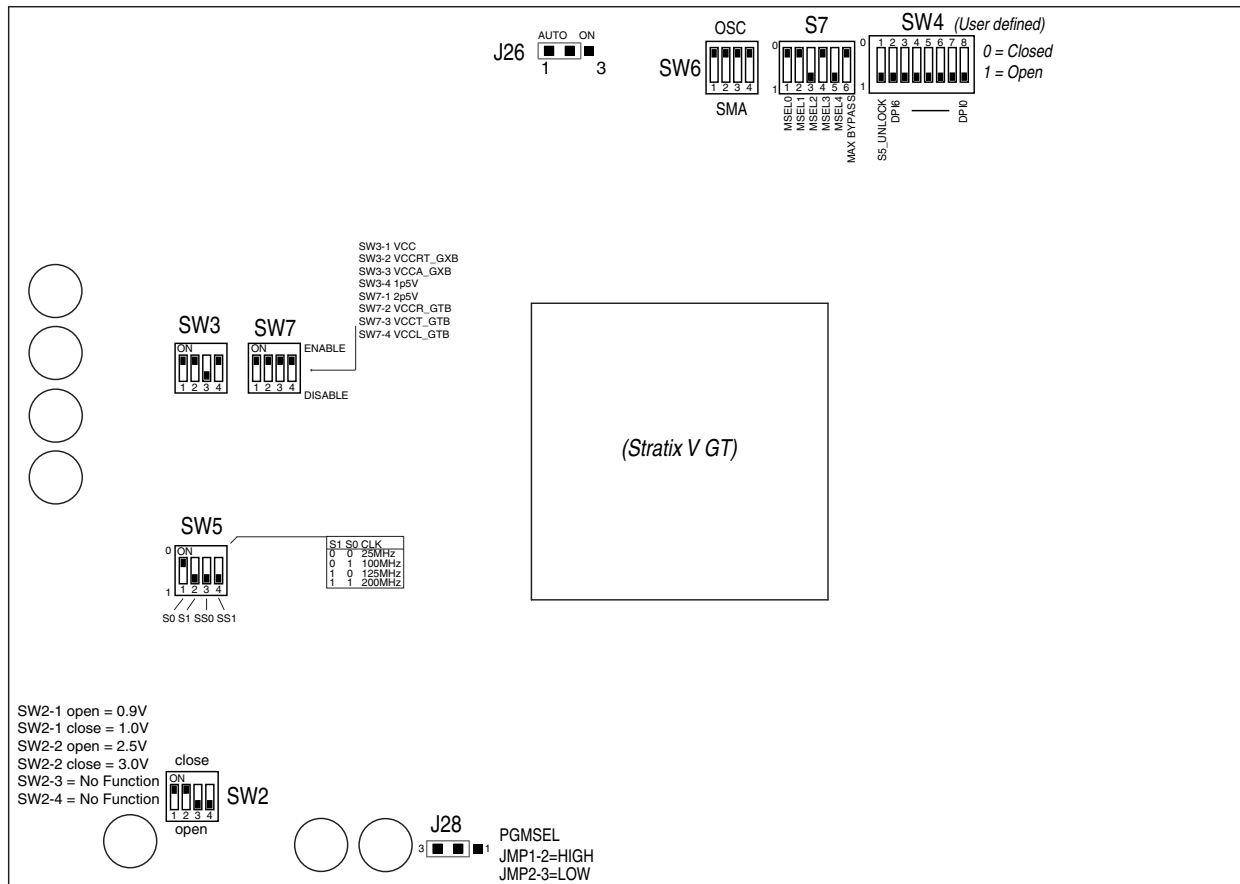
For more information about the PFL megafunction, refer to the [Parallel Flash Loader Megafunction User Guide](#).

Factory Default Switch Jumper Settings

This section shows the factory switch settings for the Stratix V GT development board.

Figure 4-1 shows the switch locations and the default position of each switch on the top side of the board.

Figure 4-1. Switch Locations and Default Settings on the Board Top



To restore the switches to their factory default settings, perform the following steps:

1. Set the DIP switch bank (SW2) to match Table 4-1 and Figure 4-1.

Table 4-1. SW2 DIP Switch Settings (Part 1 of 2)

| Switch | Board Label | Function | Default Position |
|--------|-------------|--|------------------|
| 1 | SW2-1 | Switch 1 has the following options: <ul style="list-style-type: none"> Open = VCCRT_GXB select at 0.9 V. Close (ON) = VCCRT_GXB select at 1.0 V. | Close |
| 2 | SW2-2 | Switch 2 has the following options: <ul style="list-style-type: none"> Open = VCCA_GXB select at 2.5 V. Close (ON) = VCCA_GXB select at 3.0 V. | Close |

Table 4–1. SW2 DIP Switch Settings (Part 2 of 2)

| Switch | Board Label | Function | Default Position |
|--------|-------------|---|------------------|
| 3 | SW2-3 | Switch 3 has the following options: <ul style="list-style-type: none"> ■ Open = No function. ■ Close (ON) = No function. | Open |
| 4 | SW2-4 | Switch 4 has the following options: <ul style="list-style-type: none"> ■ Open = No function. ■ Close (ON) = No function. | Open |

2. Set DIP switch bank (SW3) to match [Table 4-2](#) and [Figure 4-1](#).

Table 4–2. SW3 Dip Switch Settings

| Switch | Board Label | Function | Default Position |
|--------|-----------------|---|------------------|
| 1 | SW3-1 VCC | Switch 1 has the following options: <ul style="list-style-type: none"> ■ ON = S5GT_VCC is enabled. ■ OFF = S5GT_VCC is disabled. | ON |
| 2 | SW3-2 VCCRT_GXB | Switch 2 has the following options: <ul style="list-style-type: none"> ■ ON = VCCRT_GXB is enabled. ■ OFF = VCCRT_GXB is disabled. | ON |
| 3 | SW3-3 VCCA_GXB | Switch 3 has the following options: <ul style="list-style-type: none"> ■ ON position = VCCA_GXB is enabled. ■ OFF position = VCCA_GXB is disabled. | OFF |
| 4 | SW3-4 1p5V | Switch 4 has the following options: <ul style="list-style-type: none"> ■ ON position = 1p5V is enabled. ■ OFF position = 1p5V is disabled. | ON |

3. Set DIP switch bank (SW7) to match [Table 4-3](#) and [Figure 4-1](#).

Table 4–3. SW7 DIP Switch Settings

| Switch | Board Label | Function | Default Position |
|--------|----------------|---|------------------|
| 1 | SW7-1 2p5V | Switch 1 has the following sequence enable options: <ul style="list-style-type: none"> ■ ON position = 2p5V is enabled. ■ OFF position = 2p5V is disabled. | ON |
| 2 | SW7-2 VCCR_GTB | Switch 2 has the following sequence enable options: <ul style="list-style-type: none"> ■ ON position = VCCR_GTB is enabled. ■ OFF position = VCCR_GTB is disabled. | ON |

Table 4-3. SW7 DIP Switch Settings

| Switch | Board Label | Function | Default Position |
|--------|----------------|--|------------------|
| 3 | SW7-3 VCCT_GTB | Switch 3 has the following sequence enable options: <ul style="list-style-type: none"> ON position = VCCT_GTB is enabled. OFF position = VCCT_GTB is disabled. | ON |
| 4 | SW7-4 VCCL_GTB | Switch 4 has the following sequence enable options: <ul style="list-style-type: none"> ON position = VCCL_GTB is enabled. OFF position = VCCL_GTB is disabled. | ON |

4. Set DIP switch bank (SW4) to match [Table 4-4](#) and [Figure 4-1](#).

Table 4-4. SW4 User DIP Switch Settings

| Switch | Board Label | Function | Default Position |
|--------|-------------|--|------------------|
| 1 | S5_UNLOCK | Switch 1 has the following options: <ul style="list-style-type: none"> Closed (0) = <code>FACTORY</code> command won't be issued. JTAG will be locked out if FPGA is configured on power-up from flash. Open (1) = Unlock the FPGA and allow <code>FACTORY</code> command. JTAG will be available even if FPGA is configured on power-up from flash. | Open (1) |
| 2-8 | DPI6—DPIO | User defined options. | — |

5. Set DIP switch bank (SW5) to match [Table 4-5](#) and [Figure 4-1](#).

Table 4-5. SW5 DIP Switch Settings

| Switch | Board Label | Function | Default Position |
|--------|-------------|---|------------------|
| 1 | S0 | Determines S5GT_CLK11 frequency. ⁽¹⁾ | Closed |
| 2 | S1 | Determines S5GT_CLK11 frequency. | Open |
| 3 | SS0 | Determines S5GT_CLK11 spectrum spread. ⁽¹⁾ | Open |
| 4 | SS1 | Determines S5GT_CLK11 spectrum spread. | Open |

Note to: Table 4-5

(1) Truth tables for the SW5 settings:

S1S0Frequency

00-25 MHz

01-100 MHz (default)

10-125 MHz

11-200 MHz

SS1SS0Spread %

00-center +/- 25%

01-down -0.5%

10-down -0.75%

11-no spread (default)

6. Set DIP switch bank (SW6) to match [Table 4-6](#) and [Figure 4-1](#).

Table 4-6. SW6 DIP Switch Settings

| Switch | Board Label | Function | Default Position |
|--------|----------------|--|------------------|
| 1 | REFCLK_SEL_U32 | Switch 1 has the following options: <ul style="list-style-type: none"> ■ <i>OSC</i> enables oscillator input. ■ <i>SMA</i> enables SMA input. | OSC |
| 2 | REFCLK_SEL_U33 | Switch 2 has the following options: <ul style="list-style-type: none"> ■ <i>OSC</i> enables oscillator input. ■ <i>SMA</i> enables SMA input. | OSC |
| 3 | REFCLK_SEL_U34 | Switch 3 has the following options: <ul style="list-style-type: none"> ■ <i>OSC</i> enables oscillator input. ■ <i>SMA</i> enables SMA input. | OSC |
| 4 | REFCLK_SEL_U35 | Switch 4 has the following options: <ul style="list-style-type: none"> ■ <i>OSC</i> enables oscillator input. ■ <i>SMA</i> enables SMA input. | OSC |

7. Set DIP switch bank (S7) to match [Table 4-7](#) and [Figure 4-1](#).

Table 4-7. S7 DIP Switch Settings

| Switch | Board Label | Function | Default Position |
|--------|-------------|--|------------------|
| 1 | MSEL0 | Switch 1 has the following: <ul style="list-style-type: none"> ■ Closed = Logic 0. ■ Open = Logic 1. | Closed |
| 2 | MSEL1 | Switch 2 has the following: <ul style="list-style-type: none"> ■ Closed = Logic 0. ■ Open = Logic 1. | Closed |
| 3 | MSEL2 | Switch 3 has the following: <ul style="list-style-type: none"> ■ Closed = Logic 0. ■ Open = Logic 1. | Open |
| 4 | MSEL3 | Switch 4 has the following: <ul style="list-style-type: none"> ■ Closed = Logic 0. ■ Open = Logic 1. | Closed |
| 5 | MSEL4 | Switch 5 has the following: <ul style="list-style-type: none"> ■ Closed = Logic 0. ■ Open = Logic 1. | Open |
| 6 | MAX BYPASS | Switch 6 has the following: <ul style="list-style-type: none"> ■ Closed = Logic 0. Includes the MAX II device in the JTAG chain. ■ Open = Logic 1. Removes the MAX II device in the JTAG chain. | Closed |

8. Set jumper blocks (J26, J28) to match [Table 4-8](#) and [Figure 4-1](#).

Table 4-8. Jumper Settings


| Board Reference | Description | Shunt Position |
|-----------------|--|----------------|
| J26 | Fan select — Pins 1-2 select auto operation. | Installed |
| J26 | Fan select — Pins 2-3 select fan on. | Not installed |
| J28 | PGMSEL (logic 1) — Pins 1-2 select user-defined image. | Not Installed |
| J28 | PGMSEL (logic 0) — Pins 2-3 select factory image. | Installed |



For more information about the FPGA board settings, refer to the *Transceiver Signal Integrity Development Kit, Stratix V GT Edition Reference Manual*.

This kit ships with the Board Update Portal design example stored in the factory portion of the flash memory on the board. The design consists of a Nios II embedded processor, an Ethernet MAC, and an HTML web server.


When you power up the board with the PGMSEL jumper (J28) in the factory position (jump pins 2-3), the Stratix V GT FPGA configures with the Board Update Portal design example. The design can obtain an IP address from any DHCP server and serve a web page from the flash on your board to any host computer on the same network. The web page allows you to upload new FPGA designs to the user portion of flash memory and provides kit-specific links and design resources.

 After successfully updating the user flash memory, you can load the user design from flash memory into the FPGA. To do so, set the PGMSEL jumper (J28) to the user position (jump pins 1-2) and power cycle the board.

The source code for the Board Update Portal design resides in the `<install dir>\kits\stratixVGT_5sgtea7_si\examples` directory. If the Board Update Portal is corrupted or deleted from the flash memory, refer to [“Restoring the Flash Device to the Factory Settings” on page A-4](#) to restore the board with its original factory contents.

Connecting to the Board Update Portal Web Page


This section provides instructions to connect to the Board Update Portal web page.


 Before you proceed, ensure that you have the following:

- A PC with a connection to a working Ethernet port on a DHCP enabled network.
- A separate working Ethernet port connected to the same network for the board.
- The Ethernet and power cables that are included in the kit.

To connect to the Board Update Portal web page, perform these steps:

1. With the board powered down, set the PGMSEL jumper (J28) to the factory position (jump pins 2-3).
2. Attach the Ethernet cable from the board (J29) to your LAN.
3. Power up the board. The board connects to the LAN's gateway router and obtains an IP address. The LCD on the board displays the IP address.
4. Launch a web browser on a PC that is connected to the same network, and enter the IP address from the LCD into the browser address bar. The Board Update Portal web page appears in the browser.

 You can click *Transceiver Signal Integrity Development Kit, Stratix V GT Edition* on the Board Update Portal web page to access the kit's home page for documentation updates and additional new designs.

 You can also navigate directly to the [Transceiver Signal Integrity Development Kit, Stratix V GT Edition](#) page of the Altera website to determine if you have the latest kit software.


Using the Board Update Portal to Update User Designs

The Board Update Portal allows you to write new designs to the user portion of flash memory. Designs must be in the Nios II Flash Programmer File (**.flash**) format.

 Design files available from the [Transceiver Signal Integrity Development Kit, Stratix V GT Edition](#) page include **.flash** files. You can also create **.flash** files from your own custom design. Refer to [“Preparing Design Files for Flash Programming” on page A-2](#) for information about preparing your own design for upload.

To upload a design over the network into the user portion of flash memory on your board, perform the following steps:

1. Perform the steps in [“Connecting to the Board Update Portal Web Page”](#) to access the Board Update Portal web page.
2. In the **Hardware File Name** field, specify the **.flash** file that you either downloaded from the Altera website or created on your own. If there is a software component to the design, specify it in the same manner using the **Software File Name** field; otherwise, leave the **Software File Name** field blank.
3. Click **Upload**. The progress bar indicates the percent complete. The file takes about 20 seconds to upload.
4. To configure the FPGA with the new design after the flash memory upload process is complete, set the PGMSEL jumper (J28) to the user position (jump pins 1-2) and power cycle the board.

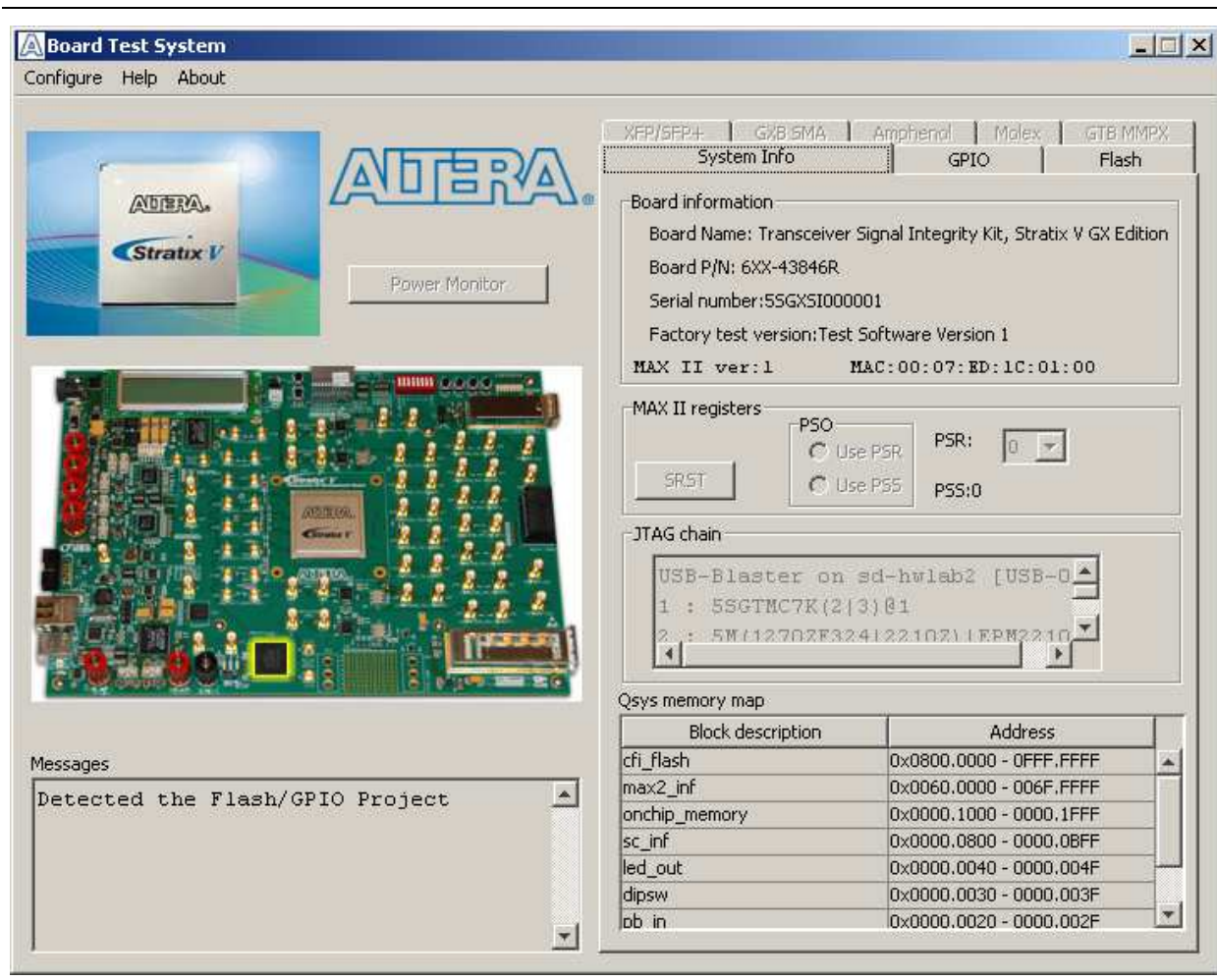
 As long as you don't overwrite the factory image in the flash memory device, you can continue to use the Board Update Portal to write new designs to the user portion of flash memory. If you do overwrite the factory image, you can restore it by following the instructions in [“Restoring the Flash Device to the Factory Settings” on page A-4](#).

This kit includes an application called the Board Test System (BTS) and related design examples. The BTS provides an easy-to-use interface to alter functional settings and observe the results. You can use the BTS to test board components, modify functional parameters, observe performance, and measure power usage. While using the BTS, you reconfigure the FPGA several times with test designs specific to the functionality you are testing.

To install the BTS, follow the steps in [“Installing the Development Kit”](#) on page 3–3.

The BTS communicates over the JTAG bus to a test design running in the Stratix V GT device. [Figure 6–1](#) shows the initial GUI for a board that is in the factory configuration.

Figure 6–1. Board Test System Graphical User Interface



Several designs are provided to test the major board features. Each design provides data for one or more tabs in the application. The Configure menu identifies the appropriate design to download to the FPGA for each tab.