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Arria 10 SoC Development Kit User Guide

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Contents

Arria 10 SoC Development Kit Overview

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This document describes the hardware features of the Arria® 10 SoC development board, including the detailed pin-out and component reference information required to create custom FPGA designs that interface with all components of the board.

General Description

The Arria 10 SoC development board provides a hardware platform for developing and prototyping low-power, high-performance, and logic-intensive designs using Altera's® Arria 10 SoC. The board provides a wide range of peripherals and memory interfaces to facilitate the development of Arria 10 SoC designs.

Figure 1-1: Arria 10 SoC Block Diagram

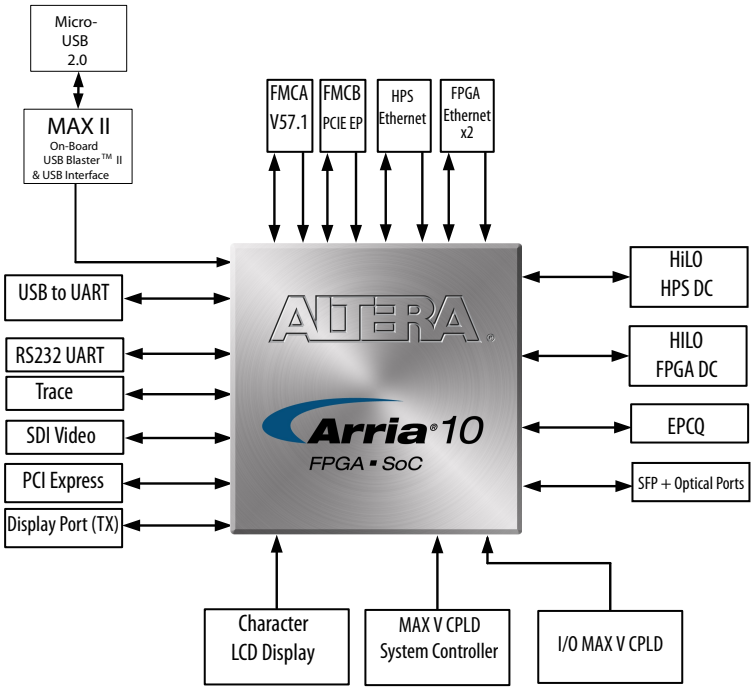
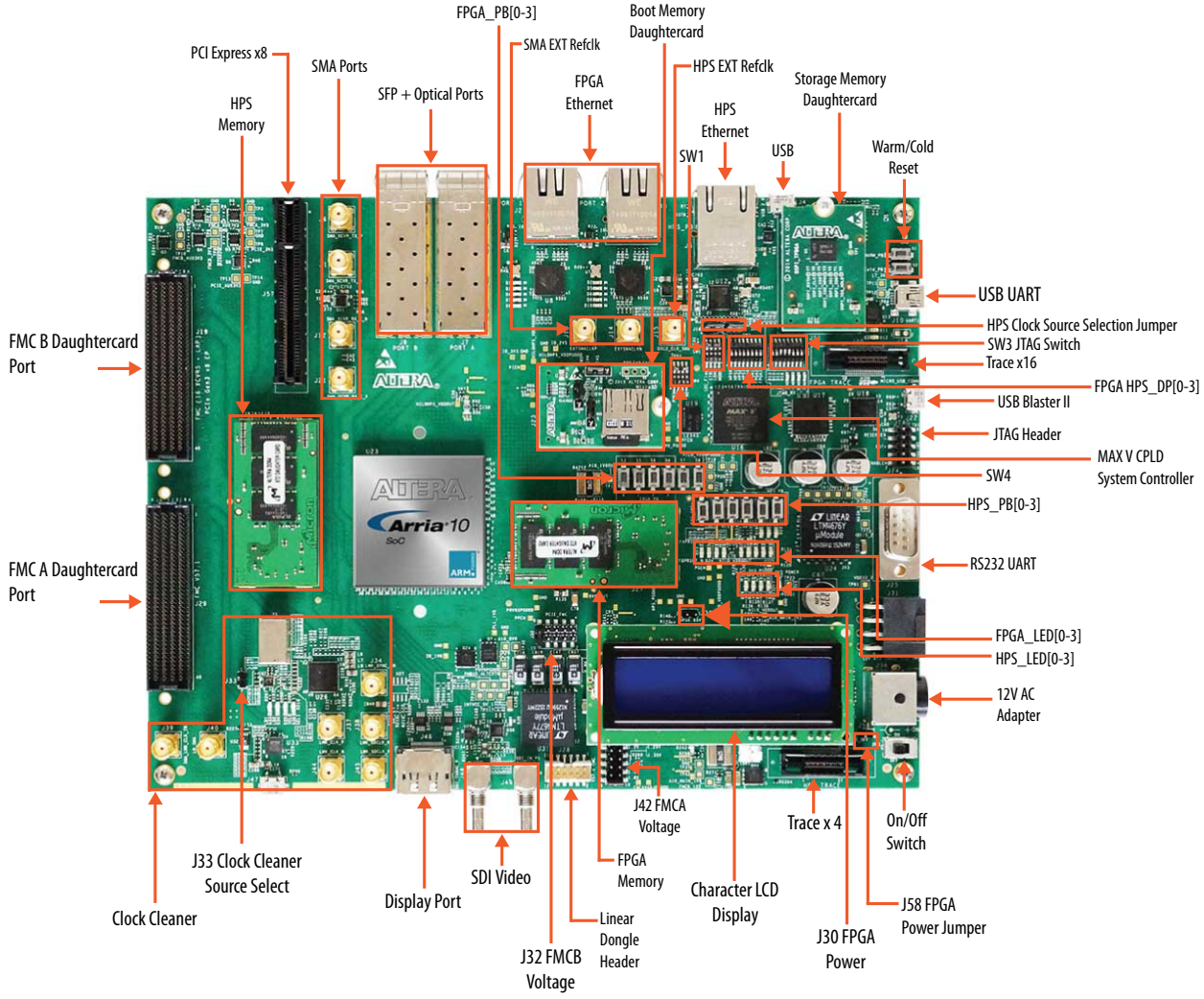


Figure 1-2: Overview of the Development Board Features



For more information about the Arria 10 SoC device family, refer to the Arria 10 SoC documentation support page.

Related Information

Arria 10 Documentation

Board Component Blocks

The development board features the following major component blocks:

- Arria 10 Soc (10AS066N3F40E2SGE2) in a 1517-pin FBGA (FineLine Ball-Grid Array) package
- FPGA configuration circuitry
  - Active Serial (AS) x1 or x4 configuration (EPCQ1024L)
  - MAX® V CPLD (5M2210ZF256) in a 256-pin FBGA package as the system controller
  - MAX V CPLD (5M2210ZF256) in a 256-pin FBGA package as the I/O multiplier CPLD
- Clocking circuitry
  - SI5338 programmable oscillator
  - LMK04828 clock cleaner
  - HPS clock options: 25 MHz, 33 MHz, and SMA input (2V5 LVCMOS)
  - SI5112 100MHz clock generator for PCIe interface
  - SI516 148.5 MHz voltage control oscillator for SDI interface
- Supported Memory
  - HPS memory size (HiLO card):
    - 2GB DDR3 (256Mb x 40 x dual rank)
    - 1GB DDR3 (256Mb x 40 x single rank)
    - 1GB DDR4 (256Mb x 40 x single rank) - *ships with kit*
  - FPGA memory size (HILO Card):
    - 4GB DDR3 (256Mb x72 x dual rank)
    - 2GB DDR3 (256Mb x72 x single rank)
    - 2GB DDR4 (256Mb x 72 x single rank) - *ships with kit*
    - 16MB QDRV (4Mb x 36)
    - 128MB RLDRAM3(16Mb x 72)
  - HPS Boot Flash (Flash card):
    - NAND flash (x8) : 128MB (MT29F1G08ABBEAH4) - *ships with kit*
    - QSPI flash: 128MB (MT25QU01GBBA8E12-0SIT) - *ships with kit*
    - SD Micro flash card: 4GB (Kingston) - *ships with kit*
  - Optional FPGA File Flash (Flash card):
    - NAND flash (x8): 128MB (MT29F1G08ABBEAH4)
    - QSPI flash: 128MB (MT25QU01GBBA8E12-0SIT)
    - SD Micro flash card: 4GB (Kingston)

- Communication ports
  - HPS Communication ports:
    - USB 2.0 port (PHY PN: USB3320C-EZK)
    - RGMII 10/100/1000 Ethernet port (PHY PN: KSZ9031RNXCA)
    - USB-UART port (FT232R)
    - DB-9 RS-232 Port (MAX3221)
    - I^2C port (I2C1 of shared I/O bit 12 and 13)
  - FPGA I/O connections:
    - FPGA V57.1 High Pin Count FMC slot
    - FPGA Altera Low Pin Count FMC slot
    - FMC_PCIe Gen2 x8 EP cable
    - FPGA PCIe GEN1/2/3 x8 RC slot
  - FPGA Communication ports:
    - 2x SGMII Gigabit Ethernet ports (PHY PN: 88E1111-B2-NDC2C000)
    - 2x 10Gb/s SFP+ ports
    - Display port (DP)
    - SDI/SDO video port
    - SPI port
    - UART port
  - FPGA Debug ports:
    - 16-bit Trace port (FPGA Trace)

- General user I/O
  - LEDs and displays
    - 4x FPGA user LEDs
    - 4x HPS user LEDs
    - Configuration load LED
    - Configuration done LED
    - Error LED
    - 3x Configuration select LEDs
    - 4x On-board USB-Blaster II status LEDs
    - 2x FMC interface LEDs
    - 2x UART data transmit and receive LEDs
    - Power on LED
    - Two-line character LCD display
  - Push buttons
    - CPU cold reset push button and one CPU warm reset push button
    - Logic reset push button
    - Program select push button
    - Program configuration push button
    - 4x FPGA user push buttons
    - 4x HPS user push buttons
    - External interrupt push button
  - DIP Switches
    - JTAG chain control DIP switch
    - Board settings DIP switch
    - FPGA configuration mode DIP switch
    - General user DIP switch
  - Power supply
    - 12V DC Input
  - Mechanical
    - 7.175" x 9.3" rectangular form factor

Recommended Operating Conditions

- Recommended ambient operating temperature range: 0C to 45C
- Maximum ICC load current: 36A
- Maximum ICC load transient percentage: 30%
- FPGA maximum power supported by the supplied heatsink/fan: 40W

Handling the Board

When handling the board, it is important to observe static discharge precautions.

Caution: Without proper anti-static handling, the board can be damaged. Therefore, use anti-static handling precautions when touching the board.

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Board Inspection

To inspect each board, perform these steps:

1. Place the board on an anti-static surface and inspect it to ensure that it has not been damaged during shipment.

   Caution: Without proper anti-static handling, you can damage the board.
2. Verify that all components on the boards appear in place and intact.

For more information about power consumption and thermal modeling, refer to *AN358: Thermal Management for FPGAs*.

Table 2-1: Arria 10 SoC Development Kit Contents

Item	Quantity
Arria 10 SoC Development Board	1
USB Cable Mini	2
USB Cable Micro	1
Ethernet Cable	1
MicroSD Daughtercard	1
Quad SPI Daughtercard	1
NAND Daughtercard	1
DDR4 HILO Memory Card	2
Quick Start Guide	1

Related Information

AN358: Thermal Management for FPGAs

Installing the Subscription Edition of the Quartus Prime Design Software

The Quartus® Prime Pro Edition software provides the necessary tools used for developing hardware and software for Altera devices.

Included in the Quartus Prime Pro Edition software are the Quartus Prime software, the Nios II EDS, and the MegaCore IP Library. To install the Altera development tools, download the Quartus Prime Pro Edition Software from the Quartus Prime Pro Edition page in the Download Center of the Altera website.

Related Information

Quartus Prime Software page

Activating Your License

Purchasing this kit entitles you to a one-year license for the Development Kit Edition (DKE) of the Quartus Prime software. After the year, your DKE license will no longer be valid and you will not be permitted to use this version of the Quartus Prime software. To continue using the Quartus Prime software, you should purchase a subscription to Quartus Prime Pro or Standard Edition.

Before using the Quartus Prime software, you must activate your license, identify specific users and computers, and obtain and install a license file. If you already have a licensed version of the subscription edition, you can use that license file with this kit. If not, follow these steps:

1. Log on at the **myAltera Account Sign In** web page, and click **Sign In**.
2. On the myAltera Home web page, click the Self-Service Licensing Center link.
3. Locate the serial number printed on the side of the development kit box below the bottom bar code. The number consists of alphanumeric characters and does not contain hyphens.
4. On the Self-Service Licensing Center web page, click the Find it with your License Activation Code link.
5. In the **Find/Activate Products** dialog box, enter your development kit serial number and click **Search**.
6. When your product appears, turn on the check box next to the product name.
7. Click **Activate Selected Products**, and click **Close**.
8. When licensing is complete, Altera emails a **license.dat** file to you. Store the file on your computer and use the License Setup page of the **Options** dialog box in the Quartus Prime software to enable the software.

Related Information

- **Altera Software Installation and Licensing**
- **myAltera Account Sign In web page**

Installing the Altera SoC Embedded Development Suite (EDS)

The Altera SoC EDS is a comprehensive tool suite for embedded software development on Altera SoC devices. It contains development tools, utility programs, run-time software, and application examples to expedite firmware and application software of SoC embedded systems.

As a part of the Altera SoC EDS, the ARM DS-5 Altera Edition Toolkit provides a comprehensive set of embedded development tools for Altera SoCs.

For more information, refer to the *ARM Development Studio 5 (DS-5) Altera Edition Toolkit*.

For the steps to install the SoC EDS Tool Suite, refer to the *Altera SoC Embedded Design Suite User Guide*.

Related Information

- **ARM Development Studio 5 (DS-5) Altera Edition Toolkit**
- **Altera SoC Embedded Design Suite User Guide**

Development Kit Installer

The development kit installer is an installable archive of supporting documentation. It does not include the software or documentation for the Quartus Prime design software, nor does it include the SoC EDS software development tools.

1. Download the Arria 10 FPGA Development Kit installer from the Arria 10 FPGA Development Kit page of the Altera website. Alternatively, you can request a development kit DVD from the Altera Kit Installations DVD Request Form page of the Altera website.
2. Run the Arria 10 FPGA Development Kit installer.
3. Follow the on-screen instructions to complete the installation process. Be sure that the installation directory you choose is in the same relative location to the Quartus Prime software installation. The installation program creates the development kit directory structure shown in the following figure.

Figure 2-1: Installed Development Kit Directory Structure

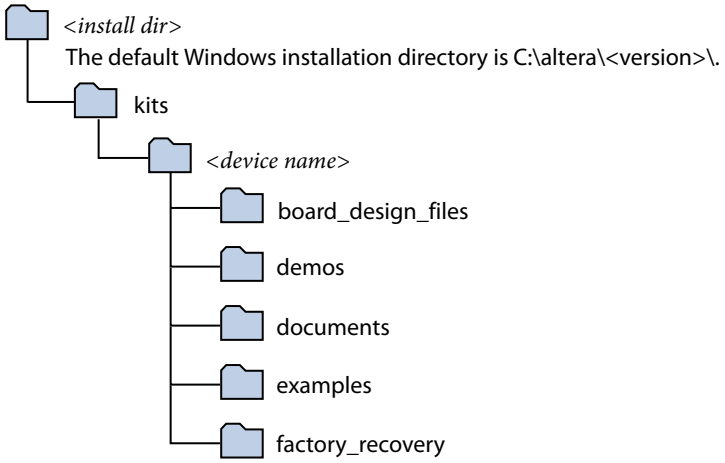

Table 2-2: Installed Directory Contents

Directory Name	Description of Contents
board_design_files	Contains schematic, layout, assembly, and bill of material board design files. Use these files as a starting point for a new prototype board design.
demos	Contains demonstration applications when available.
documents	Contains the documentation.
examples	Contains the sample design files for this kit.
factory_recovery	Contains the original data programmed onto the board before shipment. Use this data to restore the board with its original factory contents.

Installing the USB-Blaster Driver

The development board includes integrated USB-Blaster circuitry for FPGA programming. However, for the host computer and board to communicate, you must install the on-board USB-Blaster II driver on the host computer.

Installation instructions for the on-board USB-Blaster II driver for your operating system are available on the Altera website. On the Altera Programming Cable Driver Information page of the Altera website, locate the table entry for your configuration and click the link to access the instructions.

Related Information

Altera Programming Cable Driver Information

SD Card Image with Example Software

The Arria 10 GSRD (Golden System Reference Design) page on Rocketboards.org has instructions to create an SD card image.

Related Information

GSRD User Manual

Development Board Setup 3

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This section describes how to apply power to the board and provides default switch and jumper settings.

Applying Power to the Board

This development kit ships with its board switches preconfigured to support the design examples in the kit.

If you suspect that your board might not be currently configured with the default settings, follow the instructions in the Default Switch and Jumper Settings section of this chapter.

1. Power up the development board by using the included power supply.

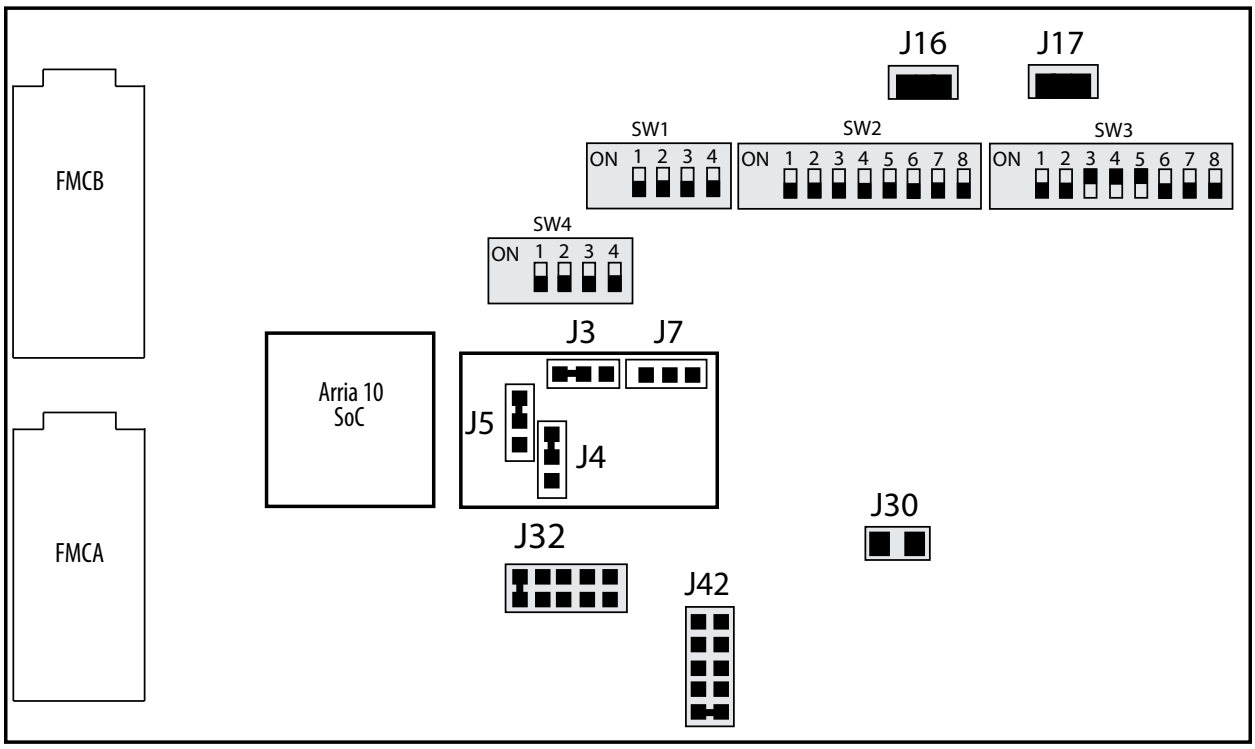
   Caution: Use only the supplied power supply. Power regulation circuitry on the board can be damaged by power supplies with greater voltage, and a lower-rated power supply may not be able to provide enough power for the board.
2. When configuration is complete, the configuration done green LED (D18) illuminates, signaling that the Arria 10 SoC device is configured successfully.

Default Switch and Jumper Settings

This topic shows you how to restore the default factory settings and explains their functions.

Caution: Do not install or remove jumpers (shunts) while the development board is powered on.

Figure 3-1: Default Switch and Jumper Settings



Note: The Switch position is represented by the black box.

To restore the switches to their factory default settings, perform these steps:

1. Set the DIP switch bank (SW1) to match "SW1 DIP Switch Settings" table and the "Default Switch and Jumper Settings" figure.

   Note: In the following table, *ON* indicates the switch is to the upper position according to the board orientation as shown in the "Default Switch and Jumper Settings" figure.

Table 3-1: SW1 Factory Default Settings

Switch	Bit Name	Bit Function	Default Position
1	I^2C flag	Switch 1.1 has the following options: • ON (0) = System MAX V is the I^2C master • OFF (1) = HPS is the I^2C master	OFF
2	DC_POWER_CTRL	Switch 1.2 has the following options: • ON (0) = Power off PCIE slot when it is present • OFF (1) = Power up PCIE directly	OFF
3	factory_load	Switch 1.3 has the following options: • ON (0) = Load user design from flash at power up • OFF (1) = Load factory design from flash at power up	OFF
4	security_mode	Resvered	OFF

Table 3-2: SW4 Switch Settings

Switch	Bit Name	Bit Function	Default Position
1	Reserved	Reserved	OFF
2	MSEL0	Switch 4.2 has the following options: • ON (Up) = MSEL0 is 1 • OFF (Down) = MSEL0 is 0	OFF
3	MSEL1	Switch 4.3 has the following options: • ON (Up) = MSEL1 is 1 • OFF (Down) = MSEL1 is 0	OFF
4	MSEL2	Switch 4.4 has the following options: • ON (Up) = MSEL2 is 1 • OFF (Down) = MSEL2 is 0	OFF

Table 3-3: MSEL Settings for each Configuration Scheme of Arria 10 SoC Devices

Configuration	V_{ccpgm} (V)	Power-On Reset (POR delay)	Valid MSEL [2:0]
JTAG-based configuration	-	-	Use any valid MSEL pin settings below
AS-Active Serial (x1 and x4)	1.8	Fast	010
		Standard	011
PS-Passive Serial	1.2/1.5/1.8	Fast	000
		Standard	001

2. Set the DIP switch bank (SW3) to match the following tables:

Table 3-4: SW3 Factory Default Settings

Switch	Board Label	Function	Default Position
1	Arria 10	ON- Arria 10 JTAG Bypass OFF- Arria 10 JTAG Enable	OFF
2	IO MAX V	ON- MAX V JTAG Bypass OFF- MAX V JTAG Enable	OFF
3	FMCA	ON- FMCA JTAG Bypass OFF- FMCA JTAG Enable	ON
4	FMCB	ON- FMCB JTAG Bypass OFF- FMCB JTAG Enable	ON
5	PCIe	ON- PCIe JTAG Bypass OFF- PCIe JTAG Enable	ON
6	MSTR0	On-Board USB Blaster II JTAG Master	OFF
7	MSTR1	On-Board USB Blaster II JTAG Master	OFF
8	MSTR2	On-Board USB Blaster II JTAG Master	OFF

3. Set the following jumper blocks to match the table below:

Table 3-5: Default Jumper Settings

Board Reference	Board Label	Description	Default Position
J16, J17	OSC2_CLK_SEL	• 00 (SHORT, SHORT): Selects the on-board 25MHz clock • 01 (SHORT, OPEN): Selects SMA clock which connected to J15 • 10 (OPEN, SHORT): Selects the on-board 33MHz clock • 11 (OPEN, OPEN): none	SHORT, SHORT
J30	HPS Core Voltage	• SHORT: HPS core 0.95 V • OPEN: HPS core 0.9 V	OPEN
J32	Voltage of FMCBVADJ	• No SHORT: 1.1 V • SHORT 1 and 2: 1.2 V • SHORT 3 and 4: 1.25 V • SHORT 5 and 6: 1.35 V • SHORT 7 and 8: 1.5 V • SHORT 9 and 10: 1.8 V	SHORT 9 and 10
J42	Voltage of FMCAVADJ	• No SHORT: 1.1 V • SHORT 1 and 2: 1.1 V • SHORT 3 and 4: 1.2 V • SHORT 5 and 6: 1.35 V • SHORT 7 and 8: 1.5 V • SHORT 9 and 10: 1.8 V	SHORT 9 and 10

Table 3-6: Default Jumper BSEL Settings for Micro-SD Daughtercard

Board Reference	Description	Default Position
J3	BSEL0	SHORT left 2 pins
J4	BSEL1	SHORT upper 2 pins(1)
J5	BSEL2	SHORT upper 2 pins(1)

Related Information

Board Settings DIP Switch on page 5-19

(1) The directions of these pins are in reference to the board arrangement as in the "Default Switch and Jumper Settings" figure.

Board Test System

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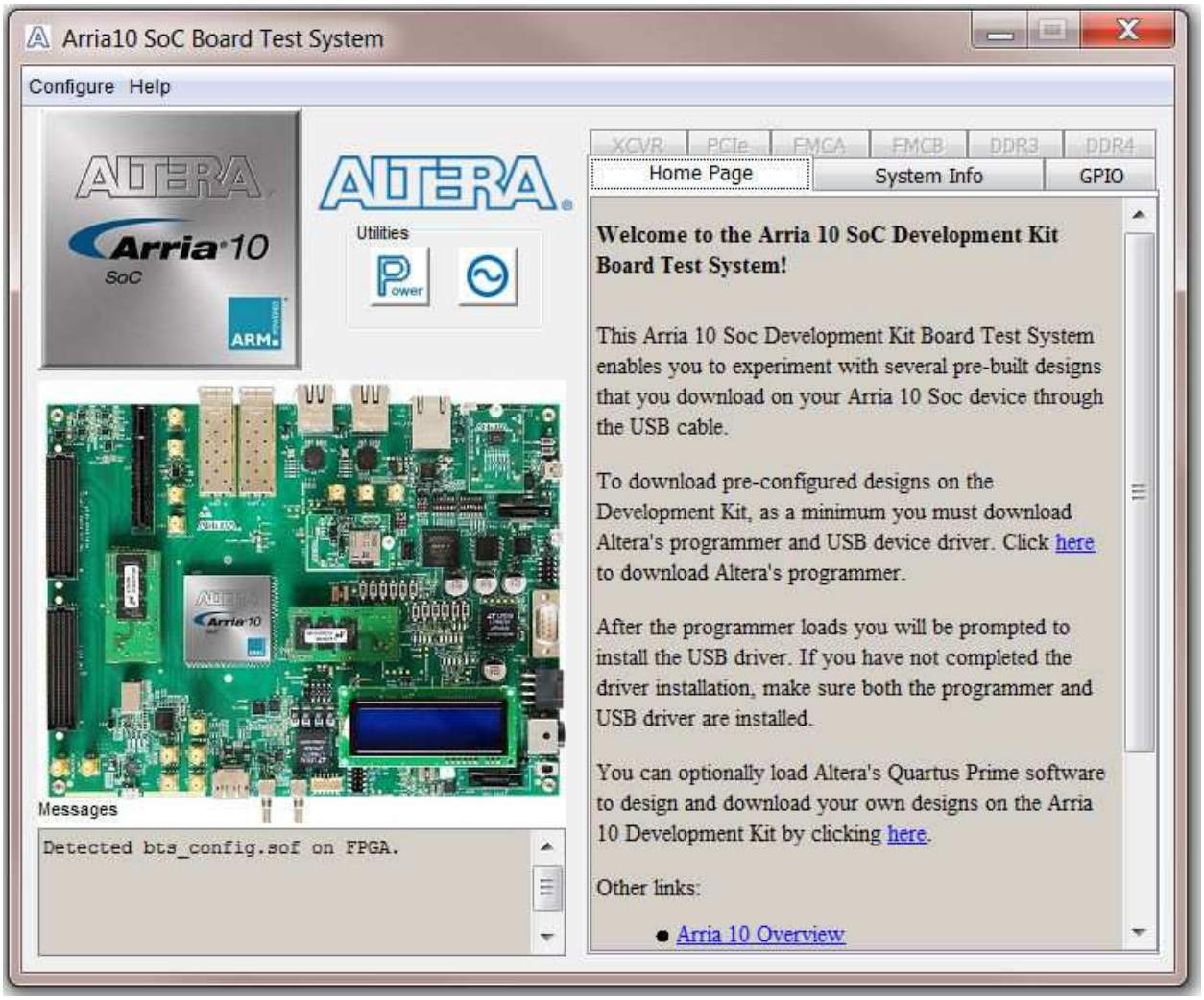
This kit includes an application called the Board Test System (BTS). The BTS provides an easy-to-use interface to alter functional settings and observe the results.

Figure 4-1: Board Test System GUI



You can use the BTS to test board components, modify functional parameters, observe performance, and measure power usage. While using the BTS, you reconfigure the FPGA several times with test designs specific to the functionality you are testing.

Several designs are provided to test the major board features. Each design provides data for one or more tabs in the application. The Configure menu identifies the appropriate design to download to the FPGA for each tab.

After successful FPGA configuration, the appropriate tab appears that allows you to exercise the related board features. Highlights appear in the board picture around the corresponding components.

The BTS communicates over the JTAG bus to a test design running in the FPGA. The Board Test System and Power Monitor share the JTAG bus with other applications like the Nios II debugger and the SignalTap® II Embedded Logic Analyzer.

Note: Because the BTS is designed based on the Quartus Prime Programmer and system console, be sure to close the other applications before you use the BTS application.

Preparing the Board

After successful FPGA configuration, follow these steps:

1. Connect the USB cable to your PC and the USB Blaster II port.
2. Change SW1 and SW3 to the following configuration:

Table 4-1: SW1 GUI Mode

Bit1	Bit2	Bit3	Bit4
ON	OFF	OFF	OFF

Table 4-2: SW3 GUI Mode

Bit1	Bit2	Bit3	Bit4	Bit5	Bit6	Bit7	Bit8
OFF	OFF	ON	ON	ON	OFF	ON	OFF

3. Run the BTS with Quartus Prime 15.1 Programmer.

   The application cannot run correctly unless Quartus Prime 15.1 Programmer is opened.

   Note: Do not use the Auto Detect function in the Quatus Prime Programmer. It may cause the board power to reset.

Running the Board Test System

To run the Board Test System (BTS), navigate to the **<Package Root Dir>\examples\board_test_system** directory and run the **BoardTestSystem.exe** application.

On Windows, you can also run the BTS from the **Start** > **All Programs** > **Altera** menu.

The BTS relies on the Quartus Prime software's specific library. Before running the BTS, open the Quartus Prime software to automatically set the environment variable `$QUARTUS_ROOTDIR`. The Board Test System uses this environment variable to locate the Quartus Prime library.

Note: The version of Quartus Prime software set in the `$QUARTUS_ROOTDIR` environment variable should be version 14.1 or later.

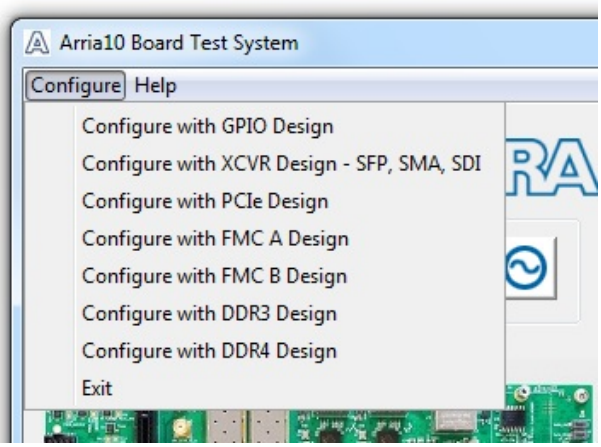
Using the Board Test System

This section describes each control in the Board Test System application.

Using the Configure Menu

Use the Configure menu to select the design you want to use. Each design example tests different board features. Choose a design from this menu and the corresponding tabs become active for testing.

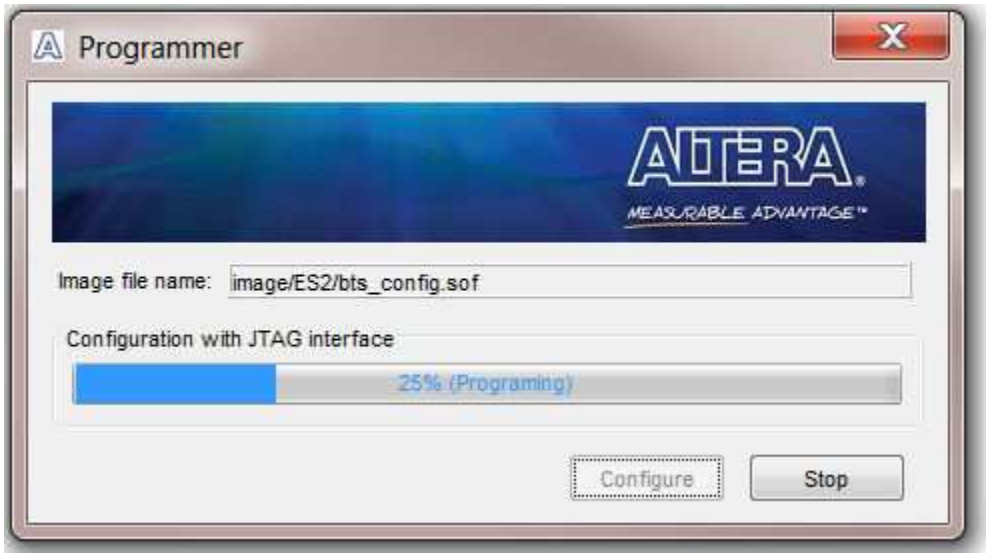
Figure 4-2: The Configure Menu



To configure the FPGA with a test system design, perform the following steps:

1. On the **Configure** menu, click the configure command that corresponds to the functionality you wish to test.
2. In the dialog box that appears, click **Configure** to download the corresponding design to the FPGA.

Figure 4-3: Programmer Dialog Window



The System Info Tab

The System Info tab shows the board's current configuration. The tab displays the JTAG chain, the Qsys memory map, and other details stored on the board.

Figure 4-4: The System Info Tab

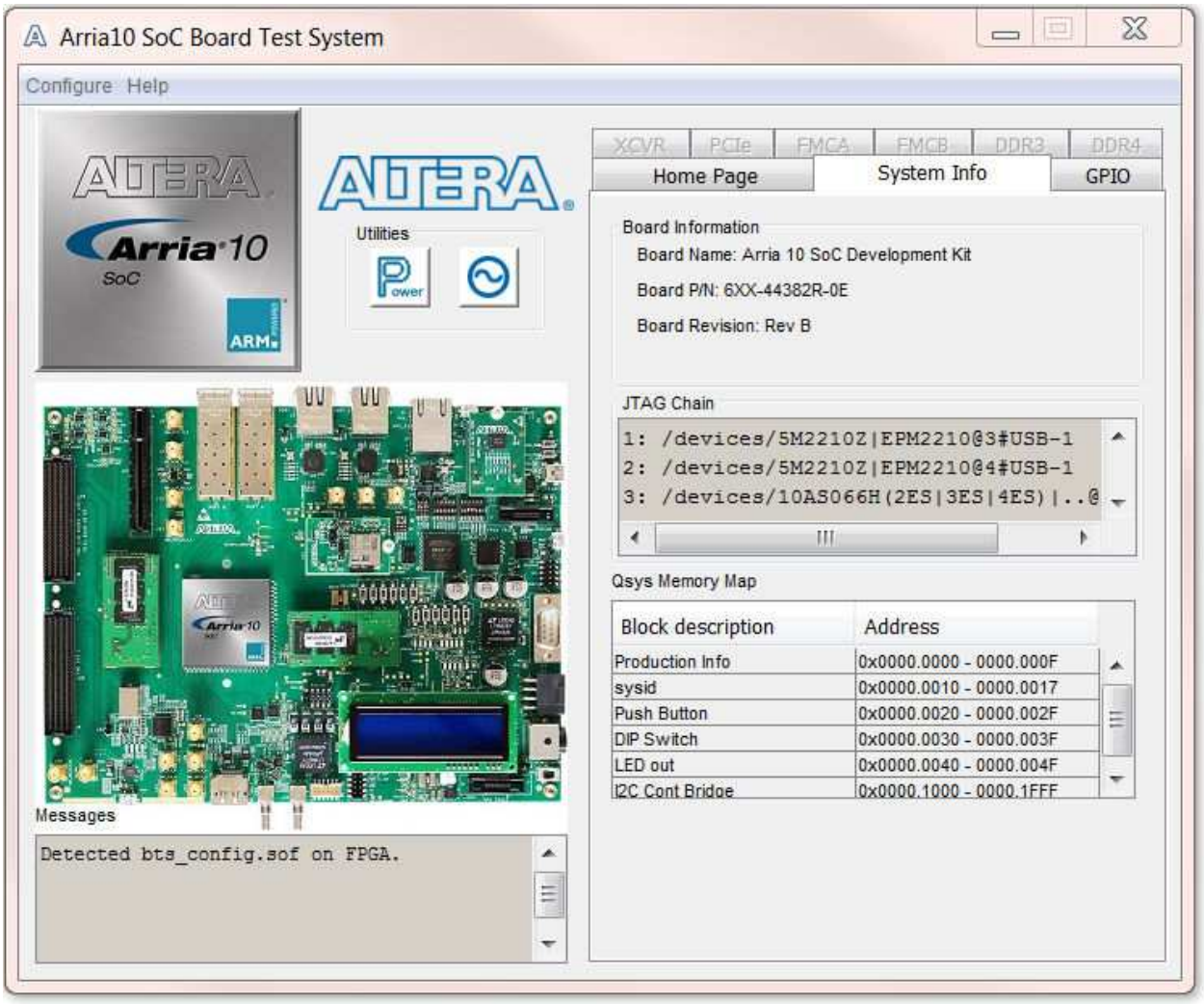


Table 4-3: Controls on the System Info Tab

Controls	Description
Board Information	The board information is updated once the GPIO design is configured. Otherwise, this control displays the default static information about your board.
Board Name	Indicates the official name of the board, given by the Board Test System.
Board P/N	Indicates the part number of the board.
Serial Number	Indicates the serial number of the board.

Controls	Description
Factory Test Version	Indicates the version of the Board Test System currently running on the board.
JTAG Chain	Shows all the devices currently in the JTAG chain.
Qsys Memory Map	Shows the memory map of the Qsys system on your board.

The GPIO Tab

The GPIO tab allows you to interact with all the general purpose user I/O components on your board. You can read DIP switch settings, turn LEDs on or off, and detect push button presses.

Figure 4-5: The GPIO Tab

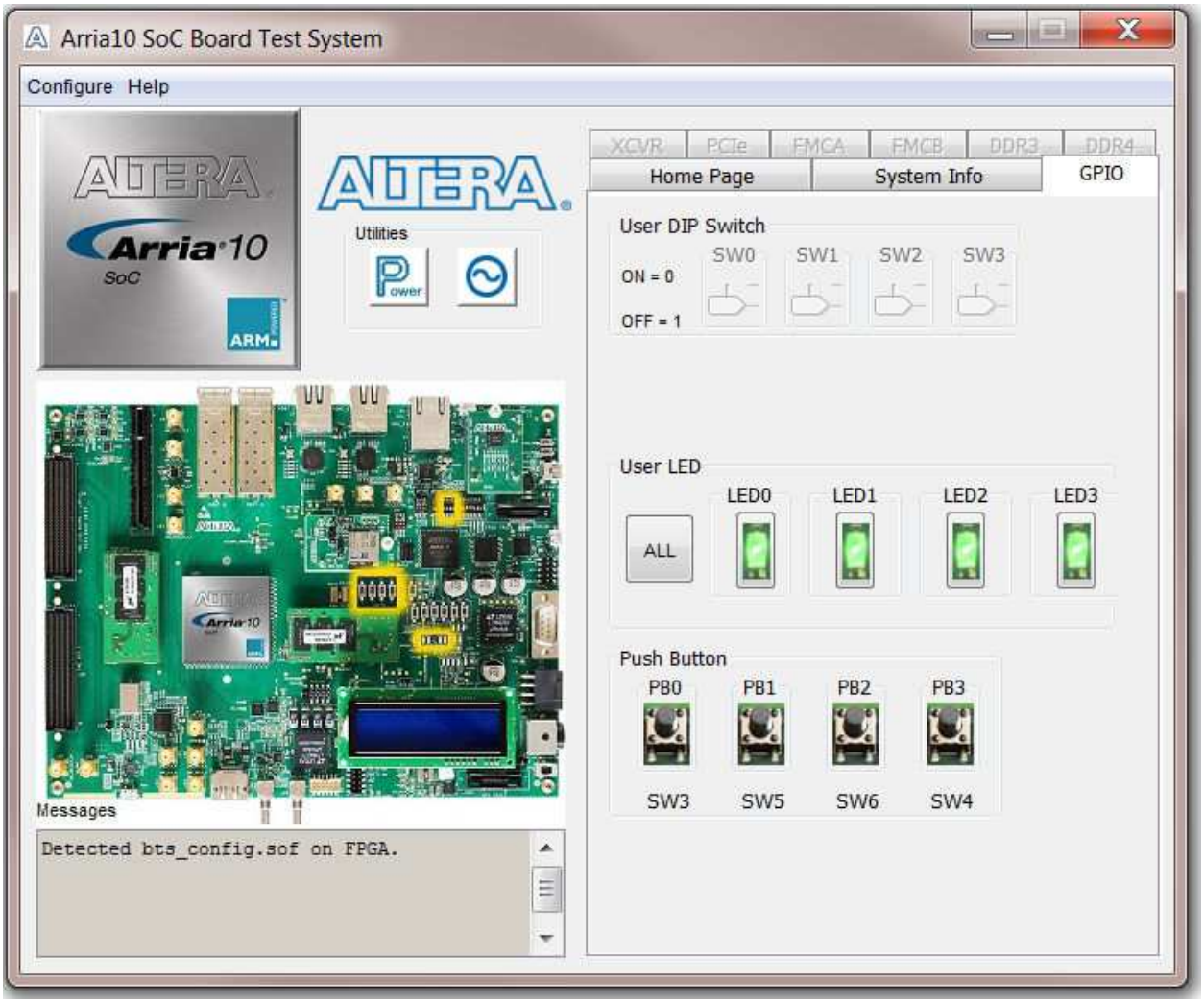


Table 4-4: Controls on the GPIO Tab

User DIP Switch	Displays the current positions of the switches in the user DIP switch bank (SW2). Change the switches on the board to see the graphical display change accordingly.
User LEDs	Displays the current state of the user LEDs for the FPGA. To toggle the board LEDs, click one of the LED [**0** to **3**] buttons to toggle the 4 green LEDs, or click the **All** button.