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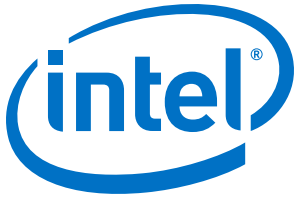

Intel® Stratix® 10 Device Datasheet

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Intel® Stratix® 10 Device Datasheet

This datasheet describes the electrical characteristics, switching characteristics, configuration specifications, and timing for Intel® Stratix® 10 devices.

Table 1. Intel Stratix 10 Device Grades and Speed Grades Supported

Device Grade	Speed Grade Supported
Extended	• –E1V (fastest) • –E2V • –E2L • –E3V • –E3X
Industrial	• –I1V • –I2V • –I2L • –I3V • –I3X

The suffix after the speed grade denotes the power options offered in Intel Stratix 10 devices.

- V—SmartVID with standard static power
- L—0.85 V fixed voltage with low static power
- X—0.80 V fixed voltage with lowest static power

Table 2. Data Status for Intel Stratix 10 Devices

Variant	Data Status
Intel Stratix 10 GX (L-Tile)	Final
Intel Stratix 10 GX (H-Tile and E-Tile)	Preliminary
Intel Stratix 10 SX	Preliminary
Intel Stratix 10 TX	Preliminary
Intel Stratix 10 MX	Preliminary

Electrical Characteristics

The following sections describe the operating conditions and power consumption of Intel Stratix 10 devices.

Operating Conditions

Intel Stratix 10 devices are rated according to a set of defined parameters. To maintain the highest possible performance and reliability of the Intel Stratix 10 devices, you must consider the operating requirements described in this section.

Absolute Maximum Ratings

This section defines the maximum operating conditions for Intel Stratix 10 devices. The values are based on experiments conducted with the devices and theoretical modeling of breakdown and damage mechanisms. The functional operation of the device is not implied for these conditions.

Caution: Conditions outside the range listed in the following table may cause permanent damage to the device. Additionally, device operation at the absolute maximum ratings for extended periods of time may have adverse effects on the device.

Table 3. Absolute Maximum Ratings for Intel Stratix 10 Devices—Preliminary

Symbol	Description	Condition	Minimum	Maximum	Unit
V_{CC}	Core voltage power supply	—	–0.50	1.26	V
V_{CCP}	Periphery circuitry and transceiver fabric interface power supply	—	–0.50	1.26	V
V_{CCERAM}	Embedded memory and digital transceiver power supply	—	–0.50	1.24	V

continued...

Symbol	Description	Condition	Minimum	Maximum	Unit
V_{CCPT}	Power supply for programmable power technology and I/O pre-driver	—	–0.50	2.46	V
V_{CCBAT}	Battery back-up power supply for design security volatile key register	—	–0.50	2.46	V
V_{CCIO_SDM}	Configuration pins power supply	—	–0.50	2.19	V
V_{CCIO}	I/O buffers power supply	3 V I/O	–0.50	4.10	V
		LVDS I/O (1)	–0.50	2.19	V
V_{CCA_PLL}	Phase-locked loop (PLL) analog power supply	—	–0.50	2.46	V
V_{CCT_GXB}	Transmitter analog power supply	—	–0.50	1.47	V
V_{CCR_GXB}	Receiver analog power supply	—	–0.50	1.47	V
V_{CCH_GXB}	Transmitter output buffer power supply	—	–0.50	2.46	V
V_{CCL_HPS}	HPS core voltage and periphery circuitry power supply	—	–0.50	1.30	V
V_{CCIO_HPS}	HPS I/O buffers power supply	LVDS I/O (1)	–0.50	2.19	V
V_{CCPLL_HPS}	HPS PLL power supply	—	–0.50	2.46	V
V_I	DC input voltage	3 V I/O	–0.30	3.80	V
		LVDS I/O	–0.30	2.19	V
I_{OUT}	DC output current per pin	—	–15 (2)(3)(4)(5)(6)	15	mA
T_J	Operating junction temperature	—	–55	125	°C
T_{STG}	Storage temperature (no bias)	—	–55	150	°C

(1) The LVDS I/O values are applicable to all dedicated and dual-function configuration I/Os.

(2) The maximum current allowed through any LVDS I/O bank pin when the device is not turned on or during power-up/power-down conditions is 10 mA.

(3) Total current per LVDS I/O bank must not exceed 100 mA.

(4) Voltage level must not exceed 1.89 V.

(5) Applies to all I/O standards and settings supported by LVDS I/O banks, including single-ended and differential I/Os.

Related Information

- AN 692: Power Sequencing Considerations for Intel Cyclone 10 GX, Intel Arria 10, and Intel Stratix 10 Devices
  Provides the power sequencing requirements for Intel Stratix 10 devices.
- Power Sequencing Considerations for Intel Stratix 10 Devices, Intel Stratix 10 Power Management User Guide
  Provides the power sequencing requirements for Intel Stratix 10 devices.

Maximum Allowed Overshoot and Undershoot Voltage

During transitions, input signals may overshoot to the voltage listed in the following table and undershoot to –1.1 V for input currents less than 100 mA and periods shorter than 20 ns.

The maximum allowed overshoot duration is specified as a percentage of high time over the lifetime of the device. A DC signal is equivalent to 100% duty cycle.

For example, when using V_{CCIO} = 1.8 V, a signal that overshoots to 2.44 V for LVDS I/O can only be at 2.44 V for ~6% over the lifetime of the device.

Table 4. Maximum Allowed Overshoot During Transitions for Intel Stratix 10 Devices (for LVDS I/O)—Preliminary

This table lists the maximum allowed input overshoot voltage and the duration of the overshoot voltage as a percentage of device lifetime. The LVDS I/O values are applicable to the VREFP_ADC and VREFN_ADC I/O pins.

Symbol	Description	LVDS I/O (V) (7)	Overshoot Duration as % at T_J = 100°C	Unit
Vi (AC)	AC input voltage	V_{CCIO} + 0.30	100	%
		V_{CCIO} + 0.35	60	%
		V_{CCIO} + 0.40	30	%
		V_{CCIO} + 0.45	20	%

continued...

(6) Applies only to LVDS I/O banks. 3 V I/O banks are not covered under this specification and must be implemented as per the power sequencing requirement. For more details, refer to *AN 692: Power Sequencing Considerations for Intel Cyclone® 10 GX, Intel Arria® 10, and Intel Stratix 10 Devices* and *Intel Stratix 10 Power Management User Guide*.

(7) The LVDS I/O values are applicable to all dedicated and dual-function configuration I/Os.

Symbol	Description	LVDS I/O (V) (7)	Overshoot Duration as % at T_J = 100°C	Unit
		V_{CCIO} + 0.50	10	%
		V_{CCIO} + 0.55	6	%
		> V_{CCIO} + 0.55	No overshoot allowed	%

Table 5. Maximum Allowed Overshoot During Transitions for Intel Stratix 10 Devices (for 3 V I/O)—Preliminary

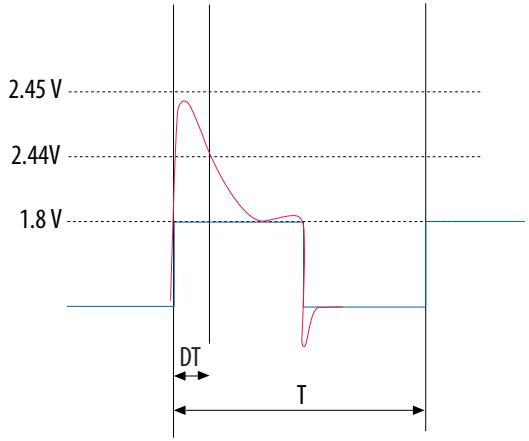
This table lists the maximum allowed input overshoot voltage and the duration of the overshoot voltage as a percentage of device lifetime.

Symbol	Description	3 V I/O (V)	Overshoot Duration as % at T_J = 100°C	Unit
Vi (AC)	AC input voltage	V_{CCIO} + 0.65	100	%
		V_{CCIO} + 0.70	42	%
		V_{CCIO} + 0.75	18	%
		V_{CCIO} + 0.80	9	%
		V_{CCIO} + 0.85	4	%
		> V_{CCIO} + 0.85	No overshoot allowed	%

For an overshoot of 2.5 V, the percentage of high time for the overshoot can be as high as 100% over a 10-year period. Percentage of high time is calculated as ([delta T]/T) × 100. This 10-year period assumes that the device is always turned on with 100% I/O toggle rate and 50% duty cycle signal.

(7) The LVDS I/O values are applicable to all dedicated and dual-function configuration I/Os.

Figure 1. Intel Stratix 10 Devices Overshoot Duration



Recommended Operating Conditions

This section lists the functional operation limits for the AC and DC parameters for Intel Stratix 10 devices.

Recommended Operating Conditions

Table 6. Recommended Operating Conditions for Intel Stratix 10 Devices—Preliminary

This table lists the steady-state voltage values expected for Intel Stratix 10 devices. Power supply ramps must all be strictly monotonic, without plateaus.

Symbol	Description	Condition	Minimum (8)	Typical	Maximum (8)	Unit
V_{CC}	Core voltage power supply	–E1V, –I1V, –E2V, –I2V, –E3V, –I3V (9)	(Typical) – 30 mV	0.8 – 0.94	(Typical) + 30 mV	V
		–E2L, –I2L	0.82	0.85	0.88	V
		–E3X, –I3X	0.77	0.8	0.83	V
V_{CCP}	Periphery circuitry and transceiver fabric interface power supply	–E1V, –I1V, –E2V, –I2V, –E3V, –I3V (9)	(Typical) – 30 mV	0.8 – 0.94	(Typical) + 30 mV	V
		–E2L, –I2L	0.82	0.85	0.88	V
		–E3X, –I3X	0.77	0.8	0.83	V
V_{CCIO_SDM}	Configuration pins power supply	1.8 V	1.71	1.8	1.89	V
$V_{CCPLLDIG\_SDM}$	Secure Device Manager (SDM) block PLL digital power supply	—	0.87	0.9	0.93	V
V_{CCPLL_SDM}	SDM block PLL analog power supply	—	1.71	1.8	1.89	V
$V_{CCFUSEWR\_SDM}$	Fuse block writing power supply	—	2.35	2.4	2.45	V
V_{CCADC}	ADC voltage sensor power supply	—	1.71	1.8	1.89	V
V_{CCERAM}	Embedded memory and digital transceiver power supply	0.9 V	0.87	0.9	0.93	V
V_{CCBAT} (10)	Battery back-up power supply (For design security volatile key register)	—	1.2	—	1.8	V

continued...

(8) This value describes the required voltage measured between the PCB power and ground ball during normal device operation. The voltage ripple includes both regulator DC ripple and the dynamic noise. Refer to power distribution network (PDN) tool for PCB power distribution network design.

(9) SmartVID graded devices require the use of a configurable voltage regulator or system controller to receive the device's settings through the Power Management Bus (PMBus™) or Pulse-Width Modulation (PWM) interface for proper performance.

Symbol	Description	Condition	Minimum (8)	Typical	Maximum (8)	Unit
V_{CCPT}	Power supply for programmable power technology and I/O pre-driver	1.8 V	1.71	1.8	1.89	V
V_{CCIO}	I/O buffers power supply	3.0 V (for 3 V I/O only)	2.85	3	3.15	V
		2.5 V (for 3 V I/O only)	2.375	2.5	2.625	V
		1.8 V	1.71	1.8	1.89	V
		1.5 V	1.425	1.5	1.575	V
		1.2 V	1.14	1.2	1.26	V
V_{CCIO_UIB}	Power supply for the Universal Interface Bus between the core and embedded HBM2 memory	1.2 V	1.17	1.2	1.23	V
V_{CCM_WORD}	Power supply for the embedded HBM2 memory	—	2.4	2.5	2.6	V
V_{CCA_PLL}	PLL analog voltage regulator power supply	—	1.71	1.8	1.89	V
V_{REFP_ADC}	Precision voltage reference for voltage sensor	—	1.2475	1.25	1.2525	V
V_I (11)(12)	DC input voltage	3 V I/O	–0.3	—	3.6	V
		LVDS I/O	–0.3	—	2.19	V
V_O	Output voltage	—	0	—	V_{CCIO}	V

continued...

(8) This value describes the required voltage measured between the PCB power and ground ball during normal device operation. The voltage ripple includes both regulator DC ripple and the dynamic noise. Refer to power distribution network (PDN) tool for PCB power distribution network design.

(10) If you do not use the design security feature in Intel Stratix 10 devices, connect V_{CCBAT} to a 1.8 V power supply. Intel Stratix 10 power-on reset (POR) circuitry monitors V_{CCBAT}.

(11) The LVDS I/O values are applicable to all dedicated and dual-function configuration I/Os.

(12) This value applies to both input and tri-stated output configuration. Pin voltage should not be externally pulled higher than the maximum value.

Symbol	Description	Condition	Minimum [8]	Typical	Maximum [8]	Unit
T_J	Operating junction temperature	Extended	0	—	100	°C
		Industrial	–40	—	100	°C
t_{RAMP} [13][14][15][16]	Power supply ramp time	Standard POR	200 µs	—	100 ms	—

(8) This value describes the required voltage measured between the PCB power and ground ball during normal device operation. The voltage ripple includes both regulator DC ripple and the dynamic noise. Refer to power distribution network (PDN) tool for PCB power distribution network design.

(13) This is also applicable to HPS power supply. For HPS power supply, refer to t_{RAMP} specifications for standard POR when HPS_PORSEL = 0 and t_{RAMP} specifications for fast POR when HPS_PORSEL = 1.

(14) t_{RAMP} is the ramp time of each individual power supply, not the ramp time of all combined power supplies.

(15) To support AS fast mode, all power supplies to the Intel Stratix 10 device must be fully ramped-up within 10 ms to the recommended operating conditions.

(16) To support AS normal mode, V_{CCIO_SDM} of the Intel Stratix 10 device must be fully ramped-up within 10 ms to the recommended operating condition.

Transceiver Power Supply Operating Conditions

Table 7. Transceiver Power Supply Operating Conditions for Intel Stratix 10 GX/SX L-Tile Devices in a Non-Bonded Configuration

Symbol	Description	Datarate	Minimum	Typical	Maximum	Unit
$V_{CCT\_GXB[L,R]}$ and $V_{CCR\_GXB[L,R]}$	Chip-to-chip (17)	1.0 Gbps to 26.6 Gbps (18) (19)	1.1	1.12	1.14	V
		1.0 Gbps to 17.4 Gbps (18) (19)	1.0	1.03 (20)	1.06	V
	Backplane (21)	1.0 Gbps to 12.5 Gbps (18)	1.0	1.03 (22), (20)	1.06	V
$V_{CCH\_GXB[L,R]}$	Transceiver high voltage power	—	1.750	1.8	1.850	V

(17) Chip-to-chip refers to transceiver links that are short reach and do not require advanced equalization such as decision feedback equalization (DFE).

(18) Stratix 10 transceivers can support data rates below 1.0 Gbps through over sampling.

(19) Bonded channels operating at datarates above 16.0 Gbps require 1.12 V ±20 mV at the pin. For channels that are placed on the same tile as the channels that require 1.12 V ±20 mV, V_{CCR_GXB} and V_{CCT_GXB} = 1.12 V ±20 mV.

(20) For a 1.03-V typical voltage, the maximum/minimum should be ± 30 mV; hence, V_{MAX} = 1.06 V. However, when these channels share the power supply with channels requiring a 1.12-V typical voltage, these channels should increase typical voltage to 1.12 V, with a maximum/minimum ± 20 mV; hence V_{MAX} = 1.14 V.

(21) Backplane applications refer to ones which require advanced equalization, such as DFE enabled, to compensate for channel loss.

(22) Refer to the Intel Quartus® Prime Pro Edition software for the typical nominal value.

Table 8. Transceiver Power Supply Operating Conditions for Intel Stratix 10 GX/SX L-Tile Devices in a Bonded Configuration

Symbol	Description	Datarate	Minimum	Typical	Maximum	Unit
$V_{CCT\_GXB[L,R]}$ and $V_{CCR\_GXB[L,R]}$	Chip-to-chip (17)	1.0 Gbps to 16.0 Gbps (18)	1.0	1.03 (20)	1.06	V
		> 16.0 Gbps to 17.4 Gbps (18) (19)	1.1	1.12	1.14	V
	Backplane (21)	1.0 Gbps to 12.5 Gbps (18)	1.0	1.03 (22), (20)	1.06	V
$V_{CCH\_GXB[L,R]}$	Transceiver high voltage power	—	1.750	1.8	1.850	V

Table 9. Transceiver Power Supply Operating Conditions for Intel Stratix 10 H-Tile Devices in a Non-Bonded Configuration

Symbol	Description	Datarate	Minimum	Typical	Maximum	Unit
$V_{CCT\_GXB[L,R]}$ and $V_{CCR\_GXB[L,R]}$	Chip-to-chip (17)and Backplane (21)	1.0 Gbps to 28.3 Gbps (GXT) (18)	1.1	1.12	1.14	V
		1.0 Gbps to 17.4 Gbps (GX) (18)	1.01	1.03 (20)	1.06	V
$V_{CCH\_GXB[L,R]}$	Transceiver high voltage power	—	1.750	1.8	1.850	V

Table 10. Transceiver Power Supply Operating Conditions for Intel Stratix 10 H-Tile Devices in a Bonded Configuration

Symbol	Description	Datarate	Minimum	Typical	Maximum	Unit
$V_{CCT\_GXB[L,R]}$ and $V_{CCR\_GXB[L,R]}$	Chip-to-chip (17) and Backplane (21)	1.0 Gbps to 16.0 Gbps (18)	1.01	1.03 (20)	1.06	V
		> 16.0 Gbps to 17.4 Gbps (18)	1.1	1.12	1.14	V
		> 17.4 Gbps to 28.3 Gbps (18)	1.10	1.12	1.14	V
$V_{CCH\_GXB[L,R]}$	Transceiver high voltage power	—	1.750	1.8	1.850	V

Note: Most VCCR_GXB and VCCT_GXB pins associated with unused transceiver channels can be grounded on a per-tile basis to minimize power consumption. Refer to the *Intel Stratix 10 Device Family Pin Connection Guidelines* and the Intel Quartus Prime pin report for information about pinning out the package to minimize power consumption for your specific design.

Table 11. Transceiver Power Supply Operating Conditions for Intel Stratix 10 TX/MX E-Tile Devices—Preliminary

Symbol	Description	Minimum (23)	Typical	Maximum (23)	Unit
V_{CCERT}	Transceiver power supply	0.87	0.9	0.93	V
V_{CCERT_PLL}	Transceiver PLL power supply	0.87	0.9	0.93	V
V_{CCEHT}	Analog power supply (23)	1.067	1.1	1.133	V
V_{CCL}	Periphery circuitry power supply	0.725	0.75	0.775	V
$V_{CCN2P5V\_IO}$	LVPECL REFCLK power supply	2.375	2.5	2.625	V
V_{CCR}	Transceiver high voltage power supply	1.71	1.8	1.89	V

Related Information

Intel Stratix 10 Device Family Pin Connection Guidelines

HPS Power Supply Operating Conditions

Table 12. HPS Power Supply Operating Conditions for Intel Stratix 10 Devices—Preliminary

This table lists the steady-state voltage and current values expected for Intel Stratix 10 system-on-a-chip (SoC) devices with ARM®-based hard processor system (HPS). Power supply ramps must all be strictly monotonic, without plateaus. Refer to Recommended Operating Conditions for Intel Stratix 10 Devices table for the steady-state voltage values expected from the FPGA portion of the Intel Stratix 10 SoC devices.

Symbol	Description	Condition	Minimum	Typical	Maximum	Unit
V_{CCL_HPS}	HPS core voltage and periphery circuitry power supply	–E2L, –I2L, –E3X, –I3X	0.87	0.9	0.93	V
			0.91	0.94	0.97	V

continued...

(23) This value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the PDN tool for the additional budget for the dynamic tolerance requirements.

Symbol	Description	Condition	Minimum	Typical	Maximum	Unit
		–E1V, –I1V, –E2V, –I2V, –E3V, –I3V (24)	0.77 – 0.91	0.8 – 0.94	0.83 – 0.97	V
$V_{CCPLLDIG\_HPS}$	HPS PLL digital power supply	–E2L, –I2L, –E3X, –I3X	0.87	0.9	0.93	V
			0.91	0.94	0.97	V
		–E1V, –I1V, –E2V, –I2V, –E3V, –I3V (24)	0.77 – 0.91	0.8 – 0.94	0.83 – 0.97	V
V_{CCPLL_HPS}	HPS PLL analog power supply	1.8 V	1.71	1.8	1.89	V
V_{CCIO_HPS}	HPS I/O buffers power supply	1.8 V	1.71	1.8	1.89	V

Related Information

- Recommended Operating Conditions on page 9
  Provides the steady-state voltage values for the FPGA portion of the device.
- HPS Clock Performance - Preliminary on page 60

DC Characteristics

Supply Current and Power Consumption

Intel offers two ways to estimate power for your design—the Excel-based Early Power Estimator (EPE) and the Intel Quartus Prime Power Analyzer feature.

Use the Excel-based EPE before you start your design to estimate the supply current for your design. The EPE provides a magnitude estimate of the device power because these currents vary greatly with the usage of the resources.

The Intel Quartus Prime Power Analyzer provides better quality estimates based on the specifics of the design after you complete place-and-route. The Power Analyzer can apply a combination of user-entered, simulation-derived, and estimated signal activities that, when combined with detailed circuit models, yield very accurate power estimates.

(24) SmartVID graded devices require the use of a configurable voltage regulator or system controller to receive the device's settings through PMBUS or PWM for proper performance.

I/O Pin Leakage Current

Table 13. I/O Pin Leakage Current for Intel Stratix 10 Devices—Preliminary

Symbol	Description	Condition	Min	Max	Unit
I_I	Input pin	V_I = 0 V to $V_{CCIOMAX}$	–80	80	µA
I_{OZ}	Tri-stated I/O pin	V_O = 0 V to $V_{CCIOMAX}$	–80	80	µA

Bus Hold Specifications

The bus-hold trip points are based on calculated input voltages from the JEDEC standard.

Table 14. Bus Hold Parameters for Intel Stratix 10 Devices—Preliminary

Parameter	Symbol	Condition	V_{CCIO} (V)										Unit
			1.2		1.5		1.8		2.5		3.0		
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Bus-hold, low, sustaining current	I_{SUSL}	$V_{IN} > V_{IL}$ (max)	8	—	12	—	30	—	60	—	70	—	µA
Bus-hold, high, sustaining current	I_{SUSH}	$V_{IN} < V_{IH}$ (min)	–8	—	–12	—	–30	—	–60	—	–70	—	µA
Bus-hold, low, overdrive current	I_{ODL}	0 V < V_{IN} < V_{CCIO}	—	125	—	175	—	200	—	300	—	500	µA
Bus-hold, high, overdrive current	I_{ODH}	0 V < V_{IN} < V_{CCIO}	—	–125	—	–175	—	–200	—	–300	—	–500	µA
Bus-hold trip point	V_{TRIP}	—	0.3	0.9	0.38	1.13	0.68	1.07	0.7	1.7	0.8	2	V

OCT Calibration Accuracy Specifications

If you enable on-chip termination (OCT) calibration, calibration is automatically performed at power up for I/Os connected to the calibration block.

Table 15. OCT Calibration Accuracy Specifications for Intel Stratix 10 Devices—Preliminary

Calibration accuracy for the calibrated on-chip series termination (R_S OCT) and on-chip parallel termination (R_T OCT) are applicable at the moment of calibration. When process, voltage, and temperature (PVT) conditions change after calibration, the tolerance may change.

Symbol	Description	Condition (V)	Calibration Accuracy			Unit
			–E1, –I1	–E2, –I2	–E3, –I3	
34-Ω, 48-Ω, 60-Ω, 80-Ω, 120-Ω, and 240-Ω R_S	Internal series termination with calibration (34-Ω, 48-Ω, 60-Ω, 80-Ω, 120-Ω, and 240-Ω setting)	V_{CCIO} = 1.2	±15	±15	±15	%
34-Ω and 40-Ω R_S	Internal series termination with calibration (34-Ω and 40-Ω setting)	V_{CCIO} = 1.5, 1.35, 1.25, 1.2	±15	±15	±15	%
25-Ω and 50-Ω R_S	Internal series termination with calibration (25-Ω and 50-Ω setting)	V_{CCIO} = 1.8, 1.5, 1.2	±15	±15	±15	%
34-Ω, 40-Ω, 48-Ω, 60-Ω, 80-Ω, 120-Ω, and 240-Ω R_T	Internal parallel termination with calibration (34-Ω, 40-Ω, 48-Ω, 60-Ω, 80-Ω, 120-Ω, and 240-Ω setting)	POD12 I/O standard, V_{CCIO} = 1.2	±15	±15	±15	%
48-Ω, 50-Ω, 60-Ω, and 120-Ω R_T	Internal parallel termination with calibration (48-Ω, 50-Ω, 60-Ω, and 120-Ω setting)	V_{CCIO} = 1.5, 1.2	–10 to +60	–10 to +60	–10 to +60	%
48-Ω, 60-Ω, and 120-Ω R_T	Internal parallel termination with calibration (48-Ω, 60-Ω, and 120-Ω setting)	V_{CCIO} = 1.25	–10 to +70	–10 to +70	–10 to +70	%
48-Ω, 60-Ω, and 120-Ω R_T	Internal parallel termination with calibration (48-Ω, 60-Ω, and 120-Ω setting)	V_{CCIO} = 1.35	–10 to +65	–10 to +65	–10 to +65	%
50-Ω R_T	Internal parallel termination with calibration (50-Ω setting)	V_{CCIO} = 1.8	–10 to +50	–10 to +50	–10 to +50	%

OCT Without Calibration Resistance Tolerance Specifications

Table 16. OCT Without Calibration Resistance Tolerance Specifications for Intel Stratix 10 Devices—Preliminary

This table lists the Intel Stratix 10 OCT without calibration resistance tolerance to PVT changes.

Symbol	Description	I/O Buffer Type	Condition (V)	Resistance Tolerance			Unit
				–E1, –I1	–E2, –I2	–E3, –I3	
25-Ω and 50-Ω R_S	Internal series termination without calibration (25-Ω and 50-Ω setting)	3 V I/O	V_{CCIO} = 3.0, 2.5, 1.8, 1.5, 1.2	–40 to +30	±40	±40	%
25-Ω and 50-Ω R_S	Internal series termination without calibration (25-Ω and 50-Ω setting)	LVDS I/O	V_{CCIO} = 1.8, 1.5, 1.2	–20 to +35	–20 to +35	–20 to +35	%
34-Ω and 40-Ω R_S	Internal series termination without calibration (34-Ω and 40-Ω setting)	LVDS I/O	V_{CCIO} = 1.5, 1.35, 1.25, 1.2	–20 to +35	–20 to +35	–20 to +35	%
48-Ω, 60-Ω, 80-Ω, and 240-Ω R_S	Internal series termination without calibration (48-Ω, 60-Ω, 80-Ω, and 240-Ω setting)	LVDS I/O	V_{CCIO} = 1.2	–20 to +35	–20 to +35	–20 to +35	%
100-Ω R_D	Internal differential termination (100-Ω setting)	LVDS I/O	V_{CCIO} = 1.8	±25	±35	±40	%

Pin Capacitance

Table 17. Pin Capacitance for Intel Stratix 10 Devices

Symbol	Description	Maximum	Unit
C_{IO_COLUMN}	Input capacitance on column I/O pins	3.5	pF
C_{OUTFB}	Input capacitance on dual-purpose clock output/feedback pins	3.5	pF

Internal Weak Pull-Up Resistor

All I/O pins, except configuration, test, and JTAG pins, have an option to enable weak pull-up. For SDM and HPS, the configuration I/O and peripheral I/O are supported with weak pull-up and weak pull-down options.

Table 18. Internal Weak Pull-Up Resistor Values for Intel Stratix 10 Devices—Preliminary

Symbol	Description	Condition (V)	Nominal Value	Resistance Tolerance	Unit
R_{PU}	Value of the I/O pin pull-up resistor before and during configuration, as well as user mode if you have enabled the programmable pull-up resistor option.	V_{CCIO} = 3.0 ±5%	25	±25%	kΩ
		V_{CCIO} = 2.5 ±5%	25	±25%	kΩ
		V_{CCIO} = 1.8 ±5%	25	±25%	kΩ
		V_{CCIO} = 1.5 ±5%	25	±25%	kΩ
		V_{CCIO} = 1.35 ±5%	25	±25%	kΩ
		V_{CCIO} = 1.25 ±5%	25	±25%	kΩ
		V_{CCIO} = 1.2 ±5%	25	±25%	kΩ

Related Information

Intel Stratix 10 Device Family Pin Connection Guidelines
Provides more information about the pins that support internal weak pull-up and internal weak pull-down features.

I/O Standard Specifications

Tables in this section list the input voltage (V_{IH} and V_{IL}), output voltage (V_{OH} and V_{OL}), and current drive characteristics (I_{OH} and I_{OL}) for various I/O standards supported by Intel Stratix 10 devices.

For minimum voltage values, use the minimum V_{CCIO} values. For maximum voltage values, use the maximum V_{CCIO} values.

You must perform timing closure analysis to determine the maximum achievable frequency for general purpose I/O standards.

Related Information

Recommended Operating Conditions on page 9

Single-Ended I/O Standards Specifications

Table 19. Single-Ended I/O Standards Specifications for Intel Stratix 10 Devices—Preliminary

I/O Standard	V_{CCIO} (V)			V_{IL}(V)		V_{IH}(V)		V_{OL} (V)	V_{OH} (V)	I_{OL} (25) (mA)	I_{OH} (25) (mA)
	Min	Typ	Max	Min	Max	Min	Max	Max	Min		
3.0-V LVTTL	2.85	3	3.15	–0.3	0.8	1.7	3.6	0.4	2.4	2	–2
3.0-V LVCMOS	2.85	3	3.15	–0.3	0.8	1.7	3.6	0.2	V_{CCIO} – 0.2	0.1	–0.1
2.5 V	2.375	2.5	2.625	–0.3	0.7	1.7	3.3	0.4	2	1	–1
1.8 V	1.71	1.8	1.89	-0.3	0.35 × V_{CCIO}	0.65 × V_{CCIO}	V_{CCIO} + 0.3	0.45	V_{CCIO} – 0.45	2	–2
1.5 V	1.425	1.5	1.575	–0.3	0.35 × V_{CCIO}	0.65 × V_{CCIO}	V_{CCIO} + 0.3	0.25 × V_{CCIO}	0.75 × V_{CCIO}	2	–2
1.2 V	1.14	1.2	1.26	–0.3	0.35 × V_{CCIO}	0.65 × V_{CCIO}	V_{CCIO} + 0.3	0.25 × V_{CCIO}	0.75 × V_{CCIO}	2	–2
Schmitt Trigger Input	1.71	1.8	1.89	—	0.35 × V_{CCIO}	0.65 × V_{CCIO}	—	—	—	—	—

Single-Ended SSTL, HSTL, and HSUL I/O Reference Voltage Specifications

Table 20. Single-Ended SSTL, HSTL, and HSUL I/O Reference Voltage Specifications for Intel Stratix 10 Devices—Preliminary

I/O Standard	V_{CCIO} (V)			V_{REF} (V)			V_{TT} (V)		
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max
SSTL-18 Class I, II	1.71	1.8	1.89	0.833	0.9	0.969	V_{REF} - 0.04	V_{REF}	V_{REF} + 0.04
SSTL-15 Class I, II	1.425	1.5	1.575	0.49 × V_{CCIO}	0.5 × V_{CCIO}	0.51 × V_{CCIO}	0.49 × V_{CCIO}	0.5 × V_{CCIO}	0.51 × V_{CCIO}
SSTL-135	1.283	1.35	1.45	0.49 × V_{CCIO}	0.5 × V_{CCIO}	0.51 × V_{CCIO}	0.49 × V_{CCIO}	0.5 × V_{CCIO}	0.51 × V_{CCIO}
SSTL-125	1.19	1.25	1.31	0.49 × V_{CCIO}	0.5 × V_{CCIO}	0.51 × V_{CCIO}	0.49 × V_{CCIO}	0.5 × V_{CCIO}	0.51 × V_{CCIO}

continued...

(25) To meet the I_{OL} and I_{OH} specifications, you must set the current strength settings accordingly. For example, to meet the 1.8- V LVCMOS specification (4 mA), you should set the current strength settings to 4 mA. Setting at lower current strength may not meet the I_{OL} and I_{OH} specifications in the datasheet.

I/O Standard	V_{CCIO} (V)			V_{REF} (V)			V_{TT} (V)		
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max
SSTL-12	1.14	1.2	1.26	0.49 × V_{CCIO}	0.5 × V_{CCIO}	0.51 × V_{CCIO}	0.49 × V_{CCIO}	0.5 × V_{CCIO}	0.51 × V_{CCIO}
HSTL-18 Class I, II	1.71	1.8	1.89	0.85	0.9	0.95	—	V_{CCIO}/2	—
HSTL-15 Class I, II	1.425	1.5	1.575	0.68	0.75	0.9	—	V_{CCIO}/2	—
HSTL-12 Class I, II	1.14	1.2	1.26	0.47 × V_{CCIO}	0.5 × V_{CCIO}	0.53 × V_{CCIO}	—	V_{CCIO}/2	—
HSUL-12	1.14	1.2	1.3	0.49 × V_{CCIO}	0.5 × V_{CCIO}	0.51 × V_{CCIO}	—	—	—
POD12	1.14	1.2	1.26	—	Internally calibrated	—	—	V_{CCIO}	—

Single-Ended SSTL, HSTL, and HSUL I/O Standards Signal Specifications

Table 21. Single-Ended SSTL, HSTL, and HSUL I/O Standards Signal Specifications for Intel Stratix 10 Devices—Preliminary

I/O Standard	$V_{IL(DC)}$ (V)		$V_{IH(DC)}$ (V)		$V_{IL(AC)}$ (V)	$V_{IH(AC)}$ (V)	V_{OL} (V)	V_{OH} (V)	I_{OL} (26) (mA)	I_{OH} (26) (mA)
	Min	Max	Min	Max	Max	Min	Max	Min		
SSTL-18 Class I	–0.3	V_{REF} –0.125	V_{REF} + 0.125	V_{CCIO} + 0.3	V_{REF} – 0.25	V_{REF} + 0.25	V_{TT} – 0.603	V_{TT} + 0.603	6.7	–6.7
SSTL-18 Class II	–0.3	V_{REF} –0.125	V_{REF} + 0.125	V_{CCIO} + 0.3	V_{REF} – 0.25	V_{REF} + 0.25	0.28	V_{CCIO} –0.28	13.4	–13.4
SSTL-15 Class I	—	V_{REF} – 0.1	V_{REF} + 0.1	—	V_{REF} – 0.175	V_{REF} + 0.175	0.2 × V_{CCIO}	0.8 × V_{CCIO}	8	–8
SSTL-15 Class II	—	V_{REF} – 0.1	V_{REF} + 0.1	—	V_{REF} – 0.175	V_{REF} + 0.175	0.2 × V_{CCIO}	0.8 × V_{CCIO}	16	–16
SSTL-135	—	V_{REF} – 0.09	V_{REF} + 0.09	—	V_{REF} – 0.16	V_{REF} + 0.16	0.2 × V_{CCIO}	0.8 × V_{CCIO}	—	—
SSTL-125	—	V_{REF} – 0.09	V_{REF} + 0.09	—	V_{REF} – 0.15	V_{REF} + 0.15	0.2 × V_{CCIO}	0.8 × V_{CCIO}	—	—

continued...

(26) To meet the I_{OL} and I_{OH} specifications, you must set the current strength settings accordingly. For example, to meet the SSTL15CI specification (8 mA), you should set the current strength settings to 8 mA. Setting at lower current strength may not meet the I_{OL} and I_{OH} specifications in the datasheet.

I/O Standard	$V_{IL(DC)}$ (V)		$V_{IH(DC)}$ (V)		$V_{IL(AC)}$ (V)	$V_{IH(AC)}$ (V)	V_{OL} (V)	V_{OH} (V)	I_{OL} (26) (mA)	I_{OH} (26) (mA)
	Min	Max	Min	Max	Max	Min	Max	Min		
SSTL-12	—	V_{REF} – 0.10	V_{REF} + 0.10	—	V_{REF} – 0.15	V_{REF} + 0.15	0.2 × V_{CCIO}	0.8 × V_{CCIO}	—	—
HSTL-18 Class I	—	V_{REF} –0.1	V_{REF} + 0.1	—	V_{REF} – 0.2	V_{REF} + 0.2	0.4	V_{CCIO} – 0.4	8	–8
HSTL-18 Class II	—	V_{REF} – 0.1	V_{REF} + 0.1	—	V_{REF} – 0.2	V_{REF} + 0.2	0.4	V_{CCIO} – 0.4	16	–16
HSTL-15 Class I	—	V_{REF} – 0.1	V_{REF} + 0.1	—	V_{REF} – 0.2	V_{REF} + 0.2	0.4	V_{CCIO} – 0.4	8	–8
HSTL-15 Class II	—	V_{REF} – 0.1	V_{REF} + 0.1	—	V_{REF} – 0.2	V_{REF} + 0.2	0.4	V_{CCIO} –0.4	16	–16
HSTL-12 Class I	–0.15	V_{REF} – 0.08	V_{REF} + 0.08	V_{CCIO} + 0.15	V_{REF} – 0.15	V_{REF} + 0.15	0.25 × V_{CCIO}	0.75 × V_{CCIO}	8	–8
HSTL-12 Class II	–0.15	V_{REF} – 0.08	V_{REF} + 0.08	V_{CCIO} + 0.15	V_{REF} – 0.15	V_{REF} + 0.15	0.25 × V_{CCIO}	0.75 × V_{CCIO}	16	–16
HSUL-12	—	V_{REF} – 0.13	V_{REF} + 0.13	—	V_{REF} – 0.22	V_{REF} + 0.22	0.1 × V_{CCIO}	0.9 × V_{CCIO}	—	—
POD12	–0.15	V_{REF} – 0.08	V_{REF} + 0.08	V_{CCIO} + 0.15	V_{REF} – 0.15	V_{REF} + 0.15	—	—	—	—

Differential SSTL I/O Standards Specifications

Table 22. Differential SSTL I/O Standards Specifications for Intel Stratix 10 Devices—Preliminary

I/O Standard	V_{CCIO} (V)			$V_{SWING(DC)}$ (V)		$V_{SWING(AC)}$ (V)		$V_{IX(AC)}$ (V)		
	Min	Typ	Max	Min	Max	Min	Max	Min	Typ	Max
SSTL-18 Class I, II	1.71	1.8	1.89	0.25	V_{CCIO} + 0.6	0.5	V_{CCIO} + 0.6	$V_{CCIO}/2$ – 0.175	—	$V_{CCIO}/2$ + 0.175
SSTL-15 Class I, II	1.425	1.5	1.575	0.2	(27)	$2(V_{IH(AC)} – V_{REF})$	$2(V_{REF} – V_{IL(AC)})$	$V_{CCIO}/2$ – 0.15	—	$V_{CCIO}/2$ + 0.15

continued...

(26) To meet the I_{OL} and I_{OH} specifications, you must set the current strength settings accordingly. For example, to meet the SSTL15CI specification (8 mA), you should set the current strength settings to 8 mA. Setting at lower current strength may not meet the I_{OL} and I_{OH} specifications in the datasheet.

(27) The maximum value for $V_{SWING(DC)}$ is not defined. However, each single-ended signal needs to be within the respective single-ended limits ($V_{IH(DC)}$ and $V_{IL(DC)}$).

I/O Standard	V_{CCIO} (V)			$V_{SWING(DC)}$ (V)		$V_{SWING(AC)}$ (V)		$V_{IX(AC)}$ (V)		
	Min	Typ	Max	Min	Max	Min	Max	Min	Typ	Max
SSTL-135	1.283	1.35	1.45	0.18	(27)	$2(V_{IH(AC)} - V_{REF})$	$2(V_{IL(AC)} - V_{REF})$	$V_{CCIO}/2 - 0.15$	—	$V_{CCIO}/2 + 0.15$
SSTL-125	1.19	1.25	1.31	0.18	(27)	$2(V_{IH(AC)} - V_{REF})$	$2(V_{IL(AC)} - V_{REF})$	$V_{CCIO}/2 - 0.15$	—	$V_{CCIO}/2 + 0.15$
SSTL-12	1.14	1.2	1.26	0.16	(27)	$2(V_{IH(AC)} - V_{REF})$	$2(V_{IL(AC)} - V_{REF})$	$V_{REF} - 0.15$	$V_{CCIO}/2$	$V_{REF} + 0.15$

Differential HSTL and HSUL I/O Standards Specifications

Table 23. Differential HSTL and HSUL I/O Standards Specifications for Intel Stratix 10 Devices—Preliminary

I/O Standard	V_{CCIO} (V)			$V_{DIF(DC)}$ (V)		$V_{DIF(AC)}$ (V)		$V_{X(AC)}$ (V)			$V_{CM(DC)}$ (V)		
	Min	Typ	Max	Min	Max	Min	Max	Min	Typ	Max	Min	Typ	Max
HSTL-18 Class I, II	1.71	1.8	1.89	0.2	—	0.4	—	0.78	—	1.12	0.78	—	1.12
HSTL-15 Class I, II	1.425	1.5	1.575	0.2	—	0.4	—	0.68	—	0.9	0.68	—	0.9
HSTL-12 Class I, II	1.14	1.2	1.26	0.16	$V_{CCIO} + 0.3$	0.3	$V_{CCIO} + 0.48$	—	$0.5 \times V_{CCIO}$	—	$0.4 \times V_{CCIO}$	$0.5 \times V_{CCIO}$	$0.6 \times V_{CCIO}$
HSUL-12	1.14	1.2	1.3	$2(V_{IH(DC)} - V_{REF})$	$2(V_{REF} - V_{IH(DC)})$	$2(V_{IH(AC)} - V_{REF})$	$2(V_{REF} - V_{IH(AC)})$	$0.5 \times V_{CCIO} - 0.12$	$0.5 \times V_{CCIO}$	$0.5 \times V_{CCIO} + 0.12$	$0.4 \times V_{CCIO}$	$0.5 \times V_{CCIO}$	$0.6 \times V_{CCIO}$

Differential I/O Standards Specifications

Table 24. Differential I/O Standards Specifications for Intel Stratix 10 Devices—Preliminary

I/O Standard	V_{CCIO} (V)			V_{ID} (mV) (28)		$V_{ICM(DC)}$ (V)			V_{OD} (V) (29) (30)			V_{OCM} (V) (29)		
	Min	Typ	Max	Min	Max	Min	Condition	Max	Min	Typ	Max	Min	Typ	Max
LVDS (31)	1.71	1.8	1.89	100	—	0.05	Data rate ≤700 Mbps	1.65	0.247	—	0.6	1.125	1.25	1.375
						1	Data rate >700 Mbps	1.6						
RSDS (32)	1.71	1.8	1.89	100	—	0.3	—	1.4	0.1	0.2	0.6	0.5	1.2	1.4
Mini-LVDS (33)	1.71	1.8	1.89	200	600	0.4	—	1.325	0.25	—	0.6	1	1.2	1.4
LVPECL (34)	1.71	1.8	1.89	300	—	0.6	Data rate ≤700 Mbps	1.7	—	—	—	—	—	—
						1	Data rate >700 Mbps	1.6						

Switching Characteristics

This section provides the performance characteristics of Intel Stratix 10 core and periphery blocks.

(28) The minimum V_{ID} value is applicable over the entire common mode range, V_{CM}.

(29) R_L range: $90 \leq R_L \leq 110\ \Omega$.

(30) The specification is only applicable to default V_{OD} setting.

(31) For optimized LVDS receiver performance, the receiver voltage input range must be within 1.0 V to 1.6 V for data rates above 700 Mbps and 0.05 V to 1.65 V for data rates below 700 Mbps.

(32) For optimized RSDS receiver performance, the receiver voltage input range must be within 0.3 V to 1.4 V.

(33) For optimized Mini-LVDS receiver performance, the receiver voltage input range must be within 0.4 V to 1.325 V.

(34) For optimized LVPECL receiver performance, the receiver voltage input range must be within 0.85 V to 1.75 V for data rates above 700 Mbps and 0.45 V to 1.95 V for data rates below 700 Mbps.

L-Tile Transceiver Performance Specifications

Transceiver Performance for Intel Stratix 10 GX/SX L-Tile Devices

Table 25. Intel Stratix 10 GX/SX L-Tile Transmitter and Receiver Datarate Performance

Symbol/Description	Transceiver Speed Grade		
	-1	-2	-3
Chip-to-chip	N/A	26.6 Gbps 8 channels per tile (35)	17.4 Gbps
Backplane	N/A	12.5 Gbps	12.5 Gbps

Note: Refer to the *Transceiver Power Supply Operating Conditions* for V_{CCR_GXB} and V_{CCT_GXB} specifications when using bonded and non-bonded transceiver channels in Intel Stratix 10 L-Tile devices.

Table 26. L-Tile ATX PLL Performance

Symbol/Description	Condition	Transceiver Speed Grade 2	Transceiver Speed Grade 3	Unit
Supported Output Frequency	Maximum Frequency	13.3	8.7	GHz
	Minimum Frequency	500		MHz
t_{LOCK} (36)	Maximum Frequency	1		ms
t_{ARESET} Required Reset Time (37) (38)	—	25		Avalon Clock Cycles

(35) Refer to *AN-778: Intel Stratix 10 Transceiver Usage* for more details on channel selection requirements.

(36) This specification applies after the ATX PLL, fPLL, or CMU PLL has completed calibration.

(37) You must use the Avalon-MM interface to hold the PLLs in reset for the specified cycles by writing to the ATX PLL, fPLL, or CMU PLL `pll_powerdown` register.

(38) 25 cycles are required if you are using a 250-MHz AVMM clock.