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Cyclone IV GX Transceiver Starter Kit

User Guide

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UG-01078-1.0

Contents

Appendix A. Programming the Flash Memory Device

Additional Information

1. About This Kit

Introduction

The Altera® Cyclone® IV GX Transceiver Starter Kit is a complete design environment that includes both the hardware and software you need to develop Cyclone IV GX FPGA designs. The PCI-SIG-compliant board and the license-free Quartus® II Web Edition software provide everything you need to begin developing custom Cyclone IV GX FPGA designs. The following list describes what you can accomplish with the kit:

- Test signal quality of the FPGA transceiver I/Os (up to 2.5 Gbps)
- Develop and test PCI Express® (PCIe) designs
- Develop embedded designs utilizing the Nios® II processor and the SSRAM memory
- Develop and test network designs utilizing the Gigabit Ethernet PHY and the FPGA transceivers
- Develop FPGAs design for cost-sensitive applications
- Measure the FPGA's low power consumption

Kit Features

This section briefly describes the Cyclone IV GX Transceiver Starter Kit contents.

Hardware

The Cyclone IV GX Transceiver Starter Kit includes the following hardware:

- Cyclone IV GX transceiver starter board—A development platform that allows you to develop and prototype hardware designs running on the Cyclone IV GX EP4CGX15 FPGA.

  For detailed information about the board components and interfaces, refer to the *Cyclone IV GX Transceiver Starter Board Reference Manual*.

- Power supply and cables—The kit includes the following items:
  - Power supply and AC adapters for North America/Japan, Europe, and the United Kingdom
  - USB cable
  - Ethernet cable

Software

The software for this kit, described in the following sections, is available on the Altera website for immediate downloading. You can also request to have Altera mail the software to you on DVDs.

Quartus II Web Edition Software

The Quartus II Web Edition Software is a license-free set of Altera tools with limited-functionality.

Download the Quartus II Web Edition Software from the Quartus II Web Edition Software page of the Altera website. Alternatively, you can request a DVD from the Altera IP and Software DVD Request Form page of the Altera website.

The Quartus II Web Edition Software includes the following items:

- Quartus II Software—The Quartus II software, including the SOPC Builder system development tool, provides a comprehensive environment for system-on-a-programmable-chip (SOPC) design. The Quartus II software integrates into nearly any design environment and provides interfaces to industry-standard EDA tools.

  To compare the Quartus II subscription and web editions, refer to *Altera Quartus II Software — Subscription Edition vs. Web Edition*. The kit also works in conjunction with the subscription edition.

- MegaCore® IP Library—A library that contains Altera IP MegaCore functions. You can evaluate MegaCore functions by using the OpenCore Plus feature to do the following:
  - Simulate behavior of a MegaCore function within your system
  - Verify functionality of your design, and quickly and easily evaluate its size and speed
  - Generate time-limited device programming files for designs that include MegaCore functions
  - Program a device and verify your design in hardware

  The OpenCore Plus hardware evaluation feature is an evaluation tool for prototyping only. You must purchase a license to use a MegaCore function in production.

  For more information about OpenCore Plus, refer to *AN 320: OpenCore Plus Evaluation of Megafunctions*.

- Nios® II Embedded Design Suite (EDS)—A full-featured set of tools that allow you to develop embedded software for the Nios II processor which you can include in your Altera FPGA designs.

Cyclone IV GX Transceiver Starter Kit Installer

The license-free Cyclone IV GX Transceiver Starter Kit installer includes all the documentation and design examples for the kit.

Download the Cyclone IV GX Transceiver Starter Kit installer from the Cyclone IV GX Transceiver Starter Kit page of the Altera website. Alternatively, you can request a development kit DVD from the Development Kits, Daughter Cards & Programming Hardware page of the Altera website.

2. Getting Started

Introduction

This user guide leads you through the following Cyclone IV GX transceiver starter board setup steps:

- Inspecting the contents of the kit
- Installing the design and kit software
- Setting up, powering up, and verifying correct operation of the transceiver starter board
- Configuring the Cyclone IV GX FPGA
- Running the Board Test System designs

For complete information about the transceiver starter board, refer to the *Cyclone IV GX Transceiver Starter Board Reference Manual*.

Before You Begin

Before using the kit or installing the software, check the kit contents and inspect the board to verify that you received all of the items listed in this section. If any of the items are missing, contact Altera before you proceed.

Inspect the Board

To inspect board, perform the following steps:

1. Place the board on an anti-static surface and inspect it to ensure that it has not been damaged during shipment.

   CAUTION Without proper anti-static handling, you can damage the board.

2. Verify that all components are on the board and appear intact.

References

Use the following links to check the Altera website for other related information:

- For the latest board design files and reference designs, refer to the Cyclone IV GX Transceiver Starter Kit page.
- For the Cyclone IV GX device documentation, refer to the Literature: Cyclone IV Devices page.
- To purchase devices from the eStore, refer to the Devices page.
- For Cyclone IV GX OrCAD symbols, refer to the Capture CIS Symbols page.
- For Nios II 32-bit embedded processor solutions, refer to the Embedded Processing page.

3. Software Installation

Introduction

This section explains how to install the following software:

- Quartus II Web Edition Software
- Cyclone IV GX Transceiver Starter Kit
- USB-Blaster™ driver

Installing the Quartus II Web Edition Software

The Quartus II Web Edition Software provides the necessary tools used for developing hardware and software for Altera FPGAs. Included in the Quartus II Web Edition Software are the Quartus II software, the Nios II EDS, and the MegaCore IP Library. The Quartus II software (including SOPC Builder) and the Nios II EDS are the primary FPGA development tools used to create the reference designs in this kit. To install the Altera development tools, perform the following steps:

1. Run the Quartus II Web Edition Software you acquired in "Software" on page 1–1.
2. Follow the installer instructions to complete the installation process.

If you have difficulty installing the Quartus II software, refer to *Quartus II Installation & Licensing for Windows and Linux Workstations*.

Licensing Considerations

The Quartus II Web Edition Software is license-free and supports Cyclone IV GX devices without any additional licensing requirement. This kit also works in conjunction with the Quartus_II Subscription Edition Software, once you obtain the proper license file. To purchase a subscription, contact your Altera sales representative.

Installing the Cyclone IV GX Transceiver Starter Kit

To install the Cyclone IV GX Transceiver Starter Kit, perform the following steps:

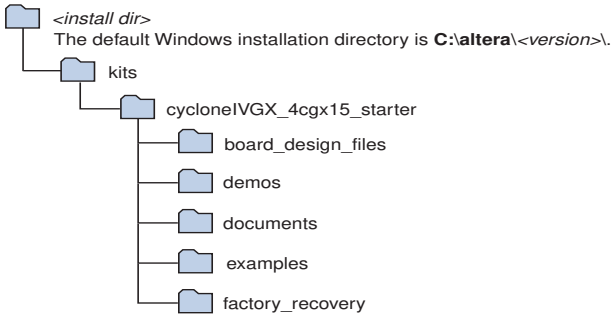
1. Run the Cyclone IV GX Transceiver Starter Kit you acquired in "Software" on page 1–1.

   If installing from the DVD and no auto-install process starts, browse to the DVD drive and double-click on the **setup.exe** file.

2. Follow the on-screen instructions to complete the installation process.

The installation program creates the Cyclone IV GX Transceiver Starter Kit directory structure shown in Figure 3–1.

Figure 3–1. Cyclone IV GX Transceiver Starter Kit Installed Directory Structure *(1)*



Note to Figure 3–1:

(1) Early-release versions might have slightly different directory names.

Table 3–1 lists the file directory names and a description of their contents.

Table 3–1. Installed Directory Contents

Directory Name	Description of Contents
board_design_files	Contains schematic, layout, assembly, and bill of material board design files. Use these files as a starting point for a new prototype board design.
demos	Contains demonstration applications.
documents	Contains the kit documentation.
examples	Contains the sample design files for the Cyclone IV GX Transceiver Starter Kit.
factory_recovery	Contains the original data programmed onto the board before shipment. Use this data to restore the board with its original factory contents.

Installing the USB-Blaster Driver

The Cyclone IV GX transceiver starter board includes integrated USB-Blaster circuitry for FPGA programming. However, for the host computer and board to communicate, you must install the USB-Blaster driver on the host computer.

Installation instructions for the USB-Blaster driver for your operating system are available on the Altera website. On the Altera Programming Cable Driver Information page of the Altera website, locate the table entry for your configuration and click the link to access the instructions.

4. Board Setup

Introduction

The instructions in this chapter explain how to set up the Cyclone IV GX transceiver starter board.

Setting Up the Board

To set up and power up the board, perform the following steps:

1. The Cyclone IV GX transceiver starter board ships with its board switches preconfigured to support the design examples in the kit. If you suspect your board might not be currently configured with the default settings, follow the instructions in "Factory Default Switch Settings" on page 4–2 to return the board to its factory settings before proceeding.
2. The transceiver starter board ships with design examples stored in the flash memory device. Verify the USER_PGM switch (S8.2) is set to the off position to load the design stored in the factory portion of flash memory. Figure 4–1 shows the switch location on the Cyclone IV GX transceiver starter board.
3. Connect the DC adapter (+9 V-16 V, 33.75 W) to the DC power jack (J4) on the FPGA board and plug the cord into a power outlet.

   CAUTION: Use only the supplied power supply. Power regulation circuitry on the board can be damaged by power supplies with greater voltage.

4. Set the POWER switch (SW1) to the on position. When power is supplied to the board, a blue LED (D12) illuminates indicating that the board has power.

The MAX II device on the board contains (among other things) a parallel flash loader (PFL) megafunction. When the board powers up, the PFL reads a design from flash memory and configures the FPGA. The USER_PGM switch (S8.2) controls which design to load. When the switch is in the off position, the PFL loads the design from the factory portion of flash memory. When the switch is in the on position, the PFL loads the design from the user hardware 1 portion of flash memory.

The kit includes a MAX II design which contains the MAX II PFL megafunction. The design resides in the *<install dir>*\kits\cycloneIVGX_4cgx15_starter\examples\max2 directory.

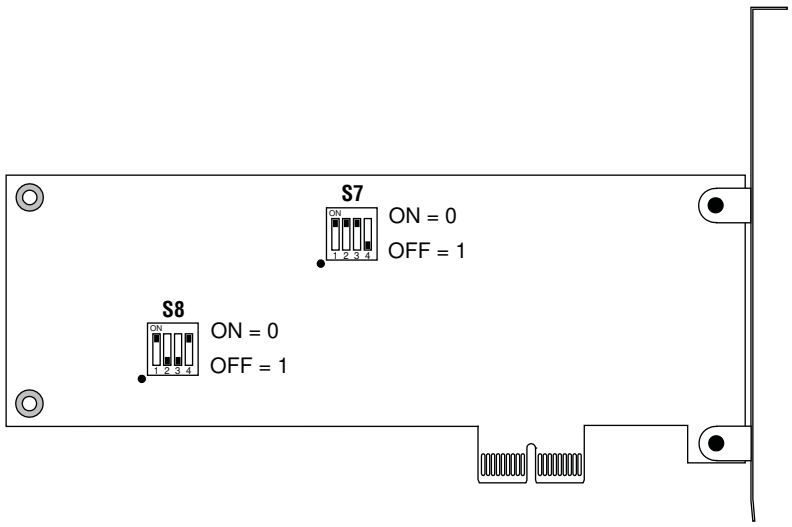
When configuration is complete, the CONF DONE LED (D2) illuminates, signaling that the Cyclone IV GX device configured successfully.

For more information about the PFL megafunction, refer to *AN 386: Using the Parallel Flash Loader with the Quartus II Software*.

Factory Default Switch Settings

This section shows the factory switch settings for the Cyclone IV GX transceiver starter board. Figure 4–1 shows the switch locations and the default position of each switch on the bottom side of the board.

Figure 4–1. Switch Locations and Default Settings on the Board Bottom



To restore the switches to their factory default settings, perform the following steps:

1. Set DIP switch bank (S8) to match Table 4–1 and Figure 4–1.

Table 4–1. S8 Dip Switch Settings

Switch	Board Label	Function	Default Position
1	CLKSEL	Switch 1 has the following options: ■ When on, the onboard clock is used for the FPGA differential clock inputs. ■ When off, the differential SMA clock is used for the FPGA differential clock inputs.	On
2	USER_PGM	Switch 2 has the following options: ■ When on, the PFL loads the user hardware 1 design on power up. ■ When off, the PFL loads the factory design on power up.	Off
3	MAX_JTAG_EN	Switch 3 has the following options: ■ When on, the MAX II EPM2210 device is removed from the JTAG chain. ■ When off, the MAX II EPM2210 device is included in the JTAG chain.	Off
4	PCIE_JTAG_EN	Switch 4 has the following options: ■ When on, the PCIe device is in removed from JTAG chain. ■ When off, the PCIe device is included in the JTAG chain.	On

2. Set DIP switch bank (S7) to match Table 4–2 and Figure 4–1.

Table 4–2. S7 Dip Switch Settings

Switch	Board Label	Function	Default Position
1	MSEL0 *(1)*	Switch 1 has the following options: ■ When on, the MSEL0 state is logic low. ■ When off, the MSEL0 state is logic high.	On
2	MSEL1 *(1)*	Switch 2 has the following options: ■ When on, the MSEL1 state is logic low. ■ When off, the MSEL1 state is logic high.	On
3	MSEL2 *(1)*	Switch 3 has the following options: ■ When on, the MSEL2 state is logic low. ■ When off, the MSEL2 state is logic high.	On
4	EPCS_nCS *(2)*	Switch 4 has the following options: ■ When on, the EPCS device defaults to disabled, but allows the MAX II device to enable or disable the EPCS device. ■ When off, the `EPCS_nCS` signal floats, requiring the MAX II device to enable or disable the EPCS device.	Off

Note to Table 4–2:

(1) The MSEL0, MSEL1, and MSEL2 switches combine to specify a single device configuration. The default 0, 0, 0 combination corresponds to a 2.5 v passive serial configuration with the standard power-on-reset delay. For a complete list of MSEL combinations, refer to the *Configuration and Remote System Upgrades in Cyclone IV Devices* chapter of the *Cyclone IV GX Device Handbook*.

(2) The board ships with a simple design example stored in the EPCS flash memory device.To load the design and see the four user LEDs (D5-D8) blink, set the S7.1 - S7.4 switches to on, off, on, on, and power cycle the board. These switch settings corresponds to a 2.5 V active serial configuration with the standard power-on-reset delay. Source code for the EPCS design resides in the <install dir>\kits\cycloneIVGX_4cgx15_starter\examples directory.

For more information about the FPGA board settings, refer to the *Cyclone IV GX Transceiver Starter Board Reference Manual*.

5. Board Update Portal

Introduction

The Cyclone IV GX Transceiver Starter Kit ships with the Board Update Portal design example stored in the factory portion of the flash memory on the board. The design consists of a Nios II embedded processor, an Ethernet MAC, and an HTML web server.

When you power up the board with the USER_PGM switch (S8.2) in the off position, the Cyclone IV GX FPGA configures with the Board Update Portal design example. The design can obtain an IP address from any DHCP server and serve a web page from the flash on your board to any host computer on the same network. The web page allows you to upload new FPGA designs to the user hardware 1 portion of flash memory, and provides links to useful information on the Altera website, including links to kit-specific and design resources.

☞ After successfully updating the user hardware 1 flash memory, you can load the user design from flash memory into the FPGA. To do so, set the USER_PGM switch (S8.2) to the on position and power cycle the board.

The source code for the Board Update Portal design resides in the <*install dir*>**\kits\cycloneIVGX_4cgx15_starter\examples** directory. If the Board Update Portal is corrupted or deleted from the flash memory, refer to "Restoring the Flash Device to the Factory Settings" on page A–4 to restore the board with its original factory contents.

Connecting to the Board Update Portal Web Page

This section provides instructions to connect to the Board Update Portal web page.

☞ Before you proceed, ensure that you have the following:

- A PC with a connection to a working Ethernet port on a DHCP enabled network.
- A separate working Ethernet port connected to the same network for the board.
- The Ethernet and power cables that are included in the kit.

To connect to the Board Update Portal web page, perform the following steps:

1. With the board powered down, set the USER_PGM switch (S8.2) to the off position.
2. Attach the Ethernet cable from the board to your LAN.
3. Power up the board. The board connects to the LAN's gateway router, and obtains an IP address. The LCD on the board displays the IP address.
4. Launch a web browser on a PC that is connected to the same network, and enter the IP address from the LCD into the browser address bar. The Board Update Portal web page appears in the browser.

5. Click Cyclone IV GX Transceiver Starter Kit on the Board Update Portal web page to access the kit's home page. Visit this page occasionally for documentation updates and additional new designs.

You can also navigate directly to the Cyclone IV GX Transceiver Starter Kit page of the Altera website to determine if you have the latest kit software.

Using the Board Update Portal to Update User Designs

The Board Update Portal allows you to write new designs to the user hardware 1 portion of flash memory. Designs must be in the Nios II Flash Programmer File (**.flash**) format.

Design files available from the Cyclone IV GX Transceiver Starter Kit page of the Altera website include **.flash** files. You can also create **.flash** files from your own custom design. Refer to "Preparing Design Files for Flash Programming" on page A–2 for information about preparing your own design for upload.

To upload a design over the network into the user portion of flash memory on your board, perform the following steps:

1. Perform the steps in "Connecting to the Board Update Portal Web Page" to access the Board Update Portal web page.
2. In the **Hardware File Name** field specify the **.flash** file that you either downloaded from the Altera website or created on your own. If there is a software component to the design, specify it in the same manner using the **Software File Name** field, otherwise leave the **Software File Name** field blank.
3. Click **Upload**. The file takes about 20 seconds to upload.
4. To configure the FPGA with the new design after the flash memory upload process is complete, set the USER_PGM switch (S8.2) to the on position and power cycle the board, or press the PGM_SEL button (S2) until the PGM 0 LED (D4) is on and the PGM 1 LED (D3) is off and then press the PGM_CONF button (S1). Refer to Table 6–2 on page 6–5 for information about the PGM LEDs.

As long as you don't overwrite the factory image in the flash memory device, you can continue to use the Board Update Portal to write new designs to the user hardware 1 portion of flash memory. If you do overwrite the factory image, you can restore it by following the instructions in "Restoring the Flash Device to the Factory Settings" on page A–4.

6. Board Test System

Introduction

The kit includes a design example and application called the Board Test System to test the functionality of the Cyclone IV GX transceiver starter board. The application provides an easy-to-use interface to alter functional settings and observe the results. You can use the application to test board components, modify functional parameters, observe performance, and measure power usage. The application is also useful as a reference for designing systems. To install the application, follow the steps in "Installing the Cyclone IV GX Transceiver Starter Kit" on page 3–1.

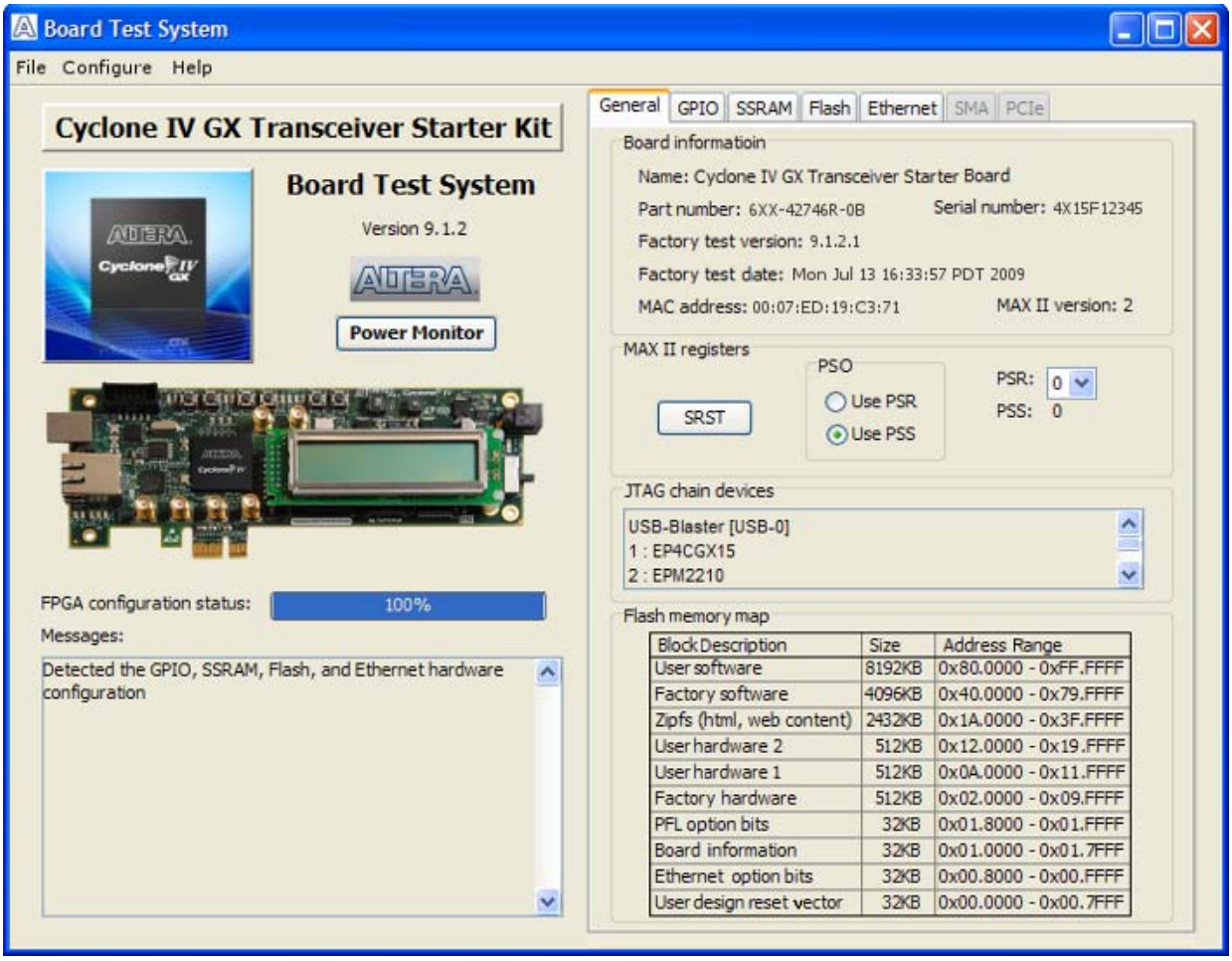
The application provides access to the following Cyclone IV GX transceiver starter board features:

- General purpose I/O (GPIO)
- SRAM
- Flash memory
- Transceivers
- PCIe

The application allows you to exercise most of the board components. While using the application, you reconfigure the FPGA several times with test designs specific to the functionality you are testing.

A GUI runs on the PC which communicates over the JTAG bus to a test design running in the Cyclone IV GX device. Figure 6–1 shows the initial GUI for a board that is in the factory configuration.

Figure 6–1. Board Test System Graphical User Interface



Several designs are provided to test the major board features. Each design provides data for one or more tabs in the application. The Configure menu identifies the appropriate design to download to the FPGA for each tab.

After successful FPGA configuration, the appropriate tab appears and allows you to exercise the related board features. Highlights appear in the board picture around the corresponding components.

The **Power Monitor** button starts the Power Monitor application that measures and reports current power information for the board. Because the application communicates over the JTAG bus to the MAX II device, you can measure the power of any design in the FPGA, including your own designs.

☞ The Board Test System and Power Monitor share the JTAG bus with other applications like the Nios II debugger and the SignalTap® II Embedded Logic Analyzer. Because the Quartus II programmer uses most of the bandwidth of the JTAG bus, other applications using the JTAG bus might time out. Be sure to close the other applications before attempting to reconfigure the FPGA using the Quartus II Programmer.

Preparing the Board

With the power to the board off, perform the following steps:

1. Connect the USB cable to the board.
2. Verify the settings for the board settings DIP switch bank (S7 and S8) match Table 4–1 on page 4–2 and Table 4–2 on page 4–3.
3. Set the USER_PGM switch (S8.2) to the on position.
4. Turn the power to the board on. The board loads the design stored in the user hardware 1 portion of flash memory into the FPGA. If your board is still in the factory configuration or if you have downloaded a newer version of the Board Test System to flash memory through the Board Update Portal, the design that loads tests accessing the GPIO, Ethernet, SSRAM, and flash memory.

CAUTION To ensure operating stability, keep the USB cable connected and the board powered on when running the demonstration application. The application cannot run correctly unless the USB cable is attached and the board is on.

Running the Board Test System

To run the application, navigate to the <*install dir*>**\kits\cycloneIVGX_4cgx15_starter\examples\board_test_system** directory and run the **BoardTestSystem.exe** application.

On Windows, click **Start** > **All Programs** > **Altera** > **Cyclone IV GX Transceiver Starter Kit** <*version*> > **Board Test System** to run the application.

A GUI appears, displaying the application tab that corresponds to the design running in the FPGA. The Cyclone IV GX transceiver starter board's flash memory ships preconfigured with the design that corresponds to the **Config**, **GPIO**, **SSRAM, Flash, and Ethernet** tabs.

If you power up your board with the USER_PGM switch (S8.2) in the off position, or if you load your own design into the FPGA with the Quartus II Programmer, you receive a message prompting you to configure your board with a valid Board Test System design. Refer to "The Configure Menu" for information about configuring your board.

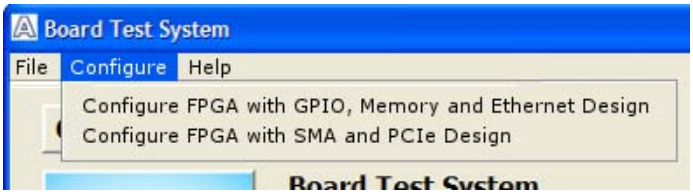
Using the Board Test System

This section describes each control in the Board Test System application.

The Configure Menu

Each test design tests different functionality and corresponds to one or more application tabs. Use the Configure menu to select the design you want to use. Figure 6–2 shows the Configure menu.

Figure 6–2. The Configure Menu



To configure the FPGA with a test system design, perform the following steps:

1. On the Configure menu, click the configure command that corresponds to the functionality you wish to test.
2. When configuration finishes, the design begins running in the FPGA. The corresponding GUI application tabs that interface with the design enable.

Board Rework Required

For the SMA tests to work correctly, you must modify your board. The Ethernet PHY and transceiver SMA connectors use the same transceiver path. The board ships with the transceiver path connected to the Ethernet PHY. A solder modification is required to change the transceiver path from the Ethernet PHY to the transceiver SMA connectors.

CAUTION

To avoid damage to your board, have an experienced technician perform the board modifications.

Table 6–1 shows the required placement of the 0 Ω resistors and 0.1 µF capacitors to enable either the Ethernet PHY or the transceiver SMA connectors.

Table 6–1. Resistor and Capacitor Placement

Loopback Tests	0 Ω Resistors at R51 and R54 0.1 µF Capacitors at C57 and C60	0 Ω Resistors at R52 and R53 0.1 µF Capacitors at C58 and C59
Transceiver SMA *(1)*	Install	Remove
Ethernet *(2)*	Remove	Install

Notes to Table 6–1:

(1) This configuration routes the transceiver channel to SMA connectors J8, J9, J10 and J11.
(2) This configuration is the factory default and routes the transceiver channel to the Ethernet PHY.

The General Tab

The **General** tab shows information about the board's current configuration. Figure 6–1 on page 6–2 shows the **General** tab. The tab displays the contents of the MAX II registers, the JTAG chain, the board's MAC address, the flash memory map, and other details stored on the board.

The following sections describe the controls on the **General** tab.

Board Information

The **Board information** controls display static information about your board.

- **Name**—Indicates the official name of the board, given by the Board Test System.
- **Part number**—Indicates the part number of the board.
- **Serial number**—Indicates the serial number of the board.
- **Factory test version**—Indicates the version of the Board Test System currently running on the board.
- **Factory test date**—Indicates the release date of the Board Test System currently running on the board.
- **MAX II version**—Indicates the version of MAX II code currently running on the board. The MAX II code resides in the <*install dir*>**\kits\cycloneIVGX_4cgx15_starter\examples** directory. Newer revisions of this code might be available on the Cyclone IV GX Transceiver Starter Kit page of the Altera website.
- **MAC address**—Indicates the MAC address of the board.

MAX II Registers

The **MAX II registers** control allow you to view and change the current MAX II register values as described in Table 6–2. Changes to the register values with the GUI take effect immediately. For example, writing a 0 to SRST resets the board.

Table 6–2. MAX II Registers

Register Name	Read/Write Capability	Description
System Reset (SRST)	Write only	Set to 0 to initiate an FPGA reconfiguration.
Page Select Register (PSR)	Read / Write	Determines which of the pages of flash memory to use for FPGA reconfiguration. The flash memory ships with pages 0 and 1 preconfigured.
Page Select Override (PSO)	Read / Write	When set to 0, the value in PSR determines the page of flash memory to use for FPGA reconfiguration. When set to 1, the value in PSS determines the page of flash memory to use for FPGA reconfiguration.
Page Select Switch (PSS)	Read only	Holds the current value of the iluminated PGM LEDs (D3-D4) based on the following encoding: ■ 0 = PGM 0 LED (D4) on and PGM 1 LED (D3) on, and corresponds to the flash memory page for the factory hardware design ■ 1 = PGM 0 LED (D4) on and PGM 1 LED (D3) off, and corresponds to the flash memory page for the user hardware 1 design ■ 2 = PGM 0 LED (D4) off and PGM 1 LED (D3) on, and corresponds to the flash memory page for the user hardware 2 design

- **PSO**—Sets the MAX II PSO register. The following options are available:
  - **Use PSR**—Allows the PSR to determine the page of flash memory to use for FPGA reconfiguration.
  - **Use PSS**—Allows the PSS to determine the page of flash memory to use for FPGA reconfiguration.
- **PSR**—Sets the MAX II PSR register. The numerical values in the list corresponds to the page of flash memory to load during FPGA reconfiguration. Refer to Table 6–2 for more information.
- **PSS**—Displays the MAX II PSS register value. Refer to Table 6–2 for the list of available options.
- **SRST**—Resets the system and reloads the FPGA with a design from flash memory based on the other MAX II register values. Refer to Table 6–2 for more information.

☞ Because the **Config** tab requires that a specific design is running in the FPGA, writing a 0 to SRST or changing the PSO value can cause the Board Test System to stop running.

JTAG Chain

The **JTAG chain** devices control shows all the devices currently in the JTAG chain. The Cyclone IV GX device is always the first device in the chain.

☞ Setting DIP switch S8.3 to the off position includes the MAX II device in the JTAG chain.

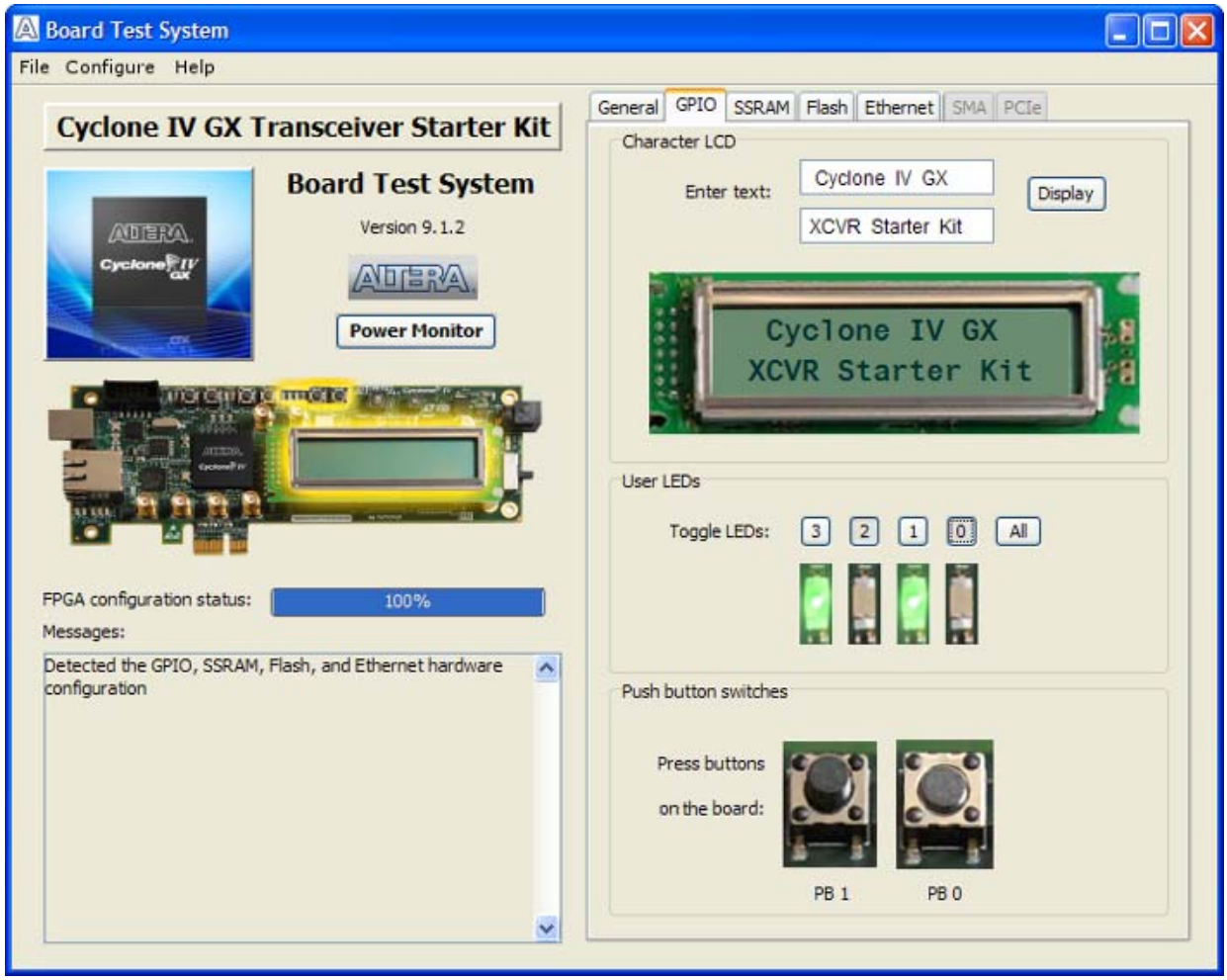
Flash Memory Map

The **Flash memory map** control shows the memory map of the flash memory device on your board.

The GPIO Tab

The **GPIO** tab allows you to interact with all the general purpose user I/O components on your board. You can write to the LCD, turn LEDs on or off, and detect push button presses. Figure 6–3 shows the **GPIO** tab.

Figure 6–3. The GPIO Tab



The following sections describe the controls on the **GPIO** tab.

Character LCD

The **Character LCD** controls allow you to display text strings on the character LCD on your board. Type text in the text boxes and then click **Display**.

☞ If you exceed the 16 character display limit on either line, a warning message appears.

User LEDs

The **User LEDs** control displays the current state of the user LEDs. Click the Toggle LEDs buttons to turn the board LEDs on and off.

Push Button Switches

The read-only **Push button switches** control displays the current state of the board user push buttons. Press a push button on the board to see the graphical display change accordingly.