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Arria V GX Starter Board

Reference Manual

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MNL-01069-1.4

Contents

Additional Information

1. Overview

This document describes the hardware features of the Arria® V GX starter board, including the detailed pin-out and component reference information required to create custom FPGA designs that interface with all components of the board.

General Description

The Arria V GX starter board provides a hardware platform for developing and prototyping low-power, high-performance, and logic-intensive designs using Altera's Arria V GX FPGA device. The board provides a wide range of peripherals and memory interfaces to facilitate the development of Arria V GX designs.

One high-speed mezzanine card (HSMC) connector is available to add additional functionality via a variety of HSMCs available from Altera® and various partners.

To see a list of the latest HSMCs available or to download a copy of the HSMC specification, refer to the Development Board Daughtercards page of the Altera website.

Design advancements and innovations, such as the PCI Express hard IP, partial reconfiguration, and hard memory controller implementation ensure that designs implemented in the Arria V GXs operate faster, with lower power, and have a faster time to market than previous FPGA families.

For more information on the following topics, refer to the respective documents:

- Arria V device family, refer to the *Arria V Device Handbook*.
- PCI Express MegaCore function, refer to the *PCI Express Compiler User Guide*.
- HSMC Specification, refer to the *High Speed Mezzanine Card (HSMC) Specification*.

Board Component Blocks

The starter board features the following major component blocks:

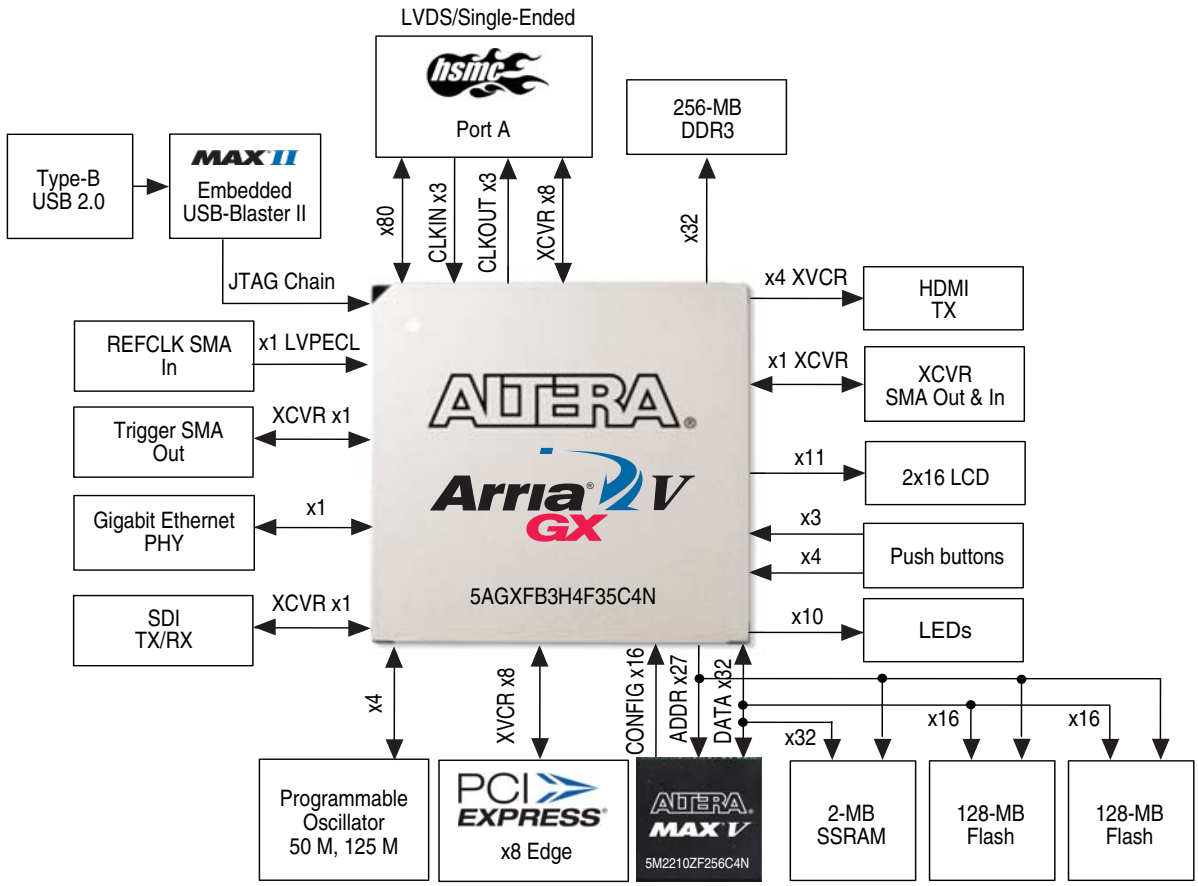
- One Arria V GX 5AGXFB3H4F35C4N FPGA in a 1152-pin FineLine BGA (FBGA) package
  - 362,000 LEs
  - 136,880 adaptive logic modules (ALMs)
  - 17,260 Kbit on-die block memory
  - 24 high-speed transceivers
  - 12 fractional phase locked loops (PLLs)
  - 2,090 18x19 multipliers
  - 544 general purpose input/output
  - 1.1-V core voltage
- MAX® V 5M2210ZF256C4N CPLD in a 256-pin FBGA package
- MAX II EPM570F100C5N CPLD in a 100-pin FBGA package
- FPGA configuration circuitry
  - MAX V CPLD 5M2210ZF256C4N System Controller and flash fast passive parallel (FPP) configuration
  - On-board USB-Blaster™ II for use with the Quartus® II Programmer
- Clocking circuitry
  - Programmable clock generator for FPGA reference clock input
  - 125-MHz LVDS oscillator for FPGA reference clock input
  - 148.5/148.35-MHz LVDS VCXO for FPGA reference clock input
  - 50-MHz single-ended oscillator for FPGA and CPLD clock input
  - 100-MHz single-ended oscillator for CPLD configuration clock input
  - SMA input (LVPECL)
- Memory
  - Two 128-Mbyte (MB) DDR3 SDRAM with a total of 32-bit data bus
  - 2-MB SSRAM
  - Two 128-MB synchronous flash

- General user I/O
  - LEDs and displays
    - Four user LEDs
    - One two-line character LCD display
    - Three configuration select LED
    - One configuration done LED
    - Four on-board USB-Blaster II status LEDs
    - Two HSMC interface transmit/receive LED (TX/RX)
    - Four PCI Express LEDs
    - Five Ethernet LEDs
    - One serial digital interface (SDI) carrier detect LED
  - Push buttons
    - One CPU reset push button
    - One configuration reset push button
    - Three general user push buttons
  - DIP switches
    - Four MAX V CPLD System Controller control switches
    - Three JTAG chain control switches
    - Three PCI Express link width switches
    - Four general user switches
- Power supply
  - 19-V (laptop) DC input
  - PCI Express edge connector power
- Mechanical
  - PCI card standard size (6.600" x 4.199")

Development Board Block Diagram

Figure 1–1 shows a block diagram of the Arria V GX starter board.

Figure 1–1. Arria V GX Starter Board Block Diagram



Handling the Board

When handling the board, it is important to observe the following static discharge precaution:

CAUTION

Without proper anti-static handling, the board can be damaged. Therefore, use anti-static handling precautions when touching the board.

2. Board Components

Introduction

This chapter introduces the major components on the Arria V GX starter board. Figure 2–1 illustrates the component locations and Table 2–1 provides a brief description of all component features of the board.

A complete set of schematics, a physical layout database, and GERBER files for the development board reside in the Arria V GX starter kit documents directory.

For information about powering up the board and installing the demonstration software, refer to the *Arria V GX Starter Kit User Guide*.

This chapter consists of the following sections:

Board Overview

This section provides an overview of the Arria V GX starter board, including an annotated board image and component descriptions. Figure 2–1 shows an overview of the board features.

Figure 2–1. Overview of the Arria V GX Starter Board Features

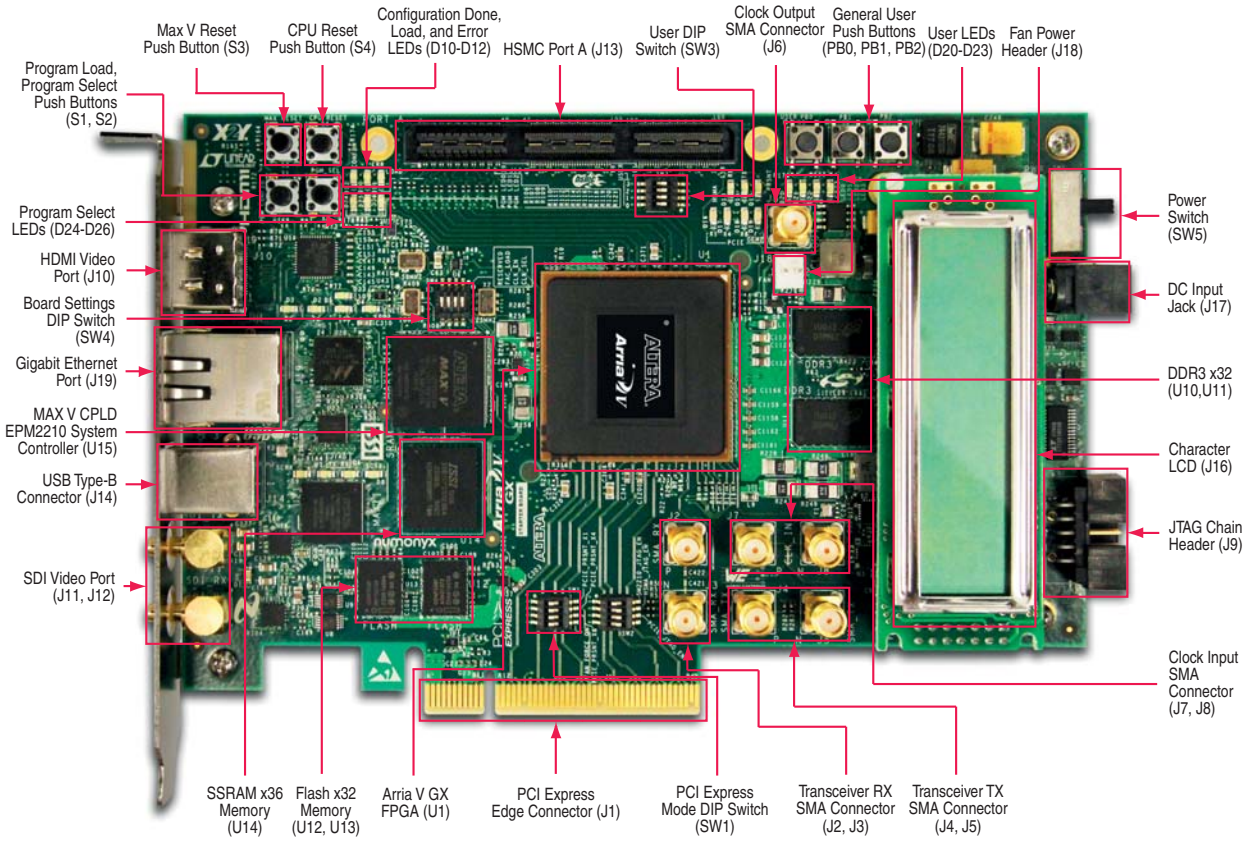


Table 2–1 describes the components and lists their corresponding board references.

Table 2–1. Arria V GX Starter Board Components (Part 1 of 3)

Board Reference	Type	Description
Featured Devices		
U1	FPGA	Arria V GX, 5AGXFB3H4F35C4N, 1152-pin FBGA.
U15	CPLD	MAX V CPLD, 5M2210ZF256C4N , 256-pin FBGA.
Configuration, Status, and Setup Elements		
J9	JTAG chain header	Provides access to the JTAG chain and disables the on-board USB-Blaster II when using an external USB-Blaster cable.
D6, D7	JTAG LEDs	Indicate transmit or receive activity of the JTAG chain. The TX and RX LEDs would flicker if the link is in use and active.
SW2	JTAG chain control DIP switch	Remove or include devices in the active JTAG chain.

Table 2–1. Arria V GX Starter Board Components (Part 2 of 3)

Board Reference	Type	Description
J14	On-Board USB-Blaster II	USB interface for programming and debugging the FPGA through embedded USB-Blaster II JTAG via a type-B USB cable.
SW4	Board settings DIP switch	Controls the MAX V CPLD 5M2210 System Controller functions such as clock enable, SMA clock input control, and which image to load from flash memory at power-up.
SW1	PCI Express DIP switch	Controls the PCI Express lane width by connecting `prsnt` pins together on the PCI Express edge connector.
S2	Image select push button	Toggles the configuration LEDs which selects the program image that loads from flash memory to the FPGA.
S1	Load image push button	Load image from flash memory to the FGPA based on the configuration LED setting.
D8, D9	System Console LEDs	Indicate transmit or receive activity of the System Console USB interface. The TX and RX LEDs would flicker if the link is in use and active.
D12	Configuration done LED	Illuminates when the FPGA is configured.
D11	Load LED	Illuminates when the MAX V CPLD 5M2210 System Controller is actively configuring the FPGA.
D10	Error LED	Illuminates when the FPGA configuration from flash memory fails.
D30	Power LED	Illuminates when 5.0-V power is present.
D24, D25, D26	Configuration LEDs	Illuminates to show the LED sequence that determines which flash memory image loads to the FPGA when you press the `PGM_SEL` push button.
D2, D3, D4, D5, D33	Ethernet LEDs	Shows the connection speed as well as transmit or receive activity.
D13, D14	HSMC port A LEDs	You can configure these LEDs to indicate transmit or receive activity.
D15	HSMC port A present LED	Illuminates when a daughtercard is plugged into the HSMC port A.
D16, D17, D18, D19	PCI Express link LEDs	You can configure these LEDs to indicate the PCI Express link width (x1, x4, x8) and Gen2 link.
Clock Circuitry		
U4	Quad-output oscillator	Programmable oscillator with default frequencies of 125 MHz, 409.6 MHz, 156.25 MHz, and 100 MHz. The frequency is programmable using the clock control GUI running on the MAX V CPLD 5M2210 System Controller.
X1	148.5-MHz oscillator	148.500-MHz voltage controlled crystal oscillator for serial digital interface (SDI) video. This oscillator is programmable to any frequency between 20–810 MHz using the clock control GUI running on the MAX V CPLD 5M2210 System Controller.
X4	50-MHz oscillator	50.000-MHz crystal oscillator for general purpose logic.
X3	100-MHz oscillator	100.000-MHz crystal oscillator for the MAX V CPLD 5M2210 System Controller.
X2	125-MHz oscillator	125.000 MHz crystal oscillator for Gigabit Ethernet.
J7, J8	Clock input SMAs	Drive LVPECL-compatible clock inputs into the clock multiplexer buffer (U5).
J6	Clock output SMA	Drive out 2.5-V CMOS clock output from the FPGA.

Table 2–1. Arria V GX Starter Board Components (Part 3 of 3)

Board Reference	Type	Description
General User Input/Output		
D20–D23	User LEDs	Four user LEDs. Illuminates when driven low.
SW3	User DIP switch	Quad user DIP switches. When the switch is ON, a logic 0 is selected.
S4	CPU reset push button	Press to reset the FPGA logic.
S3	MAX V reset push button	Press to reset the MAX V CPLD 5M2210 System Controller.
S5, S6, S7	General user push buttons	Three user push buttons. Driven low when pressed.
Memory Devices		
U10, U11	DDR3 x32 memory	256-Mbyte DDR3 SDRAM with a 32-bit data bus. The 32-bit data bus consists of two x16 devices with a single address or command bus.
U14	SSRAM x36 memory	2-Mbyte standard synchronous RAM with a 32-bit data bus and 4-bit parity.
U12, U13	Flash x32 memory	Two 128-Mbyte synchronous flash devices with 16-bit data buses for non-volatile memory. The board supports two flash devices of 16-bit interface each, which combine to allow for 256-Mbyte synchronous flash with a 32-bit data bus.
Communication Ports		
J1	PCI Express edge connector	Gold-plated edge fingers connector for up to ×8 signaling in Gen1 or Gen2 mode.
J13	HSMC port A	Provides eight transceiver channels and 84 CMOS or 17 LVDS channels per the HSMC specification.
J19	Gigabit Ethernet connector	RJ-45 connector which provides a 10/100/1000 Ethernet connection via a Marvell 88E1111 PHY and the FPGA-based Altera Triple Speed Ethernet MegaCore function in RGMII mode.
Video and Display Ports		
J16	Character LCD	Connector that interfaces to a provided 16 character × 2 line LCD module along with two standoffs.
J10	HDMI video port	A 19-pin HDMI connector that provides a HDMI video output of up to 1080i.
J11, J12	SDI video port	Two 75-Ω sub-miniature version B (SMB) connectors that provide a full-duplex SDI interface through a LMH0303 cable driver and LMH0384 cable equalizer.
Power Supply		
J1	PCI Express edge connector	Interfaces to a PCI Express root port such as an appropriate PC motherboard.
J17	DC input jack	Accepts a 14–20-V DC power supply. This input jack is not to be used while the board is plugged into a PCI Express slot.
SW5	Power switch	Switch to power on or off the board when power is supplied from the DC input jack.

Featured Device: Arria V GX FPGA

The Arria V GX starter board features a Arria V GX 5AGXFB3H4F35C4N device (U1) in a 1152-pin FBGA package.

For more information about Arria V device family, refer to the *Arria V Device Handbook*.

Table 2–2 describes the features of the Arria V GX 5AGXFB3H4F35C4N device.

Table 2–2. Arria V GX Features

ALMs	Equivalent LEs	M10K RAM Blocks	Total RAM (Kbits)	18-bit × 19-bit Multipliers	PLLs	Transceivers	Package Type
136,880	362,000	1,726	17,260	2,090	12	24	1152-pin FBGA

Table 2–3 lists the Arria V GX component reference and manufacturing information.

Table 2–3. Arria V GX Component Reference and Manufacturing Information

Board Reference	Description	Manufacturer	Manufacturing Part Number	Manufacturer Website
U1	FPGA, Arria V GX F1152, 362K LEs, leadfree	Altera Corporation	5AGXFB3H4F35C4N	www.altera.com

I/O and Transceiver Resources

Figure 2–2 illustrates the bank organization and I/O count for the Arria V GX 5AGXFB3H4F35C4N device in the 1152-pin FBGA package.

Figure 2–2. Arria V GX Device I/O Bank Diagram

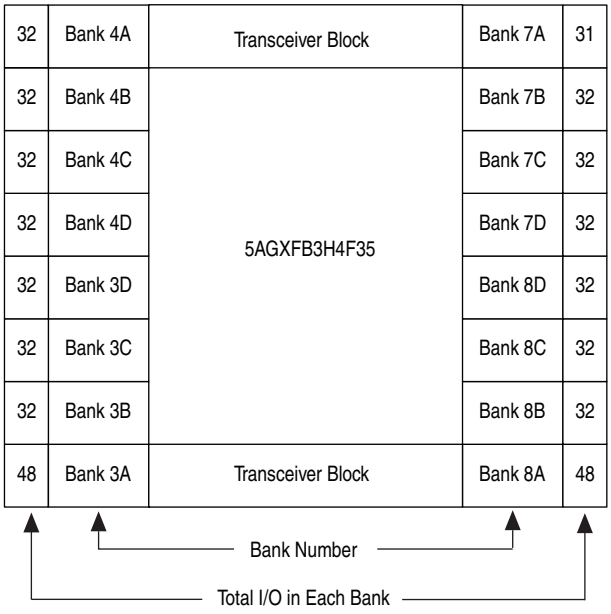


Figure 2–3 illustrates the transceiver channels on the left and right side of the Arria V GX 5AGXFB3H4F35C4N device in the 1152-pin FBGA package.

Figure 2–3. Arria V GX Device Transceiver Bank Diagram

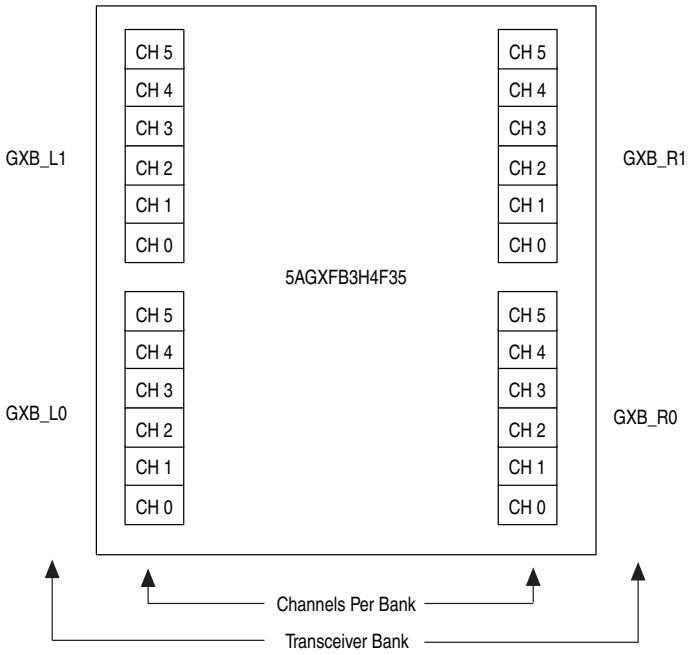


Table 2–4 lists the Arria V GX device I/O and transceiver pin count and usage by function on the board.

Table 2–4. Arria V GX Device I/O and Transceiver Pin Count

Function	I/O Standard	I/O Count	Special Pins
DDR3	1.5-V SSTL	70	One differential x4 DQS pin
Flash, SSRAM, and MAX V FSM bus	2.5-V CMOS	87	—
MAX V CPLD 5M2210 System Controller	2.5-V CMOS	10	—
PCI Express x8	2.5-V CMOS + XCVR	42	One reference clock
HSMA port A	2.5-V CMOS + LVDS + XCVR	116	Eight XCVR, 17 LVDS, six clock inputs/outputs, I^2C
Gigabit Ethernet	2.5-V CMOS + LVDS	20	One LVDS
On-Board USB-Blaster II	2.5-V CMOS	20	—
SDI video	2.5-V CMOS	15	One reference clock
HDMI video	2.5-V CMOS	14	One reference clock
Push buttons	2.5-V CMOS	4	One DEV_CLRn
DIP switches	2.5-V CMOS	4	—
Character LCD	2.5-V CMOS	11	—
LEDs	2.5-V CMOS	7	—
Clock or Oscillators	2.5-V CMOS + LVDS + PCML	21	11 reference clock
Total I/O Used:		**441**	

MAX V CPLD 5M2210 System Controller

The board utilizes the 5M2210 System Controller, an Altera MAX V CPLD, for the following purposes:

- FPGA configuration from flash
- Power measurement
- Fan control (shared with the FPGA)
- Control registers for clocks
- Control and status registers for remote system update

Figure 2–4 illustrates the MAX V CPLD 5M2210 System Controller's functionality and external circuit connections as a block diagram.

Figure 2–4. MAX V CPLD 5M2210 System Controller Block Diagram

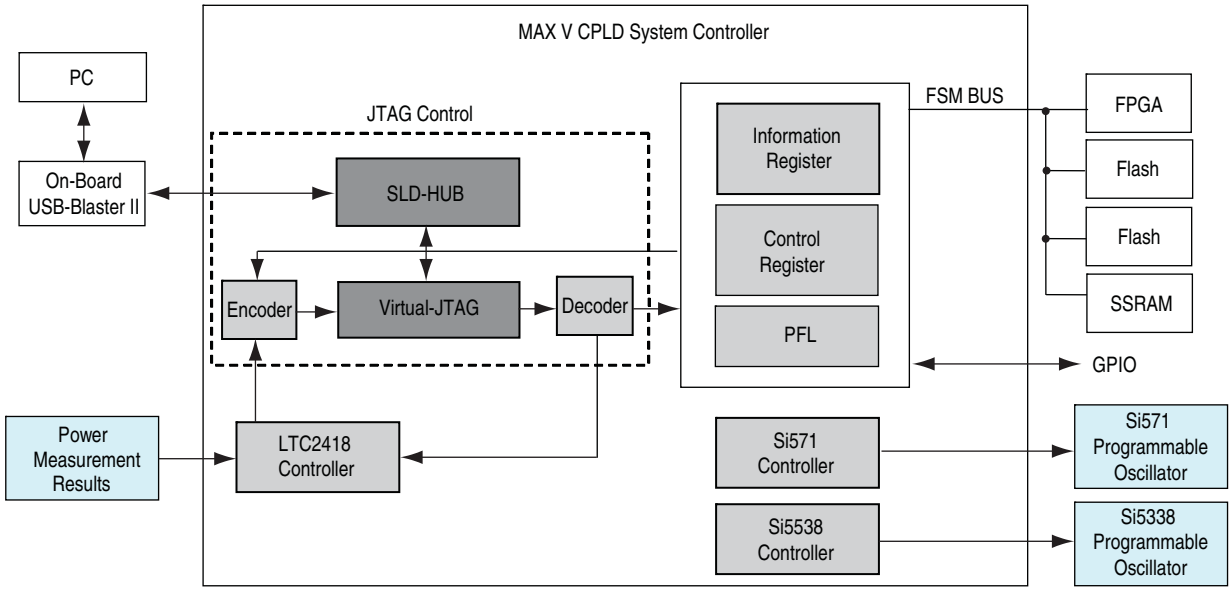


Table 2–5 lists the I/O signals present on the MAX V CPLD 5M2210 System Controller. The signal names and functions are relative to the MAX V device (U15).

Table 2–5. MAX V CPLD 5M2210 System Controller Device Pin-Out (Part 1 of 6)

Board Reference (U15)	Schematic Signal Name	I/O Standard	Description
N4	5M2210_JTAG_TMS	2.5-V	MAX V JTAG TMS
B9	CLK125_EN	2.5-V	125 MHz oscillator enable
E9	CLK50_EN	2.5-V	50 MHz oscillator enable
J5	CLK_CONFIG	2.5-V	100 MHz configuration clock input
A15	CLK_ENABLE	2.5-V	DIP switch for clock oscillator enable
A13	CLK_SEL	2.5-V	DIP switch for clock select—SMA or oscillator
J12	CLKIN_50_MAXV	2.5-V	50 MHz clock input

Table 2–5. MAX V CPLD 5M2210 System Controller Device Pin-Out (Part 2 of 6)

Board Reference (U15)	Schematic Signal Name	I/O Standard	Description
C9	CLOCK_SCL	2.5-V	Programmable oscillator I2C clock
D9	CLOCK_SDA	2.5-V	Programmable oscillator I2C data
D10	CPU_RESETN	2.5-V	FPGA reset push button
M1	EXTRA_SIG0	2.5-V	USB-Blaster II interface. Reserved for future use.
T13	EXTRA_SIG1	2.5-V	USB-Blaster II interface. Reserved for future use.
T15	EXTRA_SIG2	2.5-V	USB-Blaster II interface. Reserved for future use.
A2	FACTORY_LOAD	2.5-V	DIP switch to load factory or user design at power-up
R14	FACTORY_REQUEST	2.5-V	On-Board USB-Blaster II request to send FACTORY command
N12	FACTORY_STATUS	2.5-V	On-Board USB-Blaster II FACTORY command status
C8	FAN_FORCE_ON	2.5-V	DIP switch to on or off the fan
N7	FLASH_ADVN	2.5-V	FSM bus flash memory address valid
R5	FLASH_CEN0	2.5-V	FSM bus flash memory chip enable 0
M7	FLASH_CEN1	2.5-V	FSM bus flash memory chip enable 1
R6	FLASH_CLK	2.5-V	FSM bus flash memory clock
M6	FLASH_OEN	2.5-V	FSM bus flash memory output enable
T5	FLASH_RDYBSYN0	2.5-V	FSM bus flash memory ready 0
R7	FLASH_RDYBSYN1	2.5-V	FSM bus flash memory ready 1
P7	FLASH_RESETN	2.5-V	FSM bus flash memory reset
N6	FLASH_WEN	2.5-V	FSM bus flash memory write enable
K1	FPGA_CONF_DONE	2.5-V	FPGA configuration done LED
D3	FPGA_CONFIG_D0	2.5-V	FPGA configuration data
C2	FPGA_CONFIG_D1	2.5-V	FPGA configuration data
C3	FPGA_CONFIG_D2	2.5-V	FPGA configuration data
E3	FPGA_CONFIG_D3	2.5-V	FPGA configuration data
D2	FPGA_CONFIG_D4	2.5-V	FPGA configuration data
E4	FPGA_CONFIG_D5	2.5-V	FPGA configuration data
D1	FPGA_CONFIG_D6	2.5-V	FPGA configuration data
E5	FPGA_CONFIG_D7	2.5-V	FPGA configuration data
F3	FPGA_CONFIG_D8	2.5-V	FPGA configuration data
E1	FPGA_CONFIG_D9	2.5-V	FPGA configuration data
F4	FPGA_CONFIG_D10	2.5-V	FPGA configuration data
F2	FPGA_CONFIG_D11	2.5-V	FPGA configuration data
F1	FPGA_CONFIG_D12	2.5-V	FPGA configuration data
F6	FPGA_CONFIG_D13	2.5-V	FPGA configuration data
G2	FPGA_CONFIG_D14	2.5-V	FPGA configuration data
G3	FPGA_CONFIG_D15	2.5-V	FPGA configuration data
N3	FPGA_CVP_CONFDONE	2.5-V	FPGA configuration via protocol done LED
J3	FPGA_DCLK	2.5-V	FPGA configuration clock

Table 2–5. MAX V CPLD 5M2210 System Controller Device Pin-Out (Part 3 of 6)

Board Reference (U15)	Schematic Signal Name	I/O Standard	Description
N1	FPGA_NCONFIG	2.5-V	FPGA configuration active
J4	FPGA_NSTATUS	2.5-V	FPGA configuration ready
H1	FPGA_PR_DONE	2.5-V	FPGA partial reconfiguration done
P2	FPGA_PR_ERROR	2.5-V	FPGA partial reconfiguration error
E2	FPGA_PR_READY	2.5-V	FPGA partial reconfiguration ready
F5	FPGA_PR_REQUEST	2.5-V	FPGA partial reconfiguration request
E14	FSM_A0	2.5-V	FSM address bus
C14	FSM_A1	2.5-V	FSM address bus
C15	FSM_A2	2.5-V	FSM address bus
E13	FSM_A3	2.5-V	FSM address bus
E12	FSM_A4	2.5-V	FSM address bus
D15	FSM_A5	2.5-V	FSM address bus
F14	FSM_A6	2.5-V	FSM address bus
D16	FSM_A7	2.5-V	FSM address bus
F13	FSM_A8	2.5-V	FSM address bus
E15	FSM_A9	2.5-V	FSM address bus
E16	FSM_A10	2.5-V	FSM address bus
F15	FSM_A11	2.5-V	FSM address bus
G14	FSM_A12	2.5-V	FSM address bus
F16	FSM_A13	2.5-V	FSM address bus
G13	FSM_A14	2.5-V	FSM address bus
G15	FSM_A15	2.5-V	FSM address bus
G12	FSM_A16	2.5-V	FSM address bus
G16	FSM_A17	2.5-V	FSM address bus
H14	FSM_A18	2.5-V	FSM address bus
H15	FSM_A19	2.5-V	FSM address bus
H13	FSM_A20	2.5-V	FSM address bus
H16	FSM_A21	2.5-V	FSM address bus
J13	FSM_A22	2.5-V	FSM address bus
R3	FSM_A23	2.5-V	FSM address bus
P5	FSM_A24	2.5-V	FSM address bus
T2	FSM_A25	2.5-V	FSM address bus
J14	FSM_D0	2.5-V	FSM data bus
J15	FSM_D1	2.5-V	FSM data bus
K16	FSM_D2	2.5-V	FSM data bus
K13	FSM_D3	2.5-V	FSM data bus
K15	FSM_D4	2.5-V	FSM data bus
K14	FSM_D5	2.5-V	FSM data bus
L16	FSM_D6	2.5-V	FSM data bus

Table 2–5. MAX V CPLD 5M2210 System Controller Device Pin-Out (Part 4 of 6)

Board Reference (U15)	Schematic Signal Name	I/O Standard	Description
L11	FSM_D7	2.5-V	FSM data bus
L15	FSM_D8	2.5-V	FSM data bus
L12	FSM_D9	2.5-V	FSM data bus
M16	FSM_D10	2.5-V	FSM data bus
L13	FSM_D11	2.5-V	FSM data bus
M15	FSM_D12	2.5-V	FSM data bus
L14	FSM_D13	2.5-V	FSM data bus
N16	FSM_D14	2.5-V	FSM data bus
M13	FSM_D15	2.5-V	FSM data bus
N15	FSM_D16	2.5-V	FSM data bus
N14	FSM_D17	2.5-V	FSM data bus
P15	FSM_D18	2.5-V	FSM data bus
P14	FSM_D19	2.5-V	FSM data bus
D13	FSM_D20	2.5-V	FSM data bus
D14	FSM_D21	2.5-V	FSM data bus
F11	FSM_D22	2.5-V	FSM data bus
J16	FSM_D23	2.5-V	FSM data bus
F12	FSM_D24	2.5-V	FSM data bus
K12	FSM_D25	2.5-V	FSM data bus
M14	FSM_D26	2.5-V	FSM data bus
N13	FSM_D27	2.5-V	FSM data bus
R1	FSM_D28	2.5-V	FSM data bus
P4	FSM_D29	2.5-V	FSM data bus
N5	FSM_D30	2.5-V	FSM data bus
P6	FSM_D31	2.5-V	FSM data bus
B8	HSMA_PRSNTN	2.5-V	HSMC port A present
D6	INT_TSD_SDA	2.5-V	Internal TSD I^2C bus
E6	INT_TSD_SCL	2.5-V	Internal TSD I^2C bus
C4	LTC3880_SDA_2.5V	2.5-V	1.1-V VCC core power supply to PMBus
B4	LTC3880_SCL_2.5V	2.5-V	1.1-V VCC core power supply to PMBus
B1	LTC3880_ALERT_N_2.5V	2.5-V	1.1-V VCC core power supply to PMBus
C5	LTC3880_GPIO0_N_2.5V	2.5-V	1.1-V VCC core power supply to PMBus
L6	JTAG_5M2210_TDI	2.5-V	MAX V CPLD on-board JTAG chain data in
M5	JTAG_5M2210_TDO	2.5-V	MAX V CPLD on-board JTAG chain data out
P3	JTAG_TCK	2.5-V	JTAG chain clock
P11	M570_CLOCK	2.5-V	25-MHz clock to on-board USB-Blaster II for sending FACTORY command
P12	M570_PCIE_JTAG_EN	2.5-V	Low signal to disable the on-board USB-Blaster II when PCI Express is the master to the JTAG chain

Table 2–5. MAX V CPLD 5M2210 System Controller Device Pin-Out (Part 5 of 6)

Board Reference (U15)	Schematic Signal Name	I/O Standard	Description
P10	MAX5_BEN0	2.5-V	FSM bus MAX V byte enable 0
R11	MAX5_BEN1	2.5-V	FSM bus MAX V byte enable 1
T12	MAX5_BEN2	2.5-V	FSM bus MAX V byte enable 2
N11	MAX5_BEN3	2.5-V	FSM bus MAX V byte enable 3
T11	MAX5_CLK	2.5-V	FSM bus MAX V clock
R10	MAX5_CSN	2.5-V	FSM bus MAX V chip select
M10	MAX5_OEN	2.5-V	FSM bus MAX V output enable
N10	MAX5_WEN	2.5-V	FSM bus MAX V write enable
E11	MAX_CONF_DONEN	2.5-V	On-board USB-Blaster II configuration done LED
A4	MAX_ERROR	2.5-V	FPGA configuration error LED
A6	MAX_LOAD	2.5-V	FPGA configuration active LED
M9	MAX_RESETN	2.5-V	MAX V reset push button
B10	MSEL0	2.5-V	FPGA mode select 0
B3	MSEL1	2.5-V	FPGA mode select 1
C10	MSEL2	2.5-V	FPGA mode select 2
C12	MSEL3	2.5-V	FPGA mode select 3
C6	MSEL4	2.5-V	FPGA mode select 4
B7	OVERTEMP	2.5-V	Temperature monitor fan enable
C7	PCIE_JTAG_EN	2.5-V	DIP switch to enable the PCI Express JTAG master
D12	PGM_CONFIG	2.5-V	Load the flash memory image identified by the PGM LEDs
B14	PGM_LED0	2.5-V	Flash memory PGM select indicator 0
C13	PGM_LED1	2.5-V	Flash memory PGM select indicator 1
B16	PGM_LED2	2.5-V	Flash memory PGM select indicator 2
B13	PGM_SEL	2.5-V	Toggles the PGM_LED[2:0] LED sequence
D5	SDI_RX_BYPASS	2.5-V	SDI equalization bypass
E8	SDI_RX_EN	2.5-V	SDI receive enable
D11	SDI_TX_EN	2.5-V	SDI transmit enable
R12	SECURITY_MODE	2.5-V	Reserved for future use
E7	SENSE_CS0N	2.5-V	Power monitor chip select
A5	SENSE_SCK	2.5-V	Power monitor SPI clock
D7	SENSE_SDI	2.5-V	Power monitor SPI data in
B6	SENSE_SDO	2.5-V	Power monitor SPI data out
D4	SI571_EN	2.5-V	Si571 programmable VCXO enable
R4	USB_CFG0	2.5-V	Reserved for future use
T4	USB_CFG1	2.5-V	Reserved for future use
P8	USB_CFG2	2.5-V	Reserved for future use
T7	USB_CFG3	2.5-V	Reserved for future use
N8	USB_CFG4	2.5-V	Reserved for future use
R8	USB_CFG5	2.5-V	Reserved for future use

Table 2–5. MAX V CPLD 5M2210 System Controller Device Pin-Out (Part 6 of 6)

Board Reference (U15)	Schematic Signal Name	I/O Standard	Description
T8	USB_CFG6	2.5-V	Reserved for future use
T9	USB_CFG7	2.5-V	Reserved for future use
R9	USB_CFG8	2.5-V	Reserved for future use
P9	USB_CFG9	2.5-V	Reserved for future use
M8	USB_CFG10	2.5-V	Reserved for future use
T10	USB_CFG11	2.5-V	Reserved for future use
H5	USB_CLK	2.5-V	On-board USB-Blaster II clock

Table 2–6 lists the MAX V CPLD 5M2210 System Controller component reference and manufacturing information.

Table 2–6. MAX II CPLD 5M2210 System Controller Component Reference and Manufacturing Information

Board Reference	Description	Manufacturer	Manufacturing Part Number	Manufacturer Website
U15	IC - MAX V CPLD 2210 LES, 256 FBGA 1.8 V VCCINT	Altera Corporation	5M2210ZF256C4N	www.altera.com

FPGA Configuration

This section describes the FPGA, flash memory, and MAX V CPLD 5M2210 System Controller device programming methods supported by the Arria V GX starter board.

The Arria V GX starter board supports the following three configuration methods:

- Embedded USB-Blaster is the default method for configuring the FPGA at any time using the Quartus II Programmer in JTAG mode with the supplied USB cable.
- External USB-Blaster for configuring the FPGA using an external USB-Blaster that connects to the JTAG programming header.
- Flash memory download for configuring the FPGA using stored images from the flash memory on either power-up or pressing the PGM_CONFIG push button (S1).

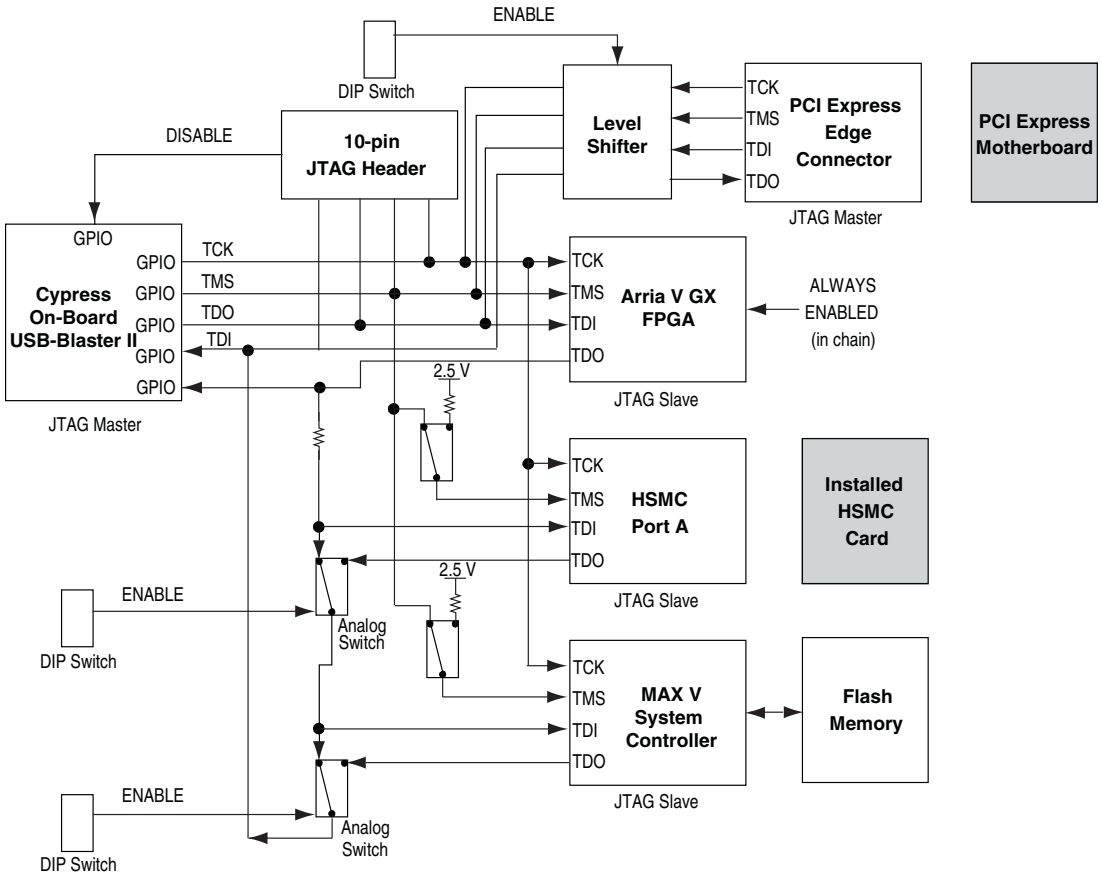
FPGA Programming over Embedded USB-Blaster

This configuration method implements a USB Type-B connector (J14), a USB 2.0 PHY device (U23), and an Altera MAX II CPLD EPM570F100C5N (U21) to allow FPGA configuration using a USB cable. This USB cable connects directly between the USB port on the board and a USB port of a PC running the Quartus II software.

The embedded USB-Blaster in the MAX II CPLD EPM570F100C5N normally masters the JTAG chain. To prevent contention between the JTAG masters, the embedded USB-Blaster is automatically disabled when you connect an external USB-Blaster to the JTAG chain through the JTAG connector.

Figure 2–5 illustrates the JTAG chain.

Figure 2–5. JTAG Chain



The JTAG DIP switch (SW2) controls the jumpers shown in Figure 2–5. To connect a device or interface in the chain, their corresponding switch must be in the OFF position. Slide all the switches in the ON position to only have the FPGA in the chain.

The MAX V CPLD 5M2210 System Controller must be in the chain to use some of the GUI interfaces.

Flash Memory Programming

Flash memory programming is possible through a variety of methods.

The default method is to use the factory design—Board Update Portal. This design is an embedded webserver, which serves the Board Update Portal web page. The web page allows you to select new FPGA designs including hardware, software, or both in an industry-standard S-Record File (**.flash**) and write the design to the user hardware page (page 1) of the flash memory over the network.

The secondary method is to use the pre-built parallel flash loader (PFL) design included in the development kit. The development board implements the Altera PFL megafunction for flash memory programming. The PFL megafunction is a block of logic that is programmed into an Altera programmable logic device (FPGA or CPLD). The PFL functions as a utility for writing to a compatible flash memory device. This pre-built design contains the PFL megafunction that allows you to write either page 0, page 1, or other areas of flash memory over the USB interface using the Quartus II software. This method is used to restore the development board to its factory default settings.

Other methods to program the flash memory can be used as well, including the Nios® II processor.

For more information on the Nios II processor, refer to the Nios II Processor page of the Altera website.

FPGA Programming from Flash Memory

On either power-up or by pressing the program configuration push button, PGM_CONFIG (S1), the MAX V CPLD 5M2210 System Controller's PFL configures the FPGA from the flash memory. The PFL megafunction reads 16-bit data from the flash memory and converts it to fast passive parallel (FPP) format. This 16-bit data is then written to the dedicated configuration pins in the FPGA during configuration.

Pressing the PGM_CONFIG push button (S1) loads the FPGA with a hardware page based on which PGM_LED[2:0] LED (D11, D12, D13) illuminates.

Table 2–7 defines the design that loads when you press the PGM_CONFIG push button.

Table 2–7. PGM_LED Settings *(1)*

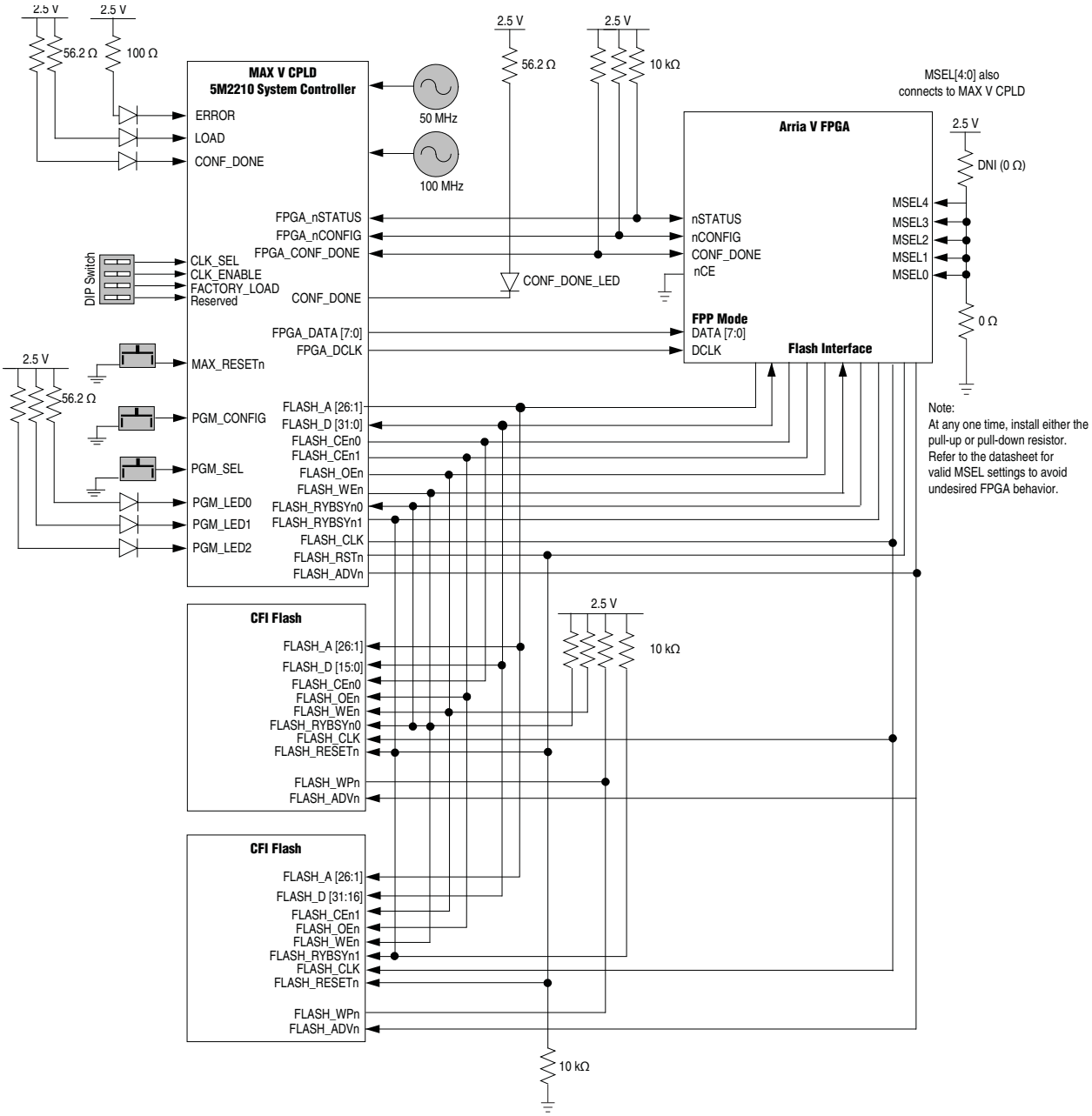
PGM_LED0	PGM_LED1	PGM_LED2	Design
ON	OFF	OFF	Factory
OFF	ON	OFF	User design 1
OFF	OFF	ON	User design 2

Note to Table 2–7:

(1) ON indicates a setting of '0' while OFF indicates a setting of '1'.

Figure 2–6 shows the PFL configuration.

Figure 2–6. PFL Configuration



For information about the flash memory map storage, refer to the *Arria V GX Starter Kit User Guide*.

FPGA Programming over External USB-Blaster

The JTAG programming header provides another method for configuring the FPGA using an external USB-Blaster device with the Quartus II Programmer running on a PC. The external USB-Blaster connects to the board through the JTAG header (J9).

For more information on the following topics, refer to the respective documents:

- Board Update Portal and PFL design, refer to the *Arria V GX Starter Kit User Guide*.
- PFL megafunction, refer to *Parallel Flash Loader Megafunction User Guide.*

Status Elements

The development board includes status LEDs. This section describes the status elements.

Table 2–8 lists the LED board references, names, and functional descriptions.

Table 2–8. Board-Specific LEDs (Part 1 of 2)

Board Reference	Schematic Signal Name	I/O Standard	Description
D30	Power	5.0-V	Blue LED. Illuminates when 5.0 V power is active.
D12	MAX_CONF_DONEn	2.5-V	Green LED. Illuminates when the FPGA is successfully configured. Driven by the MAX V CPLD 5M2210 System Controller.
D11	MAX_LOAD	2.5-V	Green LED. Illuminates when the MAX V CPLD 5M2210 System Controller is actively configuring the FPGA. Driven by the MAX V CPLD 5M2210 System Controller.
D10	MAX_ERROR	2.5-V	Red LED. Illuminates when the MAX V CPLD 5M2210 System Controller fails to configure the FPGA. Driven by the MAX V CPLD 5M2210 System Controller.
D24 D25 D26	PGM_LED[0] PGM_LED[1] PGM_LED[2]	2.5-V	Green LEDs. Illuminates to indicate which hardware page loads from flash memory when you press the PGM_SEL push button.
D6, D7 D8, D9	JTAG_RX, JTAG_TX SC_RX, SC_TX	2.5-V	Green LEDs. Illuminates to indicate USB-Blaster II receive and transmit activities.
D2	ENET_LED_TX	2.5-V	Green LED. Illuminates to indicate Ethernet PHY transmit activity. Driven by the Marvell 88E1111 PHY.
D3	ENET_LED_RX	2.5-V	Green LED. Illuminates to indicate Ethernet PHY receive activity. Driven by the Marvell 88E1111 PHY.
D33	ENET_LED_LINK10	2.5-V	Green LED. Illuminates to indicate Ethernet linked at 10 Mbps connection speed. Driven by the Marvell 88E1111 PHY.
D5	ENET_LED_LINK100	2.5-V	Green LED. Illuminates to indicate Ethernet linked at 100 Mbps connection speed. Driven by the Marvell 88E1111 PHY.
D4	ENET_LED_LINK1000	2.5-V	Green LED. Illuminates to indicate Ethernet linked at 1000 Mbps connection speed. Driven by the Marvell 88E1111 PHY.

Table 2–8. Board-Specific LEDs (Part 2 of 2)

Board Reference	Schematic Signal Name	I/O Standard	Description
D1	SDI_RX_CDn	3.3-V	Green LED. Illuminates to indicate that input signal is detected at the SDI RX port. Driven by the SDI cable equalizer.
D15	HSMA_PRSNTn	3.3-V	Green LED. Illuminates when HSMC port A has a board or cable plugged-in such that pin 160 becomes grounded. Driven by the add-in card.

Table 2–9 lists the board-specific LEDs component references and manufacturing information.

Table 2–9. Board-Specific LEDs Component References and Manufacturing Information

Board Reference	Description	Manufacturer	Manufacturer Part Number	Manufacturer Website
D1 – D9, D11 – D15, D24 – D26, D33	Green LEDs	Lumex Inc.	SML-LXT0805GW-TR	www.lumex.com
D10	Red LED	Lumex Inc.	SML-LXT0805IW-TR	www.lumex.com
D30	Blue LED	Lumex Inc.	SML-LX0805USBC-TR	www.lumex.com

Setup Elements

The starter board includes several different kinds of setup elements. This section describes the following setup elements:

- Board settings DIP switch
- JTAG settings DIP switch
- PCI Express control DIP switch
- CPU reset push button
- MAX V reset push button
- Image load push button
- Image select push button

Table 2–10 lists the switch and push button component references and manufacturing information.

Table 2–10. Switch and Push Button Component References and Manufacturing Information

Board Reference	Description	Manufacturer	Manufacturer Part Number	Manufacturer Website
SW1, SW2, SW4	Four-position DIP switch	C&K Components/ ITT Industries	TDA04H0SB1	www.ittcannon.com
S1–S4	Push button	Panasonic	EVQPAC07K	www.panasonic.com