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VCU110 Evaluation Board

User Guide

UG1073 (v1.3) March 15, 2017

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Revision History

The following table shows the revision history for this document.

Date	Version	Revision
03/15/2017	1.3	Updated Micron HMC part number throughout. Updated Table 1-16, Table 1-18, Table 1-51, and Table 1-52.
03/26/2016	1.2	Updated Dual Quad-SPI Flash Memory, Micro-SD Card Interface, and FMC HPC1 Connector J2. Updated Table 1-15, Table 1-16, Table 1-17, Table 1-18, Table 1-19, Table 1-20, Table 1-23, Table 1-24, Table 1-25, Table 1-40, and Table 1-59. Added thickness information to Appendix F, Board Specifications.
01/16/2016	1.1	Updated the UltraScale XCVU190-2FLGC2104EES9847 FPGA part number throughout.
11/21/2015	1.0	Initial Xilinx release.

Table of Contents

VCU110 Evaluation Board Features

Overview

The VCU110 evaluation board for the Xilinx Virtex® UltraScale™ XCVU190-2FLGC2104EES9847 FPGA provides a hardware environment for developing and evaluating designs targeting the UltraScale XCVU190-2FLGC2104EES9847 FPGA. The VCU110 evaluation board provides features common to many evaluation systems, including QDRII+ and RLD3 component memory, a hybrid memory cube component memory, a CFP4 Quad C form-factor pluggable module connector, an Ethernet PHY, general purpose I/O, a four-lane PCI Express® interface connector, and two UART interfaces. Other features can be supported using VITA-57 FPGA mezzanine cards (FMC) attached to two high pin count (HPC) FMC connectors.

See Appendix H, Additional Resources and Legal Notices for references to documents, files, and resources relevant to the VCU110 board.

VCU110 Evaluation Board Features

The VCU110 evaluation board features are listed here. Detailed information for each feature is provided in Feature Descriptions, starting on page 12.

- Virtex UltraScale XCVU190-2FLGC2104EES9847 FPGA
- 144 Mb QDRII+ component memory interface (1 x 18-bit SIO device)
- 2 x 576 Mb RLD3 component memories (1 x 36-bit x 16M), 1 x 18-bit x 32M CIO devices)
- 4 GB Hybrid Memory Cube (HMC)
- Dual 512 Mb Quad-SPI (QSPI) flash memory
- Micro secure digital (SD) connector
- USB JTAG interface through Digilent module with micro-B USB connector
- Clock sources:
  - SI5335A Quad clock generator
  - Si570 IIC programmable LVDS clock generator

  - Three SI5328 clock multiplier and jitter attenuators
  - SMA user clock connector pair (differential)
- 52 GTY transceivers (13 Quads)
  - 5 Quads connected to Interlaken connector
  - 2 Quads connected to 2 BullsEye™ SMA connectors
  - 2 Quads connected to EXAMAX connector
  - 4 Quads connected to CPF4 connector
- 52 GTH transceivers (13 Quads)
  - 8 Quads connected to HMC
  - 2 Quads connected to FMC HPC0 connector DP
  - 2 Quads connected to FMC HPC1 connector DP
  - 1 Quad connected to PCIe® cable connector
- Ethernet PHY SGMII interface with RJ-45 connector
- Dual USB-to-UART bridge with micro-B USB connector
- Status LEDs
- User I/O (pushbuttons, DIP switch, LEDs)
- Pmod header
- Two VITA 47.1 FMC HPC connectors
- Configuration options:
  - Quad-SPI flash memory
  - USB JTAG configuration port (Digilent module)
  - Platform cable 2 mm 2x7 shrouded header J3 JTAG configuration port
- Zynq® XC7Z010 based system controller

Block Diagram

The VCU110 evaluation board block diagram is shown in Figure 1-1.

The VCU110 board schematics are available for download from the Xilinx Virtex UltraScale FPGA VCU110 Evaluation Kit website. The page numbers shown in Figure 1-1 refer to schematic page numbers in the VCU110 schematic XTP407.

CAUTION! *The VCU110 evaluation board can be damaged by electrostatic discharge (ESD). Follow ESD prevention measures when handling the board.*

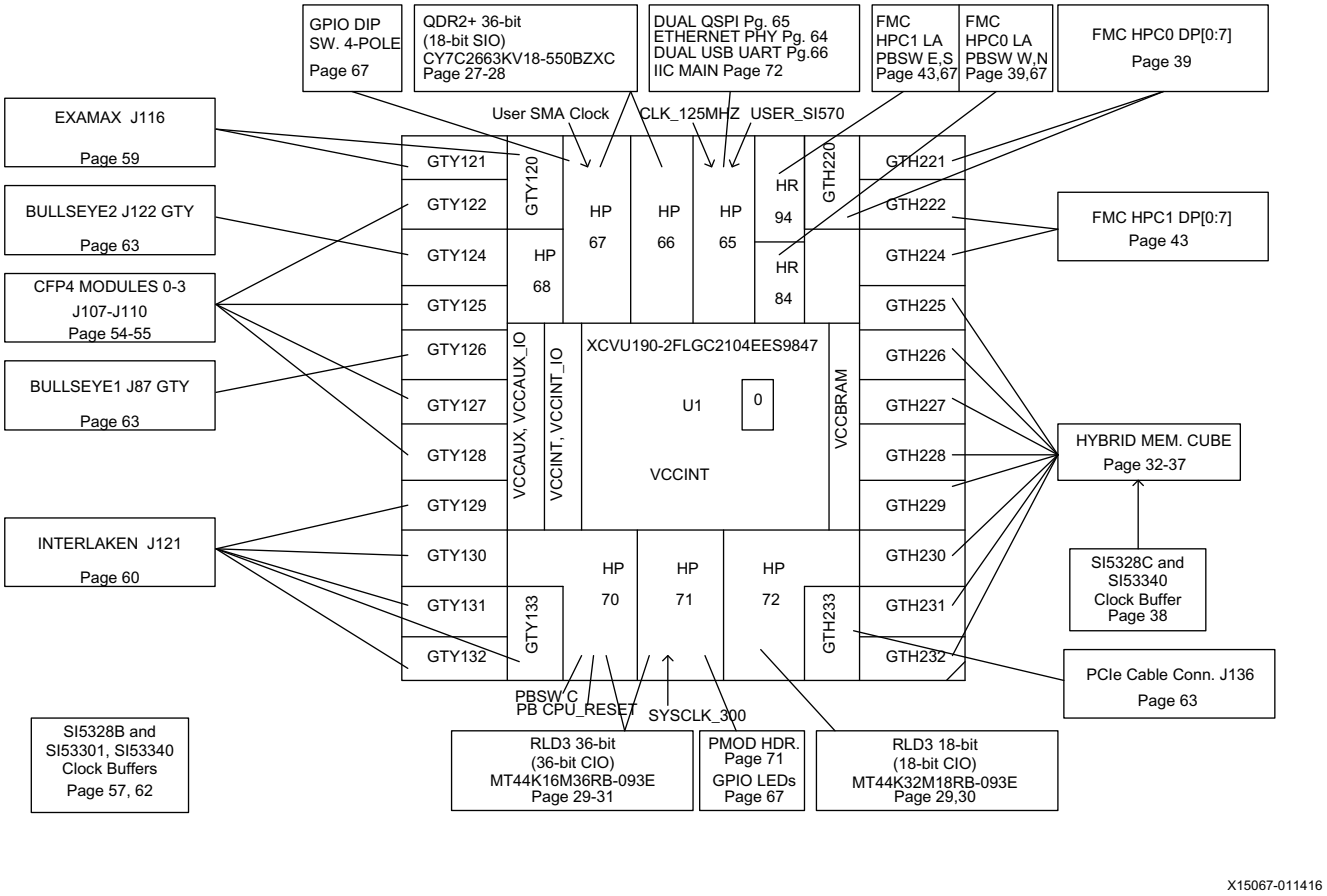

Figure 1-1: **VCU110 Evaluation Board Block Diagram**

Board Layout

Figure 1-2 shows the VCU110 evaluation board. Each numbered feature that is referenced in Figure 1-2 is described in Table 1-1. Detailed information is provided under Feature Descriptions.

IMPORTANT: *The image in Figure 1-2 is for reference only and might not reflect the current revision of the board.*

CAUTION! *The VCU110 evaluation board can be damaged by electrostatic discharge (ESD). Follow ESD prevention measures when handling the board.*

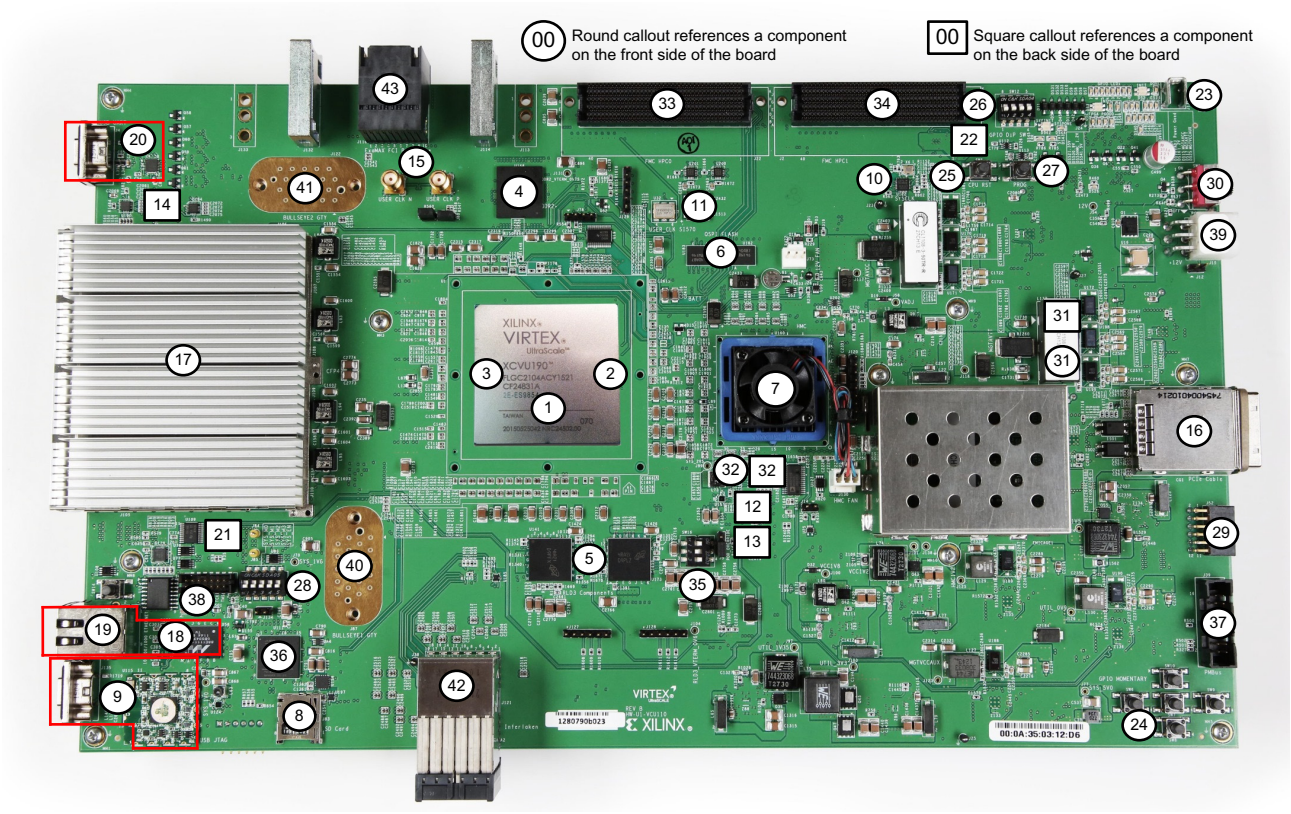

Figure 1-2: **VCU110 Board Component Locations**

Table 1-1: **VCU110 Board Component Descriptions**

Callout	Feature	Notes	Schematic 0381556 Page Number
1	Virtex UltraScale XCVU190-2FLGC2104EES9847 FPGA, (U1) (with fan-sink on soldered FPGA)	XCVU190-2FLGC2104EES9847, COFAN 30-5530-03	
2	GTY Transceivers, 13 Quads	Embedded within FPGA U1	9-12
3	GTH Transceivers, 13 Quads	Embedded within FPGA U1	13-16
4	QDR2+ Component Memory, 576 Mb 18-bit QDR2+ SIO component memory I/F (U168)	Cypress CY7C2663KV18-550BZXC	26
5	RLD3 Component Memory, RLD3 36-bit and 18-bit component memory I/F (U141, U173)	Micron MT44K16M36RB-093E Micron MT44K32M18RB-093E	28-29
6	Dual Quad-SPI Flash Memory (128Mb) (U114)	Micron N25Q128A11ESF40G	62
7	2 GB Hybrid Memory Cube (HMC) (U160) (with fan-sink)	Micron MT43A4G40200NFA, RADIAN XLX027	31-36
8	Micro-SD Card Interface connector (J83)	Molex 5025700893	56
9	USB JTAG Interface (U115), w/Micro-B connector	Digilent USB JTAG module	25
10	System Clock. multi-output clock generator, SYSCLK and other clocks, 1.8V LVDS (U122)	SI5335A-B02436-GM, 4 outputs: 300 MHz, 125 MHz, 90 MHz, 33.33 MHz	46
11	Programmable User Clock, I2C programmable user clock LVDS (U32) with 1-to-2 LVDS buffer (U32)	Silicon Labs SI570BAB0000544DG (default 156.250MHz) with Si53340 buffer	47
12	Jitter-Attenuating Clock Multipliers for HMC jitter attenuated clock (U57)	Silicon Labs SI5328B-C-GMR	37
13	Jitter-Attenuating Clock Multipliers for ExaMAX jitter attenuated clock (U181)	Silicon Labs SI5328C-C-GM	59
14	Jitter-Attenuating Clock Multipliers for CFP4 module jitter attenuated clock (U179)	Silicon Labs SI5328C-C-GM	55
15	User SMA Clock source, user differential SMA clock P/N (J34/J35)	Rosenberger 32K10K-400L5	60
16	PCIe Cable Connector, (J136), with cage (CG1)	J136 Molex 0755860010 CG1 Molex 0745400401	60
17	CFP Module Quad Connectors (CFP4), (J108-J110)	4x Yamaichi CN121S-056-0001	52-53
18	10/100/1,000Mb/s Tri-Speed Ethernet PHY w/RJ45, SGMII mode only, (U58,P3)	Marvell M88E1111-BAB1C000 with Halo HFJ11-1G01E-L12RL RJ45	61
19	Ethernet PHY Status LEDs, LEDs are integrated into P3 bezel	Halo HFJ11-1G01E-L12RL RJ45 integrated status LEDs (Rev B)	61
20	Dual USB-to-UART Bridge, bridge device (U34) with mini-B connector (J4)	Silicon Labs CP2105-F01-GM bridge, Hirose ZX62D-AB-5P8 connector	63
21	I2C Bus, Topology and Bus Switches, I2C Bus MUX (U28)	TI TCA9548APWR	69

Table 1-1: **VCU110 Board Component Descriptions *(Cont'd)***

Callout	Feature	Notes	Schematic 0381556 Page Number
22	I2C Bus, Topology and Bus Switches, I2C Bus MUX (U80)	TI PCA9544ARGYR	69
23	User GPIO LEDs, (DS6-DS10, DS31-DS33)	GPIO LEDs, green 0603 Lumex SML-LX0603GW-TR	64
24	User Pushbuttons, active-High (SW6-SW10)	E-Switch TL3301EF100QG in North, South, East, West, Center pattern	64
25	CPU Reset Pushbutton, user CPU reset, active-High (SW5)	E-Switch TL3301EF100QG	64
26	GPIO DIP Switch, (SW12)	4-pole C&K SDA04H1SBD	64
27	Program_B Pushbutton Switch, FPGA PROG pushbutton (SW4)	E-Switch TL3301EF100QG	64
28	System controller mode DIP switch, DIP switch (SW15) See Switches and Appendix C, Getting Started with System Controller	5-pole C&K SDA05H1SBD	51
29	User PMOD GPIO Header, PMOD header (J52) w/level-shifters (U41)	2x6 0.1 inch male header Sullins PBC36DAAN; TI TXS0108EPWR	68
30	Power On/Off Slide Switch SW1	C&K 1201M2S3AQE2	71
31	VCU110 Board Power System, power management system (top and bottom)	Maxim MAX15301 and MAX15303 digital POL controllers	72-86
32	Monitoring Voltage and Current, power management voltage and current sensing SYSMON external circuitry (top and bottom)	Analog Devices MUX ADG707BRUZ TI op amps INA333AIDGKR	66-67
33	FMC HPC0 Connector J22	Samtec ASP_134486-01	38-41
34	FMC HPC1 Connector J2	Samtec ASP_134486-01	42-45
35	Mode DIP switch (SW16) see FPGA Device Configuration	3-pole C&K SDA03H1SBD	3
36	VCU110 Zynq-7000 AP SoC XC7Z010 System Controller (U111)	XC7Z010CLG225	48-50
37	2x8 shrouded PMBus connector (J39), see Monitoring Voltage and Current	Assman AWHW16G-0202	70
38	2x7 2 mm shrouded JTAG cable connector (J3) See USB JTAG Interface	MOLEX 87832-1420	25
39	12V power input 2x6 connector (J15). See Power On/Off Slide Switch SW1	MOLEX 39-30-1060	71
40	Samtec BULLSEYE1 Connector (J87)		60
41	Samtec BULLSEYE2 Connector (J122)		60
42	Interlaken Connector (J121)	TYCO 2187194	58

Table 1-1: **VCU110 Board Component Descriptions *(Cont'd)***

Callout	Feature	Notes	Schematic 0381556 Page Number
43	ExaMAX Backplane Connector, (J116)	FCI 10126363-101LF	57

Notes:

1. The VCU110 board schematics are available for download from the VCU110 Evaluation Kit website.
2. The VCU110 board jumper header locations are shown in Figure A-1.

Feature Descriptions

Virtex UltraScale XCVU190-2FLGC2104EES9847 FPGA

[Figure 1-2, callout 1]

The VCU110 board is populated with the Virtex UltraScale XCVU190-2FLGC2104EES9847 FPGA. For further information on Virtex UltraScale FPGAs, see *Virtex UltraScale Architecture Data Sheet* (DS893), [Ref 1].

FPGA Device Configuration

The VCU110 board supports two of the five UltraScale FPGA configuration modes:

- Master SPI using the onboard dual Quad SPI (QSPI) flash memory
- JTAG using either:
  - USB JTAG configuration port (Digilent module U115), or
  - Xilinx platform cable, 2 mm, keyed flat cable header (J3)

Each configuration interface corresponds to one or more configuration modes and bus widths as listed in Table 1-2. The mode switches M2, M1, and M0 are on SW16 positions 1, 2, and 3 respectively as shown in Figure 1-3. The FPGA default mode setting M[2:0] = 101, selecting the JTAG configuration mode.

Table 1-2: **VCU110 Board FPGA Configuration Modes**

Configuration Mode	SW16 DIP Switch Settings (M[2:0])	Bus Width	CCLK Direction
Master SPI	001	x1, x2, x4	Output
JTAG	101	x1	Not applicable

For full details on configuring the FPGA, see *UltraScale Architecture Configuration User Guide* (UG570) [Ref 2].

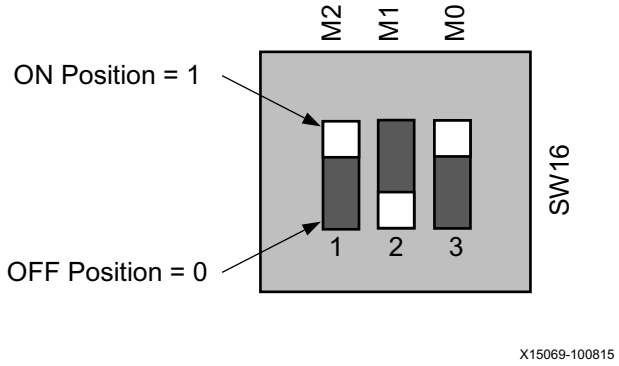

Figure 1-3: **SW16 Default Settings**

Encryption Key Backup Circuit

The XCVU190 FPGA U1 implements bitstream encryption key technology. The VCU110 board provides the encryption key backup battery circuit shown in Figure 1-4. The Seiko TS518FE rechargeable 1.5V lithium button-type battery B1 is soldered to the board with the positive output connected to the XCVU190 FPGA U1 V_{CCBATT} pin AN13. The battery supply current I_{BATT} specification is 150 nA maximum when board power is off. B1 is charged from the SYS_1V8 1.8V rail through a series diode with a typical forward voltage drop of 0.38V and a 4.7 kΩ current limiting resistor. The nominal charging voltage is 1.42V.

Figure 1-4 shows the encryption key battery backup circuit.

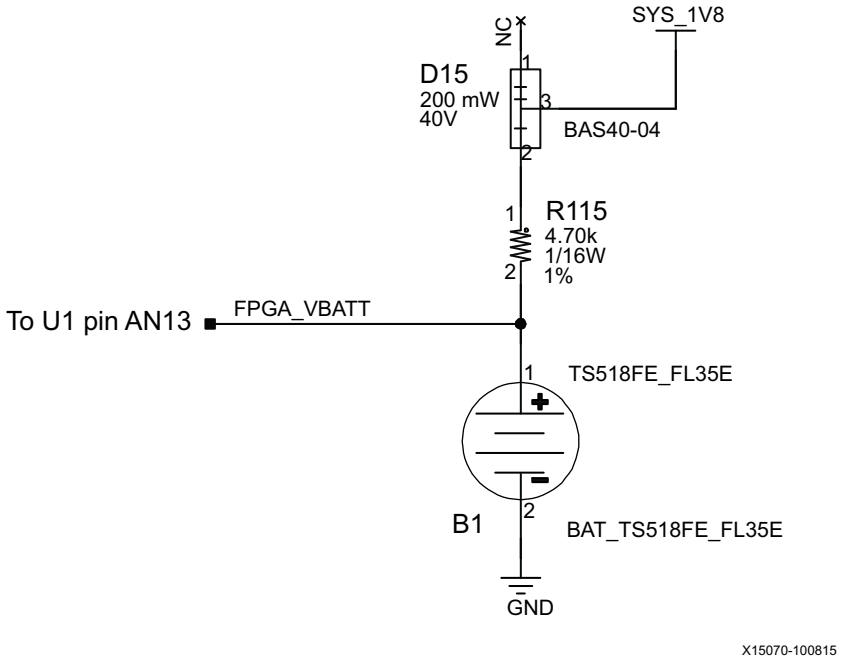

Figure 1-4: **Encryption Key Backup Circuit**

I/O Voltage Rails

There are eight I/O banks available on the XCVU190 device and the VCU110 board. The voltages applied to the FPGA I/O banks (shown in Figure 1-5) used by the VCU110 board are listed in Table 1-3.

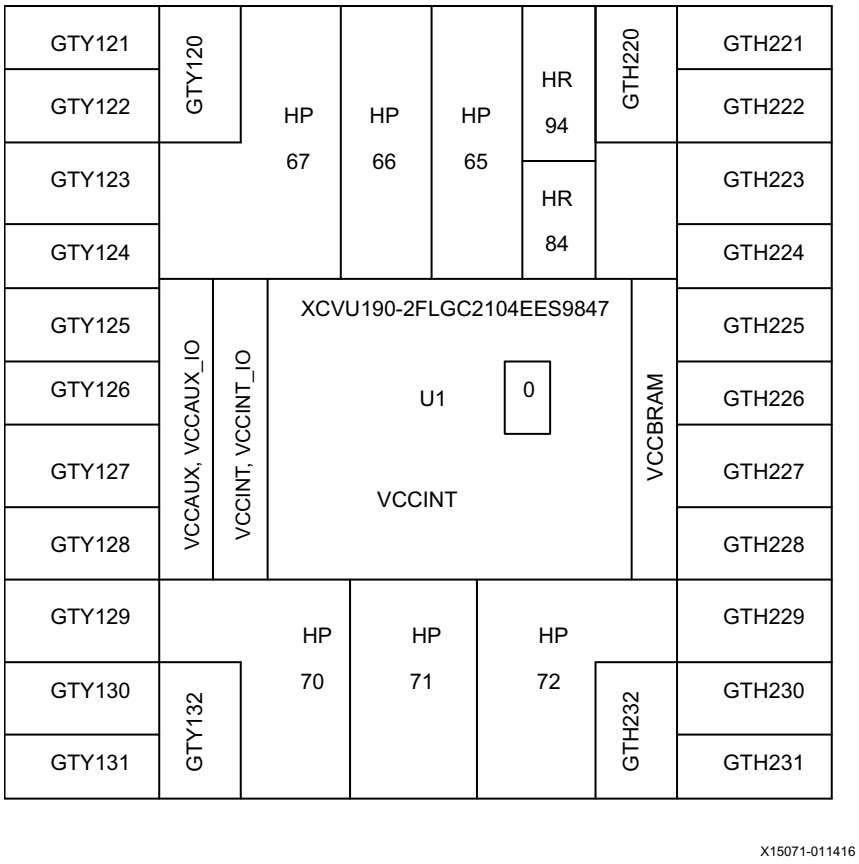

Figure 1-5: **UltraScale XCVU190 Bank Locations**

Table 1-3: **I/O Bank Voltage Rails**

FPGA (U1) Bank	Power Supply Rail Net Name	Voltage
Bank 0	VCC1V8_FPGA	1.8V
HP Bank 65	VCC1V8_FPGA	1.8V
HP Bank 66	VCC1V5_FPGA	1.5V
HP Bank 67	VCC1V5_FPGA	1.5V
HP Bank 68	VADJ_1V8_FPGA	1.8V
HP Bank 70	VCC1V2_FPGA	1.2V
HP Bank 71	VCC1V2_FPGA	1.2V
HP Bank 72	VCC1V2_FPGA	1.2V

Table 1-3: **I/O Bank Voltage Rails *(Cont'd)***

FPGA (U1) Bank	Power Supply Rail Net Name	Voltage
HR Bank 84	VCC1V8_FPGA	1.8V
HR Bank 94	VCC1V8_FPGA	1.8V

QDR2+ Component Memory

[Figure 1-2, callout 4]

The 144 Mb QDR2+ component memory system is comprised of one 18-bit separate I/O (SIO) device (Cypress CY7C2663KV18-550BZXC) located at U168. This memory system is connected to the XCVU190 HP banks 66 and 67. The DDR4 0.75V V_{TT} termination voltage (net QDR2_VTERM_0V75) is sourced from TI TPS51200DR linear regulator U167. The connections between QDR2 component memory U168 and XCVU190 banks 66 and 67 are listed in Table 1-4.

Table 1-4: **QDR2 Memory U168 18-bit SIO I/F to FPGA U1 Banks 66 and 67**

FPGA (U1) Pin	Schematic Net Name	I/O Standard	Pin Number	Pin Name
AM23	QDR2_18B_D0	HSTL_I_DCI	P10	D0
AM24	QDR2_18B_D1	HSTL_I_DCI	N11	D1
AN23	QDR2_18B_D2	HSTL_I_DCI	M11	D2
AP22	QDR2_18B_D3	HSTL_I_DCI	K10	D3
AM26	QDR2_18B_D4	HSTL_I_DCI	J11	D4
AN25	QDR2_18B_D5	HSTL_I_DCI	G11	D5
AN26	QDR2_18B_D6	HSTL_I_DCI	E10	D6
AP25	QDR2_18B_D7	HSTL_I_DCI	D11	D7
AP23	QDR2_18B_D8	HSTL_I_DCI	C11	D8
AU26	QDR2_18B_D9	HSTL_I_DCI	B3	D9
AT26	QDR2_18B_D10	HSTL_I_DCI	C3	D10
AR25	QDR2_18B_D11	HSTL_I_DCI	D2	D11
AT24	QDR2_18B_D12	HSTL_I_DCI	F3	D12
AR24	QDR2_18B_D13	HSTL_I_DCI	G2	D13
AU22	QDR2_18B_D14	HSTL_I_DCI	J3	D14
AT22	QDR2_18B_D15	HSTL_I_DCI	L3	D15
AR22	QDR2_18B_D16	HSTL_I_DCI	M3	D16
AR23	QDR2_18B_D17	HSTL_I_DCI	N2	D17
BA22	QDR2_18B_A0	HSTL_I_DCI	A3	A0
AY24	QDR2_18B_A1	HSTL_I_DCI	A9	A1
AW23	QDR2_18B_A2	HSTL_I_DCI	B4	A2

Table 1-4: **QDR2 Memory U168 18-bit SIO I/F to FPGA U1 Banks 66 and 67 *(Cont'd)***

FPGA (U1) Pin	Schematic Net Name	I/O Standard	Pin Number	Pin Name
AV24	QDR2_18B_A3	HSTL_I_DCI	B8	A3
AW22	QDR2_18B_A4	HSTL_I_DCI	C5	A4
BB24	QDR2_18B_A5	HSTL_I_DCI	C6	A5 (BL2/BL4)
BE23	QDR2_18B_A6	HSTL_I_DCI	C7	A6
BD23	QDR2_18B_A7	HSTL_I_DCI	N5	A7
BC23	QDR2_18B_A8	HSTL_I_DCI	N6	A8
BE24	QDR2_18B_A9	HSTL_I_DCI	N7	A9
BF22	QDR2_18B_A10	HSTL_I_DCI	P44	A10
BF21	QDR2_18B_A11	HSTL_I_DCI	P55	A11
BC24	QDR2_18B_A12	HSTL_I_DCI	P77	A12
BB23	QDR2_18B_A13	HSTL_I_DCI	P88	A13
BE22	QDR2_18B_A14	HSTL_I_DCI	R33	A14
BD22	QDR2_18B_A15	HSTL_I_DCI	R44	A15
BB22	QDR2_18B_A16	HSTL_I_DCI	R55	A16
BA24	QDR2_18B_A17	HSTL_I_DCI	R77	A17
BA25	QDR2_18B_A18	HSTL_I_DCI	R88	A18
AV23	QDR2_18B_A19	HSTL_I_DCI	R9	A19
AY25	QDR2_18B_A20	HSTL_I_DCI	A10	NC_72M
AY22	QDR2_18B_A21	HSTL_I_DCI	A2	NC_144M
AN24	QDR2_18B_BWS0_B	HSTL_I_DCI	B7	BWS0_BS0_B_B
AT25	QDR2_18B_BWS1_B	HSTL_I_DCI	A5	BWS1_BS1_B_B
AU23	QDR2_18B_K_P	DIFF_HSTL_I_D	B6	K
AU24	QDR2_18B_K_N	DIFF_HSTL_I_D	A6	K_B
AY23	QDR2_18B_WPS_B	HSTL_I_DCI	A7	WPS_B
BF24	QDR2_18B_RPS_B	HSTI_I	A8	RPS_B
AW25	QDR2_18B_DOFF_B	HSTL_I_DCI	H1	DOFF_B
AN28	QDR2_18B_Q0	HSTL_I_DCI	P11	Q0
AM29	QDR2_18B_Q1	HSTL_I_DCI	M10	Q1
AN29	QDR2_18B_Q2	HSTL_I_DCI	L11	Q2
AM31	QDR2_18B_Q3	HSTL_I_DCI	K11	Q3
AP28	QDR2_18B_Q4	HSTL_I_DCI	J10	Q4
AN31	QDR2_18B_Q5	HSTL_I_DCI	F11	Q5
AR27	QDR2_18B_Q6	HSTL_I_DCI	E11	Q6
AR29	QDR2_18B_Q7	HSTL_I_DCI	C10	Q7
AR30	QDR2_18B_Q8	HSTL_I_DCI	B11	Q8

Table 1-4: **QDR2 Memory U168 18-bit SIO I/F to FPGA U1 Banks 66 and 67 *(Cont'd)***

FPGA (U1) Pin	Schematic Net Name	I/O Standard	Pin Number	Pin Name
AV29	QDR2_18B_Q9	HSTL_I_DCI	B2	Q9
AV28	QDR2_18B_Q10	HSTL_I_DCI	D3	Q10
AU29	QDR2_18B_Q11	HSTL_I_DCI	E3	Q11
AW26	QDR2_18B_Q12	HSTL_I_DCI	F2	Q12
AU28	QDR2_18B_Q13	HSTL_I_DCI	G3	Q13
AU27	QDR2_18B_Q14	HSTL_I_DCI	K3	Q14
AT29	QDR2_18B_Q15	HSTL_I_DCI	L2	Q15
AT27	QDR2_18B_Q16	HSTL_I_DCI	N3	Q16
AT31	QDR2_18B_Q17	HSTL_I_DCI	P3	Q17
AT30	QDR2_18B_CQ	HSTL_I_DCI	A11	CQ
AV26	QDR2_18B_CQ_B	HSTL_I_DCI	A1	CQ_B
NA	NA	NA	P6	QVLD

The VCU110 QDR2+ 18-bit SIO memory component interface adheres to the constraints guidelines documented in the QDRII+ Design Guidelines section of the *LogiCORE IP UltraScale Architecture-Based FPGAs Memory Interface Solutions Product Guide V5.0* (PG150) [Ref 3] for Vivado Design Suite. The VCU110 QDR2 memory component interface is a 40Ω impedance implementation.

For more details about the Cypress QDR2+ component memory, see the Cypress CY7C2663KV18-550BZXC data sheet [Ref 21].

RLD3 Component Memory

[Figure 1-2, callout 5]

The 1152 Mb RLD3 component memory system is comprised of two 576 Mb RLDRAM3 devices (Micron MT44K16M36RB-093E 36-bit and MT44K32M18RB-093E 18-bit) located at U141 and U173. This memory system is connected to the XCVU190 HP banks 70, 71 and 72. The RLD3 0.6V V_{TT} termination voltage (net RLD3_VTERM_0V6) is sourced from TI TPS51200DR linear regulator U143. The connections between RLD3 component memory U141 and XCVU190 banks 70 and 71 are listed in Table 1-5.

Table 1-5: **RLD3 Memory U141 36-bit I/F to FPGA U1 Banks 70 and 71**

FPGA (U1) Pin	Schematic Net Name	I/O Standard
C27	RLD3_36B_DQ0	SSTL12
D29	RLD3_36B_DQ1	SSTL12
A29	RLD3_36B_DQ2	SSTL12
B27	RLD3_36B_DQ3	SSTL12

Table 1-5: **RLD3 Memory U141 36-bit I/F to FPGA U1 Banks 70 and 71 *(Cont'd)***

FPGA (U1) Pin	Schematic Net Name	I/O Standard
B26	RLD3_36B_DQ4	SSTL12
A28	RLD3_36B_DQ5	SSTL12
C28	RLD3_36B_DQ6	SSTL12
C29	RLD3_36B_DQ7	SSTL12
B28	RLD3_36B_DQ8	SSTL12
K29	RLD3_36B_DQ9	SSTL12
J26	RLD3_36B_DQ10	SSTL12
K28	RLD3_36B_DQ11	SSTL12
N27	RLD3_36B_DQ12	SSTL12
L28	RLD3_36B_DQ13	SSTL12
K26	RLD3_36B_DQ14	SSTL12
M27	RLD3_36B_DQ15	SSTL12
K27	RLD3_36B_DQ16	SSTL12
L29	RLD3_36B_DQ17	SSTL12
H27	RLD3_36B_DQ18	SSTL12
J27	RLD3_36B_DQ19	SSTL12
G26	RLD3_36B_DQ20	SSTL12
F29	RLD3_36B_DQ21	SSTL12
G28	RLD3_36B_DQ22	SSTL12
E27	RLD3_36B_DQ23	SSTL12
E29	RLD3_36B_DQ24	SSTL12
F26	RLD3_36B_DQ25	SSTL12
F28	RLD3_36B_DQ26	SSTL12
N29	RLD3_36B_DQ27	SSTL12
N32	RLD3_36B_DQ28	SSTL12
M30	RLD3_36B_DQ29	SSTL12
N30	RLD3_36B_DQ30	SSTL12
K31	RLD3_36B_DQ31	SSTL12
M32	RLD3_36B_DQ32	SSTL12
J32	RLD3_36B_DQ33	SSTL12
J31	RLD3_36B_DQ34	SSTL12
K32	RLD3_36B_DQ35	SSTL12
E28	RLD3_36B_DM0	SSTL12
L30	RLD3_36B_DM1	SSTL12
D26	RLD3_36B_QK0_P	SSTL12

Table 1-5: **RLD3 Memory U141 36-bit I/F to FPGA U1 Banks 70 and 71 *(Cont'd)***

FPGA (U1) Pin	Schematic Net Name	I/O Standard
D27	RLD3_36B_QK0_N	SSTL12
N28	RLD3_36B_QK1_P	DIFF_SSTL12
M28	RLD3_36B_QK1_N	DIFF_SSTL12
H28	RLD3_36B_QK2_P	DIFF_SSTL12
H29	RLD3_36B_QK2_N	DIFF_SSTL12
M31	RLD3_36B_QK3_P	DIFF_SSTL12
L31	RLD3_36B_QK3_N	DIFF_SSTL12
A26	RLD3_36B_QVLD0	SSTL12
G27	RLD3_36B_QVLD1	SSTL12
D25	RLD3_36B_A0	SSTL12
C24	RLD3_36B_A3	SSTL12
D24	RLD3_36B_A4	SSTL12
F23	RLD3_36B_A5	SSTL12
E23	RLD3_36B_A8	SSTL12
B22	RLD3_36B_A9	SSTL12
C23	RLD3_36B_A10	SSTL12
G21	RLD3_36B_A13	SSTL12
F24	RLD3_36B_A14	SSTL12
A23	RLD3_36B_A17	SSTL12
B23	RLD3_36B_A18	SSTL12
C25	RLD3_36B_BA0	SSTL12
E24	RLD3_36B_BA1	SSTL12
B25	RLD3_36B_BA2	SSTL12
C22	RLD3_36B_BA3	SSTL12
A25	RLD3_36B_WE_B	SSTL12
A24	RLD3_36B_REF_B	SSTL12
G25	RLD3_36B_CK_P	DIFF_SSTL12
F25	RLD3_36B_CK_N	DIFF_SSTL12
F21	RLD3_36B_RESET_B	SSTL12
E22	RLD3_36B_CS_B	SSTL12
H23	RLD3_36B_DK0_P	DIFF_SSTL12
G23	RLD3_36B_DK0_N	DIFF_SSTL12
H22	RLD3_36B_DK1_P	DIFF_SSTL12
G22	RLD3_36B_DK1_N	DIFF_SSTL12

The connections between RLD3 component memory U173 and XCVU190 bank 72 are listed in Table 1-6.

Table 1-6: **RLD3 Memory U173 18-bit I/F to FPGA U1 Bank 72**

FPGA (U1) Pin	Schematic Net Name	I/O Standard
K16	RLD3_18B_DQ0	SSTL12
L15	RLD3_18B_DQ1	SSTL12
L20	RLD3_18B_DQ2	SSTL12
L18	RLD3_18B_DQ3	SSTL12
J16	RLD3_18B_DQ4	SSTL12
L19	RLD3_18B_DQ5	SSTL12
K18	RLD3_18B_DQ6	SSTL12
M20	RLD3_18B_DQ7	SSTL12
K19	RLD3_18B_DQ8	SSTL12
N19	RLD3_18B_DQ9	SSTL12
M16	RLD3_18B_DQ10	SSTL12
M17	RLD3_18B_DQ11	SSTL12
N20	RLD3_18B_DQ12	SSTL12
P16	RLD3_18B_DQ13	SSTL12
M15	RLD3_18B_DQ14	SSTL12
P17	RLD3_18B_DQ15	SSTL12
P20	RLD3_18B_DQ16	SSTL12
P19	RLD3_18B_DQ17	SSTL12
L16	RLD3_18B_DM0	SSTL12
N17	RLD3_18B_DM1	SSTL12
A20	RLD3_18B_A0	SSTL12
F20	RLD3_18B_A3	SSTL12
E18	RLD3_18B_A4	SSTL12
H18	RLD3_18B_A5	SSTL12
G18	RLD3_18B_A8	SSTL12
H19	RLD3_18B_A9	SSTL12
J19	RLD3_18B_A10	SSTL12
F18	RLD3_18B_A13	SSTL12
A19	RLD3_18B_A14	SSTL12
H20	RLD3_18B_A17	SSTL12
J20	RLD3_18B_A18	SSTL12
E19	RLD3_18B_BA0	SSTL12

Table 1-6: **RLD3 Memory U173 18-bit I/F to FPGA U1 Bank 72 *(Cont'd)***

FPGA (U1) Pin	Schematic Net Name	I/O Standard
A18	RLD3_18B_BA1	SSTL12
B20	RLD3_18B_BA2	SSTL12
G20	RLD3_18B_BA3	SSTL12
B18	RLD3_18B_WE_B	SSTL12
C20	RLD3_18B_REF_B	SSTL12
D20	RLD3_18B_CK_P	DIFF_SSTL12
D19	RLD3_18B_CK_N	DIFF_SSTL12
E21	RLD3_18B_RESET_B	SSTL12
F19	RLD3_18B_CS_B	SSTL12
B21	RLD3_18B_DK0_P	DIFF_SSTL12
A21	RLD3_18B_DK0_N	DIFF_SSTL12
C19	RLD3_18B_DK1_P	DIFF_SSTL12
C18	RLD3_18B_DK1_N	DIFF_SSTL12
K17	RLD3_18B_QK0_P	DIFF_SSTL12
J17	RLD3_18B_QK0_N	DIFF_SSTL12
N18	RLD3_18B_QK1_P	DIFF_SSTL12
M18	RLD3_18B_QK1_N	DIFF_SSTL12
J15	RLD3_18B_QVLD0	SSTL12

The VCU110 RLD3 36-bit and 18-bit memory component interfaces adhere to the constraints guidelines documented in the RLD3 Design Guidelines section of *LogiCORE IP UltraScale Architecture-Based FPGAs Memory Interface Solutions Product Guide* (PG150) [Ref 3] for Vivado Design Suite. The VCU110 RLD3 memory component interface is a 40Ω impedance implementation.

For more details about the Micron RLD3 component memory, see the Micron MT44K16M36RB-093E/ MT44K32M18RB-093E data sheet [Ref 22].

Dual Quad-SPI Flash Memory

[Figure 1-2, callout 6]

The dual 512 Mb Quad-SPI flash memories are located at U182 and U183 and provide 1 Gb of nonvolatile storage that can be used for configuration and data storage.

- Part number: MT25QU512ABA8E12-0SIT (Micron)
- Supply voltage: 1.8V
- Datapath width: 8 bits
- Data rate: various depending on Single/Dual/Quad mode

Note: For details on Bank 0 pins, see the *UltraScale Architecture Configuration User Guide* (UG570) [Ref 2].

Figure 1-6 shows the connections of the linear dual Quad-SPI flash memory on the VCU110 evaluation board. For more details, see the Micron N25QU512ABA8E12-0SIT data sheet [Ref 22].

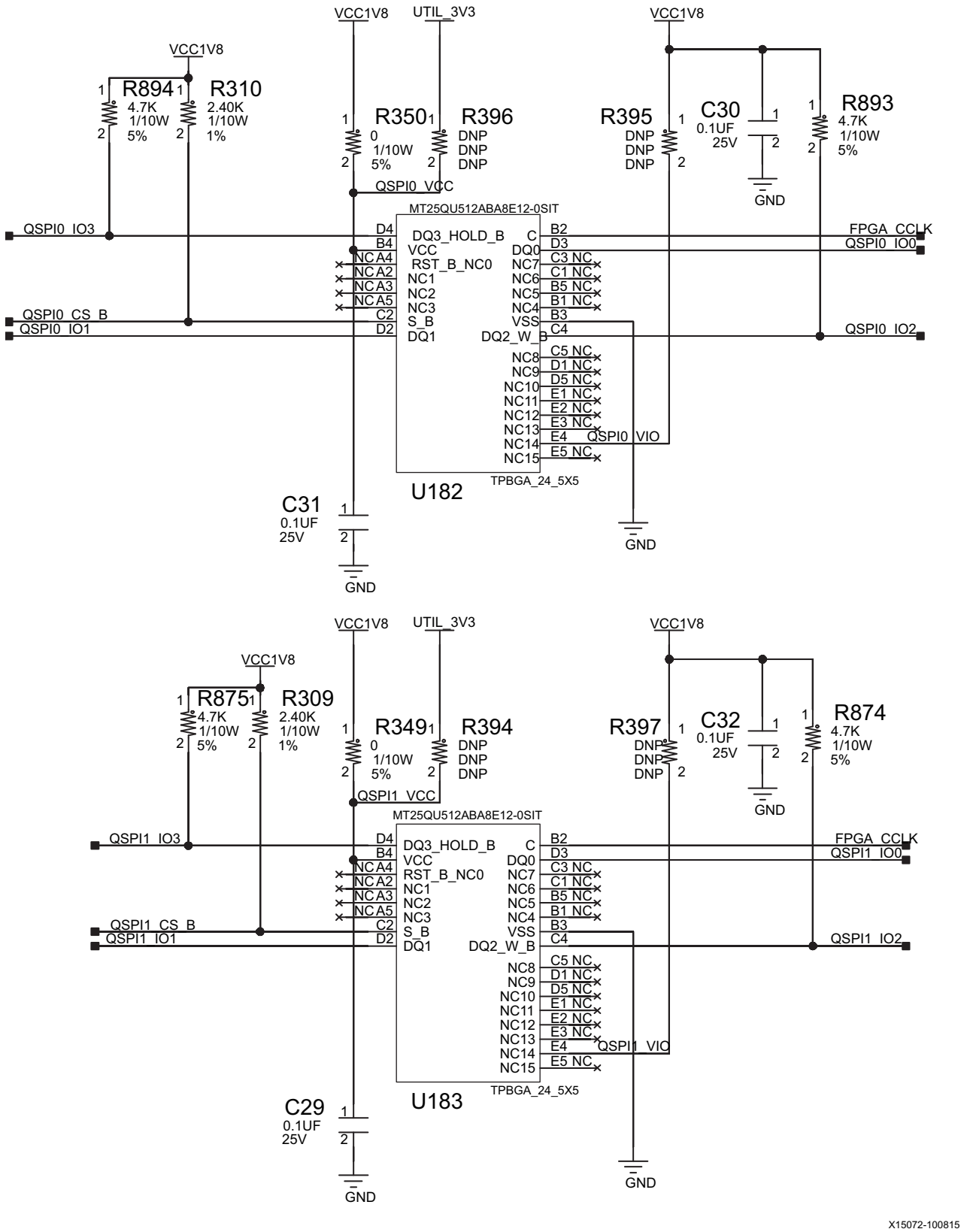

Figure 1-6: **Dual 512 Mb Quad-SPI Flash Memory**

The connections between the dual Quad SPI components U182, U183 and XCVU190 banks 0 and 65 are listed in Table 1-7.

Table 1-7: **Dual-QSPI Memory U182, U183 I/F to FPGA U1 Banks 0 and 65**

FPGA (U1) Pin	Schematic Net Name	I/O Standard	QSPI Memory		
			Pin Number	Pin Name	Reference Designator
AM14	QSPI0_IO0	(1)	D3	DQ0	U182
AK14	QSPI0_IO1	(1)	D2	DQ1	U182
AF16	QSPI0_IO2	(1)	C4	DQ2_W_B	U182
AH14	QSPI0_IO3	(1)	D4	DQ3_HOLD_B	U182
AF14	QSPI0_CS_B	(1)	C2	S_B	U182
AB16	FPGA_CCLK	(1)	B2	C	U182
BE19	QSPI1_IO0	LVCMOS18	D3	DQ0	U183
BF19	QSPI1_IO1	LVCMOS18	D2	DQ1	U183
BD18	QSPI1_IO2	LVCMOS18	C4	DQ2_W_B	U183
BE18	QSPI1_IO3	LVCMOS18	D4	DQ3_HOLD_B	U183
AP20	QSPI1_CS_B	LVCMOS18	C2	S_B	U183
AB16	FPGA_CCLK	(1)	B2	C	U183

Notes:

1. Bank 0 V_{CCO} = 1.8V; Bank 0 I/O standards are not specified.

Hybrid Memory Cube

[Figure 1-2, callout 7]

The HMC component memory system is comprised of one 16-lane 2 GB device (Micron MT43A4G40200NFA) located at U160. This memory system is connected to the XCVU190 MGTH banks 225-232 (8 MGTH Quads).