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VC709 Evaluation Board for the Virtex-7 FPGA

User Guide

UG887 (v1.5.1) August 12, 2016

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Revision History

The following table shows the revision history for this document.

Date	Version	Revision
02/04/2013	1.0	Initial Xilinx release.
06/04/2013	1.1	Changed XC7VX690T-2FFG1761CES to XC7VX690T-2FFG1761C throughout the document. Changed SiT9122 to SiT9102. The data rate in Linear BPI Flash Memory, page 22 changed from 40 MHz to 80 MHz. Added items 28 and 29 to the board photograph in Figure 1-2. FPGA EMCC clock information was added to Table 1-7, Table 1-8, Figure 1-13, and FPGA EMCC Clock, page 34. In Table 1-18, the DS1 description for RED changed. Replaced Figure 1-22 *Configuration Mode and Upper Linear Flash Address Switch*. Enhanced section Switches, page 52. Updated part ordering information in FMC_VADJ Voltage, page 62. Updated Figure 1-29 *VC709 Board Configuration Circuit*. Replaced Appendix C, *Master UCF Listing* with Master Constraints File Listing. Updated References, page 97.
01/07/2014	1.2	Revised the content of Table 1-16, page 46. Revised Table 1-20 to correct connection of FMC1_HPC_LA29_N, page 58 to FPGA pin T30 (Was W30). Revised all links and references in Appendix F, Additional Resources and revised links to web pages and documents throughout document to conform to latest linking style convention. Added caution note about power connections to J18 on the VC709 board on page 98. Revised link under Declaration of Conformity in Appendix G to point directly at the Certificate PDF instead of XTP251, the list of Certificates of Conformity.
03/11/2014	1.2.1	Tech Pubs edit. Technical content not affected.

Date	Version	Revision
04/30/2014	1.3	Revised the data rate for the small outline dual-inline memory modules (SODIMMs) in VC709 Board Features and Dual DDR3 Memory SODIMMs.
12/04/2014	1.4	Added MT28GU01GAAA1EGC-0SIT part number for the BPI parallel NOR flash memory component to Table 1-1, Linear BPI Flash Memory, and References. Added a note to Table 1-1. Updated User SMA Clock (USER_SMA_CLOCK_P and USER_SMA_CLOCK_N), Jitter-Attenuated Clock, I2C Bus, and Power Management. Updated part number in Figure 1-4. Updated Figure 1-11 to correct net names. Added I/O standard information to Table 1-4, Table 1-5, Table 1-6, Table 1-8, Table 1-14, Table 1-19, and Table 1-20. Added PCIe® edge connector information after Table 1-12. Updated description for XADC_GPIO_3, 2, 1, 0 in Table 1-25. Updated Table A-3 and added Figure A-3. Updated VC709 Board XDC Listing. Updated References.
09/02/2015	1.4.1	Made typographical edits.
03/18/2016	1.5	Updated Figure 1-16. Added thickness information in Appendix E, Board Specifications.
08/12/2016	1.5.1	Made a typographical edit.

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Chapter 1

VC709 Evaluation Board Features

Overview

The VC709 evaluation board for the Virtex®-7 FPGA provides a hardware environment for developing and evaluating designs targeting the Virtex-7 XC7VX690T-2FFG1761C FPGA. The VC709 board provides features common to many embedded processing systems, including dual DDR3 small outline dual-inline memory module (SODIMM) memories, an 8-lane PCI Express® interface, general purpose I/O, and a UART interface. Other features can be added by using mezzanine cards attached to the VITA-57 FPGA mezzanine connector (FMC) provided on the board. A high pin count (HPC) FMC is provided. See VC709 Board Features for a complete list of features. The details for each feature are described in Feature Descriptions, page 10.

Additional Information

See Appendix F, Additional Resources for references to documents, files, and resources relevant to the VC709 board.

VC709 Board Features

- Virtex-7 XC7VX690T-2FFG1761C FPGA
- 2X 4 GB 1600MTs DDR3 memory SODIMMs
- 128 MB linear byte-wide peripheral interface (BPI) flash memory
- USB JTAG through Digilent module
- Clock generation
  - Fixed 200 MHz LVDS oscillator
  - Fixed 233.33 MHz LVDS oscillator
  - I^2C programmable LVDS oscillator
  - SMA connectors
  - SMA connectors for GTH transceiver clocking
- GTH transceivers
  - FMC HPC connector (ten transceivers)
  - SMA connectors (one pair for MGT_REFCLK)
  - PCI Express (eight lanes)
  - 4 X Small form-factor pluggable plus (SFP+) connectors
- PCI Express endpoint connectivity
  - Gen1 8-lane (x8)

  - Gen2 8-lane (x8)
  - Gen3 8-lane (x8)
- 4 X SFP+ connectors
- USB-to-UART bridge
- I^2C bus
  - I^2C MUX
  - I^2C EEPROM (1 KB)
  - USER I^2C programmable LVDS oscillator
  - 2 X DDR3 SODIMM socket
  - FMC HPC connector
  - 4 X SFP+ connector
  - I^2C programmable jitter-attenuating precision clock multiplier
- Status LEDs
  - 12VDC power on
  - TI controlled power good
  - Linear power good
  - FPGA INIT
  - FPGA DONE
- User I/O
  - User LEDs (eight GPIO)
  - User pushbuttons (five directional)
  - CPU reset pushbutton
  - User DIP switch (8-pole GPIO)
- Switches
  - Power on/off slide switch
  - FPGA_PROG_B pushbutton
  - Configuration mode DIP switch
- VITA 57.1 FMC HPC connector
- Power management
  - PMBus voltage and current monitoring through TI power controllers
- XADC header
- Configuration options
  - Linear BPI flash memory
  - USB JTAG (Digilent) configuration port

The VC709 board block diagram is shown in Figure 1-1.

Caution! The VC709 board can be damaged by electrostatic discharge (ESD). Follow standard ESD prevention measures when handling the board.

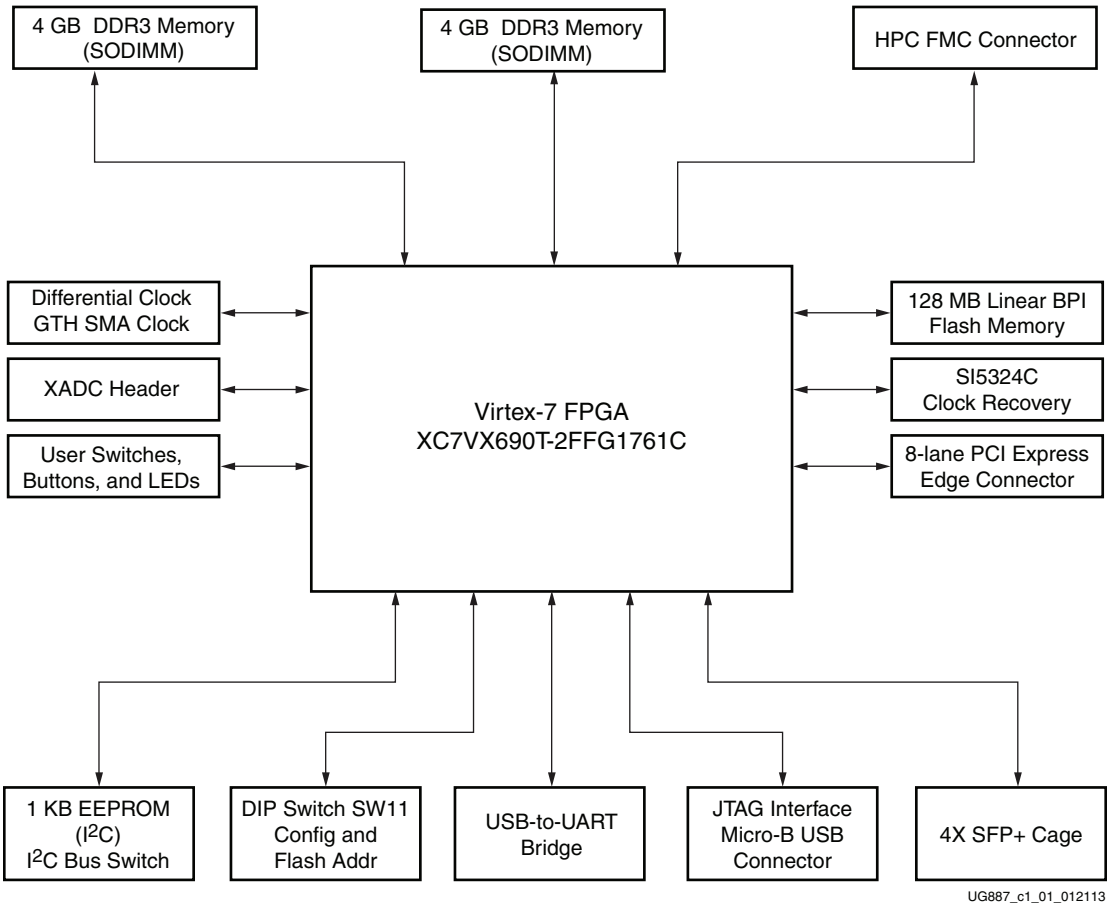

Figure 1-1: **VC709 Board Block Diagram**

Feature Descriptions

Figure 1-2 shows the VC709 board. Each numbered feature that is referenced in Figure 1-2 is described in Table 1-1 and following sections.

Note: The image in Figure 1-2 is for reference only and might not reflect the current revision of the board.

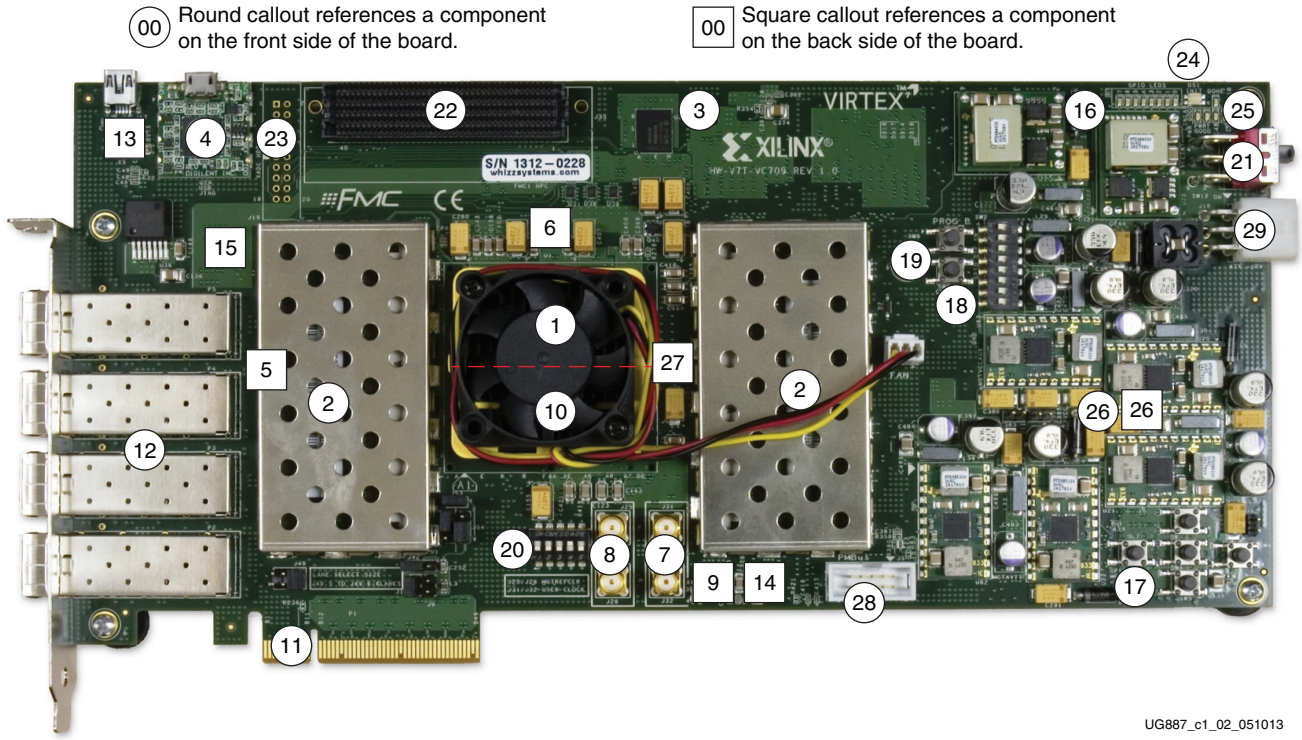

Figure 1-2: **VC709 Board Component Locations**

Table 1-1: **VC709 Board Component Descriptions**

Callout	Reference Designator	Component Description	Notes	Schematic 0381499 Page Number
1	U1	Virtex-7 FPGAXC7VX690T-2FFG1761C with cooling fan	XC7VX690T-2FFG1761C	
2	J1, J3	Two DDR3 SODIMM memories (4 GB each)	Micron MT8KTF51264HZ-1G9E1	10, 14
3	U3	BPI parallel NOR flash memory (1 Gb)	Micron PC28F00AG18FE/ MT28GU01GAAA1EGC-0SIT	24
4	U26	USB JTAG interface (micro-B USB connector)	Digilent USB JTAG module	5
5	U51	System clock, 200 MHz, LVDS (back side of board)	SiTime SIT9102-243N25E200.0000	3
6	U34	I^2C programmable user clock LVDS, 156.250 MHz default frequency (back side of board)	Silicon Labs SI570BAB0000544DG (I^2C 0x5D)	3

Table 1-1: **VC709 Board Component Descriptions *(Cont'd)***

Callout	Reference Designator	Component Description	Notes	Schematic 0381499 Page Number
7	J31, J32	User SMA clock	Rosenberger 32K10K-400L5	3
8	J25, J26	GTH transceiver SMA reference clock	Rosenberger 32K10K-400L5	30
9	U24	Jitter-attenuated clock (back side of board)	Silicon Labs SI5324C-C-GM	4
10	U1	GTH transceiver Quad 111–Quad 119	Embedded within FPGA U1	30, 36–38
11	P1	PCI Express connector	8-lane card edge connector	35
12	P2–P5	4 X SFP/SFP+ module connector (I^2C 0x50)	Molex 74441-0010	31–35
13	U44, J17	USB-to-UART bridge with mini-B USB connector	Silicon Labs CP2103GM	6
14	U52	I^2C bus switch (I^2C 0x74) (back side of board)	TI PCA9548ARGER	29
15	U14	I^2C bus switch (I^2C 0x75) (back side of board)	TI PCA9546ARGVR	29
16	DS2–DS9	User LEDs, Green	Lumex SML-LX0603GW	25
17	SW3–SW7	User pushbuttons, active-High	E-Switch TL3301EP100QG	25
18	SW2	User DIP switch, active-High	8-pole C and K SDA08H1SBD	25
19	SW8, SW9	CPU RESET, FPGA PROG pushbuttons	E-Switch TL3301EP100QG	25, 7
20	SW11	Configuration mode/upper linear flash address DIP switch	5-pole C and K SDA05H1IBD	7
21	SW12	Power on/off slide switch	C and K 1201M2S3AQE2	46
22	J35	FMC HPC connector	Samtec ASP_134486_01	18–21
23	J19	Xilinx XADC header	2 x 10 0.1-inch male header	27
24	DS1	INIT LED, dual color Red/Green	Avago HSMF-C155	38
25	DS10, DS14, DS16–DS18	Power ON and Power GOOD LEDs	Lumex SML-LX0603GW	38
26	Various	Power management system (front and back side of board)	TI UCD9248PFC in conjunction with various regulators	45–56
27	U13	Memory clock, 233.33 MHz, LVDS (back side of board)	SiTime SIT9122AC-2D3-25E233.333333	3
28	J35	2 x 5 shrouded PMBus connector	Assman HW10G-0202	46
29	J18	12V power input 2 x 3 connector	Molex 39-30-1060	46

Notes:

1. Jumper header locations are identified in Appendix A, Default Switch and Jumper Settings.

Virtex-7 XC7VX690T-2FFG1761C FPGA

[Figure 1-2, callout 1]

The VC709 board is populated with the Virtex-7 XC7VX690T-2FFG1761C FPGA.

For further information on Virtex-7 FPGAs, see *7 Series FPGAs Overview* (DS180) [Ref 1].

FPGA Configuration

The VC709 board supports two of the five 7 series FPGA configuration modes:

- Master BPI using the onboard linear BPI flash memory
- JTAG using a type-A to micro-B USB cable for connecting the host PC to the VC709 board configuration port

Each configuration interface corresponds to one or more configuration modes and bus widths as listed in Table 1-2. The mode switches M2, M1, and M0 are on SW11 positions 3, 4, and 5 respectively as shown in Figure 1-3.

Note: To determine the FPGA type resident on the VC709 board, see the Virtex-7 VC709 Evaluation Kit Master Answer Record (AR 51901).

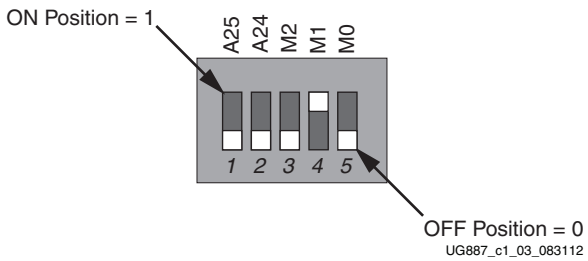

Figure 1-3: **SW11 Default Settings**

The default mode setting is M[2:0] = 010, which selects Master BPI at board power-on. See Configuration Options, page 66 for detailed information about the mode switch SW11.

Table 1-2: **VC709 Board FPGA Configuration Modes**

Configuration Mode	SW13 DIP Switch Settings (M[2:0])	Bus Width	CCLK Direction
Master BPI	010	x8, x16	Output
JTAG	101	x1	Not applicable

For full details on configuring the FPGA, see *7 Series FPGAs Configuration User Guide* (UG470) [Ref 2].

I/O Voltage Rails

There are 17 I/O banks available on the Virtex-7 device. Fourteen I/O banks are available on the VC709 board, and banks 12, 16, and 18 are not used. The voltages applied to the FPGA I/O banks used by the VC709 board are listed in Table 1-3.

Table 1-3: **I/O Voltage Rails**

FPGA (U1) Bank	Power Supply Rail Net Name	Voltage
Bank 0	VCC1V8_FPGA	1.8V
Bank 12	NOT USED	1.8V
Bank 13	VCC1V8_FPGA	1.8V
Bank 14	VCC1V8_FPGA	1.8V
Bank 15	VCC1V8_FPGA	1.8V
Bank 16	NOT USED	1.8V
Bank 17	VCC1V8_FPGA	1.8V
Bank 18	NOT USED	1.8V
Bank 19	VCC1V8_FPGA	1.8V
Bank 31	VCC1V5_FPGA	1.5V
Bank 32	VCC1V5_FPGA	1.5V
Bank 33	VCC1V5_FPGA	1.5V
Bank 34	VCC1V8_FPGA	1.8V
Bank 35	VADJ_FPGA	1.8V
Bank 36	FMC1_VIO_B_M2C	Variable
Bank 37	VCC1V5_FPGA	1.5V
Bank 38	VCC1V5_FPGA	1.5V
Bank 39	VCC1V5_FPGA	1.5V

Dual DDR3 Memory SODIMMs

[Figure 1-2, callout 2]

The memory modules at J1 and J3 are 4 GB DDR3 small outline dual-inline memory modules (SODIMMs), providing volatile synchronous dynamic random access memory (SDRAM) for storing user code and data.

- Part number: MT8KTF51264HZ-1G9E1 (Micron Technology)
- Supply voltage: 1.5V
- Datapath width: 64 bits
- Data rate: Up to 1600 MT/s

Each DDR3 interface is implemented across three I/O banks: 37, 38, and 39 for J1 and 31, 32 and 33 for J3. Each bank is a 1.5V high-performance bank having a dedicated DCI VRP/N resistor connection. An external 0.75V reference V_{TTREF} is provided for data interface banks 37, 39, 31, and 33. Any interface connected to these banks that requires a reference voltage must use this FPGA voltage reference. The connections between the DDR3 memory SODIMM sockets and the FPGA are listed in Table 1-4 and Table 1-5.

Table 1-4: **DDR3 SODIMM Socket J1 Connections to the FPGA**

XCVX690T (U1) Pin	Net Name	I/O Standard	DDR3 SODIMM Memory J1	
			Pin Number	Pin Number
A20	DDR3_A_A0	SSTL15	98	A0
B19	DDR3_A_A1	SSTL15	97	A1
C20	DDR3_A_A2	SSTL15	96	A2
A19	DDR3_A_A3	SSTL15	95	A3
A17	DDR3_A_A4	SSTL15	92	A4
A16	DDR3_A_A5	SSTL15	91	A5
D20	DDR3_A_A6	SSTL15	90	A6
C18	DDR3_A_A7	SSTL15	86	A7
D17	DDR3_A_A8	SSTL15	89	A8
C19	DDR3_A_A9	SSTL15	85	A9
B21	DDR3_A_A10	SSTL15	107	A10/AP
B17	DDR3_A_A11	SSTL15	84	A11
A15	DDR3_A_A12	SSTL15	83	A12_BC_N
A21	DDR3_A_A13	SSTL15	119	A13
F17	DDR3_A_A14	SSTL15	80	A14
E17	DDR3_A_A15	SSTL15	78	A15
D21	DDR3_A_BA0	SSTL15	109	BA0
C21	DDR3_A_BA1	SSTL15	108	BA1
D18	DDR3_A_BA2	SSTL15	79	BA2
N14	DDR3_A_D0	SSTL15	5	DQ0

Table 1-4: **DDR3 SODIMM Socket J1 Connections to the FPGA *(Cont'd)***

XCVX690T (U1) Pin	Net Name	I/O Standard	DDR3 SODIMM Memory J1	
			Pin Number	Pin Number
N13	DDR3_A_D1	SSTL15	7	DQ1
L14	DDR3_A_D2	SSTL15	15	DQ2
M14	DDR3_A_D3	SSTL15	17	DQ3
M12	DDR3_A_D4	SSTL15	4	DQ4
N15	DDR3_A_D5	SSTL15	6	DQ5
M11	DDR3_A_D6	SSTL15	16	DQ6
L12	DDR3_A_D7	SSTL15	18	DQ7
K14	DDR3_A_D8	SSTL15	21	DQ8
K13	DDR3_A_D9	SSTL15	23	DQ9
H13	DDR3_A_D10	SSTL15	33	DQ10
J13	DDR3_A_D11	SSTL15	35	DQ11
L16	DDR3_A_D12	SSTL15	22	DQ12
L15	DDR3_A_D13	SSTL15	24	DQ13
H14	DDR3_A_D14	SSTL15	34	DQ14
J15	DDR3_A_D15	SSTL15	36	DQ15
E15	DDR3_A_D16	SSTL15	39	DQ16
E13	DDR3_A_D17	SSTL15	41	DQ17
F15	DDR3_A_D18	SSTL15	51	DQ18
E14	DDR3_A_D19	SSTL15	53	DQ19
G13	DDR3_A_D20	SSTL15	40	DQ20
G12	DDR3_A_D21	SSTL15	42	DQ21
F14	DDR3_A_D22	SSTL15	50	DQ22
G14	DDR3_A_D23	SSTL15	52	DQ23
B14	DDR3_A_D24	SSTL15	57	DQ24
C13	DDR3_A_D25	SSTL15	59	DQ25
B16	DDR3_A_D26	SSTL15	67	DQ26
D15	DDR3_A_D27	SSTL15	69	DQ27
D13	DDR3_A_D28	SSTL15	56	DQ28
E12	DDR3_A_D29	SSTL15	58	DQ29
C16	DDR3_A_D30	SSTL15	68	DQ30
D16	DDR3_A_D31	SSTL15	70	DQ31
A24	DDR3_A_D32	SSTL15	129	DQ32

Table 1-4: **DDR3 SODIMM Socket J1 Connections to the FPGA *(Cont'd)***

XCVX690T (U1) Pin	Net Name	I/O Standard	DDR3 SODIMM Memory J1	
			Pin Number	Pin Number
B23	DDR3_A_D33	SSTL15	131	DQ33
B27	DDR3_A_D34	SSTL15	141	DQ34
B26	DDR3_A_D35	SSTL15	143	DQ35
A22	DDR3_A_D36	SSTL15	130	DQ36
B22	DDR3_A_D37	SSTL15	132	DQ37
A25	DDR3_A_D38	SSTL15	140	DQ38
C24	DDR3_A_D39	SSTL15	142	DQ39
E24	DDR3_A_D40	SSTL15	147	DQ40
D23	DDR3_A_D41	SSTL15	149	DQ41
D26	DDR3_A_D42	SSTL15	157	DQ42
C25	DDR3_A_D43	SSTL15	159	DQ43
E23	DDR3_A_D44	SSTL15	146	DQ44
D22	DDR3_A_D45	SSTL15	148	DQ45
F22	DDR3_A_D46	SSTL15	158	DQ46
E22	DDR3_A_D47	SSTL15	160	DQ47
A30	DDR3_A_D48	SSTL15	163	DQ48
D27	DDR3_A_D49	SSTL15	165	DQ49
A29	DDR3_A_D50	SSTL15	175	DQ50
C28	DDR3_A_D51	SSTL15	177	DQ51
D28	DDR3_A_D52	SSTL15	164	DQ52
B31	DDR3_A_D53	SSTL15	166	DQ53
A31	DDR3_A_D54	SSTL15	174	DQ54
A32	DDR3_A_D55	SSTL15	176	DQ55
E30	DDR3_A_D56	SSTL15	181	DQ56
F29	DDR3_A_D57	SSTL15	183	DQ57
F30	DDR3_A_D58	SSTL15	191	DQ58
F27	DDR3_A_D59	SSTL15	193	DQ59
C30	DDR3_A_D60	SSTL15	180	DQ60
E29	DDR3_A_D61	SSTL15	182	DQ61
F26	DDR3_A_D62	SSTL15	192	DQ62
D30	DDR3_A_D63	SSTL15	194	DQ63
M13	DDR3_A_DM0	SSTL15	11	DM0

Table 1-4: **DDR3 SODIMM Socket J1 Connections to the FPGA *(Cont'd)***

XCVX690T (U1) Pin	Net Name	I/O Standard	DDR3 SODIMM Memory J1	
			Pin Number	Pin Number
K15	DDR3_A_DM1	SSTL15	28	DM1
F12	DDR3_A_DM2	SSTL15	46	DM2
A14	DDR3_A_DM3	SSTL15	63	DM3
C23	DDR3_A_DM4	SSTL15	136	DM4
D25	DDR3_A_DM5	SSTL15	153	DM5
C31	DDR3_A_DM6	SSTL15	170	DM6
F31	DDR3_A_DM7	SSTL15	187	DM7
M16	DDR3_A_DQS0_N	DIFF_SSTL15	10	DQS0_N
N16	DDR3_A_DQS0_P	DIFF_SSTL15	12	DQS0_P
J12	DDR3_A_DQS1_N	DIFF_SSTL15	27	DQS1_N
K12	DDR3_A_DQS1_P	DIFF_SSTL15	29	DQS1_P
G16	DDR3_A_DQS2_N	DIFF_SSTL15	45	DQS2_N
H16	DDR3_A_DQS2_P	DIFF_SSTL15	47	DQS2_P
C14	DDR3_A_DQS3_N	DIFF_SSTL15	62	DQS3_N
C15	DDR3_A_DQS3_P	DIFF_SSTL15	64	DQS3_P
A27	DDR3_A_DQS4_N	DIFF_SSTL15	135	DQS4_N
A26	DDR3_A_DQS4_P	DIFF_SSTL15	137	DQS4_P
E25	DDR3_A_DQS5_N	DIFF_SSTL15	152	DQS5_N
F25	DDR3_A_DQS5_P	DIFF_SSTL15	154	DQS5_P
B29	DDR3_A_DQS6_N	DIFF_SSTL15	169	DQS6_N
B28	DDR3_A_DQS6_P	DIFF_SSTL15	171	DQS6_P
E28	DDR3_A_DQS7_N	DIFF_SSTL15	186	DQS7_N
E27	DDR3_A_DQS7_P	DIFF_SSTL15	188	DQS7_P
E18	DDR3_A_CLK0_N	DIFF_SSTL15	103	CK0_N
E19	DDR3_A_CLK0_P	DIFF_SSTL15	101	CK0_P
F19	DDR3_A_CLK1_N	DIFF_SSTL15	104	CK1_N
G19	DDR3_A_CLK1_P	DIFF_SSTL15	102	CK1_P
K19	DDR3_A_CKE0	SSTL15	73	CKE0
J18	DDR3_A_CKE1	SSTL15	74	CKE1
E20	DDR3_A_RAS_B	SSTL15	110	RAS_B
F20	DDR3_A_WE_B	SSTL15	113	WE_B
K17	DDR3_A_CAS_B	SSTL15	115	CAS_B

Table 1-4: **DDR3 SODIMM Socket J1 Connections to the FPGA *(Cont'd)***

XCVX690T (U1) Pin	Net Name	I/O Standard	DDR3 SODIMM Memory J1	
			Pin Number	Pin Number
H20	DDR3_A_ODT0	SSTL15	116	ODT0
H18	DDR3_A_ODT1	SSTL15	120	ODT1
J17	DDR3_A_S0_B	SSTL15	114	S0_B
J20	DDR3_A_S1_B	SSTL15	121	S1_B
P18	DDR3_A_RESET_B	SSTL15	30	RESET_B
G17	DDR3_A_TEMP_EVENT_B	SSTL15	198	EVENT_B

Table 1-5: **DDR3 SODIMM Socket J3 Connections to the FPGA**

XCVX690T (U1) Pin	Net Name	I/O Standard	DDR3 SODIMM Memory J3	
			Pin Number	Pin Name
AN19	DDR3_B_A0	SSTL15	98	A0
AR19	DDR3_B_A1	SSTL15	97	A1
AP20	DDR3_B_A2	SSTL15	96	A2
AP17	DDR3_B_A3	SSTL15	95	A3
AP18	DDR3_B_A4	SSTL15	92	A4
AJ18	DDR3_B_A5	SSTL15	91	A5
AN16	DDR3_B_A6	SSTL15	90	A6
AM16	DDR3_B_A7	SSTL15	86	A7
AK18	DDR3_B_A8	SSTL15	89	A8
AK19	DDR3_B_A9	SSTL15	85	A9
AM17	DDR3_B_A10	SSTL15	107	A10/AP
AM18	DDR3_B_A11	SSTL15	84	A11
AL17	DDR3_B_A12	SSTL15	83	A12_BC_N
AK17	DDR3_B_A13	SSTL15	119	A13
AM19	DDR3_B_A14	SSTL15	80	A14
AL19	DDR3_B_A15	SSTL15	78	A15
AR17	DDR3_B_BA0	SSTL15	109	BA0
AR18	DDR3_B_BA1	SSTL15	108	BA1
AN18	DDR3_B_BA2	SSTL15	79	BA2
AN24	DDR3_B_D0	SSTL15	5	DQ0
AM24	DDR3_B_D1	SSTL15	7	DQ1
AR22	DDR3_B_D2	SSTL15	15	DQ2

Table 1-5: **DDR3 SODIMM Socket J3 Connections to the FPGA *(Cont'd)***

XCVX690T (U1) Pin	Net Name	I/O Standard	DDR3 SODIMM Memory J3	
			Pin Number	Pin Name
AR23	DDR3_B_D3	SSTL15	17	DQ3
AN23	DDR3_B_D4	SSTL15	4	DQ4
AM23	DDR3_B_D5	SSTL15	6	DQ5
AN21	DDR3_B_D6	SSTL15	16	DQ6
AP21	DDR3_B_D7	SSTL15	18	DQ7
AK23	DDR3_B_D8	SSTL15	21	DQ8
AJ23	DDR3_B_D9	SSTL15	23	DQ9
AL21	DDR3_B_D10	SSTL15	33	DQ10
AM21	DDR3_B_D11	SSTL15	35	DQ11
AJ21	DDR3_B_D12	SSTL15	22	DQ12
AJ20	DDR3_B_D13	SSTL15	24	DQ13
AK20	DDR3_B_D14	SSTL15	34	DQ14
AL20	DDR3_B_D15	SSTL15	36	DQ15
AW22	DDR3_B_D16	SSTL15	39	DQ16
AW23	DDR3_B_D17	SSTL15	41	DQ17
AW21	DDR3_B_D18	SSTL15	51	DQ18
AV21	DDR3_B_D19	SSTL15	53	DQ19
AU23	DDR3_B_D20	SSTL15	40	DQ20
AV23	DDR3_B_D21	SSTL15	42	DQ21
AR24	DDR3_B_D22	SSTL15	50	DQ22
AT24	DDR3_B_D23	SSTL15	52	DQ23
BB24	DDR3_B_D24	SSTL15	57	DQ24
BA24	DDR3_B_D25	SSTL15	59	DQ25
AY23	DDR3_B_D26	SSTL15	67	DQ26
AY24	DDR3_B_D27	SSTL15	69	DQ27
AY25	DDR3_B_D28	SSTL15	56	DQ28
BA25	DDR3_B_D29	SSTL15	58	DQ29
BB21	DDR3_B_D30	SSTL15	68	DQ30
BA21	DDR3_B_D31	SSTL15	70	DQ31
AY14	DDR3_B_D32	SSTL15	129	DQ32
AW15	DDR3_B_D33	SSTL15	131	DQ33
BB14	DDR3_B_D34	SSTL15	141	DQ34

Table 1-5: **DDR3 SODIMM Socket J3 Connections to the FPGA *(Cont'd)***

XCVX690T (U1) Pin	Net Name	I/O Standard	DDR3 SODIMM Memory J3	
			Pin Number	Pin Name
BB13	DDR3_B_D35	SSTL15	143	DQ35
AW12	DDR3_B_D36	SSTL15	130	DQ36
AY13	DDR3_B_D37	SSTL15	132	DQ37
AY12	DDR3_B_D38	SSTL15	140	DQ38
BA12	DDR3_B_D39	SSTL15	142	DQ39
AU12	DDR3_B_D40	SSTL15	147	DQ40
AU13	DDR3_B_D41	SSTL15	149	DQ41
AT12	DDR3_B_D42	SSTL15	157	DQ42
AU14	DDR3_B_D43	SSTL15	159	DQ43
AV13	DDR3_B_D44	SSTL15	146	DQ44
AW13	DDR3_B_D45	SSTL15	148	DQ45
AT15	DDR3_B_D46	SSTL15	158	DQ46
AR15	DDR3_B_D47	SSTL15	160	DQ47
AL15	DDR3_B_D48	SSTL15	163	DQ48
AJ15	DDR3_B_D49	SSTL15	165	DQ49
AK14	DDR3_B_D50	SSTL15	175	DQ50
AJ12	DDR3_B_D51	SSTL15	177	DQ51
AJ16	DDR3_B_D52	SSTL15	164	DQ52
AL16	DDR3_B_D53	SSTL15	166	DQ53
AJ13	DDR3_B_D54	SSTL15	174	DQ54
AK13	DDR3_B_D55	SSTL15	176	DQ55
AR14	DDR3_B_D56	SSTL15	181	DQ56
AT14	DDR3_B_D57	SSTL15	183	DQ57
AM12	DDR3_B_D58	SSTL15	191	DQ58
AP11	DDR3_B_D59	SSTL15	193	DQ59
AM13	DDR3_B_D60	SSTL15	180	DQ60
AN13	DDR3_B_D61	SSTL15	182	DQ61
AM11	DDR3_B_D62	SSTL15	192	DQ62
AN11	DDR3_B_D63	SSTL15	194	DQ63
AT22	DDR3_B_DM0	SSTL15	11	DM0
AL22	DDR3_B_DM1	SSTL15	28	DM1
AU24	DDR3_B_DM2	SSTL15	46	DM2

Table 1-5: **DDR3 SODIMM Socket J3 Connections to the FPGA *(Cont'd)***

XCVX690T (U1) Pin	Net Name	I/O Standard	DDR3 SODIMM Memory J3	
			Pin Number	Pin Name
BB23	DDR3_B_DM3	SSTL15	63	DM3
BB12	DDR3_B_DM4	SSTL15	136	DM4
AV15	DDR3_B_DM5	SSTL15	153	DM5
AK12	DDR3_B_DM6	SSTL15	170	DM6
AP13	DDR3_B_DM7	SSTL15	187	DM7
AP22	DDR3_B_DQS0_N	DIFF_SSTL15	10	DQS0_N
AP23	DDR3_B_DQS0_P	DIFF_SSTL15	12	DQS0_P
AK22	DDR3_B_DQS1_N	DIFF_SSTL15	27	DQS1_N
AJ22	DDR3_B_DQS1_P	DIFF_SSTL15	29	DQS1_P
AU21	DDR3_B_DQS2_N	DIFF_SSTL15	45	DQS2_N
AT21	DDR3_B_DQS2_P	DIFF_SSTL15	47	DQS2_P
BB22	DDR3_B_DQS3_N	DIFF_SSTL15	62	DQS3_N
BA22	DDR3_B_DQS3_P	DIFF_SSTL15	64	DQS3_P
BA14	DDR3_B_DQS4_N	DIFF_SSTL15	135	DQS4_N
BA15	DDR3_B_DQS4_P	DIFF_SSTL15	137	DQS4_P
AR12	DDR3_B_DQS5_N	DIFF_SSTL15	152	DQS5_N
AP12	DDR3_B_DQS5_P	DIFF_SSTL15	154	DQS5_P
AL14	DDR3_B_DQS6_N	DIFF_SSTL15	169	DQS6_N
AK15	DDR3_B_DQS6_P	DIFF_SSTL15	171	DQS6_P
AN14	DDR3_B_DQS7_N	DIFF_SSTL15	186	DQS7_N
AN15	DDR3_B_DQS7_P	DIFF_SSTL15	188	DQS7_P
AU17	DDR3_B_CLK0_N	DIFF_SSTL15	101	CK0_P
AT17	DDR3_B_CLK0_P	DIFF_SSTL15	103	CK0_N
AV18	DDR3_B_CLK1_N	DIFF_SSTL15	102	CK1_P
AU18	DDR3_B_CLK1_P	DIFF_SSTL15	104	CK1_N
AW17	DDR3_B_CKE0	SSTL15	73	CKE0
AW18	DDR3_B_CKE1	SSTL15	74	CKE1
AV19	DDR3_B_RAS_B	SSTL15	110	RAS_B
AU19	DDR3_B_WE_B	SSTL15	113	WE_B
AT20	DDR3_B_CAS_B	SSTL15	115	CAS_B
AT16	DDR3_B_ODT0	SSTL15	116	ODT0
AW16	DDR3_B_ODT1	SSTL15	120	ODT1

Table 1-5: **DDR3 SODIMM Socket J3 Connections to the FPGA *(Cont'd)***

XCVX690T (U1) Pin	Net Name	I/O Standard	DDR3 SODIMM Memory J3	
			Pin Number	Pin Name
AV16	DDR3_B_S0_B	SSTL15	114	S0_B
AT19	DDR3_B_S1_B	SSTL15	121	S1_B
BB19	DDR3_B_RESET_B	SSTL15	30	RESET_B
AU16	DDR3_B_TEMP_EVENT_B	SSTL15	198	EVENT_B

The VC709 DDR3 SODIMM interfaces adhere to the constraints guidelines documented in the DDR3 Design Guidelines section of *7 Series FPGAs Memory Interface Solutions User Guide* (UG586) [Ref 3]. The VC709 DDR3 SODIMM interfaces are 40Ω impedance implementations. Other memory interface details are also available in *7 Series FPGAs Memory Interface Solutions User Guide* (UG586) [Ref 3] and *7 Series FPGAs Memory Resources User Guide* (UG473) [Ref 4].

Linear BPI Flash Memory

[Figure 1-2, callout 3]

The linear BPI flash memory located at U3 provides 128 MB of nonvolatile storage that can be used for configuration or software storage. The data, address, and control signals are connected to the FPGA. The BPI flash memory device is packaged in a 64-pin BGA.

- Part number: PC28F00AG18FE/MT28GU01GAAA1EGC-0SIT

  Note: MT28GU01GAAA1EGC-0SIT is a new Micron part, and either part might be installed on the VC709 board.
- Supply voltage: 1.8V
- Datapath width: 16 bits (26 address lines and 7 control signals)
- Data rate: Up to 80 MHz

The linear BPI flash memory can synchronously configure the FPGA in Master BPI mode at the 80 MHz data rate supported by the flash memory by using a configuration bitstream generated with BitGen options for synchronous configuration. The fastest configuration method uses the external 80 MHz oscillator connected to the FPGA EMCCLK pin.

Multiple bitstreams can be stored in the linear BPI flash. The two most significant address bits (A25, A24) of the flash memory are connected to DIP switch SW11 positions 1 and 2 respectively, and to the RS1 and RS0 pins of the FPGA. By placing valid XC7VX690T bitstreams at four different offset addresses in the flash memory, 1 of the 4 bitstreams can be selected to configure the FPGA by appropriately setting the DIP switch SW11. The connections between the BPI flash memory and the FPGA are listed in Table 1-6.

Table 1-6: **BPI Flash Memory Connections to the FPGA**

FPGA (U1) Pin	Net Name	I/O Standard	BPI Flash Memory (U3)	
			Pin Number	Pin Name
AJ28	FLASH_A0	LVCMOS18	A1	A1
AH28	FLASH_A1	LVCMOS18	B1	A2
AG31	FLASH_A2	LVCMOS18	C1	A3
AF30	FLASH_A3	LVCMOS18	D1	A4
AK29	FLASH_A4	LVCMOS18	D2	A5
AK28	FLASH_A5	LVCMOS18	A2	A6
AG29	FLASH_A6	LVCMOS18	C2	A7
AK30	FLASH_A7	LVCMOS18	A3	A8
AJ30	FLASH_A8	LVCMOS18	B3	A9
AH30	FLASH_A9	LVCMOS18	C3	A10
AH29	FLASH_A10	LVCMOS18	D3	A11
AL30	FLASH_A11	LVCMOS18	C4	A12
AL29	FLASH_A12	LVCMOS18	A5	A13
AN33	FLASH_A13	LVCMOS18	B5	A14
AM33	FLASH_A14	LVCMOS18	C5	A15
AM32	FLASH_A15	LVCMOS18	D7	A16
AV41	FLASH_A16	LVCMOS18	D8	A17
AU41	FLASH_A17	LVCMOS18	A7	A18
BA42	FLASH_A18	LVCMOS18	B7	A19
AU42	FLASH_A19	LVCMOS18	C7	A20
AT41	FLASH_A20	LVCMOS18	C8	A21
BA40	FLASH_A21	LVCMOS18	A8	A22
BA39	FLASH_A22	LVCMOS18	G1	A23
BB39	FLASH_A23	LVCMOS18	H8	A24
AW42	FLASH_A24	LVCMOS18	B6	A25
AW41	FLASH_A25	LVCMOS18	B8	A26
NA	NC	NA	H1	A27
AM36	FLASH_D0	LVCMOS18	F2	DQ0

Table 1-6: **BPI Flash Memory Connections to the FPGA *(Cont'd)***

FPGA (U1) Pin	Net Name	I/O Standard	BPI Flash Memory (U3)	
			Pin Number	Pin Name
AN36	FLASH_D1	LVCMOS18	E2	DQ1
AJ36	FLASH_D2	LVCMOS18	G3	DQ2
AJ37	FLASH_D3	LVCMOS18	E4	DQ3
AK37	FLASH_D4	LVCMOS18	E5	DQ4
AL37	FLASH_D5	LVCMOS18	G5	DQ5
AN35	FLASH_D6	LVCMOS18	G6	DQ6
AP35	FLASH_D7	LVCMOS18	H7	DQ7
AM37	FLASH_D8	LVCMOS18	E1	DQ8
AG33	FLASH_D9	LVCMOS18	E3	DQ9
AH33	FLASH_D10	LVCMOS18	F3	DQ10
AK35	FLASH_D11	LVCMOS18	F4	DQ11
AL35	FLASH_D12	LVCMOS18	F5	DQ12
AJ31	FLASH_D13	LVCMOS18	H5	DQ13
AH34	FLASH_D14	LVCMOS18	G7	DQ14
AJ35	FLASH_D15	LVCMOS18	E7	DQ15
AM34	FLASH_WAIT	LVCMOS18	F7	WAIT
BB41	FPGA_FWE_B	LVCMOS18	G8	WE_B
BA41	FLASH_OE_B	LVCMOS18	F8	OE_B
N10	FPGA_CCLK	LVCMOS18	E6	CLK
AL36	FLASH_CE_B	LVCMOS18	B4	CE_B
AY37	FLASH_ADV_B	LVCMOS18	F6	ADV_B
AG11	FPGA_INIT_B	LVCMOS18	D4	RST_B

Additional FPGA bitstreams can be stored and used for configuration by setting the Warm Boot Start Address (WBSTAR) register contained in 7 series FPGAs. More information is available in the reconfiguration and multiboot section in *7 Series FPGAs Configuration User Guide* (UG470) [Ref 2].

The configuration section of *7 Series FPGAs Configuration User Guide* (UG470) [Ref 2] provides details on the Master BPI configuration mode.

Figure 1-4 shows the linear BPI flash memory on the VC709 board. For more details, see the Micron Technology, Inc. MT28GU01GAAA1EGC data sheet.

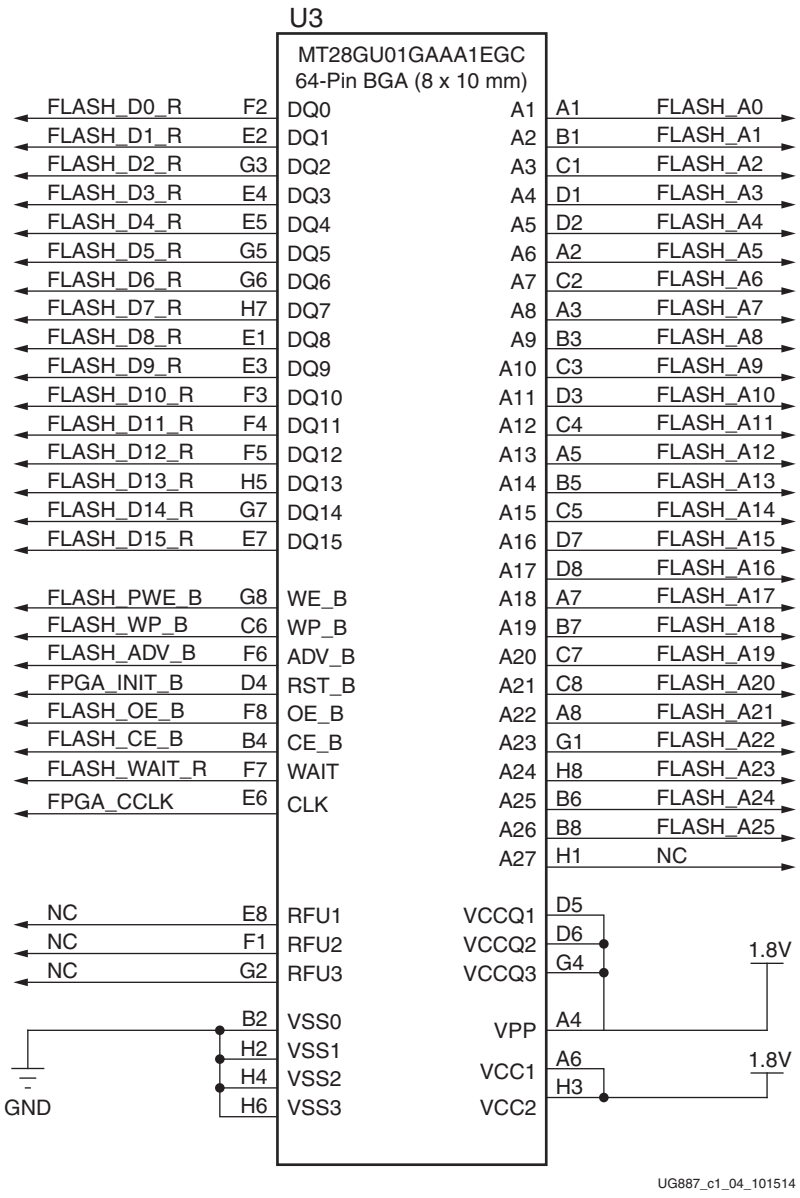

Figure 1-4: **128 MB Linear Flash Memory (U3)**