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# **Zynq-7000 All Programmable SoC ZC702 Evaluation Kit**

## ***Getting Started Guide***

UG926 (v1.2.1) September 20, 2012



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## Revision History

The following table shows the revision history for this document.

Date	Version	Revision
05/25/2012	1.0	Initial Xilinx release.
05/29/2012	1.1	Added <a href="#">Figure 4-3</a> and the text just before and after it.
06/21/12	1.2	<a href="#">Chapter 1, Introduction</a> : Added a "Reference Designs and Demonstrations" group to section <a href="#">ZC702 Evaluation Kit Contents, page 6</a> . Changed cable from Digilent USB JTAG to Digilent USB-to-JTAG. Added that the SD MMC card contains bootable configuration files for the Base TRD demo design files and Linux applications platform. Updated USB JTAG interface information and added details to the clock sources list in section <a href="#">Key Features, page 7</a> . Changed FMC1 and FMC2 connector types to LPC I/O expansion connectors. Added tables of default settings to the section <a href="#">Default Jumper and Switch Settings, page 9</a> . <a href="#">Chapter 2, Zynq-7000 All Programmable SoC ZC702 Evaluation Kit Built-In Self-Test</a> : Updated switch settings in the <a href="#">Introduction, page 13</a> . Added bring-up details through the chapter. Settings were added to section <a href="#">Run the BIST Application, page 19</a> . Added <a href="#">Chapter 3, Getting Started with the Base Targeted Reference Design</a> . Added <a href="#">Chapter 4, Evaluating the AMS101 Evaluation Card</a> . Additional references were added through the book and to <a href="#">Appendix A, Additional Resources</a> .
09/21/12	1.2.1	Updated title.

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# Introduction

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## Overview

The ZC702 Evaluation kit shown in [Figure 1-1](#) is based on the XC7Z020 CLG484-1 All Programmable SoC device. For additional information, see the Zynq™-7000 All Programmable SoC Family Product Table [\[Ref 1\]](#). (See [Appendix A](#), for references.) A built-in self-test (BIST) is provided for the ZC702 Evaluation kit. The BIST provides a convenient way to test many of the board's features on power-up. The tutorials and reference designs available on the ZC702 product page can be used to further explore the capabilities of the ZC702 board and the Zynq-7000 All Programmable SoC [\[Ref 2\]](#). For the most up-to-date information on the content provided with the ZC702 Evaluation kit, see the ZC702 product page [\[Ref 3\]](#). UG873, *Zynq-7000 Concepts, Tools, and Techniques Guide* shows the basic hardware and software flow using the ZC702 board [\[Ref 4\]](#). The Zynq-7000 All Programmable SoC documentation page is also helpful [\[Ref 5\]](#).



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Figure 1-1: ZC702 Evaluation Kit

This user guide also describes a Base Targeted Reference Design (TRD) based on Zynq-7000 All Programmable SoC architecture. The Base TRD showcases various features and

capabilities of the Zynq Z-7020 All Programmable SoC for the embedded domain in a single package. TRDs are key components of the Xilinx Targeted Design Platform (TDP) strategy. TDPs from Xilinx provide customers with basic scalable design platforms for the creation of FPGA-based solutions in a wide variety of applications and industries.

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## ZC702 Evaluation Kit Contents

The ZC702 Evaluation kit includes the following items:

- ZC702 evaluation board featuring the XC7Z020 CLG484-1
- Agile Mixed Signal (AMS) evaluation board
- Full seat ISE® Design Suite Embedded Edition design tools
  - Device-locked to the Zynq-7000 XC7Z020 CLG484-1 device
- Board design files
  - Schematics
  - Board layout files
  - Bill of materials
- Documentation
  - *Getting Started Guide* (this document)
  - Hardware user guide (UG850, *ZC702 Evaluation Board for the Zynq-7000 XC7Z020 All Programmable SoC User Guide* [Ref 6])
  - TRD user guide (UG925, *Zynq-7000 All Programmable SoC ZC702 Base Targeted Reference Design User Guide* [Ref 7])
- Reference Designs and Demonstrations
  - BIST Utility and Demonstration
  - Targeted Reference Design (TRD), demonstrating a video processing pipeline.  
**Note:** The video demonstration contains the licensed IPs with no timeout. To recompile this design, the user needs to register for an evaluation IP license for the Video IP.
  - AMS demonstration, providing an overview of the analog capabilities of the Zynq-7000 All Programmable SoC devices.
- 12V AC adapter power supply
- Cables
  - RJ-45 Ethernet cable
  - HDMI™ cable

- USB Type-A to USB Micro-B cable (Digilent USB-to-JTAG Programming Port)
- USB Type-A to USB Mini-B cable (serial UART)
- USB flash drive (contains reference design, documents, and board source files)
- Secure Digital Multimedia Card (SD MMC) (contains bootable configuration files for the Base TRD demonstration design files and Linux applications platform)

The kit contains the software and reference designs, a demonstration, and documents to help the user get started quickly.

---

## Key Features

Key features of the ZC702 evaluation board include:

- Zynq-7000 XC7Z020-1CLG484 device
- 1 GB DDR3 component memory (four 256 Mb x 8 devices)
- 128 Mb Quad SPI flash memory
- USB 2.0 ULPI (UTMI+ low pin interface) transceiver
- SD MMC connector
- USB JTAG interface through the Digilent USB-to-JTAG programming port
- Clock sources:
  - Fixed user clock—(200 MHz) LVDS oscillator (differential)
  - Programmable user clock—I2C programmable (10 MHz to 810 MHz, with a default setting of 156.250 MHz) LVDS oscillator (differential)
  - Zynq processor reference clock—Fixed (33.33 MHz) LVCMOS oscillator (single-ended)
- Ethernet PHY RGMII interface with RJ-45 connector
- 10/100/1,000 tri-speed Ethernet PHY
- USB-to-UART bridge
- HDMI codec
- I2C bus
- I2C bus multiplexed to:
  - Si570 user clock
  - ADV7511 HDMI codec
  - M24C08 EEPROM (1 KB)

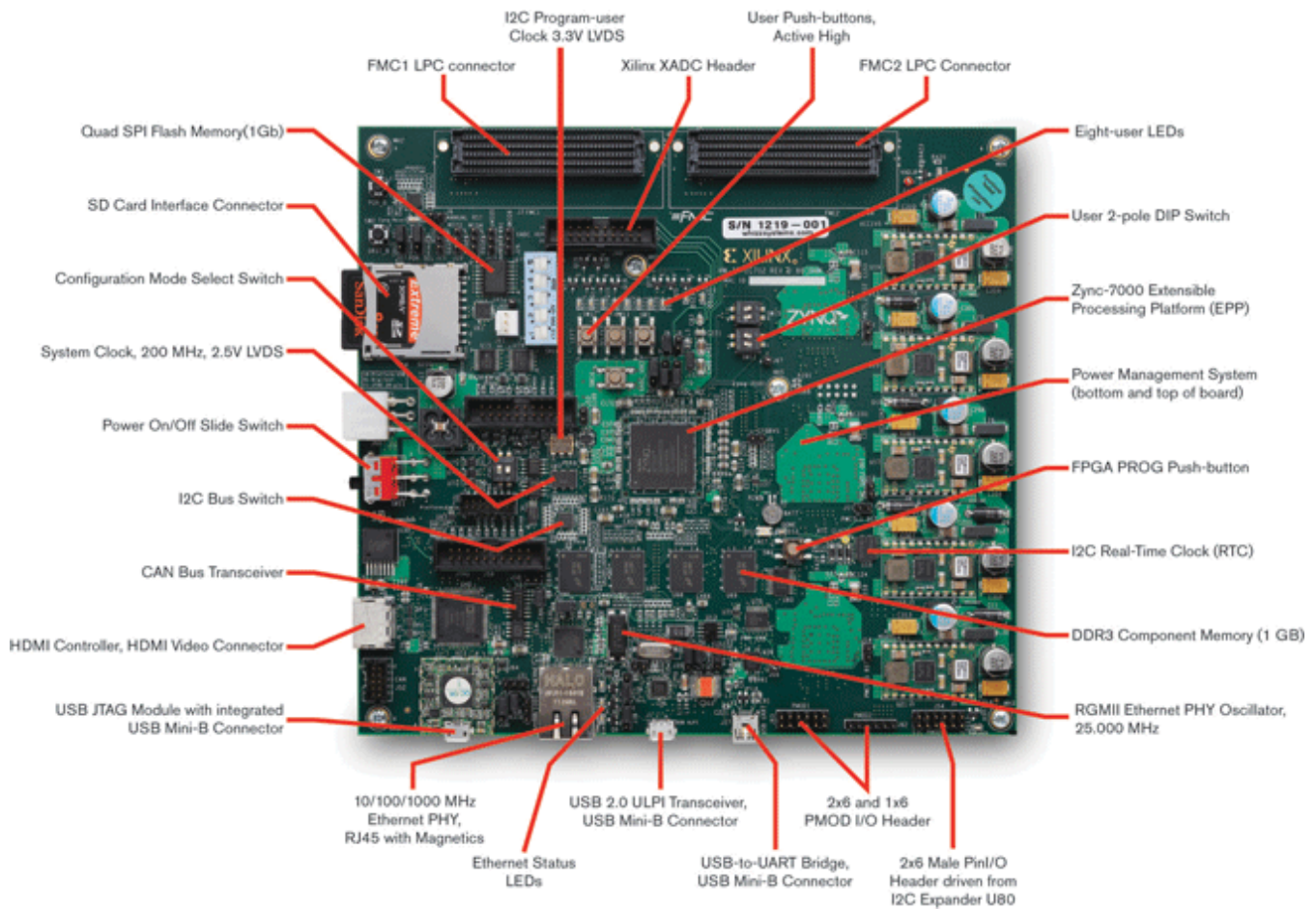


- 1-to-16 TCA6416APWR port expander
- RTC-8564JE real-time clock
- FMC1 LPC I/O expansion connector
- FMC2 LPC I/O expansion connector
- PMBUS data/clock
- Status LEDs:
  - Ethernet status
  - Power good
  - FPGA INIT
  - FPGA DONE
- User I/O:
  - Eight user LEDs
  - Two user pushbuttons
  - Two user switches (2-position DIP switches)
- CPU reset pushbutton
- Two VITA 57.1 FMC LPC connectors
- Power on/off slide switch
- Power management with PMBus voltage and current monitoring through TI power controllers
- XADC header with access to dual 12-bit 1 MSPS XADC port
- (SW1 – POR\_B) boot configuration options:
  - SD MMC Boot mode
  - Quad SPI flash memory
  - USB JTAG configuration port (Digilent module)
  - Platform cable header JTAG configuration port

For more detailed information about ZC702 board features, peripheral devices, and pinouts, see the hardware user guide UG850, *ZC702 Evaluation Board for the Zynq-7000 XC7Z020 All Programmable SoC User Guide* [Ref 6].

# Default Jumper and Switch Settings

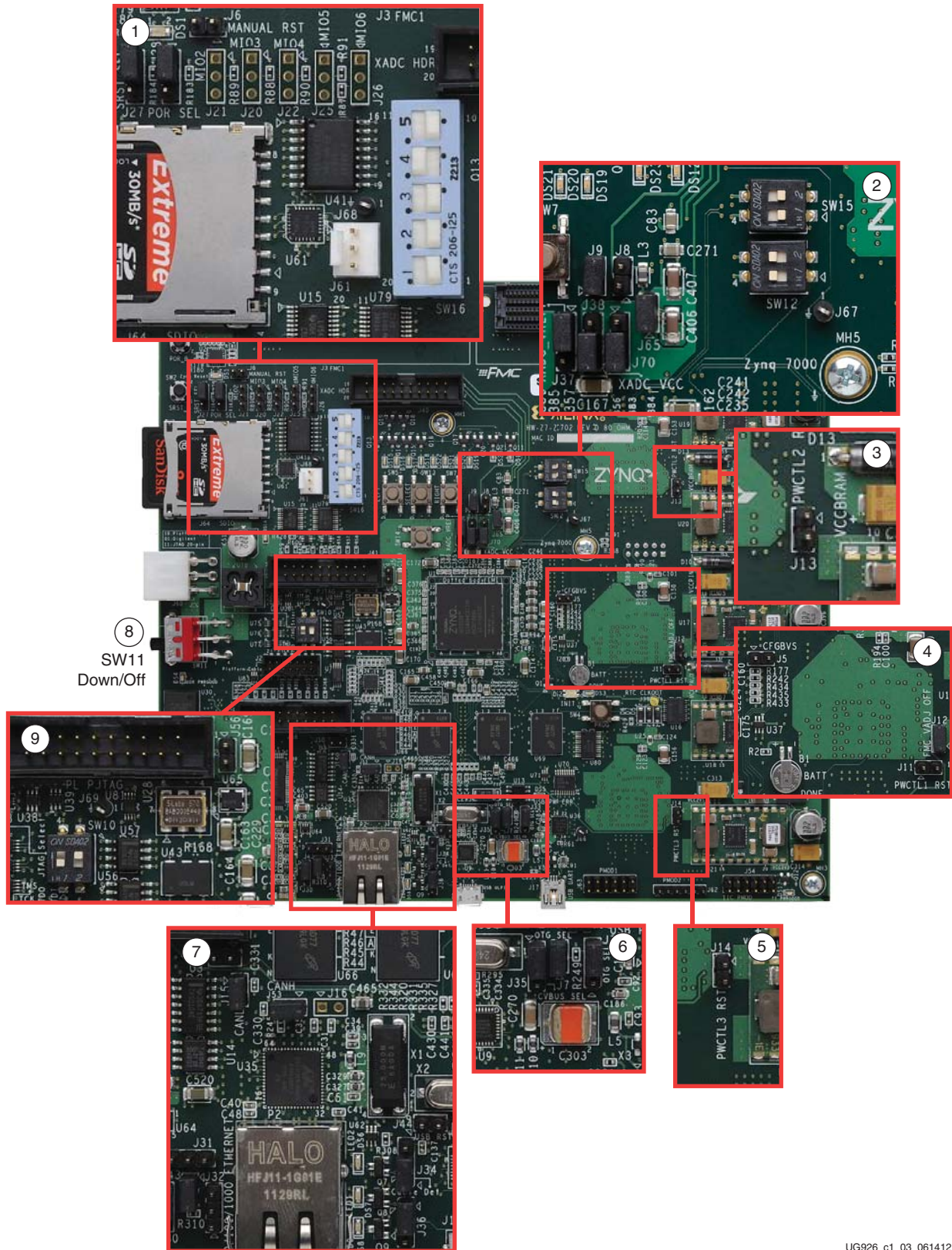
Figure 1-1 calls out the major features on the ZC702 board. See UG850, *ZC702 Evaluation Board for the Zynq-7000 XC7Z020 All Programmable SoC User Guide* [Ref 6] for more detailed information about the ZC702 board.



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Figure 1-2: Feature Callout for the ZC702 Board

Default factory settings of jumpers and switches on the ZC702 board are highlighted in Figure 1-3. Default switch and jumper settings are listed in Table 1-1 and Table 1-2.



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Figure 1-3: Default Jumper and Switch Settings on the ZC702 Board

Table 1-1: Default Switch Settings

Switch	Position	Setting	Figure 1-3 Callout
SW10 (JTAG chain input select two-position DIP switch)	1	Off	9
	2	On	
SW12 (two-position DIP switch)	1	Off	2
	2	Off	
SW15 (two-position DIP switch)	1	Off	2
	2	Off	
SW16 (five-position DIP switch)	1	Right	1
	2	Right	
	3	Right	
	4	Right	
	5	Right	
SW11 (power slide switch)		Off	8
	1	Down	

Default jumper positions are shown in Figure 1-3 and listed in Table 1-2.

Table 1-2: Default Jumper Settings

Jumper	Function	Default Position	Figure 1-3 Callout
<b>HDR_1 X 2</b>			
J5	CFGBVS short to GND	OFF	4
J6	POR Master Reset	OFF	1
J7	USB 2.0 USB_VBUS_SEL	1-2	6
J8	XADC GND L3 Bypass	OFF	2
J9	XADC GND	ON	2
J10	ARM HDR J41 pin 2 to VADJ	OFF	7
J11	UCD9248 U32 ADDR52 RESET_B	OFF	4
J12	FMC_VADJ_ON_B	ON	4
J13	UCD9248 U33 ADDR53 RESET_B	OFF	3
J14	UCD9248 U34 ADDR54 RESET_B	OFF	5
J15	CAN BUS COMMON-MODE CANH HDR	1-2	7
J43	Ethernet PHY HDR	1-2	7
J44	USB 2.0 USB_RESET_B	OFF	7
J53	CAN BUS COMMON-MODE CANL HDR	1-2	7
J56	JTAG HDR J58 pin 2 3.3V SEL	OFF	9
J65	XADC_VCC5V0 = VCC5V0	OFF	2

Table 1-2: Default Jumper Settings (Cont'd)

Jumper	Function	Default Position	Figure 1-3 Callout
<b>HDR_1 X 3</b>			
J27	PS_SRST_B	1-2	1
J28	PS_POR_B	1-2	1
J30	Ethernet PHY HDR	1-2	7
J31	Ethernet PHY HDR	NONE	7
J32	Ethernet PHY HDR	NONE	7
J33	USB 2.0 Mode	2-3	6
J34	USB 2.0 J1 ID SEL	1-2	7
J35	USB 2.0 J1 VBUS CAP SEL	1-2	6
J36	USB 2.0 J1 GND SEL	1-2	7
J37	XADC_VREP SEL	1-2	2
J38	XADC_VCC SEL	2-3	2
J70	XADC_VREF Source SEL	2-3	2

# Zynq-7000 All Programmable SoC ZC702 Evaluation Kit Built-In Self-Test

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## Introduction

The BIST tests many of the features offered by the Zynq-7000 All Programmable SoC ZC702 Evaluation kit. The test is stored in the onboard nonvolatile Quad SPI flash memory, and configures the All Programmable SoC when the mode switch SW16 is set to where SW1, 2, 3, and 5 are switched to the right and SW4 is switched to the left.

indicating QSPI configuration. This exercise of running the BIST demonstration should take approximately 10 to 15 minutes.

**Note:** For a description of all the features on the ZC702 board, see UG850, *ZC702 Evaluation Board for the Zynq-7000 XC7Z020 All Programmable SoC User Guide* [Ref 6].

---

## BIST Setup Requirements

These are the prerequisites for running the BIST demonstration.

- Hardware setup:
  - ZC702 evaluation board with XC7Z020 CLG484-1 part
    - A power adaptor and power cable for the ZC702 board
  - USB Type-A to Mini-B cable (for UART)
  - AC power adapter (12 VDC)
- Windows software and driver setup:
  - TeraTerm Pro (or similar) terminal program (might already be installed)
  - USB-UART driver from Silicon Labs [Ref 8] (might already be installed)

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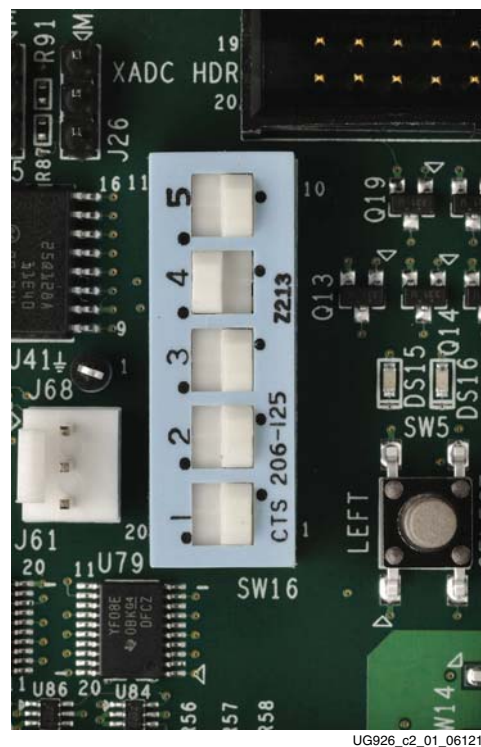
## Hardware BIST Board Setup

This section describes the hardware setup and use of the terminal program for running the BIST application. It contains step-by-step instructions for board bring-up.

### ZC702 Evaluation Board Setup

The default jumper and switch settings of the ZC702 board are shown in [Figure 1-3](#), [Table 1-1](#), and [Table 1-2](#).

1. Set the SW16 switch as shown in [Figure 2-1](#), where SW1, 2, 3, and 5 are switched to the right and SW4 is switched to the left for the BIST to boot from Quad SPI device and run the system demonstration utility.



*Figure 2-1:* Settings for the Mode Switch to Boot from Quad SPI Mode

---

## Hardware Bring-Up

This section describes the steps for hardware bring-up.

1. Be sure to have the SW16 Mode switch settings set to those shown in [Figure 2-1](#).

2. With the ZC702 board switched OFF (SW11 in the down position, as shown in [Figure 1-3](#)), plug the USB Mini-B cable into the Mini USB port J17 labeled USB UART on the ZC702 board and the other end into a open USB port on your PC (see [Figure 2-2](#)).

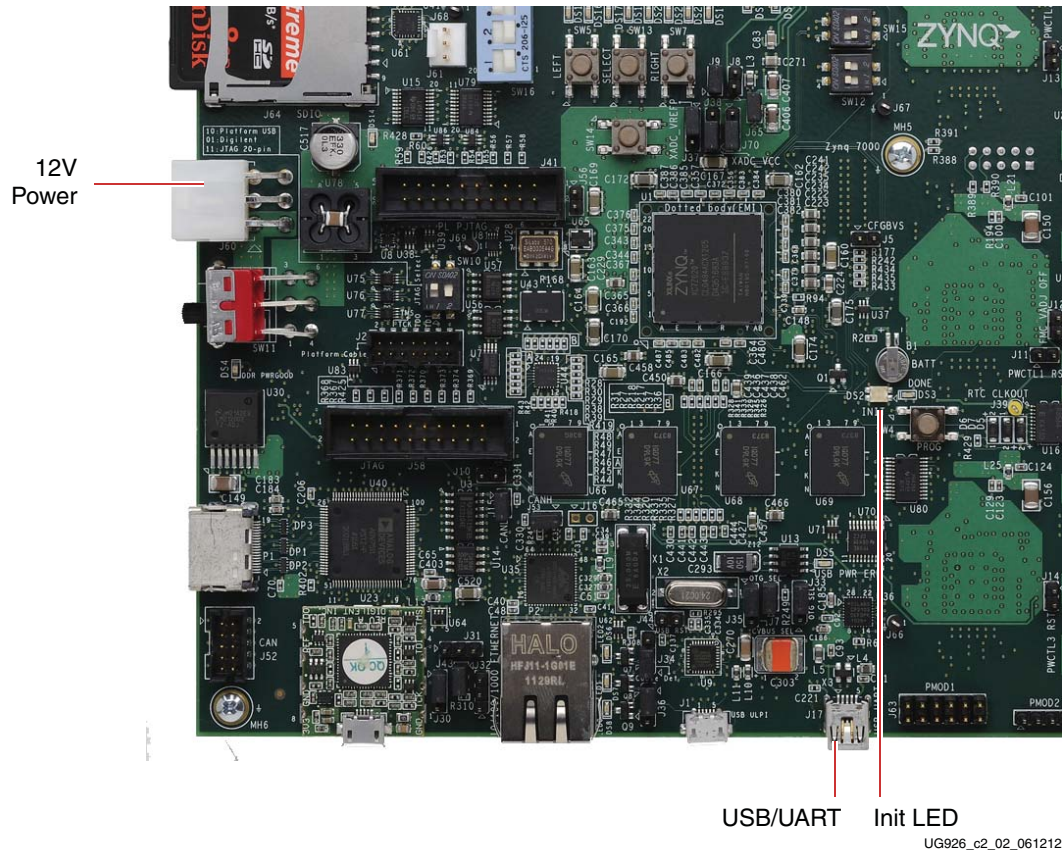


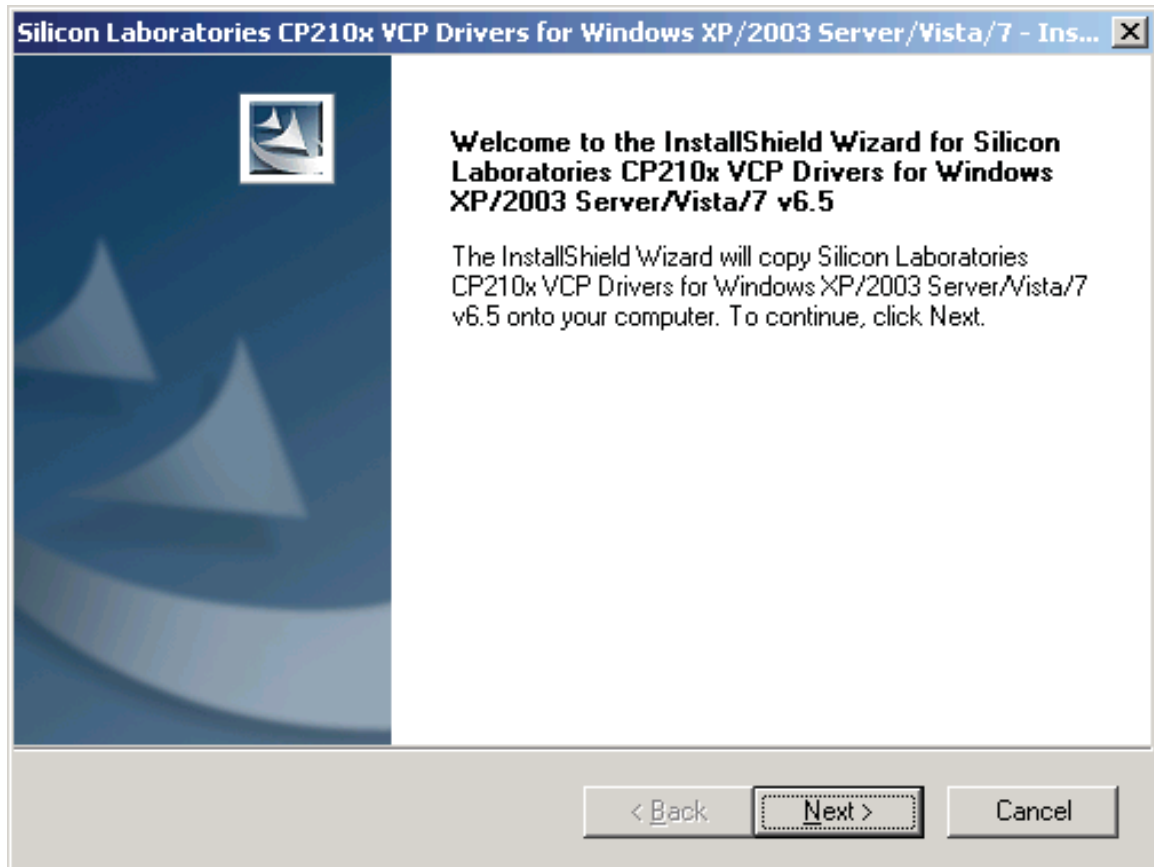
Figure 2-2: ZC702 with the UART and Power Cable Attached

3. Connect the power cable.
4. Switch the ZC702 board's power to ON (SW11 switched up as shown in [Figure 1-3](#)).

## Install the USB-UART Driver

1. Run the downloaded executable UART-USB driver file, listed in [BIST Setup Requirements, page 13](#). Running the executable file enables USB-to-UART communications with a host PC.





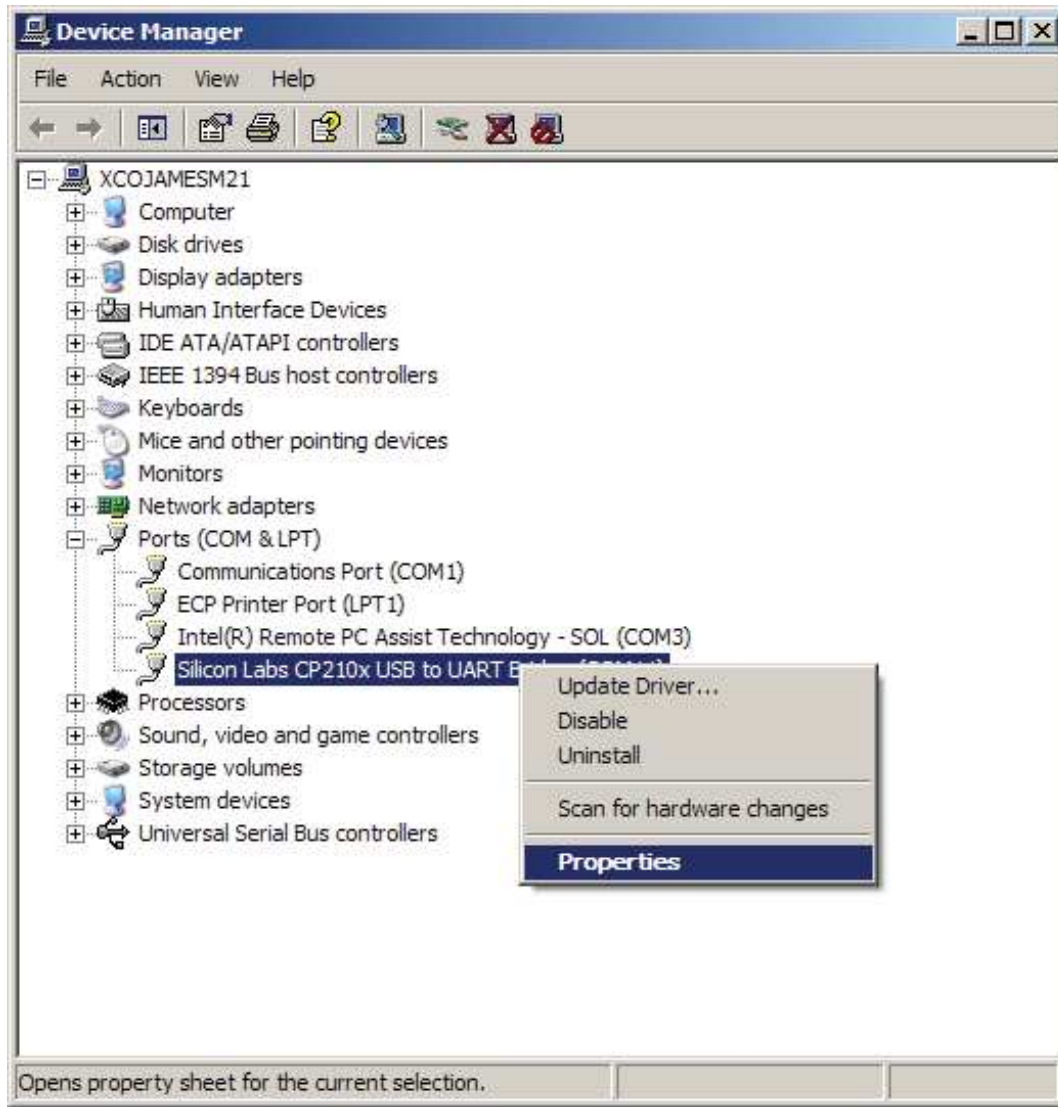
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Figure 2-3: UART Cable Driver Installation

2. Set the USB-UART connection to a known COM Port and baud rate in the Device Manager.
  - a. Right-click **My Computer** and select **Properties**.
  - b. Select **Device Manager** on the left side. (On Windows XP, select the **Hardware** tab and then the **Device Manager** button.
  - c. Right-click the **Silicon Labs** device in the list and select **Properties**.
  - d. Click the **Port Settings** tab. Click the **Advanced...** button.
  - e. Select an open COM port between COM1 and COM4. This allows the computer to remember the assignment and not reassign it each time the board serial UART port is plugged in.
  - f. Select the baud rate = **115200**, Data bits = **8**, Parity = **None**, Stop Bits = **1**, and Flow control = **None**. Click **OK**.

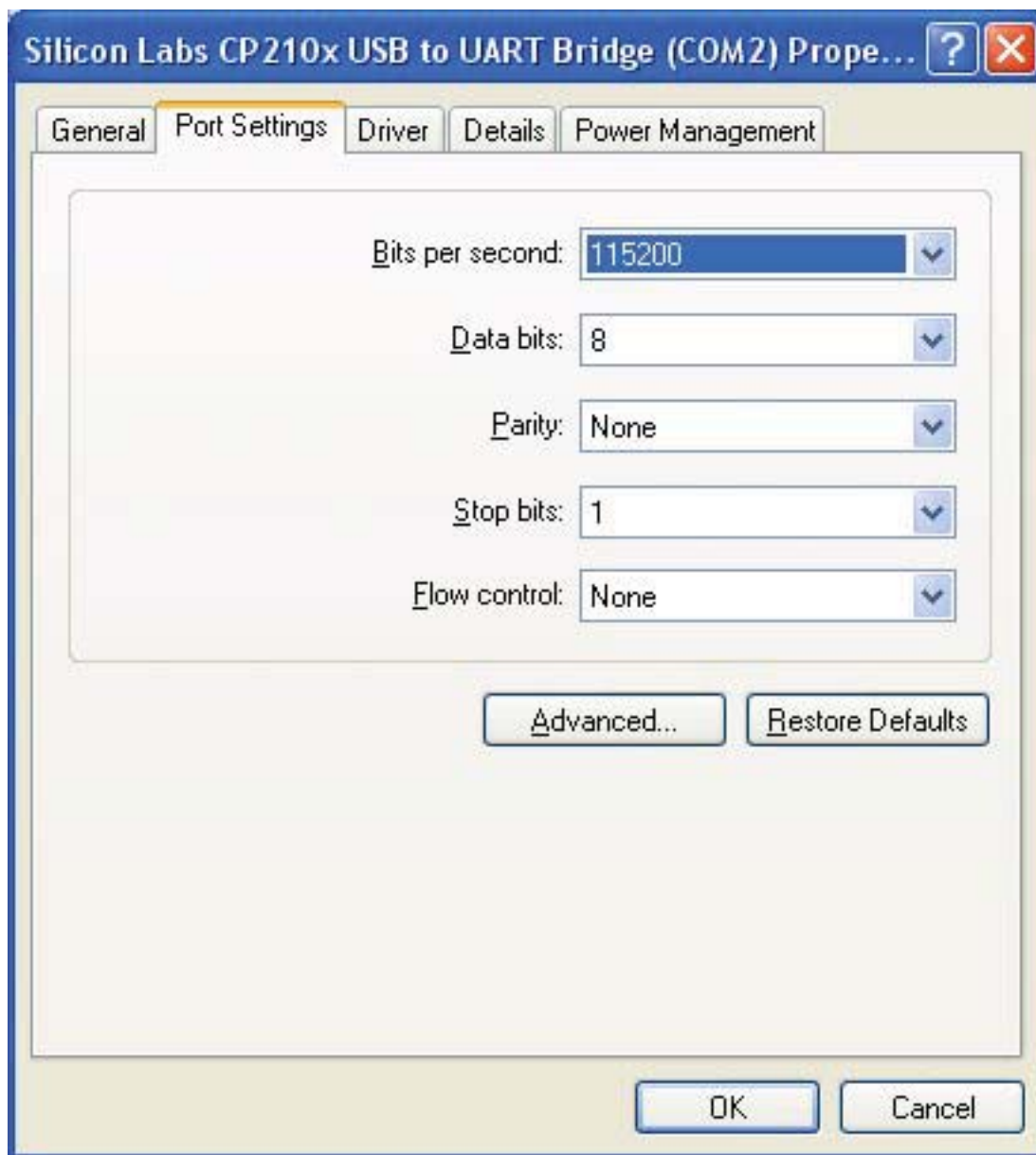
**Note:** Steps and diagrams refer to using a Windows XP or Windows 7 host PC.

Figure 2-4 through Figure 2-6 show the steps for setting the USB-UART port.



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Figure 2-4: Configuring the Driver



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Figure 2-5: UART Port Setting Tab

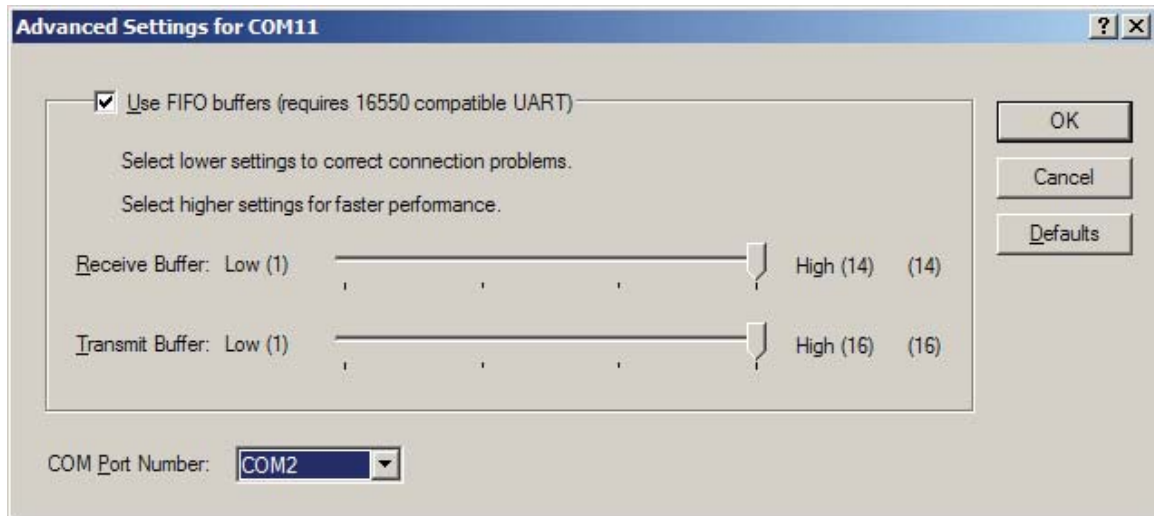
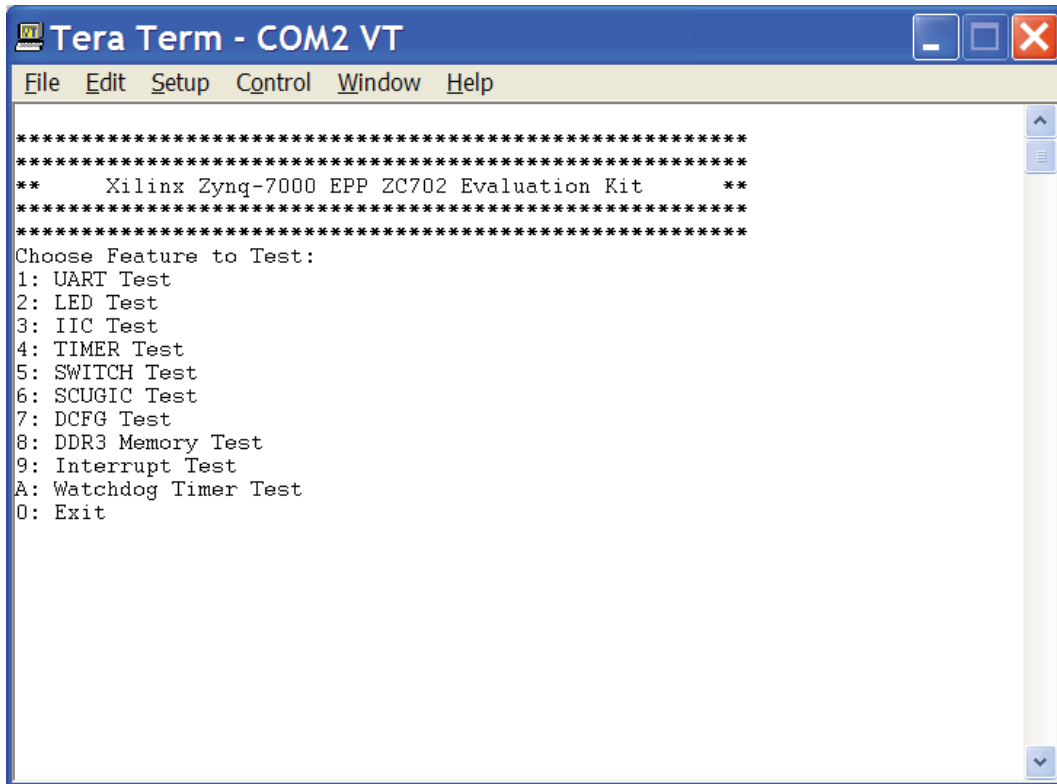


Figure 2-6: Select a COM Port (between COM1 and COM4)

---

## Run the BIST Application

1. Start Tera Term or a comparable installed terminal program. Configure it to have the following settings:  
Baud = **115200**, Data = **8**, P = **None**, Stop = **1** and Flow = **None**.
2. Press POR\_B (SW1) located in the top left corner of the ZC702 board and view the BIST output on the terminal window (see [Figure 2-7](#)).



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Figure 2-7: BIST Main Menu

3. Select each relevant test and observe the test results.

For more information on the BIST software and additional tutorials, including how to restore the default content of the onboard Quad SPI flash nonvolatile storage, see the ZC702 resource page [\[Ref 3\]](#).

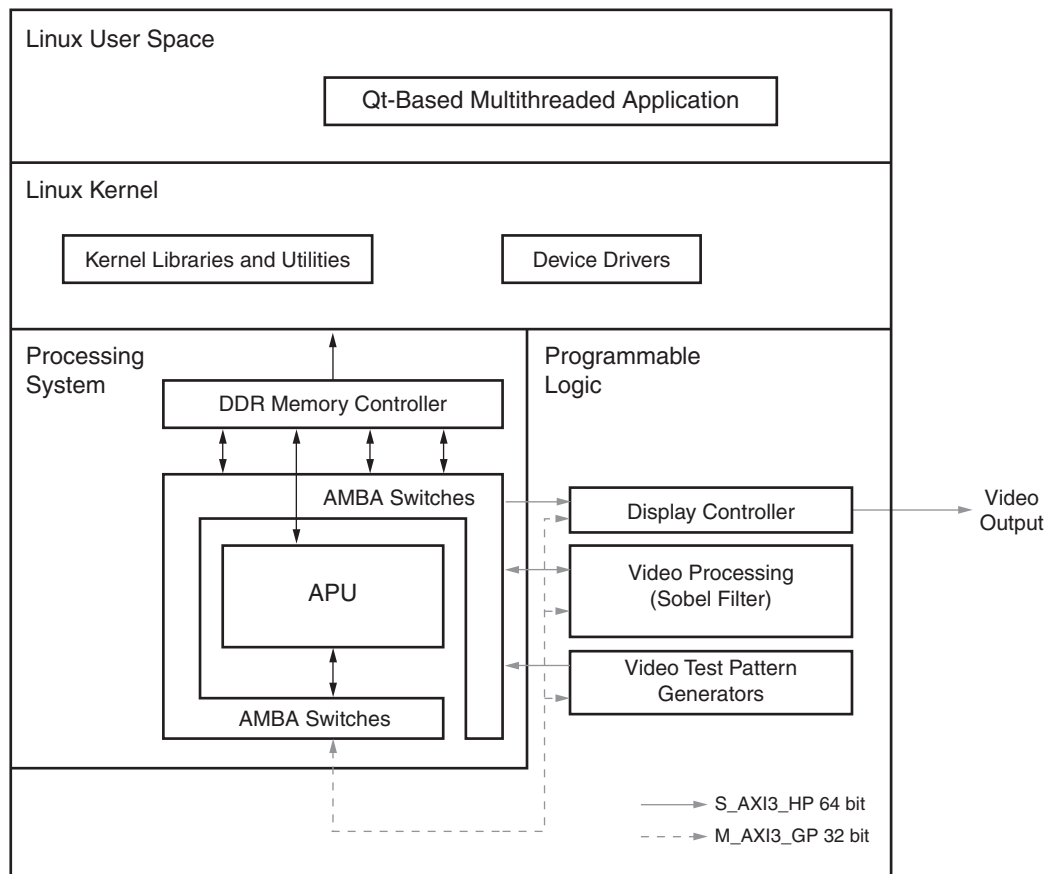
For more detailed information about these BIST tests, refer to UG850, *ZC702 Evaluation Board for the Zynq-7000 XC7Z020 All Programmable SoC User Guide* [\[Ref 6\]](#). Also refer to the ZC702 BIST User Guide found in the **Docs & Designs** tab on [www.xilinx.com/zc702](http://www.xilinx.com/zc702) [\[Ref 3\]](#) i.e., the ZC702 BIST PDF file, XTP180.

If any of the BIST tests fail, check the settings of the switches and jumpers as shown in [Figure 1-3](#), [Table 1-1](#), and [Table 1-2](#). If these settings are correct and the test still fails, please contact Xilinx Support and open a [WebCase](#).

# Getting Started with the Base Targeted Reference Design

## Introduction

Figure 3-1 shows the system block diagram for Zynq-7000 All Programmable SoC Base TRD.



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Figure 3-1: Zynq-7000 All Programmable SoC Base TRD System Block Diagram

The Base TRD showcases various features and capabilities of the Zynq Z-7020 All Programmable SoC device for the embedded domain in a single package. The Base TRD consists of two processing elements: The Zynq-7000 All Programmable SoC PS and an

interconnect logic-based video accelerator. The All Programmable SoC allows the user to implement a specific functionality either as a software program running on the Zynq-7000 All Programmable SoC PS or as a hardware design inside the PL. The Base TRD demonstrates how the user can seamlessly switch between a software or a hardware implementation, contributing to ease of use. The TRD also demonstrates the value of offloading computation-intensive tasks onto PL, thereby freeing the CPU resources to be available for user-specific applications.

This section of the document provides step by step instructions for bringing up the board and for running a video demonstration out of the box.

The ZC702 Evaluation kit comes with an SD card loaded with binaries that enable the user to run the video demonstration and software application. It also includes the binaries necessary to configure and boot the Zynq-7000 All Programmable SoC board.

**Note:** The screen captures in this document are conceptual representations of their subjects and provide general information only.

---

## Base TRD Key Features

The PS includes:

- Two ARM Cortex-A9 MPCore processors, each with a 32 KB instruction cache, a 32 KB data cache, and a NEON™ media processing engine and vector floating-point processor (VFPv3).
- 512 KB of level 2 cache
- 256 KB of on-chip RAM
- ARM AMBA® AXI interconnect
- Multi-protocol, 32-bit DDR DRAM controller
- 1 GB DDR3 running at 533 MHz
- Standard peripheral interfaces including USB, Ethernet, UART, I2C, SD MMC, and GPIO
- Clocks and reset for PL
- High bandwidth interconnect between PS and PL

The PL includes:

- Two AXI interconnects, 64-bit wide at 150 MHz
- One AXI interconnect, 32-bit wide at 75 MHz
- AXI VDMA(s)
- A full HD video input and output interface

- A Sobel accelerator
- Two AXI Performance Monitors

The software includes:

- Xilinx Zynq-7000 All Programmable SoC standard Linux kernel (based on Open Source Linux version 3.x)
- Linux device drivers for TRD-specific IPs.
- A Qt-based Linux application demonstrating the video processing pipeline
- A command line menu-based Linux application demonstrating the video processing pipeline

**Note:** The video demonstration contains the licensed IPs with no timeout.

---

## Base TRD Hardware Setup Requirements

These items are required to run and test the Base TRD and the video demonstration:

- The ZC702 evaluation board with the XC7Z020 CLG484-1 part
- USB Type-A to USB Mini-B cable (for UART communications) and a Tera Term Pro (or similar) terminal program
- USB-UART drivers from Silicon Labs [\[Ref 8\]](#)
- AC power adapter (12 VDC)
- An HDMI cable
- SD MMC flash card containing TRD binaries formatted with FAT32

**Note:** The included SD MMC is pre-loaded with required binaries. The binaries are loaded into the first partition of the SD MMC card and include:

- BOOT.bin
- devicetree.dtb
- zImage
- ramdisk8M.image.gz
- qt\_lib.img
- init.sh
- run\_sobel.sh
- sobel\_cmd
- sobel\_qt
- zynq.png



- A USB Micro-B to female A adaptor with USB hub is needed for connecting a keyboard and a mouse (not included with the kit)
- USB mouse and keyboard (not included with the kit)
- A display monitor that supports full HD resolution: 1920 x 1080p @ 60 Hz (not included with the kit)

**Note:** The example mentioned in this package has been tested with a Dell model #P2412H display monitor. However, the example should work well with any HDMI-compatible output device.

---

## TRD Demonstration Procedure

This section provides a procedure for setting up the ZC702 board and running the demonstration provided with the kit.

### Board Setup

1. Connect the cables as shown in [Figure 3-2](#) to prepare the ZC702 board to run the TRD video demonstration.

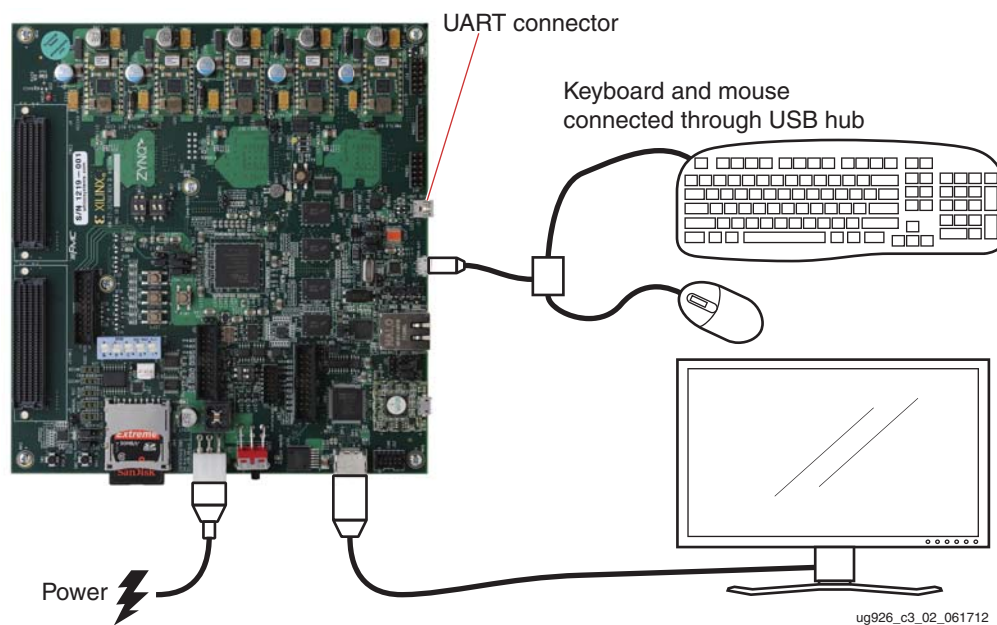
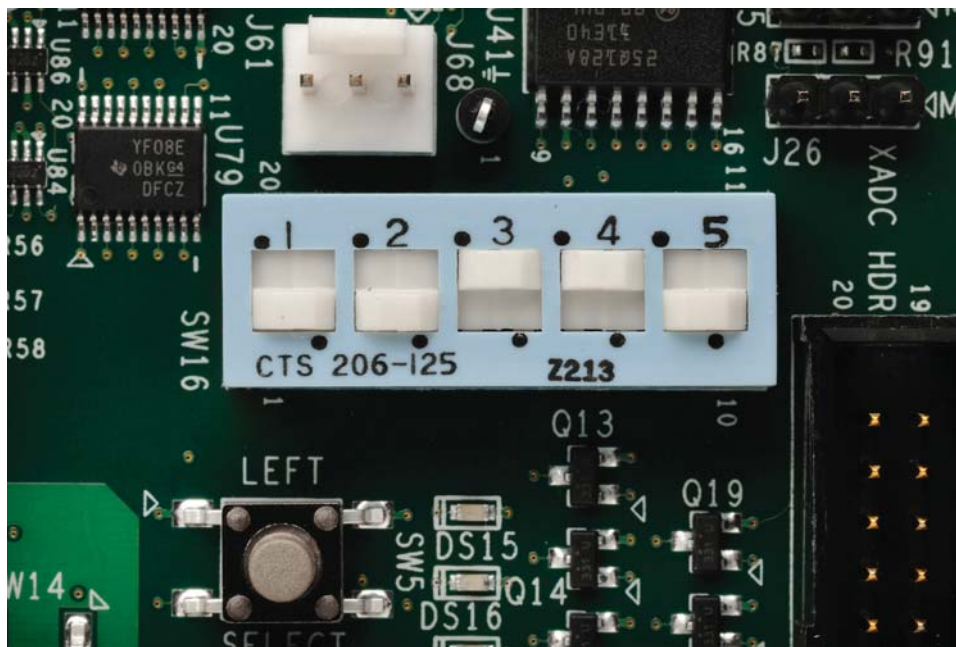


Figure 3-2: ZC702 Board Setup for a Video Demonstration

- a. Connect an LCD monitor to the HDMI out port of the ZC702 board using an HDMI cable.
- b. Connect a keyboard and mouse to the USB hub, which is connected to the ZC702 board Micro-B USB connector.

- Note:** The USB Micro-B to female A adaptor cable and USB hub are not included in the kit.
- c. Connect the USB Mini-B cable into the Mini USB port J17 labeled **USB UART** on the ZC702 board and the USB Type-A cable into an open USB port on the host PC for UART communications.
  - d. Connect the power supply to the ZC702 board. Do not switch the power on.
2. Insert the SD MMC, which contains the TRD binaries, into the SD slot on the ZC702 board.

**Note:** If the evaluation kit design files were downloaded online, copy the entire folder `zynq_base_trd_14.x/sd_image` onto the primary partition of the SD-MMC card (which is formatted as FAT32) using an SD-MMC card reader. The files in the SD-MMC card should match the list described in [SD MMC flash card containing TRD binaries formatted with FAT32, page 23](#).
  3. Make sure the switches are set as shown in [Figure 3-3](#), which allows the ZC702 board to boot from the SD-MMC card.



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Figure 3-3: Switch Settings for the Mode Switch to Boot from the SD-MMC Card

4. Make sure the monitor is set for HDMI or DVI 1920x1080.