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Zynq-7000 All Programmable SoC: ZC702 Evaluation Kit and Video and Imaging Kit (ISE Design Suite 14.5)

Getting Started Guide

UG926 (v4.0) May 14, 2013

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0402905-01

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
05/25/2012	1.0	Initial Xilinx release.
05/29/2012	1.1	Added Figure 4-3 and the text just before and after it.
06/21/2012	1.2	Chapter 1, Introduction: Added a "Reference Designs and Demonstrations" group to section ZC702 Evaluation Kit Contents, page 8. Changed cable from Digilent USB JTAG to Digilent USB-to-JTAG. Added that the SD MMC card contains bootable configuration files for the Base TRD demo design files and Linux applications platform. Updated USB JTAG interface information and added details to the clock sources list in section For reference design files, documents, and board source files, go to the ZVIK Product Page at www.xilinx.com/ZVIK and click on the Docs & Designs tab., page 10. Changed FMC1 and FMC2 connector types to LPC I/O expansion connectors. Added tables of default settings to the section Default Jumper and Switch Settings, page 11. Chapter 2, ZC702 Evaluation Kit Built-In Self-Test: Updated switch settings in the Introduction, page 15. Added bring-up details through the chapter. Settings were added to section Run the BIST Application, page 22. Added Chapter 3, Getting Started with the Base Targeted Reference Design. Added Chapter 4, Using the AMS101 Evaluation Card. Additional references were added through the book and to Appendix A, Additional Resources.
09/18/2012	2.0	The ZC702 evaluation kit now includes a USB Micro-B to female A adapter. Added information about the Zynq-7000 AP SoC Video and Imaging Kit (ZVIK) to the Overview, page 7 and a new section Zynq-7000 AP SoC Video and Imaging Kit Contents, page 10. Photos are updated in Figure 1-3: *Feature Callout for the ZC702 Board* and Figure 2-2: *ZC702 with the UART and Power Cable Attached*. The TRD Demonstration Procedure, page 30 adds information on how to demo the video application using an external video source supporting use of the ZVIK. Added Table 3-1 and Table 3-2. Added support for 720p video resolution in the video demo application in Running the Video Demonstration for 720p Video Resolution, page 39.
11/12/2012	2.1	Updated for ISE® Design Suite v14.3. Document and web site references changed throughout the book. In BIST Setup Requirements, page 15, "A power adapter and power cable for the ZC702 board" was removed. In ZC702 Evaluation Board Setup, page 16, step 1 changed. In Install the USB-UART Driver, page 18,step 1 and step 2 changed. An introduction was added to Chapter 3. In Base TRD Key Features, page 27, "1 GB DDR3 running at 533 MHz" was removed. In Base TRD Hardware Setup Requirements, page 28, `zImage` and `ramdisk8M.image.gz` became `uImage` and `uramdisk8M.image.gz`. The USB stick (or key) is not included in the kit. Instead, download files from the ZC702 Product Page at www.xilinx.com/zc702 and click on the **Docs & Designs** tab. Standoffs and a new Figure 3-3 showing mounting hardware details were added to TRD Demonstration Procedure, page 30. Figure 3-6 and Figure 3-7 were replaced to illustrate the QT-based GUI and minimized GUI mode. USB key was removed from Chapter 4. *Next Steps* became Chapter 5.

Date	Version	Revision
01/24/2013	3.0	Updated for ISE Design Suite 14.5. Revised eighth bullet on page 28 to replace sentence ending in "to exercise the portions of the demo ..." to be "use the frame buffer console terminal that will come up, once user exit the demo." Added third note on page 29. Revised Figure 3-6, page 34 and Figure 3-7, page 35.
02/12/2013	3.0.1	Removed stray internal draft banner from the cover page, and from the first page in each chapter and appendix.
05/14/2013	4.0	Deleted "Key Features of the ZC702 Evaluation Board" section. The Base TRD Key Features, page 27 were updated for the Programmable Logic (PL) to "One Performance Monitor". The required binaries in Base TRD Hardware Setup Requirements, page 28 were updated to include "`zynq-zc702-base-trd.dts`". Port "P1" was labelled in Figure 3-2. Figure 3-6 and Figure 3-7 were replaced to illustrate the QT-based GUI and minimized GUI mode. In Running the Video Demonstration for 720p Video Resolution, page 39, the instructions were updated for running QT based GUI in 720p mode and running the UART Menu based Demonstration Application in 720p mode.

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Introduction

Overview

The Zynq™-7000 All Programmable SoC (AP SoC) ZC702 evaluation kit shown in Figure 1-1 is based on the XC7Z020 CLG484-1 AP SoC. For additional information, see the Zynq-7000 AP SoC product table [Ref 1]. A built-in self-test (BIST) is provided for the ZC702 evaluation kit. The BIST provides a convenient way to test many of the board's features on power-up. The tutorials and reference designs available on the ZC702 product page can be used to further explore the capabilities of the ZC702 board and the Zynq-7000 AP SoC [Ref 2]. For the most up-to-date information on the content provided with the ZC702 evaluation kit, see the Zynq-7000 SoC ZC702 Evaluation Kit Product Page www.xilinx.com/zc702. UG873, *Zynq-7000 All Programmable SoC: Concepts, Tools, and Techniques* shows the basic hardware and software flow using the ZC702 board. The Zynq-7000 AP SoC documentation page is also helpful [Ref 3].

Figure 1-1: **ZC702 Evaluation Kit**

The Zynq-7000 AP SoC Video and Imaging Kit (ZVIK) shown in Figure 1-2 is based on the ZC702 evaluation kit and includes all of the components of the ZC702 kit with the

addition of components enabling HD video input from an High-Definition Multimedia Interface (HDMI™) source or from the included HD image sensor. All of the information presented in this guide related to the ZC702 evaluation kit applies to the ZVIK. For the most current information on the content provided with the ZVIK, see the Zynq-7000 All Programmable SoC Video and Imaging Kit product page [Ref 4].

Figure 1-2: **Zynq-7000 AP SoC Video and Imaging Kit**

This user guide also describes a Base Targeted Reference Design (TRD) based on Zynq-7000 AP SoC architecture. The Base TRD showcases various features and capabilities of the Zynq Z-7020 AP SoC for the embedded domain in a single package.

TRDs are key components of the Xilinx Targeted Design Platform (TDP) strategy. TDPs from Xilinx provide customers with basic scalable design platforms for the creation of FPGA-based solutions in a wide variety of applications and industries.

Note: In the remainder of this document, the Zynq-7000 AP SoC ZC702 evaluation kit is referred to as the *ZC702 Evaluation Kit* and the Zynq-7000 AP SoC Video and Imaging Kit is referred to as *ZVIK*.

ZC702 Evaluation Kit Contents

The ZC702 evaluation kit includes the following items:

- ZC702 evaluation board featuring the XC7Z020 CLG484-1
- Agile Mixed Signal (AMS) evaluation board
- Full seat ISE® Design Suite Embedded Edition design tools
  - Device-locked to the Zynq-7000 XC7Z020 CLG484-1 device

- Board design files
  - Schematics
  - Board layout files
  - Bill of materials
- Documentation
  - *Getting Started Guide* (this document)
  - Hardware user guide (UG850, *ZC702 Evaluation Board for the Zynq-7000 XC7Z020 All Programmable SoC User Guide*)
  - TRD user guide (UG925, *Zynq-7000 All Programmable SoC ZC702 Base Targeted Reference Design User Guide*)
- Reference Designs and Demonstrations
  - BIST Utility and Demonstration
  - Targeted Reference Design (TRD), demonstrating a video processing pipeline.

    Note: The video demonstration contains the licensed IPs with no timeout. To recompile this design, the user needs to register for an evaluation IP license for the Video IP.
  - AMS demonstration, providing an overview of the analog capabilities of the Zynq-7000 AP SoC devices.
- 12V AC adapter power supply
- Cables
  - RJ-45 Ethernet cable
  - HDMI cable
  - USB Type-A to USB Micro-B cable (Digilent USB-to-JTAG Programing Port)
  - USB Type-A to USB Mini-B cable (serial UART)
  - USB Micro-B to female A adapter (for connecting USB hub, keyboard, and mouse)
- Secure Digital Multimedia Card (SD MMC) (contains bootable configuration files for the Base TRD demonstration design files and Linux platform applications)

The kit contains the software and reference designs, a demonstration, and documents to help the user get started quickly.

For reference design files, documents, and board source files, go to the ZC702 Product Page at www.xilinx.com/zc702 and click on the **Docs & Designs** tab.

Zynq-7000 AP SoC Video and Imaging Kit Contents

The ZVIK contains all of the items included in the ZC702 evaluation kit plus the following items. For more information on the HDMI input/output FMC module and ON Semiconductor image sensor, refer to the Avnet product page [Ref 10].

- HDMI input/output FPGA mezzanine card (FMC) module
- ON Semiconductor VITA 2000 Color Image Sensor module
- Standard interchangeable $^{2}/_{3}$-inch 8 mm C-mount lens
- Infrared (IR) cut filter
- Camera tripod
- Lens holder
- Cables
  - Second HDMI cable
  - LCEDI image sensor cable

For reference design files, documents, and board source files, go to the ZVIK Product Page at www.xilinx.com/ZVIK and click on the **Docs & Designs** tab.

Key Features of the ZVIK

Key features of the additional components of the Zynq-7000 AP SoC Video and Imaging kit include:

- HDMI input/output FMC module
  - HDMI input
  - HDMI output
  - Video clock synthesizer
  - Interface for ON Semiconductor VITA image sensor module
- ON Semiconductor VITA 2000 color image sensor module
  - Supports up to WXGA resolution: 1920 (H) x 1200 (V) format
  - 92 frames per second (fps) at full resolution
  - 4.8 µm x 4.8 µm pixel size $^{2}/_{3}$-inch optical format
  - Pipelined and triggered global shutter, rolling shutter

- Random programmable region of interest (ROI) readout
- Automatic exposure control (AEC)

- Standard interchangeable $^{2}/_{3}$-inch, 8 mm C-mount lens

Default Jumper and Switch Settings

Figure 1-3 calls out the major features on the ZC702 board. See UG850, *ZC702 Evaluation Board for the Zynq-7000 XC7Z020 All Programmable SoC User Guide* for more detailed information about the ZC702 board.

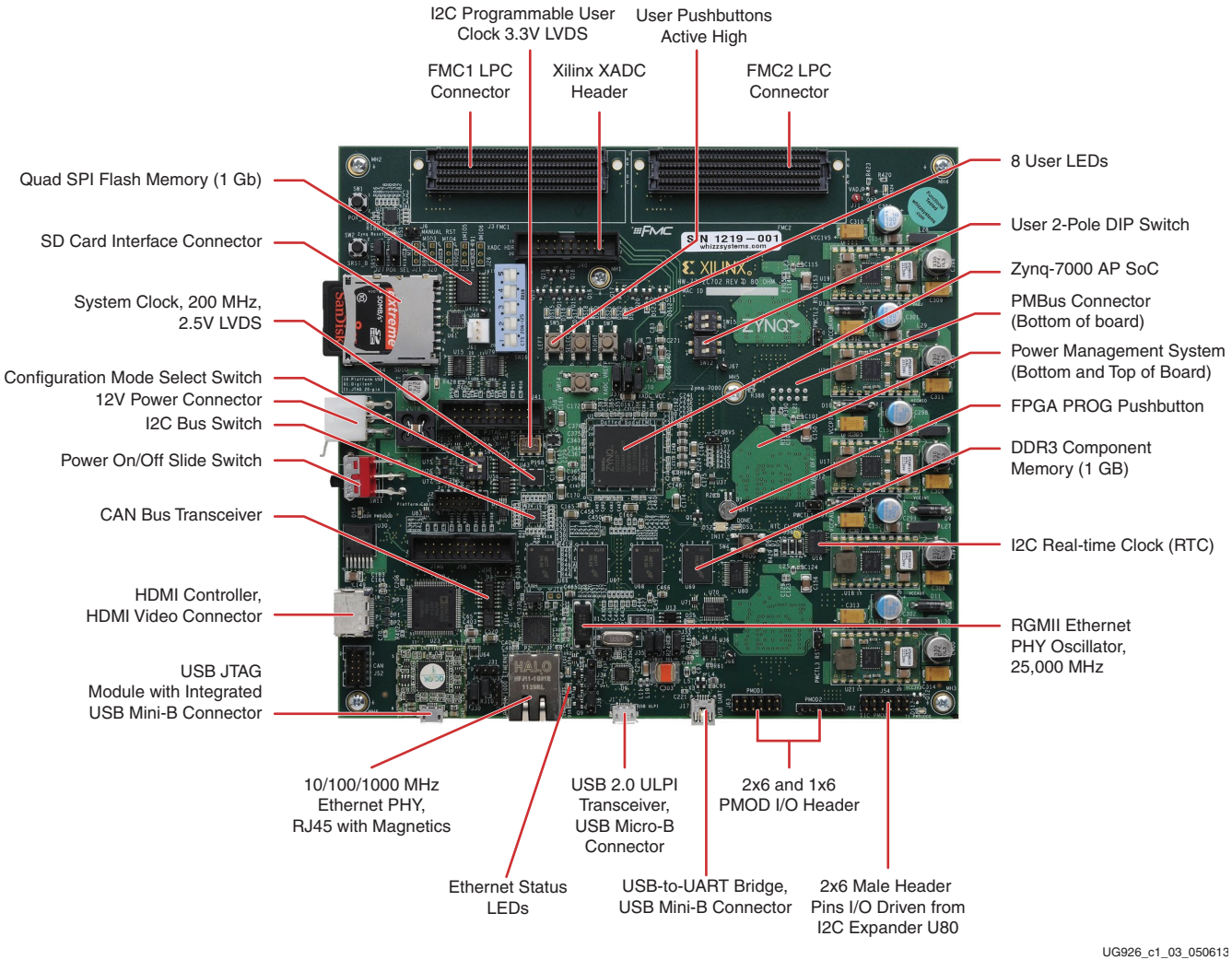

Figure 1-3: **Feature Callout for the ZC702 Board**

Default factory settings of jumpers and switches on the ZC702 board are highlighted in Figure 1-4. Default switch and jumper settings are listed in Table 1-1 and Table 1-2.

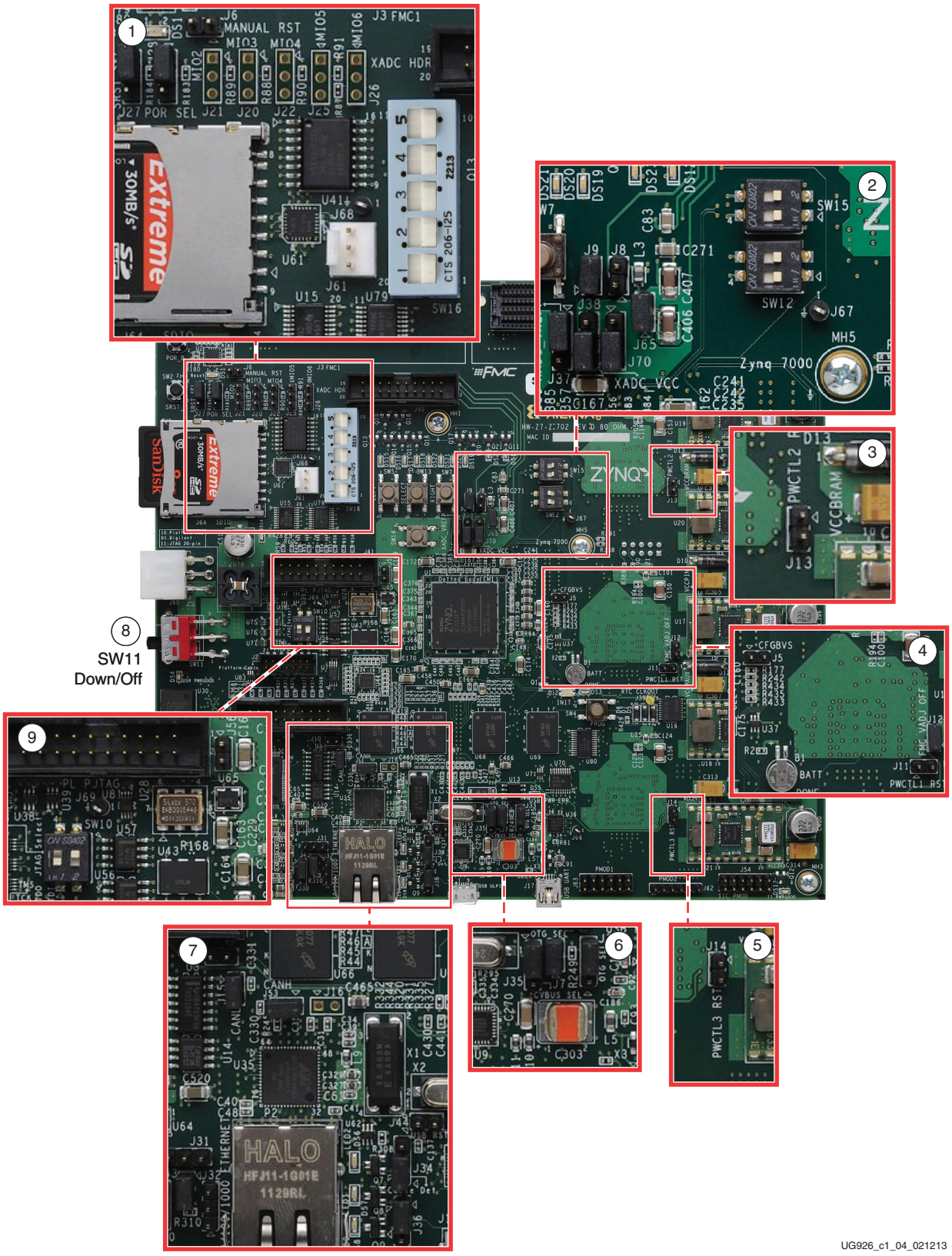

Figure 1-4: **Default Jumper and Switch Settings on the ZC702 Board**

Table 1-1: **Default Switch Settings**

Switch	Position	Setting	Figure 1-4 Callout
SW10 (JTAG chain input select two-position DIP switch)	1	Off	9
	2	On	
SW12 (two-position DIP switch)	1	Off	2
	2	Off	
SW15 (two-position DIP switch)	1	Off	2
	2	Off	
SW16 (five-position DIP switch)	1	Right	1
	2	Right	
	3	Right	
	4	Right	
	5	Right	
SW11 (power slide switch)		Off	8
	1	Down	

Default jumper positions are shown in Figure 1-4 and listed in Table 1-2.

Table 1-2: **Default Jumper Settings**

Jumper	Function	Default Position	Figure 1-4 Callout
HDR_1 X 2			
J5	CFGBVS short to GND	OFF	4
J6	POR Master Reset	OFF	1
J7	USB 2.0 USB_VBUS_SEL	ON	6
J8	XADC GND L3 Bypass	OFF	2
J9	XADC GND	ON	2
J10	ARM HDR J41 pin 2 to VADJ	OFF	7
J11	UCD9248 U32 ADDR52 RESET_B	OFF	4
J12	FMC_VADJ_ON_B	ON	4
J13	UCD9248 U33 ADDR53 RESET_B	OFF	3
J14	UCD9248 U34 ADDR54 RESET_B	OFF	5
J15	CAN BUS COMMON-MODE CANH HDR	ON	7
J43	Ethernet PHY HDR	ON	7
J44	USB 2.0 USB_RESET_B	OFF	7
J53	CAN BUS COMMON-MODE CANL HDR	ON	7
J56	JTAG HDR J58 pin 2 3.3V SEL	OFF	9
J65	XADC_VCC5V0 = VCC5V0	ON	2

Table 1-2: **Default Jumper Settings *(Cont'd)***

Jumper	Function	Default Position	Figure 1-4 Callout
HDR_1 X 3			
J27	PS_SRST_B	1-2	1
J28	PS_POR_B	1-2	1
J30	Ethernet PHY HDR	1-2	7
J31	Ethernet PHY HDR	NONE	7
J32	Ethernet PHY HDR	NONE	7
J33	USB 2.0 Mode	2-3	6
J34	USB 2.0 J1 ID SEL	1-2	7
J35	USB 2.0 J1 VBUS CAP SEL	1-2	6
J36	USB 2.0 J1 GND SEL	1-2	7
J37	XADC_VREP SEL	1-2	2
J38	XADC_VCC SEL	2-3	2
J70	XADC_VREF Source SEL	2-3	2

ZC702 Evaluation Kit Built-In Self-Test

Introduction

The BIST tests many of the features offered by the ZC702 evaluation kit. The test is stored in the onboard nonvolatile Quad SPI flash memory and configures the AP SoC when mode switch SW16 is set to where SW1, 2, 3, and 5 are switched to the right and SW4 is switched to the left, indicating QSPI configuration. This exercise of running the BIST demonstration should take approximately 10 to 15 minutes.

Note: For a description of all the features on the ZC702 board, see UG850, *ZC702 Evaluation Board for the Zynq-7000 XC7Z020 All Programmable SoC User Guide*.

BIST Setup Requirements

These are the prerequisites for running the BIST demonstration.

- Hardware setup:
  - ZC702 evaluation board with XC7Z020 CLG484-1 part
  - USB Type-A to Mini-B cable (for UART)
  - AC power adapter (12 VDC)
- Windows software and driver setup:
  - Tera Term Pro [Ref 8] (or similar) terminal program (might already be installed)
  - USB-UART driver from Silicon Labs [Ref 9] (might already be installed)

Hardware BIST Board Setup

This section describes the hardware setup and use of the terminal program for running the BIST application. It contains step-by-step instructions for board bring-up.

ZC702 Evaluation Board Setup

The default jumper and switch settings of the ZC702 board are shown in Figure 1-4, Table 1-1, and Table 1-2.

1. Set the SW16 switch as shown in Figure 2-1, where position 1, 2, 3, and 5 are switched to the right and position 4 is switched to the left for the BIST to boot from Quad SPI device and run the system demonstration utility.

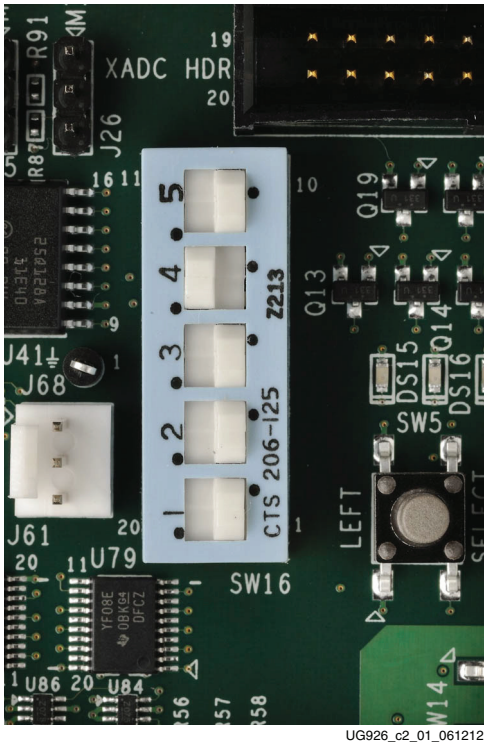

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Figure 2-1: **Settings for the Mode Switch to Boot from Quad SPI Mode**

Hardware Bring-Up

This section describes the steps for hardware bring-up.

1. Be sure to have the SW16 Mode switch settings set to those shown in Figure 2-1.
2. With the ZC702 board switched OFF (SW11 in the down position, as shown in Figure 1-4), plug the USB Mini-B cable into the Mini USB port J17 labeled USB UART on the ZC702 board and the other end into a open USB port on your PC (Figure 2-2).

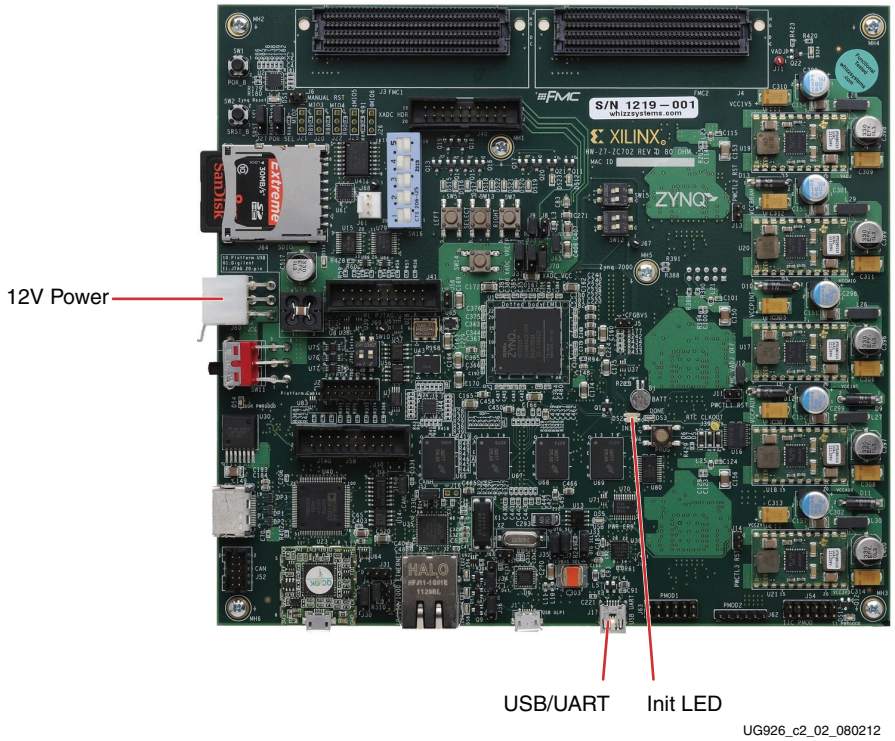

Figure 2-2: **ZC702 with the UART and Power Cable Attached**

3. Connect the power cable.
4. Switch the ZC702 board's power to ON (SW11 switched up as shown in Figure 1-4).

Install the USB-UART Driver

1. Run the downloaded executable UART-USB driver file, listed in BIST Setup Requirements, page 15. Running the executable file enables USB-to-UART communications with a host PC. This driver downloads and executes automatically when the board is powered up or it can be downloaded from the Silicon Laboratories web site [Ref 9].

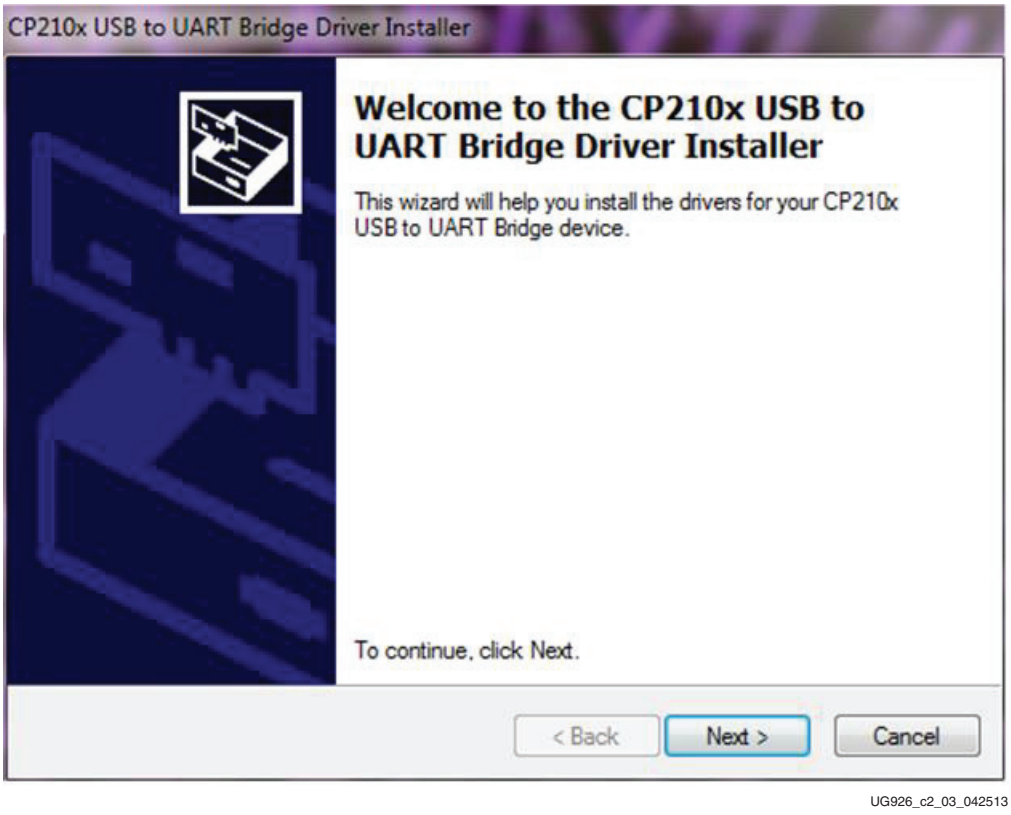

Figure 2-3: **UART Cable Driver Installation**

2. Set the USB-UART connection to a known COM Port and baud rate in the Device Manager.
   a. Left-click **Start Menu** and select **Control Panel** in Windows 7.
   b. Select **Device Manager** on the left side.
   c. Right-click the **Silicon Labs** device in the list and select **Properties.**
   d. Click the **Port Settings** tab. Click the **Advanced...** button.
   e. Select an open COM port between COM1 and COM4. This allows the computer to remember the assignment and not reassign it each time the board serial UART port is plugged in.
   f. Select the baud rate = **115200**, Data bits = **8**, Parity = **None**, Stop Bits = **1**, and Flow control = **None.** Click **OK**.

Note: Steps and diagrams refer to using a Windows XP or Windows 7 host PC.

Figure 2-4 through Figure 2-6 show the steps for setting the USB-UART port.

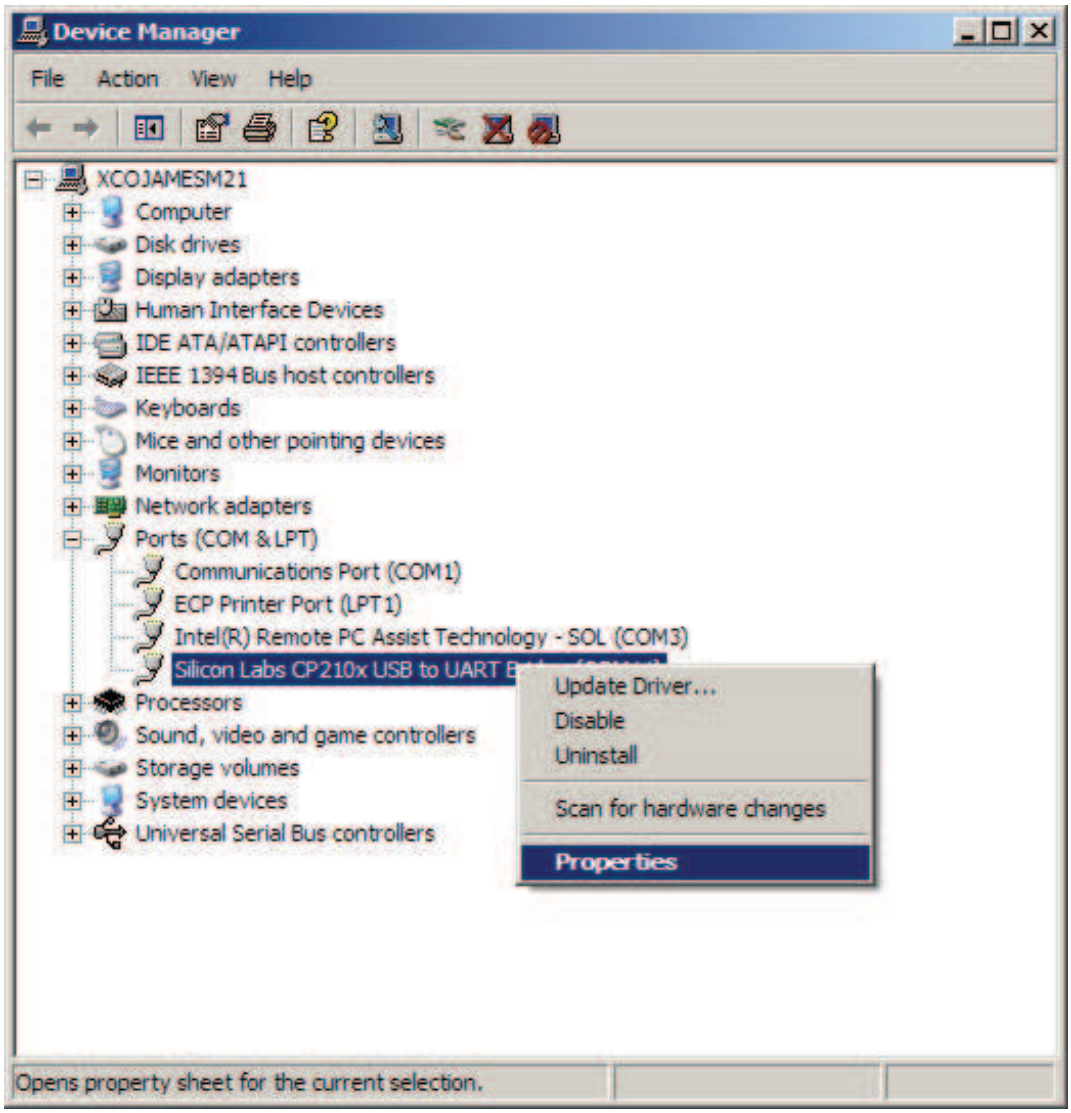

Figure 2-4: **Configuring the Driver**

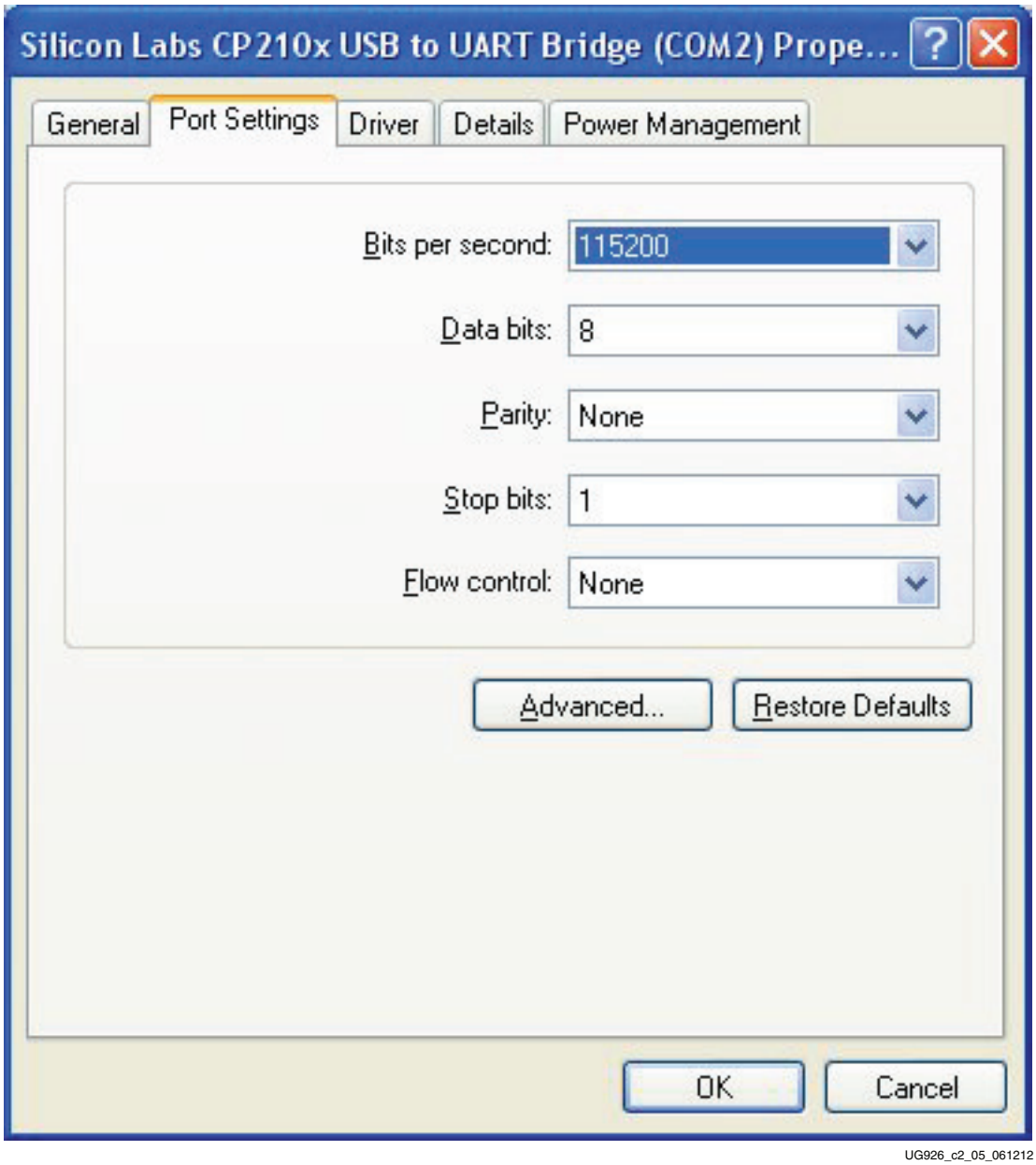

Figure 2-5: **UART Port Setting Tab**

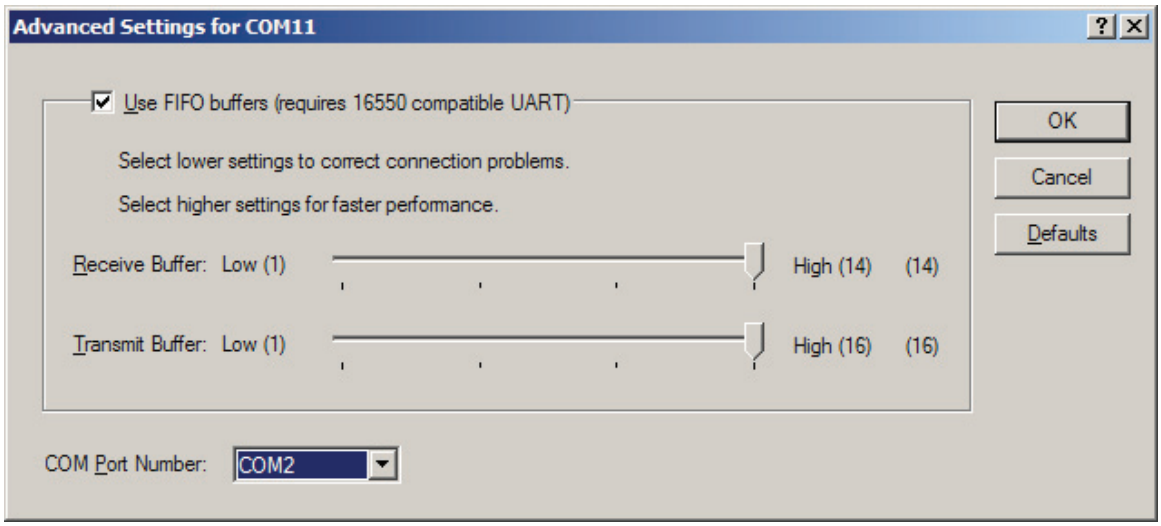

Figure 2-6: **Select a COM Port (between COM1 and COM4)**

Run the BIST Application

1. Start Tera Term or a comparable installed terminal program. Configure it to have the following settings:
   Baud = **115200**, Data = **8**, Parity = **None**, Stop = **1** and Flow = **None**.
2. Press POR_B (SW1) located in the top left corner of the ZC702 board and view the BIST output on the terminal window (Figure 2-7).

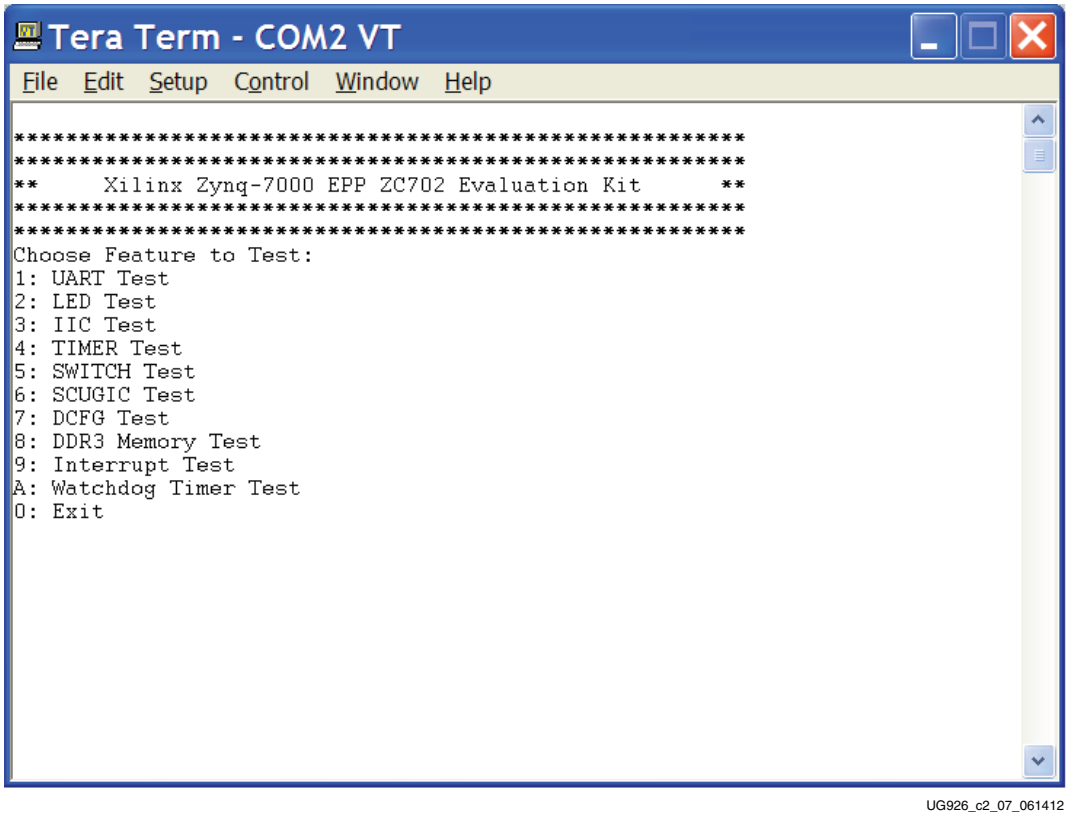

Figure 2-7: **BIST Main Menu**

3. Select each relevant test and observe the test results.

For more information on the BIST software and additional tutorials, including how to restore the default content of the onboard Quad SPI flash nonvolatile storage, see the ZC702 resource page [Ref 4].

For more detailed information about these BIST tests, refer to UG850, *ZC702 Evaluation Board for the Zynq-7000 XC7Z020 All Programmable SoC User Guide*. Also refer to the ZC702 BIST User Guide found in the **Docs & Designs** tab on www.xilinx.com/zc702, that is, the ZC702 BIST PDF file, XTP180.

If any of the BIST tests fail, check the settings of the switches and jumpers as shown in Figure 1-4, Table 1-1, and Table 1-2. If these settings are correct and the test still fails, please contact Xilinx Support at www.xilinx.com/support and open a WebCase.

Chapter 3

Getting Started with the Base Targeted Reference Design

Introduction

This section provides step by step instructions for bringing up the board and running the video Targeted Reference Design (TRD). In this design, the Zynq-7000 AP SoC performs real-time processing of a 1080p60 video stream—either in Processing System (PS) software or Programmable Logic (PL) hardware accelerator. The video processing path is user-selectable through a graphical user interface (GUI) running on Linux in the Zynq-7000 AP SoC PS. The GUI also displays detailed information about system usage statistics and system performance.

Figure 3-1 shows the system block diagram for Zynq-7000 AP SoC Base TRD.