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WT32i BLUETOOTH AUDIO MODULE

DATA SHEET

Tuesday, 22 July 2014

Version 1.21

VERSION HISTORY

VERSION	COMMENT
1.0	First version
1.1	Added example how to protect the battery by shutting down the regulators at certain voltage level
1.2	Fixed PCM pin numbering
1.21	Design check list added

TABLE OF CONTENTS

WT32i *Bluetooth®* Audio Module

DESCRIPTION

WT32i is an audio specific *Bluetooth* 3.0 module with excellent radio frequency performance and enhanced audio features, enabling a best in class *Bluetooth* audio experience. In addition to a certified *Bluetooth* radio and software stack, WT32i also contains a DSP, stereo audio codec, and battery charger making it ideal for fixed and portable audio applications. WT32i includes Bluegiga's iWRAP6 *Bluetooth* stack software which implements A2DP, AVRCP v.1.5 profiles and supports aptX® and AAC audio codecs for stereo audio applications. For hands-free applications iWRAP6 software also supports HFP v.1.6, HSP, MAP and PBAP and CVC® echo cancellation software. For data communications to Android and iOS applications iWRAP6 also implements *Bluetooth* Serial Port Profile (SPP) and Apple iAP profiles. WT32i is an ideal solution for developers who want to quickly integrate the latest *Bluetooth* audio technologies without the time and costs typically involved with a *Bluetooth* audio chipset design.

APPLICATIONS:

- Stereo speakers and sound bars
- Hi-Fi devices
- Hands-free kits
- Stereo headsets

Figure 1: WT32i Bluetooth Audio Module

KEY FEATURES:

- *Bluetooth* 3.0 compliant
- Excellent Radio Performance
  - Transmit power: +6.5 dBm
  - Receiver sensitivity: -90 dBm
  - Link budget: 96.5 dB
- Integrated chip antenna or U.FL antenna connector
- Audio features
  - Integrated DSP
  - 16-bit stereo codec
  - 44.1kHz ADC, 48kHz DAC
  - Analog, I2S, PCM, SPDIF, and microphone interfaces
  - Optional aptX® and AAC stereo audio codecs
  - Optional CVC® echo cancellation
  - Wide Band Speech
- Built-in battery charger
- UART host interface
- 802.11 co-existence interface
- 10 software programmable IO pins
- Operating voltage: 1.8V to 3.6V
- Temperature range: -40C to +85C
- *Bluetooth*, CE, FCC, IC, Korea and Japan qualified
- Integrated iWRAP6 *Bluetooth* stack
  - 13 *Bluetooth* profiles
  - Apple iAP1 and iAP2 compatibility

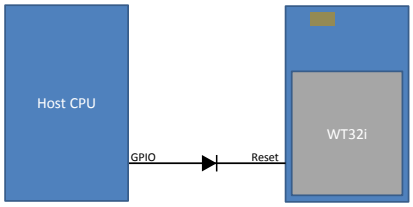
1 Design Check List

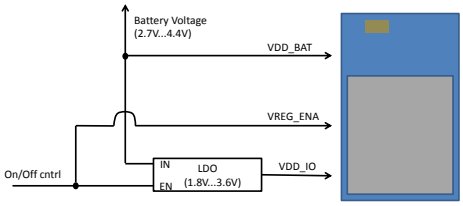
POWERING THE MODULE

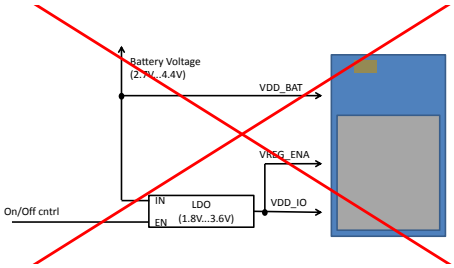
- Make sure that VRE_ENA is connected correctly
- Use iWRAP command SET CONTROL VREGEN command to configure the VREG_ENA pin according to the HW

- Reserve test points for SPI interface for debugging and FW updates

- The internal power on reset does not work properly if the host pulls the reset line low during boot. To prevent this, place a diode to the reset input.

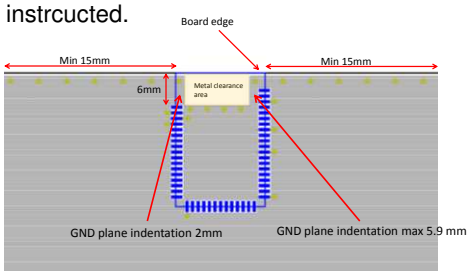


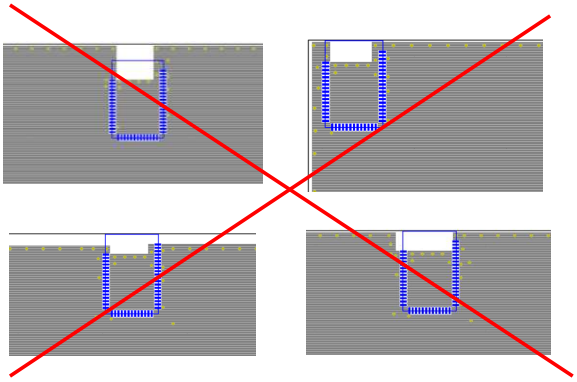




RF LAYOUT

- Make sure that the layout for the antenna is done as instrcucted.



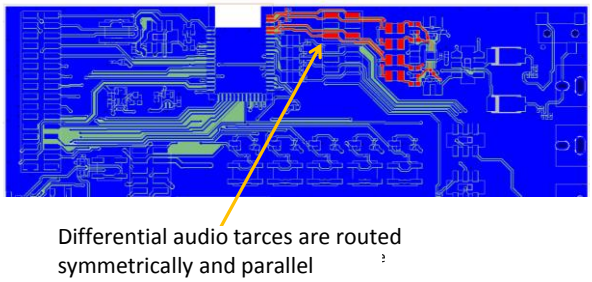


AUDIO DESIGN AND LAYOUT

- See the example schematics on pages 49 -52
- Avoid using single ended audio traces. Always use differential audio signaling when possible
- Use solid GND plane and make sure that all the GND pins are connected to it by placing a GND via right next to any GND pins.

- When routing single ended audio traces, make sure that the return current (i.e. GND) follows the traces all the way from start to the end

- DO NOT COMPROMISE AUDIO ROUTING



2 WT32i Product Numbering

Product code	Description
WT32i-A-AI6	WT32i Bluetooth Module with internal chip antenna and iWRAP6 *Bluetooth* software
WT32i-A-AI6-APTX	WT32i Bluetooth Module with internal chip antenna and aptX® audio codec capable iWRAP6 *Bluetooth* software.
WT32i-A-AI6IAP	WT32i Bluetooth Module with internal chip antenna and Apple iAP capable iWRAP6 *Bluetooth* software. Available only to Apple MFI licensees. Contact sales@bluegiga.com for more information.
WT32i-E-AI6	WT32i Bluetooth Module with U.FL connector and iWRAP6 *Bluetooth* software
WT32i-E-AI6-APTX	WT32i Bluetooth Module with U.FL connector and aptX® audio codec capable iWRAP6 *Bluetooth* software.
WT32i-E-AI6IAP	WT32i Bluetooth Module with U.FL connector and Apple iAP capable iWRAP6 *Bluetooth* software. Available only to Apple MFI licensees. Contact sales@bluegiga.com for more information.
DKWT32i-A	WT32i development kit

3 Block diagram

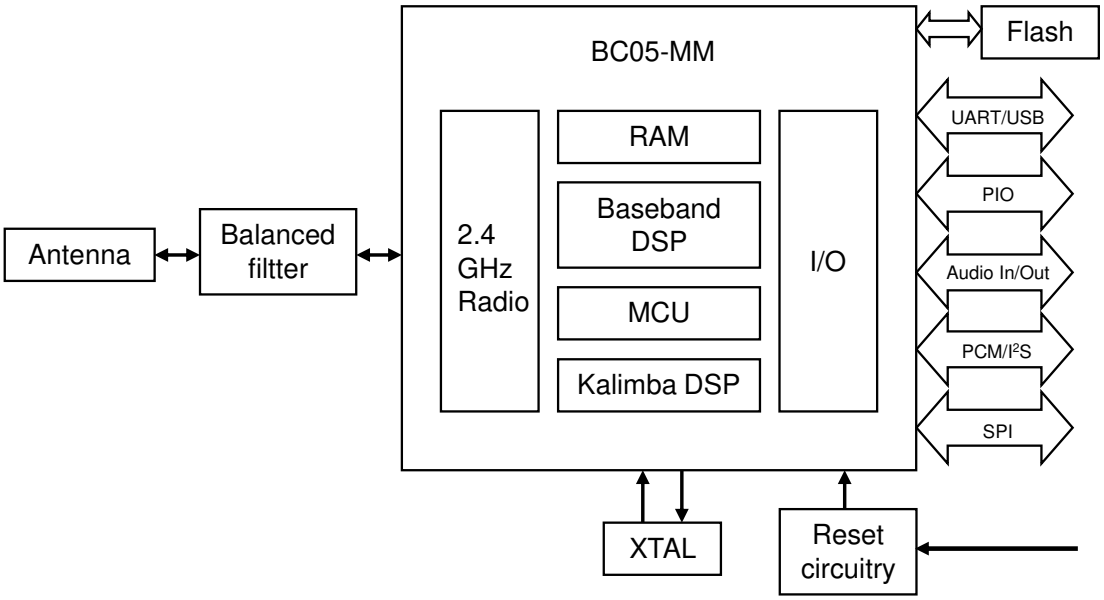


Figure 2: Block Diagram of WT32i

BC05-MM

The BlueCore®5-Multimedia External is a single-chip radio and baseband IC for Bluetooth 2.4GHz systems. It provides a fully compliant Bluetooth v3.0 specification system for data and voice. BlueCore5-Multimedia External contains the Kalimba DSP coprocessor with double the MIPS of BlueCore3-Multimedia External, supporting enhanced audio applications.

XTAL

Ther reference clock of WT32i is generated with 26 MHz crystal. All BC05-MM internal digital clocks are generated using a phase locked loop, which is locked to the frequency of either the 26 MHz crystal or an internally generated watchdog clock frequency of 1kHz.

RESET CIRCUITRY

The internal reset circuitry keeps BC05-MM in reset during boot in order for the supply voltages to stabilize. This is to prevent corruption of the flash memory during booting. Please see chapter 6.1 for more detailed description.

BALANCED FILTER

The internal balanced filter provides optimal impedance matching and band pass filtering in order to achieve lowest possible in-band and out-of-band emissions.

ANTENNA

The antenna is a ceramic chip antenna with high efficiency. The antenna is insensitive to surrounding dielectric materials and requires only a small clearance underneath which makes it compatible with previous WT32I designs and well suitable for designs with high density.

FLASH

16 Mbit flash memory is used for storing the Bluetooth protocol stack and Virtual Machine applications. It can also be used as an optional external RAM for memory-intensive applications.

4 Pinout and Terminal Description

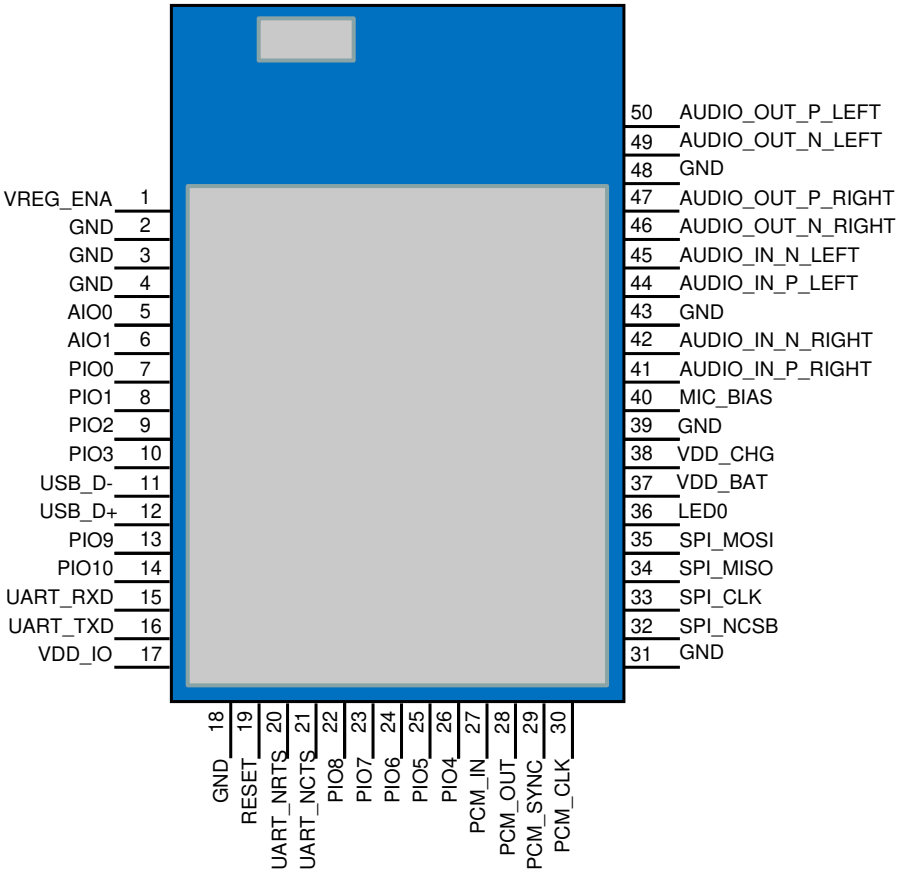


Figure 3: WT32i

Pin Number	Pin Name	Pad Type	Description
1	VREG_ENA	Input	SW configurable enable pin for the internal regulators
2-4, 18, 31, 39, 43, 48	GND	GND	GND
17	VDD_IO	Power supply	1.7V - 3.6V power supply for the serial interfaces and GPIOs
37	VDD_BAT	Power supply / Charger output	2.7V - 4.4V supply voltage for the internal regulators and output of the battery charger
38	VDD_CHG	Power supply	Nominal 5V supply voltage for the battery charger

Table 1: Supply Terminal Descriptions

Pin Number	Pin Name	Pin Type	Description
19	RESET	RESET	Active high reset. If not used, leave floating. When connected, make sure that the reset is either pulled high or floating (connected to high impedance) during boot.
5	AIO0	Configurable I/O	AIO0 and AIO1 can be used to read the voltage level through the internal ADC (refer to iWRAP User Guide for details). AIO pins can also be configured to be used as general digital IO pins through PS settings. Internal clocks can be routed out through AIO pins by setting corresponding PS settings. Note that the AIO pins are powered from internal 1.5V supply so the maximum voltage level of the AIO pins is 1.5V.
6	AIO1		
7	PIO0	Configurable CMOS I/O	General purpose IO's can be configured with iWRAP for various functions. Each IO can be configured individually as output or input with strong or weak pull-up/-down. Using particular PS setting GPIO pins can be used to implement WiFi co-existence signaling between WT32i and a WiFi radio. Software I2C interface can be implemented for slow I2C functions such as configuring external audio codec or display.
8	PIO1		
9	PIO2		
10	PIO3		
13	PIO9		
14	PIO10		
22	PIO8		
23	PIO7		
24	PIO6		
25	PIO5		
26	PIO4		
11	USB_D-	I/O	USB data minus
12	USB_D+	I/O	USB data plus with selectable internal 1.5k pull-up resistor
15	UART_RXD	CMOS Input, weak internal pull-down	UART data input
16	UART_TXD	CMOS output, tristate, weak internal pull-up	UART data output
20	UART_NRTS	CMOS output, tristate, weak internal pull-up	UART request to send, active low
21	UART_NCTS	CMOS Input, weak internal pull-down	UART clear to send, active low
32	SPI_NCSB	CMOS Input, weak internal pull-down	SPI chip select
33	SPI_CLK	CMOS Input, weak internal pull-down	SPI clock

34	SPI_MISO	CMOS Input, weak internal pull-down	SPI data input
35	SPI_MOSI	CMOS output, tristate, weak internal pull-down	SPI data output
36	LED0	Open drain output	LED driver

Table 2: Terminal Descriptions

Pin Number	Pin Name	Pin Type	Description
40	MIC_BIAS	Analog	
41	AUDIO_IN_P_RIGHT	Analog	
42	AUDIO_IN_N_RIGHT	Analog	
44	AUDIO_IN_P_LEFT	Analog	
45	AUDIO_IN_N_LEFT	Analog	
46	AUDIO_OUT_N_RIGHT	Analog	
47	AUDIO_OUT_P_RIGHT	Analog	
49	AUDIO_OUT_N_LEFT	Analog	
50	AUDIO_OUT_P_LEFT	Analog	
27	PCM_IN / I2S IN	CMOS input, weak internal pull-down	PCM or I2S data input
28	PCM_OUT / I2S_OUT	CMOS outptu, tristate, weak internal pull-down	PCM or I2S data output
29	PCM_SYNC / I2S_WS	Bidirectional, weak internal down	PCM sync or I2S word select. WT32i can operate as a PCM/I2S master providing the sync or as a slave receiving the sync
30	PCM_CLK / I2S_SCK	Bidirectional, weak internal down	PCM or I2S clock. WT32i can operate as a PCM/I2S master providing the clock or as a slave receiving the clock.

Table 3: Audio Terminal Descriptions

5 Electrical Characteristics

5.1 Absolute Maximum Ratings

	Min	Max	Unit
Storage temperature range	-40	+85	°C
Operating temperature range	-40	+85	°C
VDD_IO	-0.4	3.6	V
VDD_BAT	-0.4	4.4	V
VDD_CHG	-0.4	6.5	V
Digital Terminal voltages	VSS - 0.4V	VDD + 0.4V	V
AIO voltages	VSS - 0.4V	1.9V	V

Table 4: Absolute Maximum Ratings

5.2 Recommended Operating Conditions

	Min	Max	Unit
Storage temperature range	-40	+85	°C
Operating temperature range	-40	+85	°C
VDD_IO	1.7	3.6	V
VDD_BAT	2.7	4.4	V
VDD_CHG	0	6.5	V
Digital Terminal voltages	0	VDD	V
AIO voltages	0	1.5V	V

Table 5: Recommended Operating Conditions

5.3 Digital Terminals

Input/Output Characteristic	Min	Max	Unit
V_{IL} input logic level low	-0.3	0.25 x VDD	V
V_{IL} input logic level high	0.625 x VDD	VDD + 0.3	V
V_{OL} output logic level low, I_{OL} = 4.0mA	0	0.125	V
V_{OL} output logic level high, I_{OL} = -4.0mA	0.75 x VDD	VDD	V
Strong pull-up	-100	-10	µA
Strong pull-down	10	100	µA
Weak pull-up	-5	-0.2	µA
Weak pull-down	0.2	5	µA

Table 6: Digital Terminal Characteristics

5.4 Audio Characteristics

5.4.1 ADC

Parameter	Conditions		Min	Typ	Max	Unit
Resolution	-		-	-	16	Bits
Input Sample Rate, F_{sample}	-		8	-	44.1	kHz
Signal to Noise Ratio, SNR		F_{sample}				
		8kHz	-	79	-	dB
		11.025kHz	-	77	-	dB
		16kHz	-	76	-	dB
		22.050kHz	-	76	-	dB
		32kHz	-	75	-	dB
		44.1kHz	-	75	-	dB
Input full scale at maximum gain (differential)			-	4	-	mV rms
Input full scale at minimum gain (differential)			-	800	-	mV rms
3dB Bandwidth			-	20	-	kHz
Microphone mode input impedance			-	6.0	-	kHz
THD+N @ 30mV rms input			-	0.04	-	%

Table 7: ADC characteristics

5.4.2 DAC

Parameter	Conditions		Min	Typ	Max	Unit
Resolution	-		-	-	16	Bits
Output Sample Rate, F_{sample}	-		8	-	48	kHz
Signal to Noise Ratio, SNR		F_{sample}				
		8kHz	-	95	-	dB
		11.025kHz	-	95	-	dB
		16kHz	-	95	-	dB
		22.050kHz	-	95	-	dB
		32kHz	-	95	-	dB
		44.1kHz	-	95	-	dB
Output Full Voltage Swing (differential)			-	750	-	mV rms
Allowed Load	Resistive		16	-	O.C.	Ω
	Capacitive		-	-	500	pF
THD+N 16Ω Load			-	-	0.1	%
THD+N 100Ω Load			-	-	0.01	%

Table 8: DAC Characteristics

5.4.3 A2DP Codecs

5.4.3.1 SBC

SBC codec is the default codec used for Bluetooth A2DP connections. Any Bluetooth device supporting A2DP audio profile supports SBC codec. SBC was originally design to provide reasonable good audio quality while keeping low computational complexity. SBC does not require high bit rates. Thus it works sufficiently with Bluetooth where the bandwidth and the processing power are limited.

5.4.3.2 aptX®

The aptX is widely used in high quality audio devices. aptX can provide dynamic range up to 120 dB and it has the shortest coding delay (<2ms) than other coding algorithms. Using aptX® the whole system latency can be reduced significantly because unlike SBC, it does not require buffering the audio. SBC reproduces a limited audio band width whereas aptX® encode the entire frequency range of audio.

aptX® is more robust and resilient coding scheme than SBC and thus re-transmits does not occur as with SBC.

Both SBC and aptX® have flat frequency response up to 14 kHz. Up to 14 kHz both algorithms produce good quality audio with very little distortion. At frequencies higher than 14 kHz the benefit of aptX® becomes obvious. SBC exhibits increasing attenuation with increasing frequency but aptX® retains high reproduction quality.

aptX® requires purchasing a license for each Bluetooth address and the license agreement must be done with CSR. The combination of aptX® license and the Bluetooth address is programmed into the module in the module production line.

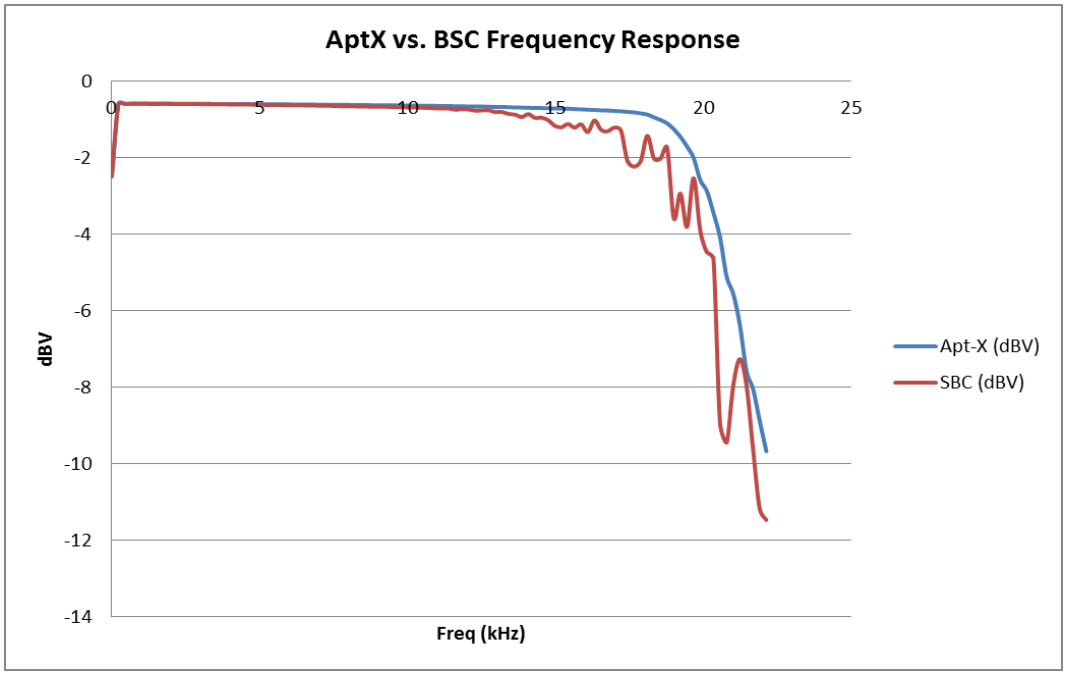


Figure 4: Frequency response of aptX and SBC codecs

5.4.3.3 AAC

AAC (Advanced Audio Coding) achieves better sound quality than MP3 and it is the default audio format for YouTube and iPhone among others. AAC has long latency (>100ms) compared to aptX®. Because of high processing capacity requirement for encoding, WT32i does not support AAC as A2DP source. Thus WT32i can be used for receiving (A2DP sink) AAC (from iPhone for example) but it cannot transmit AAC coded audio.

5.5 RF Characteristics

5.5.1 RF Transceiver

Transceiver characteristic		Min	Typ	Max	Unit
Maximum transmit power		5	6.5	8	dBm
Minimum transmit power			-17		dBm
Transmit power stability over the temperature range			+/- 0.5		dB
Transmit power variation within the BT band				1	dB
Sensitivity DH1	RT		-90		dBm
	-40C		-91		dBm
	+85C		-86		dBm
Sensitivity 3DH5	RT		-83		dBm
	-40C		-84		dBm
	+85C		-80		dBm

Table 9: Transceiver characteristics

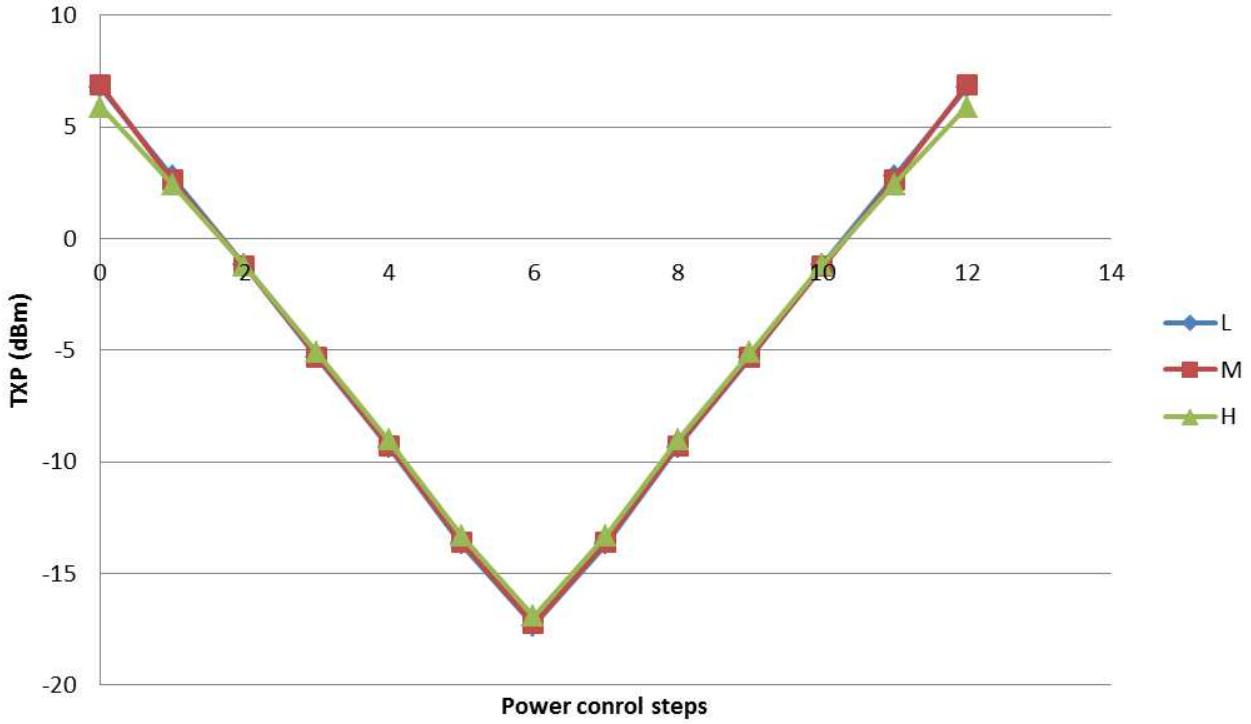


Table 10: Power control of WT32i

Standard	Band / Frequency	Min (AVG / PEAK)	Typ (AVG / PEAK)	Max (AVG / PEAK)	Limit by the Standard (AVG / PEAK)	Unit
FCC part 15 transmitter spurious emissions	2nd harmonic		50 / 61		54 / 74	dBuV/m
	3rd harmonic		< 40 / 50		54 / 74	dBuV/m
	Band edge 2390MHz				54 / 74	dBuV/m
	Band edge 2483.5MHz				54 / 74	dBuV/m
	Band edge 2400MHz (conducted)				-20	dBc
	Band edge 2483.5MHz (conducted)				-20	dBc
ETSI EN 300 328 transmitter spurious emissions	Band edge 2400MHz				-30	dBm
	2nd harmonic		-35		-30	dBm
	3rd harmonic		<-40		-30	dBm
ETSI EN 300 328 receiver spurious emissions	(2400 - 2479) MHz				-47	dBm
	(1600 - 1653) MHz				-47	dBm

Table 11: WT32i-A spurious emissions

Note: All the emissions tested with maximum 8 dBm TX power

5.5.2 Antenna Characteristics

Note: Antenna characteristics may vary depending on the mother board layout. Following characteristics have been measured using DKWT32i

- Antenna efficiency -3.5 dB (45%)
- Peak gain 0 dBi

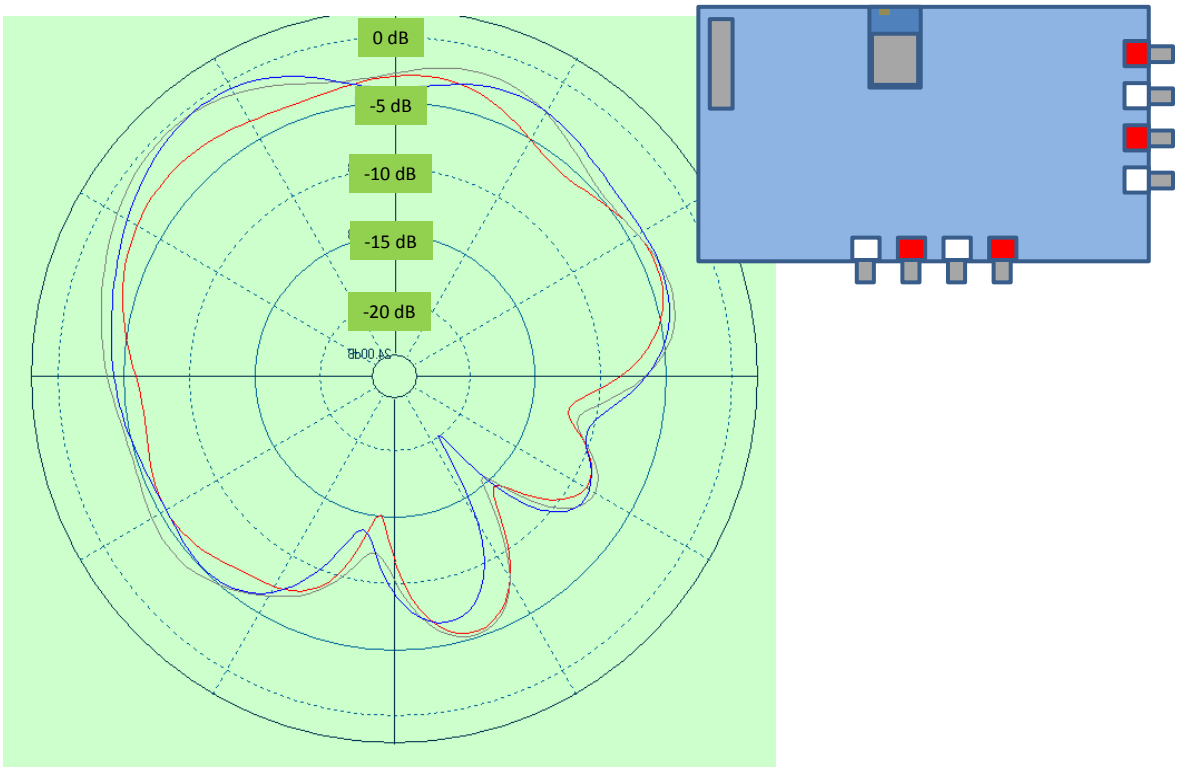


Figure 5: Top view radiation pattern of DKWT32i

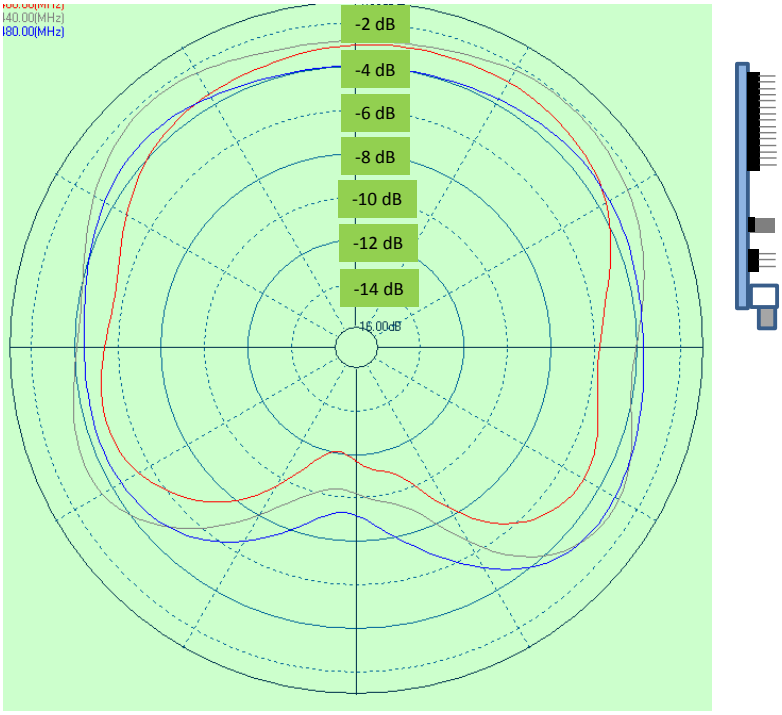


Figure 6: Side view radiation pattern of DKWT32i

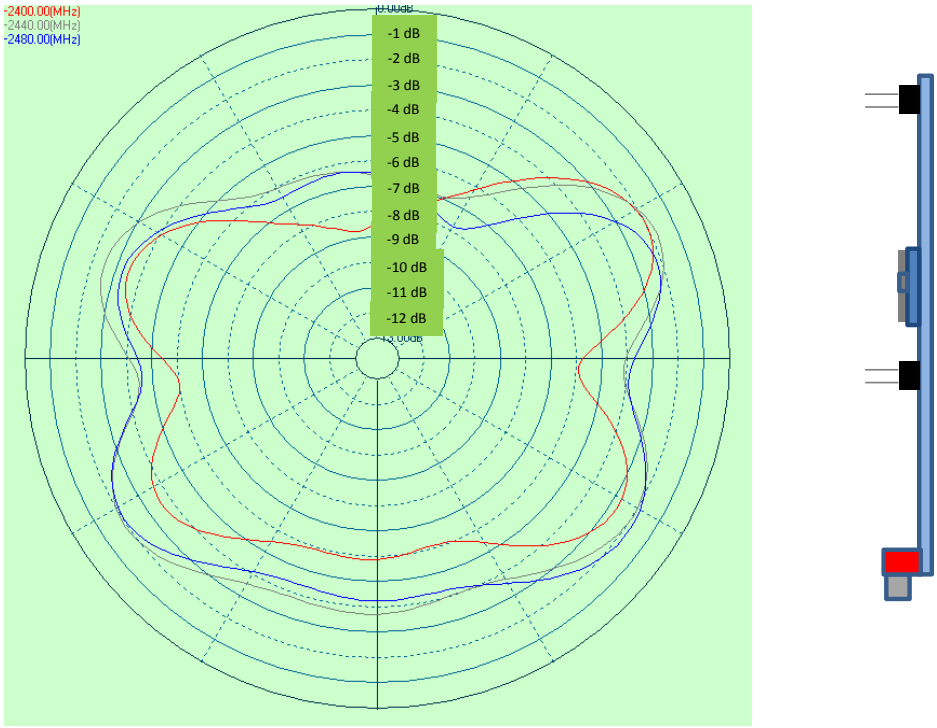


Figure 7: Front view radiation pattern

5.6 Current Consumption

Operation Mode		Peak	Average	Unit
Idle	SET BT PAGEMODE 0 2000 0	12	2.0	mA
	SET BT PAGEMODE 0 2000 1		2.0	
	SET BT PAGEMODE 0 2000 2		2.0	
	SET BT PAGEMODE 1 2000 0	32	2.0	
	SET BT PAGEMODE 1 2000 1		2.1	
	SET BT PAGEMODE 1 2000 2		2.1	
	SET BT PAGEMODE 2 2000 0		23	
	SET BT PAGEMODE 2 2000 1		2.2	
	SET BT PAGEMODE 2 2000 2		2.1	
	SET BT PAGEMODE 3 2000 0		23	
	SET BT PAGEMODE 3 2000 1		2.3	
	SET BT PAGEMODE 3 2000 2		2.2	
	SET BT PAGEMODE 4 2000 0		23	
	SET BT PAGEMODE 4 2000 1		2.3	
	SET BT PAGEMODE 4 2000 2		2.2	
Sleep	SET BT PAGEMODE 0 2000 0	12	0.08	mA
	SET BT PAGEMODE 0 2000 1		0.08	
	SET BT PAGEMODE 0 2000 2		0.08	
	SET BT PAGEMODE 1 2000 0	32	0.18	
	SET BT PAGEMODE 1 2000 1		0.18	
	SET BT PAGEMODE 1 2000 2		0.18	
	SET BT PAGEMODE 2 2000 0		23.5	
	SET BT PAGEMODE 2 2000 1		0.31	
	SET BT PAGEMODE 2 2000 2		0.19	
	SET BT PAGEMODE 3 2000 0		23	
	SET BT PAGEMODE 3 2000 1		0.4	
	SET BT PAGEMODE 3 2000 2		0.29	
	SET BT PAGEMODE 4 2000 0		23	
	SET BT PAGEMODE 4 2000 1		0.4	
	SET BT PAGEMODE 4 2000 2		0.29	
Connected, Sniff disabled	SET BT SNIFF 0 20 1 8		4.7	
Connected + Sniff, Master	SET BT SNIFF 40 20 1 8		3.9	
Connected + Sniff, Master	SET BT SNIFF 1000 20 1 8		2.5	
Connected + Sniff, Slave	SET BT SNIFF 40 20 1 8		3.6	
Connected + Sniff, Slave	SET BT SNIFF 1000 20 1 8		2.5	
A2DP Audio Streaming	A2DP SINK, INTERNAL CODEC	75	28	mA
A2DP Audio Streaming	A2DP SOURCE, INTERNAL CODEC	70	23	

Table 12: Current consumption of WT32i

6 Power Control and Regulation

WT32i contains an internal battery charger and a switch mode regulator that is mainly used for internal blocks of the module. The module can be powered from a single 3.3 V supply provided that VDD_CHG is floating. Alternatively the module can be powered from a battery connected to VDD_BAT and using an external regulator for VDD_IO. 1.8 V to 3.3 V supply voltage for VDD_IO can be used to give desired signal levels for the digital interfaces of the module. USB, however, requires 3.3 V for proper operation and thus, when USB is in use, 3.3 V for VDD_IO is required.

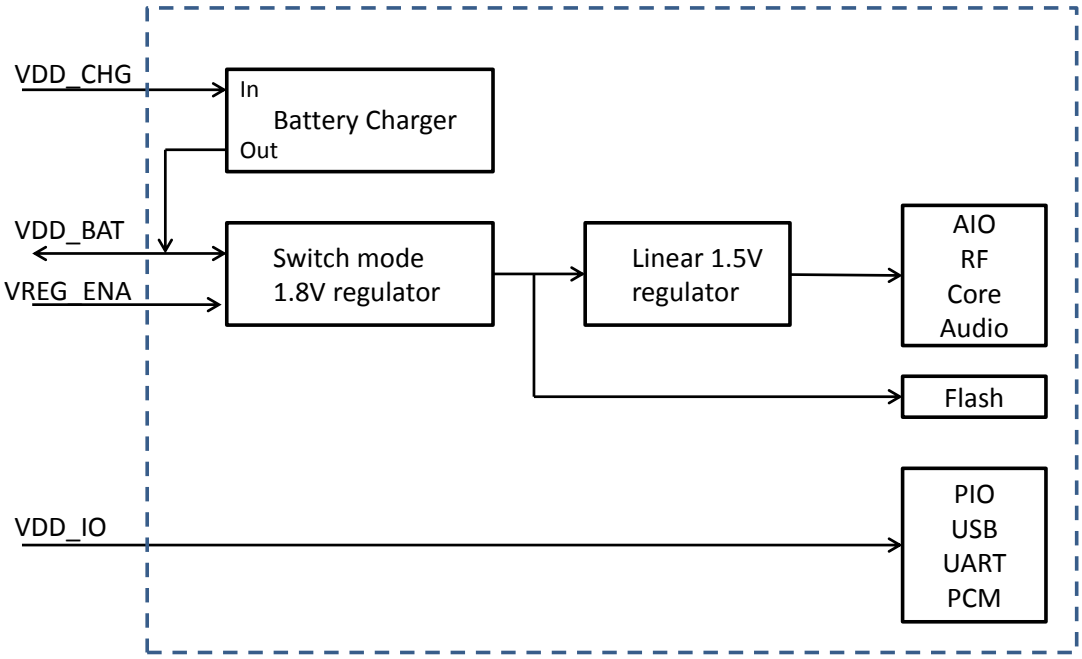


Figure 8: Power supply configuration of WT32i

VDD_ENA is software configurable enable pin for the internal regulators. Using iWRAP the enable pin can be configured to

1. Latch on the internal regulators at the rising edge
2. Turn the regulators on at rising edge and turn off the regulators at falling edge
3. Latch the regulators on at the rising edge and turn off the regulators at the following rising edge

GPIO can be configured to control an external regulator.

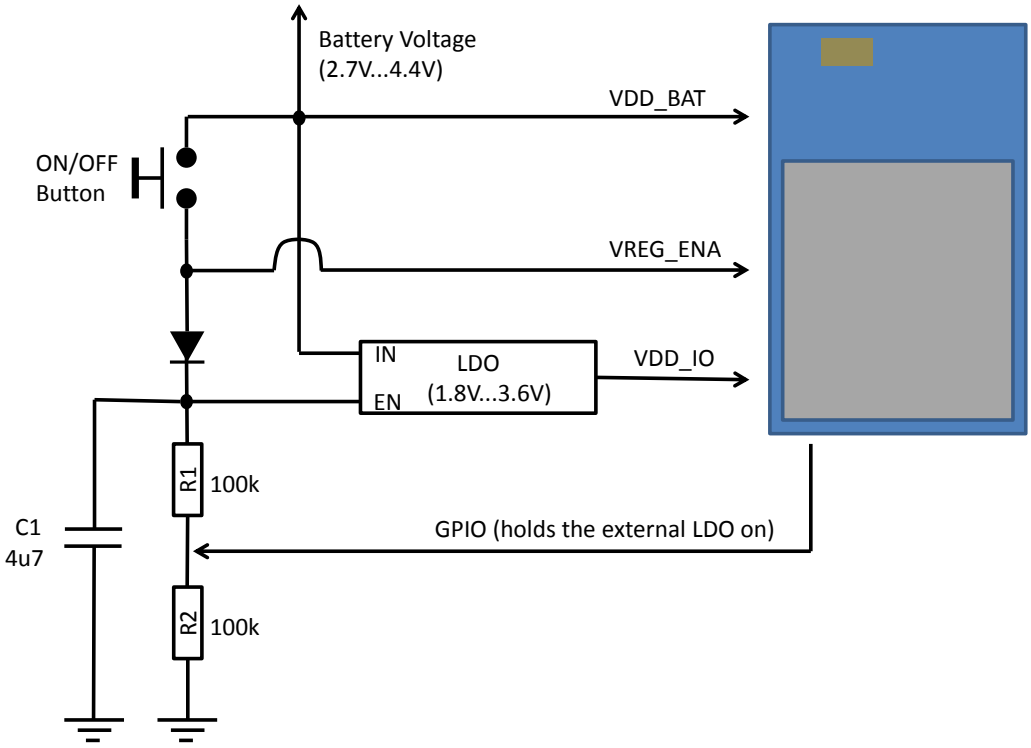


Figure 9: Example of making a power on/off button using the latch feature of the internal regulators

iWRAP Example: *Creating an on/off button with PIO2 holding the external regulator on*

"SET CONTROL VREGEN 2 4"

(PIO is defined with a bit mask. 4 in hexadecimal is 100 in binary corresponding to PIO2)

NOTE: With the configuration shown above, when doing a SW reset for the module C1 will hold the enable pin of the external regulator high until iWRAP has booted. This will prevent the module from turning off during reset. When resetting through the reset pin one has to make sure that the enable pin is held high as long as the reset pin is held active.

Figure 10 shows an example how to arrange power control when on/off button is not implemented. VREG_ENA pin must not be connected to VDD_IO because leakage from VDD_BAT to VDD_IO will prevent VREG_ENA to fall low enough to turn off the internal regulators.

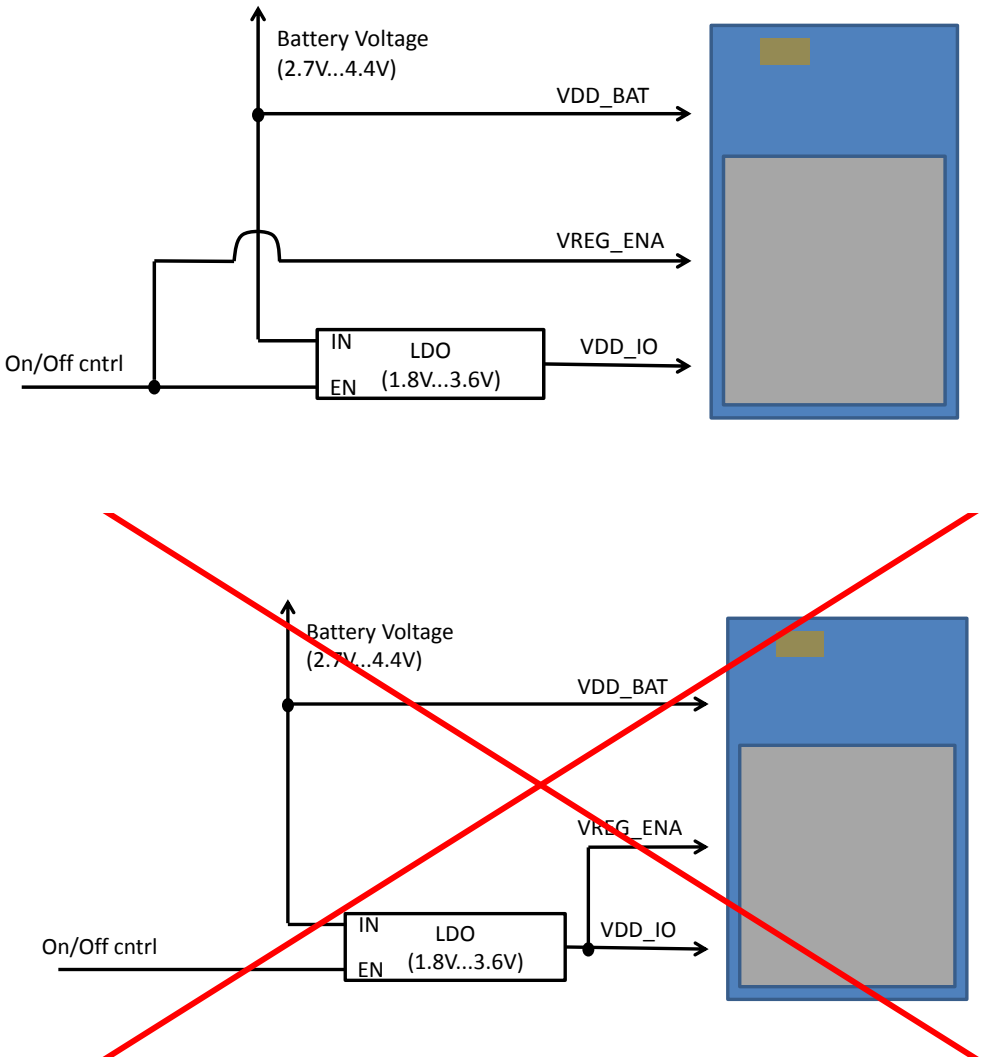


Figure 10: Correct and wrong connection for the power on/off control

6.1 Protecting the Battery by Configuring the Module to Turn Off at Certain Voltage

It is important not to let the battery be drained to voltages below 2.8V. In iWRAP it is possible to define certain level when the module turns off the regulators.

iWRAP Example: *Configure WT32i to start sending low battery warning at 3.4V, turn off at 3.3V and cease the low battery warning at 4.0V. Set PIO0 to indicate low batter*

"SET CONTROL BATTERY 3400 3300 4000 10"

6.2 Reset

WT32i may be reset from several sources: reset pin, power on reset, a UART break character or through software configured watchdog timer.

At reset, the digital I/O pins are set to inputs for bi-directional pins and outputs are tri-state.

The chip status after a reset is as follows:

- Warm Reset: data rate and RAM data remain available
- Cold Reset: data rate and RAM data are not available

Table 13 shows the pin states of WT32i on reset. Pull-up (PU) and pull-down (PD) default to weak values unless specified otherwise.

Pin Name / Group	I/O Type	No Core Voltage Reset	Full Chip Reset
USB	Digital bi-directional	N/A	N/A
UART_RX	Digital input with PD	PD	PD
UART_CTS			
UART_TX	Digital output with PU	PU	PU
UART_RTS			
SPI_MOSI	Digital input with PD	PD	PD
SPI_CLK			
SPI_MISO	Digital tristate output with PD		
SPI_CS	Digital input with PU	PU	PU
PCM_IN	Digital input with PD	PD	PD
PCM_CLK	Digital bi-directional with PD		
PCM_SYNC			
PCM_OUT	Digital tri-state output with PD		
GPIO	Digital bi-directional with PU/PD	PD	PD

Table 13: Pin states on reset

6.2.1 Internal POR

WT32i has two internal POR circuits. One is internally to the BC5 chip. In BC5 the power on reset occurs when the core supply voltage (output of the internal 1.5V regulator) falls below typically 1.26V and is released when VDD_CORE rises above typically 1.31V.

Another POR circuit is embedded to the module and it keeps the module in reset until supply voltages have stabilized. This is to prevent corruption of the internal flash memory during boot. The embedded POR is shown in the figure Figure 2Figure 11.

Because the POR is based on a simple RC time constant it will not work if the supply voltage ramps very slowly or if the reset pin is not connected to high impedance. It is recommended that the power ramp will not take more than 10 msec. If the reset pin is connected to a host it is good to place a diode between the host and the module as shown in Figure 12. A diode will prevent the host from pulling the reset low before the internal flash has its supply stabilized.