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CS8422

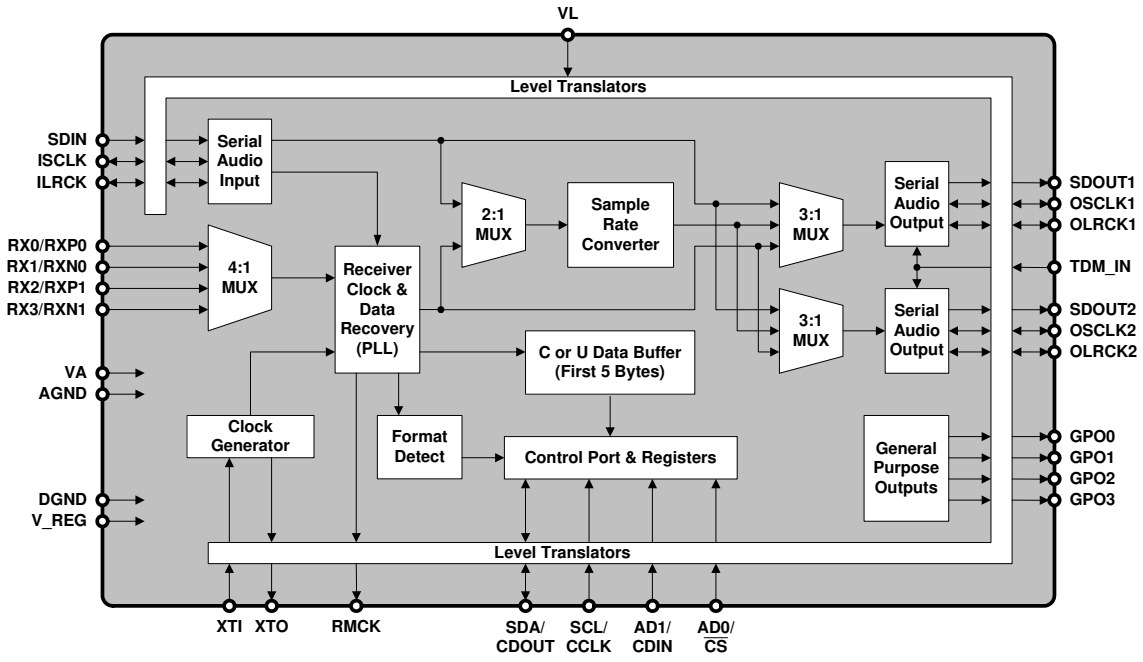
24-bit, 192-kHz, Asynchronous Sample Rate Converter with Integrated Digital Audio Interface Receiver

Sample Rate Converter Features

- 140 dB Dynamic Range
- -120 dB THD+N
- No External Master Clock Required
- Supports Sample Rates up to 211 kHz
- Input/Output Sample Rate Ratios from 6:1 to 1:6
- Master Mode Master Clock/Sample Rate Ratio Support: 64, 96, 128, 192, 256, 384, 512, 768, 1024
- 16, 18, 20, or 24-bit Data I/O
- Dither Automatically Applied and Scaled to Output Resolution
- Multiple Device Outputs are Phase Matched

Digital Audio Interface Receiver Features

- Complete EIAJ CP1201, IEC-60958, AES3, S/PDIF Compatible Receiver
- 28 kHz to 216 kHz Sample Rate Range
- 2:1 Differential AES3 or 4:1 S/PDIF Input Mux
- De-emphasis Filtering for 32 kHz, 44.1 kHz, and 48 kHz
- Recovered Master Clock Output: 64 x Fs, 96 x Fs, 128 x Fs, 192 x Fs, 256 x Fs, 384 x Fs, 512 x Fs, 768 x Fs, 1024 x Fs
- 49.152 MHz Maximum Recovered Master Clock Frequency
- Ultralow-jitter Clock Recovery
- High Input Jitter Tolerance
- No External PLL Filter Components Required
- Selectable and Automatic Clock Switching
- AES3 Direct Output and AES3 TX Pass-through
- On-chip Channel Status Data Buffering
- Automatic Detection of Compressed Audio Streams
- Decodes CD Q Sub-Code



System Features

- SPI™ or I²C™ Software Mode and Stand-Alone Hardware Mode
- Flexible 3-wire Digital Serial Audio Input Port
- Dual Serial Audio Output Ports with Independently Selectable Data Paths
- Master or Slave Mode Operation for all Serial Audio Ports
- Time Division Multiplexing (TDM) Mode
- Integrated Oscillator for use with External Crystal
- Four General-purpose Output Pins (GPO)
- +3.3 V Analog Supply (VA)
- +1.8 V to 5.0 V Digital Interface (VL)
- Space-saving 32-pin QFN Package

General Description

The CS8422 is a 24-bit, high-performance, monolithic CMOS stereo asynchronous sample rate converter with an integrated digital audio interface receiver that decodes audio data according to the EIAJ CP1201, IEC-60958, AES3, and S/PDIF interface standards.

Audio data is input through the digital interface receiver or a 3-wire serial audio input port. Audio is output through one of two 3-wire serial audio output ports. Serial audio data outputs can be set to 24, 20, 18, or 16-bit word-lengths. Data into the digital interface receiver and serial audio input port can be up to 24-bits long. Input and output data can be completely asynchronous, synchronous to an external clock through XTI, or synchronous to the recovered master clock.

The CS8422 can be controlled through the control port in Software Mode or in a Stand-Alone Hardware Mode. In Software Mode, the user can control the device through an SPI or I²C control port.

Target applications include digital recording systems (DVD-R/RW, CD-R/RW, PVR, DAT, MD, and VTR), digital mixing consoles, high-quality D/A, effects processors, and computer audio systems.

The CS8422 is available in a space-saving QFN package in Commercial (-40° C to +85° C) grade. The CDB4822 is also available for device evaluation and implementation suggestions. Please refer to "Ordering Information" on page 81 for complete details.

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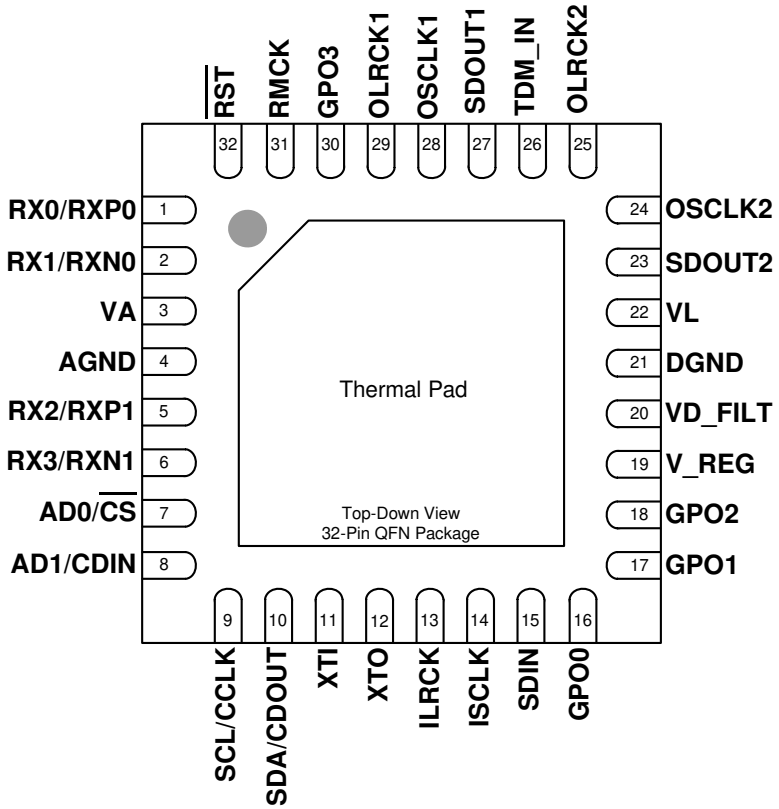
1. PIN DESCRIPTION

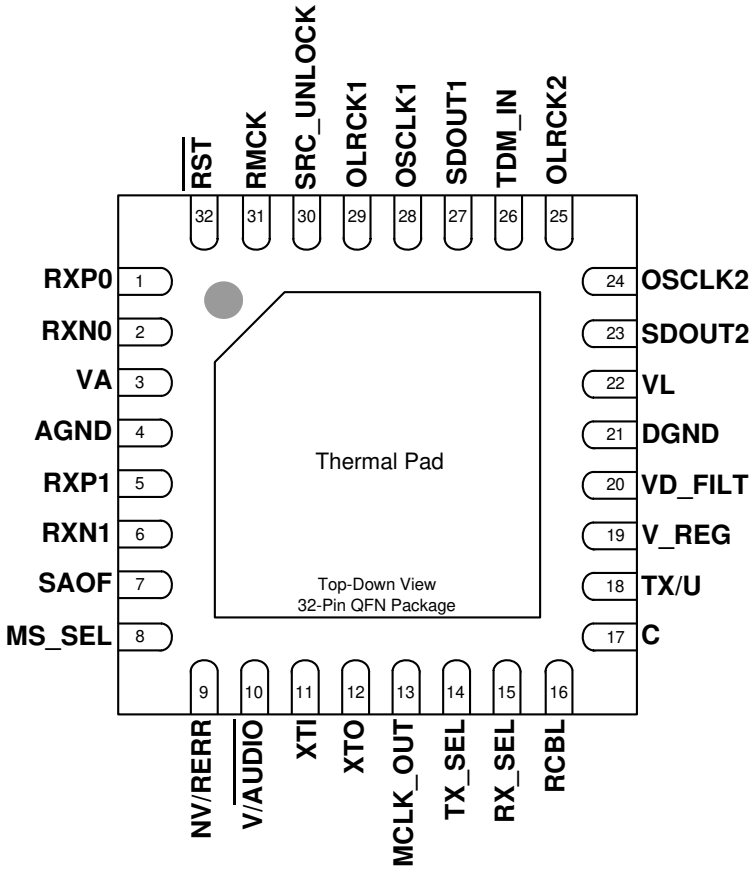
1.1 Software Mode



Pin Name	Pin #	Pin Description
RX[3:0], RXP/RXN[1:0]	1 2 5 6	**AES3/SPDIF Input** *(Input)* - Single-ended or differential receiver inputs carrying AES3 or S/PDIF encoded digital data. RX[3:0] comprise the single-ended input multiplexer. RXP[1:0] comprise the non-inverting inputs of the differential input multiplexer and RXN[1:0] comprise the inverting inputs of the differential input multiplexer. Unused inputs should be tied to AGND/DGND.
VA	3	**Analog Power** *(Input)* - Analog power supply, nominally +3.3 V. Care should be taken to ensure that this supply is as noise-free as possible, as noise on this pin will directly affect the jitter performance of the recovered clock.
AGND	4	**Analog Ground** *(Input)* - Ground for the analog circuitry in the chip. AGND and DGND should be connected to a common ground area under the chip.
AD0/$\overline{CS}$	7	**Address Bit 0 (I²C) / Software Chip Select (SPI)** *(Input)* - A falling edge on this pin puts the CS8422 into SPI Control Port Mode. With no falling edge, the CS8422 defaults to I²C Mode. In I²C Mode, AD0 is a chip address pin. In SPI Mode, $\overline{CS}$ is used to enable the control port interface on the CS8422. See "Control Port Description" on page 43.
AD1/CDIN	8	**Address Bit 1 (I²C) / Serial Control Data in (SPI)** *(Input)* - In I²C Mode, AD1 is a chip address pin. In SPI Mode, CDIN is the input data line to the control port interface. See "Control Port Description" on page 43.
SCL/CCLK	9	**Software Clock** *(Input)* - Serial control interface clock used to clock control data bits into and out of the CS8422.
SDA/CDOUT	10	**Serial Control Data I/O (I²C) / Data Out (SPI)** *(Input/Output)* - In I²C Mode, SDA is the control I/O data line. In SPI Mode, CDOUT is the output data from the control port interface on the CS8422.

Pin Name	Pin #	Pin Description
XTI	11	**Crystal/Oscillator In** *(Input)* - Crystal or digital clock input for Master clock. See "SRC Master Clock" on page 38 for more details.
XTO	12	**Crystal Out** *(Output)* - Crystal output for Master clock. See "SRC Master Clock" on page 38 for more details.
ILRCK	13	**Serial Audio Input Left/Right Clock** (*Input*/*Output*) - Word rate clock for the audio data on the SDIN pin.
ISCLK	14	**Serial Audio Input Bit Clock** (*Input*/*Output*) - Serial bit clock for audio data on the SDIN pin.
SDIN	15	**Serial Audio Input Data Port** (*Input*) - Audio data serial input pin.
GPO[3:0]	16 17 18 30	**General Purpose Outputs** *(Output)* - See page 51 for details. In I²C Mode, a 20 kΩ pull-up resistor to VL on GPO2 will set AD2 chip address bit to 1, otherwise AD2 will be 0.
V_REG	19	**Voltage Regulator In** (*Input*) - Regulator power supply input, nominally +3.3 V.
VD_FILT	20	**Digital Voltage Regulator** *(Output)* - Digital core voltage regulator output. Should be connected to digital ground through a 10 µF capacitor. Typically +2.5 V. Cannot be used as an external voltage source.
DGND	21	**Digital & I/O Ground** *(Input)* - Ground for the I/O and core logic. AGND and DGND should be connected to a common ground area under the chip.
VL	22	**Logic Power** (*Input*) - Input/Output power supply, typically +1.8 V, +2.5 V, +3.3 V, or +5.0 V.
SDOUT2	23	**Serial Audio Output 2 Data Port** *(Output)* - Audio data serial output 2 pin.
OSCLK2	24	**Serial Audio Output 2 Bit Clock** *(Input/Output)* - Serial bit clock for audio data on the SDOUT2 pin.
OLRCK2	25	**Serial Audio Output 2 Left/Right Clock** (*Input*/*Output*) - Word rate clock for the audio data on the SDOUT2 pin.
TDM_IN	26	**Serial Audio Output TDM Input** (*Input*) - Time Division Multiplexing serial audio data input. Should remain grounded when not used. See "Time Division Multiplexing (TDM) Mode" on page 27.
SDOUT1	27	**Serial Audio Output 1 Data Port** (*Output*) - Audio data serial output 1 pin.
OSCLK1	28	**Serial Audio Output 1 Bit Clock** (*Input*/*Output*) - Serial bit clock for audio data on the SDOUT 1 pin.
OLRCK1	29	**Serial Audio Output 1 Left/Right Clock** (*Input*/*Output*) - Word rate clock for the audio data on the SDOUT 1 pin.
RMCK	31	**Recovered Master Clock** *(Output)* - Recovered master clock from the PLL. Frequency is 128x, 192x, 256x, 384x, 512x, 768x, or 1024x Fs, where Fs is the sample rate of the incoming AES3-compatible data, or ISCLK/64.
$\overline{\text{RST}}$	32	**Reset** *(Input)* - When $\overline{\text{RST}}$ is low the CS8422 enters a low power mode and all internal states are reset. On initial power up $\overline{\text{RST}}$ must be held low until the power supply is stable and all input clocks are stable in frequency and phase.
THERMAL PAD	-	**Thermal Pad** - Thermal relief pad. Should be connected to the ground plane for optimized heat dissipation.

1.2 Hardware Mode



Pin Name	Pin #	Pin Description
RXP/RXN[1:0]	1 2 5 6	**AES3/SPDIF Input** *(Input)* - Differential receiver inputs carrying AES3 or S/PDIF encoded digital data. RXP[1:0] comprise the non-inverting inputs of the differential input multiplexer; and RXN[1:0] comprise the inverting inputs of the input multiplexer. Unused inputs should be tied to AGND.
VA	3	**Analog Power** *(Input)* - Analog power supply, nominally +3.3 V. Care should be taken to ensure that this supply is as noise-free as possible, as noise on this pin will directly affect the jitter performance of the recovered clock.
AGND	4	**Analog Ground** *(Input)* - Ground for the analog circuitry in the chip. AGND and DGND should be connected to a common ground area under the chip.
SAOF	7	**Serial Audio Output Format Select** *(Input)* - Used to select the serial audio output format after $\overline{\text{RST}}$ is released. See Table 4 on page 42 for format settings.
MS_SEL	8	**Master/Slave Select** *(Input)* - Used to select Master or Slave settings for the output serial audio ports after $\overline{\text{RST}}$ is released. See Table 5 on page 42 for format settings.
NV/RERR	9	**Non-Validity Receiver Error/Receiver Error** *(Output)* - Receiver error indicator. NVERR is output by default, RERR is selected by a 20 kΩ resistor to VL.
V/$\overline{\text{AUDIO}}$	10	**Validity Data/AUDIO** (*Output*) - If a 20 kΩ pull-down is present on this pin, it will output serial Validity data from the AES3 receiver, clocked by the rising and falling edges of OLRCK2 in master mode. If a 20 kΩ pull-up is present, the pin will be low when valid linear PCM data is present at the AES3 input.
XTI	11	**Crystal/Oscillator In** *(Input)* - Crystal or digital clock input for Master clock. See "SRC Master Clock" on page 38.
XTO	12	**Crystal Out** *(Output)* - Crystal output for Master clock. See "SRC Master Clock" on page 38.

Pin Name	Pin #	Pin Description
MCLK_OUT	13	**Buffered MCLK** *(Output)* **-** Buffered output of XTI clock. If a 20 kΩ pull-up resistor to VL is present on this pin, the SRC MCLK source will be the PLL clock, otherwise it will be the ring oscillator.
TX_SEL	14	**TX Pin MUX Selection** *(Input)* - Used to select the AES3-compatible receiver input for pass-through to the TX pin.
RX_SEL	15	**Receiver MUX Selection** *(Input)* - Used to select the active AES3-compatible receiver input.
RCBL	16	**Receiver Channel Status Block** *(Output)* -Indicates the beginning of a received channel status block. Will go high for one subframe during each Z preamble following the first detected Z preamble. If no Z preamble is detected, output is indeterminate. See Figure 19 on page 36 for more detail.
C	17	**Channel Status Data** (*Output*) - Serial channel status data output from the AES3-compatible receiver, clocked by the rising and falling edges of OLRCK2 in master mode. A 20 kΩ pull-up resistor to VL must be present on this pin to put the part in Hardware Mode.
TX/U	18	**Receiver MUX Pass-through/User Data** (*Output*) - If no 20 kΩ pull-up resistor is present on this pin it will output a copy of the receiver mux input selected by the TX_SEL pin. If a 20 kΩ pull-up resistor to VL is present on this pin, it will output serial User data from the AES3 receiver, clocked by the rising and falling edges of OLRCK2 in master mode.
V_REG	19	**Voltage Regulator In** (*Input*) - Regulator power supply input, nominally +3.3 V.
VD_FILT	20	**Digital Voltage Regulator Out** *(Output)* - Digital core voltage regulator output. Should be connected to digital ground through a 10 µF capacitor. Cannot be used as an external voltage source.
DGND	21	**Digital & I/O Ground** *(Input)* - Ground for the I/O and core logic. AGND and DGND should be connected to a common ground area under the chip.
VL	22	**Logic Power** (*Input*) - Input/Output power supply, typically +1.8 V, +2.5 V, +3.3 V, or +5.0 V.
SDOUT2	23	**Serial Audio Output 2 Data Port** *(Output)* - Audio data serial output 2 pin.
OSCLK2	24	**Serial Audio Output 2 Bit Clock** *(Input/Output)* - Serial bit clock for audio data on the SDOUT2 pin.
OLRCK2	25	**Serial Audio Output 2 Left/Right Clock** *(Input/Output)* - Word rate clock for the audio data on the SDOUT2 pin.
TDM_IN	26	**Serial Audio Output 1 TDM Input** *(Input)* - Time Division Multiplexing serial audio data input. Grounded when not used. See "Time Division Multiplexing (TDM) Mode" on page 27 for details.
SDOUT1	27	**Serial Audio Output 1 Data Port** *(Output)* - Audio data serial output 1 pin. A 20 kΩ pull-up to VL present on this pin will disable de-emphasis auto detect.
OSCLK1	28	**Serial Audio Output 1 Bit Clock** *(Input/Output)* - Serial bit clock for audio data on the SDOUT1 pin.
OLRCK1	29	**Serial Audio Output 1 Left/Right Clock** *(Input/Output)* - Word rate clock for the audio data on the SDOUT1 pin.
SRC_UNLOCK	30	**SRC Unlock Indicator** (*Output*) - Indicates when the SRC is unlocked. See "SRC Locking" on page 37 for more details.
RMCK	31	**Recovered Master Clock** *(Output)* **-** Recovered master clock from the PLL. Frequency is 128 x, 256 x, or 512 x Fs, where Fs is the sample rate of the incoming AES3-compatible data or ISCLK/64. If a 20 kΩ pull-up to VL is present on this pin, the SDOUT1 MCLK source will be RMCK, otherwise it will be the clock input through XTI-XTO.
$\overline{\text{RST}}$	32	**Reset** *(Input)* - When $\overline{\text{RST}}$ is low the CS8422 enters a low power mode and all internal states are reset. On initial power up $\overline{\text{RST}}$ must be held low until the power supply is stable and all input clocks are stable in frequency and phase.
THERMAL PAD	-	**Thermal Pad** - Thermal relief pad. Should be connected to the ground plane for optimized heat dissipation.

2. CHARACTERISTICS AND SPECIFICATIONS

(All Min/Max characteristics and specifications are guaranteed over the Specified Operating Conditions. Typical performance characteristics and specifications are derived from measurements taken at nominal supply voltages and T_A = 25° C.)

RECOMMENDED OPERATING CONDITIONS

GND = 0 V, all voltages with respect to 0 V.

Parameter	Symbol	Min	Nominal	Max	Units
Power Supply Voltage	VL VA V_REG	1.71 3.135 3.135	3.3 3.30 3.30	5.25 3.465 3.465	V V V
Ambient Operating Temperature: Commercial Grade	T_A	-40	-	+85	°C

ABSOLUTE MAXIMUM RATINGS

DGND = AGND = 0 V; all voltages with respect to 0 V. Operation beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

Parameter	Symbol	Min	Max	Units
Power Supply Voltage	VL VA V_REG	-0.3 -0.3 -0.3	6.0 4.3 4.3	V V V
Input Current, Any Pin Except Supplies (Note 1)	I_{in}	-	±10	mA
Input Voltage, Any Pin Except RXP[1:0], RXN[1:0], or RX[3:0]	V_{in}	-0.3	VL+0.4	V
Input Voltage, RXP[1:0], RXN[1:0], or RX[3:0]	V_{in}	-0.3	VA+0.4	V
Ambient Operating Temperature (power applied)	T_A	-55	+125	°C
Storage Temperature	T_{stg}	-65	+150	°C

Notes:

1. Transient currents of up to 100 mA will not cause SCR latch-up.

PERFORMANCE SPECIFICATIONS - SAMPLE RATE CONVERTER

XTI-XTO = 24.576 MHz; Input signal = 1.000 kHz, Measurement Bandwidth = 20 to Fso/2 Hz, and Word Width = 24-Bits. (Note 2)

Parameter	Min	Typ	Max	Units
Resolution	16	-	24	bits
Sample Rate Slave Master	XTI/2048 XTI/512	- -	XTI/128 XTI/128	kHz kHz
Sample Rate Ratio - Upsampling	-	-	1:6	Fsi:Fso
Sample Rate Ratio - Downsampling	-	-	6:1	Fsi:Fso
Interchannel Gain Mismatch	-	0.0	-	dB
Interchannel Phase Deviation	-	0.0	-	Degrees
Gain Error	-0.2	-	0	dB
Peak Idle Channel Noise Component	-	-	-144	dBFS
Dynamic Range - Unweighted (20 Hz to Fso/2, -60 dBFS Input)				
32 kHz:48 kHz	-	140	-	dB
44.1 kHz:48 kHz	-	141	-	dB
44.1 kHz:192 kHz	-	138	-	dB
48 kHz:44.1 kHz	-	140	-	dB
48 kHz:96 kHz	-	141	-	dB
96 kHz:48 kHz	-	140	-	dB
192 kHz:32 kHz	-	141	-	dB
Total Harmonic Distortion + Noise (20 Hz to Fso/2, 0 dBFS Input)				
32 kHz:48 kHz	-	-134	-	dB
44.1 kHz:48 kHz	-	-134	-	dB
44.1 kHz:192 kHz	-	-133	-	dB
48 kHz:44.1 kHz	-	-131	-	dB
48 kHz:96 kHz	-	-135	-	dB
96 kHz:48 kHz	-	-136	-	dB
192 kHz:32 kHz	-	-137	-	dB

Notes:

2. Fsi indicates the input sample rate. Fso indicates the output sample rate. Numbers separated by a colon indicate the ratio of Fsi to Fso.

DIGITAL FILTER CHARACTERISTICS

Parameter	Min	Typ	Max	Units
Passband (Upsampling or Downsampling)	-	-	0.4535* min(Fsi,Fso)	Fs
Passband Ripple	-	-	± 0.05	dB
Stopband (Downsampling)	0.5465*Fso	-	-	Fs
Stopband Attenuation	125	-	-	dB
Group Delay	See “Group Delay” on page 70			

DC ELECTRICAL CHARACTERISTICS

AGND = DGND = 0 V; all voltages with respect to 0 V.

Parameter		Min	Typ	Max	Units
Power-Down Mode (Note 3)					
Supply Current in power down	VA	-	4.7	-	µA
	V_REG	-	1	-	µA
	VL = 1.8 V	-	0.3	-	µA
	VL = 2.5 V	-	7.1	-	µA
	VL = 3.3 V	-	16.9	-	µA
	VL = 5.0 V	-	102.6	-	µA
Normal Operation (Note 4)					
Supply Current at 48 kHz Fsi and Fso	VA	-	18.8	-	mA
	V_REG	-	15.2	-	mA
	VL = 1.8 V	-	2.7	-	mA
	VL = 2.5 V	-	3.8	-	mA
	VL = 3.3 V	-	5.2	-	mA
	VL = 5.0 V	-	5.3	-	mA
Supply Current at 192 kHz Fsi and Fso	VA	-	18.9	-	mA
	V_REG	-	32.4	-	mA
	VL = 1.8 V	-	6.2	-	mA
	VL = 2.5 V	-	8.8	-	mA
	VL = 3.3 V	-	12	-	mA
	VL = 5.0 V	-	18	-	mA

Notes:

3. Power-Down Mode is defined as $\overline{\text{RST}}$ = LOW with all clocks and data lines held static and no crystal attached across XTI - XTO.
4. Normal operation is defined as $\overline{\text{RST}}$ = HIGH. The typical values shown were measured with the digital interface receiver in differential mode, serial audio output port 1 in master mode sourced by the SRC, and serial audio output port 2 in master mode sourced by the AES3 receiver output.

DIGITAL INTERFACE SPECIFICATIONS

AGND = DGND = 0 V; all voltages with respect to 0 V.

Parameter	Symbol	Min	Typ	Max	Units
Input Leakage Current (Note 5)	I_{in}	-	-	+32	µA
Input Capacitance	I_{in}	-	8	-	pF
Digital Interface Receiver - RXP[1:0], RXN[1:0], RX[3:0]					
Differential Input Sensitivity, RXP to RXN (Note 6)		-	-	200	mVpp
Differential Input Impedance, RXP and RXN to GND		-	11	-	kΩ
Single-Ended Input Sensitivity, RX pins, Receiver Input Mode 1 (Note 6)		-	-	200	mVpp
Single-Ended Input Impedance, RX pins, Receiver Input Mode 1		-	11	-	kΩ
High-Level Input Voltage, RX pins in Digital mode	V_{IH}	0.55xVA	-	VA+0.3	V
Low-Level Input Voltage, RX pins in Digital mode	V_{IL}	-0.3	-	0.8	V
Digital I/O					
High-Level Output Voltage (I_{OH} = -4 mA)	V_{OH}	.77xVL	-	-	V
Low-Level Output Voltage (I_{OL} = 4 mA)	V_{OL}	-	-	0.6	V
High-Level Input Voltage	V_{IH}	0.65xVL	-	-	V
Low-Level Input Voltage	V_{IL}	-	-	0.3xVL	V
Input Hysteresis		-	0.2	-	V

Notes:

5. When a digital signal is sent to the AES RX pins, the pins will draw approximately 730 µA from the digital signal's supply from the time $\overline{RST}$ is released until the RX_MODE, RX_SEL, and INPUT_TYPE bits in register 03h are properly configured to allow a digital input signal on the driven pins, see Section 11.3 on page 49.
6. Maximum sensitivity in accordance with AES3-2003 section 8.3.3. Measured with eye diagram height at the specified voltage and width of at least 50% of one-half the biphase symbol period.

SWITCHING SPECIFICATIONS

Inputs: Logic 0 = 0 V, Logic 1 = VL; C_L = 20 pF.

Parameter	Symbol	Min	Typ	Max	Units
$\overline{\text{RST}}$ pin Low Pulse Width (Note 7)		1	-	-	ms
PLL Clock Recovery Sample Rate Range (Note 8)		28	-	216	kHz
RMCK Output Jitter (Note 9) Differential RX Mode		-	200	-	ps RMS
Single-Ended RX Mode		-	475	-	ps RMS
XTI Frequency Crystal		12	-	27.000	MHz
Digital Clock Source		1.024	-	49.152	MHz
XTI Pulse Width High/Low		9	-	-	ns
VL = 3.3 V, 5 V					
RMCK/MCLK_OUT Output Frequency		-	-	49.152	MHz
RMCK/MCLK_OUT Output Duty Cycle		45	50	55	%
Slave Mode					
ISCLK Frequency		-	-	49.152	MHz
ISCLK High Time	t_{sckh}	9.2	-	-	ns
ISCLK Low Time	t_{sckl}	9.2	-	-	ns
OSCLK Frequency		-	-	26.9	MHz
OSCLK High Time	t_{sckh}	16.7	-	-	ns
OSCLK Low Time	t_{sckl}	16.7	-	-	ns
I/OLRCK Edge to I/OSCLK Rising Edge	t_{lcks}	5.7	-	-	ns
I/OSCLK Rising Edge to I/OLRCK Edge	t_{lckd}	4.2	-	-	ns
OSCLK Falling Edge/OLRCK Edge to SDOUT Output Valid	t_{dpd}	-	-	15	ns
SDIN/TDM_IN Setup Time Before I/OSCLK Rising Edge	t_{ds}	3.6	-	-	ns
SDIN/TDM_IN Hold Time After I/OSCLK Rising Edge	t_{dh}	5.5	-	-	ns
TDM Mode OLRCK High Time (Note 10)	t_{lrckh}	20	-	-	ns
TDM Mode OLRCK Rising Edge to OSCLK Rising Edge	t_{fss}	5.3	-	-	ns
TDM Mode OSCLK Rising Edge to OLRCK Falling Edge	t_{fsh}	4.2	-	-	ns
Master Mode (Note 11)					
I/OSCLK Frequency (non-TDM Mode)		48*Fsi/o	-	128*Fsi/o	MHz
I/OLRCK Duty Cycle		49.5	-	50.5	%
I/OSCLK Duty Cycle		45	-	55	%
I/OSCLK Falling Edge to I/OLRCK Edge	t_{lcks}	-	-	4.2	ns
OSCLK Falling Edge to SDOUT Output Valid	t_{dpd}	-	-	4.6	ns
SDIN Setup Time Before I/OSCLK Rising Edge	t_{ds}	2.7	-	-	ns
SDIN Hold Time After I/OSCLK Rising Edge	t_{dh}	5.5	-	-	ns
TDM Mode OSCLK Frequency (Note 12)		-	-	49.152	MHz

Parameter	Symbol	Min	Typ	Max	Units
TDM Mode OSCLK Falling Edge to OLRCK Edge	t_{fsm}	-	-	4.2	ns
VL = 1.8 V, 2.5 V					
RMCK/MCLK_OUT Output Frequency (VL = 1.8 V)		-	-	13.5	MHz
RMCK/MCLK_OUT Output Frequency (VL = 2.5 V)		-	-	31	MHz
RMCK/MCLK_OUT Output Duty Cycle (VL = 1.8 V)		37	50	63	%
RMCK/MCLK_OUT Output Duty Cycle (VL = 2.5 V)		45	50	55	%
Slave Mode					
ISCLK Frequency		-	-	49.152	MHz
ISCLK High Time	t_{sckh}	9.2	-	-	ns
ISCLK Low Time	t_{sckl}	9.2	-	-	ns
OSCLK Frequency		-	-	15.7	MHz
OSCLK High Time	t_{sckh}	28.7	-	-	ns
OSCLK Low Time	t_{sckl}	28.7	-	-	ns
I/OLRCK Edge to I/OSCLK Rising Edge	t_{lcks}	7.4	-	-	ns
I/OSCLK Rising Edge to I/OLRCK Edge	t_{lckd}	6.2	-	-	ns
OSCLK Falling Edge/OLRCK Edge to SDOUT Output Valid	t_{dpd}	-	-	29.5	ns
SDIN/TDM_IN Setup Time Before I/OSCLK Rising Edge	t_{ds}	4.7	-	-	ns
SDIN/TDM_IN Hold Time After I/OSCLK Rising Edge	t_{dh}	7.3	-	-	ns
TDM Mode OLRCK High Time (Note 10)	t_{lrckh}	20	-	-	ns
TDM Mode OLRCK Rising Edge to OSCLK Rising Edge	t_{fss}	7.0	-	-	ns
TDM Mode OSCLK Rising Edge to OLRCK Falling Edge	t_{fsh}	6.2	-	-	ns
Master Mode (Note 11)					
I/OSCLK Frequency (non-TDM Mode)		48*Fsi/o	-	128*Fsi/o	MHz
I/OLRCK Duty Cycle		45	-	55	%
I/OSCLK Duty Cycle		45	-	55	%
I/OSCLK Falling Edge to I/OLRCK Edge	t_{lcks}	-	-	5.7	ns
OSCLK Falling Edge to SDOUT Output Valid (VL = 1.8 V)	t_{dpd}	-	-	11.2	ns
OSCLK Falling Edge to SDOUT Output Valid (VL = 2.5 V)	t_{dpd}	-	-	6.4	ns
SDIN Setup Time Before I/OSCLK Rising Edge	t_{ds}	4.7	-	-	ns
SDIN Hold Time After I/OSCLK Rising Edge	t_{dh}	7.3	-	-	ns
TDM Mode OSCLK Frequency (Note 12)		-	-	31	MHz
TDM Mode OSCLK Falling Edge to OLRCK Edge (VL = 1.8V)	t_{fsm}	-	-	9.6	ns
TDM Mode OSCLK Falling Edge to OLRCK Edge (VL = 2.5V)	t_{fsm}	-	-	5.7	ns

Notes:

7. After powering up the CS8422, $\overline{RST}$ should be held low until the power supplies and clocks are settled.
8. If ISCLK is selected as the clock source for the PLL, then the Sample Rate = ISCLK/64.

9. Typical base band jitter in accordance with AES-12id-2006 section 3.4.2. Measurements are Time Interval Error (TIE) taken with 3rd order 100 Hz to 40 kHz band-pass filter. Measured with Sample Rate = 48 kHz.
10. OLRCK must remain high for at least 1 OSCLK period and at most 255 OSCLK periods in TDM Mode.
11. In TDM formatted master mode, the TDM_IN pin is not supported.
12. In TDM formatted master mode, the OSCLK frequency is fixed at 256*OLRCK.

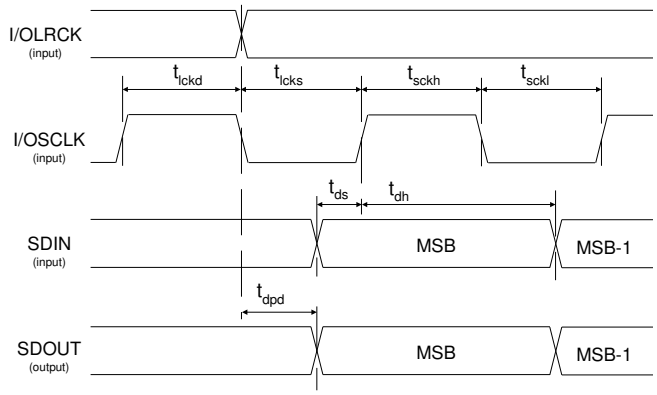


Figure 1. Non-TDM Slave Mode Timing

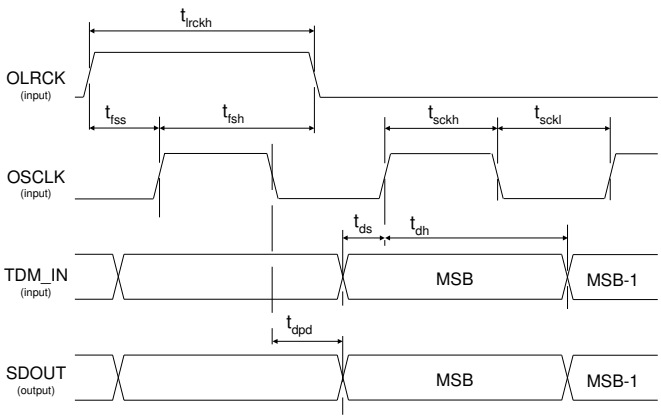


Figure 2. TDM Slave Mode Timing

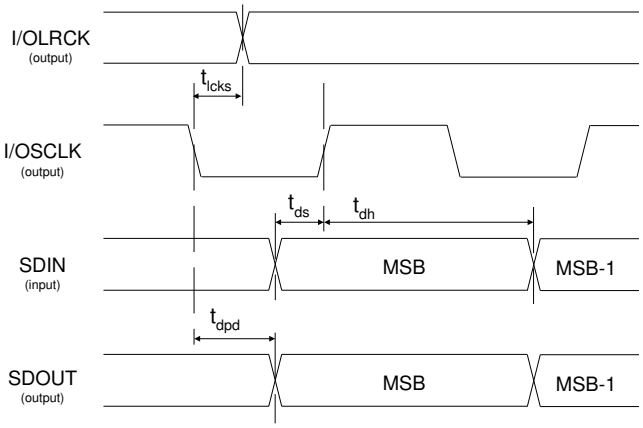


Figure 3. Non-TDM Master Mode Timing

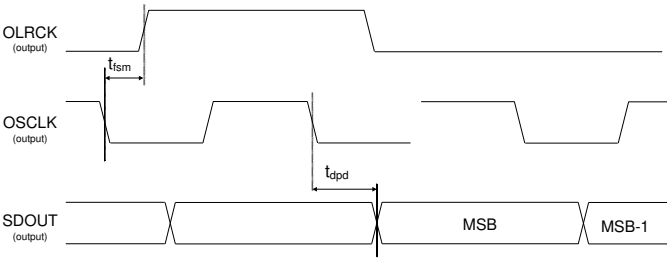


Figure 4. TDM Master Mode Timing

SWITCHING CHARACTERISTICS - CONTROL PORT - SPI MODE

Inputs: Logic 0 = 0 V, Logic 1 = VL; C_L = 20 pF.

Parameter	Symbol	Min	Max	Unit
CCLK Clock Frequency	f_{sck}	0	6.0	MHz
$\overline{RST}$ Rising Edge to $\overline{CS}$ Falling	t_{srs}	500	-	µs
CCLK Edge to $\overline{CS}$ Falling (Note 13)	t_{spi}	500	-	ns
$\overline{CS}$ High Time Between Transmissions	t_{csh}	1.0	-	µs
$\overline{CS}$ Falling to CCLK Edge	t_{css}	20	-	ns
CCLK Low Time	t_{scl}	66	-	ns
CCLK High Time	t_{sch}	66	-	ns
CDIN to CCLK Rising Setup Time	t_{dsu}	40	-	ns
CCLK Rising to DATA Hold Time (Note 14)	t_{dh}	15	-	ns
CCLK Falling to CDOUT Valid (Note 15)	t_{scdov}	-	100	ns
Time from $\overline{CS}$ Rising to CDOUT High-Z	t_{cscdo}	-	100	ns
CDOUT Rise Time	t_{r1}	-	25	ns
CDOUT Fall Time	t_{f1}	-	25	ns
CCLK and CDIN Rise Time (Note 16)	t_{r2}	-	100	ns
CCLK and CDIN Fall Time (Note 16)	t_{f2}	-	100	ns

Notes:

13. t_{spi} only needed before first falling edge of $\overline{CS}$ after $\overline{RST}$ rising edge. t_{spi} = 0 at all other times.
14. Data must be held for sufficient time to bridge the transition time of CCLK.
15. CDOUT should *not* be sampled during this time.
16. For f_{sck} < 1 MHz.

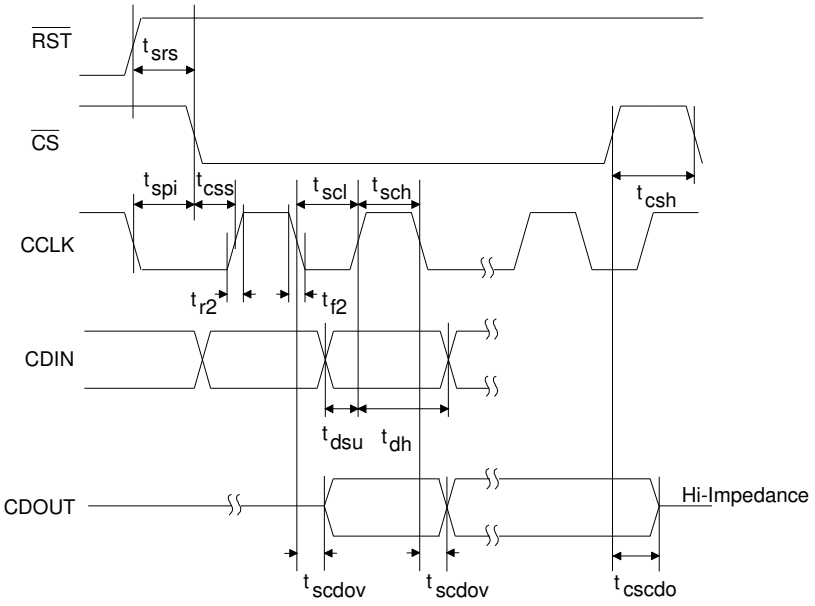


Figure 5. SPI Mode Timing

SWITCHING CHARACTERISTICS - CONTROL PORT - I²C MODE

Inputs: Logic 0 = 0 V, Logic 1 = VL; C_L = 20 pF.

Parameter	Symbol	Min	Max	Unit
SCL Clock Frequency	f_{scl}	-	100	kHz
$\overline{RST}$ Rising Edge to Start	t_{irs}	500	-	µs
Bus Free Time Between Transmissions	t_{buf}	4.7	-	µs
Start Condition Hold Time (prior to first clock pulse)	t_{hdst}	4.0	-	µs
Clock Low time	t_{low}	4.7	-	µs
Clock High Time	t_{high}	4.0	-	µs
Setup Time for Repeated Start Condition	t_{sust}	4.7	-	µs
SDA Hold Time from SCL Falling (Note 17)	t_{hdd}	10	-	ns
SDA Setup time to SCL Rising	t_{sud}	250	-	ns
Rise Time of SCL and SDA	t_{rc}, t_{rd}	-	1000	ns
Fall Time SCL and SDA	t_{fc}, t_{fd}	-	300	ns
Setup Time for Stop Condition	t_{susp}	4.7	-	µs
Acknowledge Delay from SCL Falling	t_{ack}	300	1000	ns

Notes:

17. Data must be held for sufficient time to bridge the transition time, t_{fc}, of SCL.

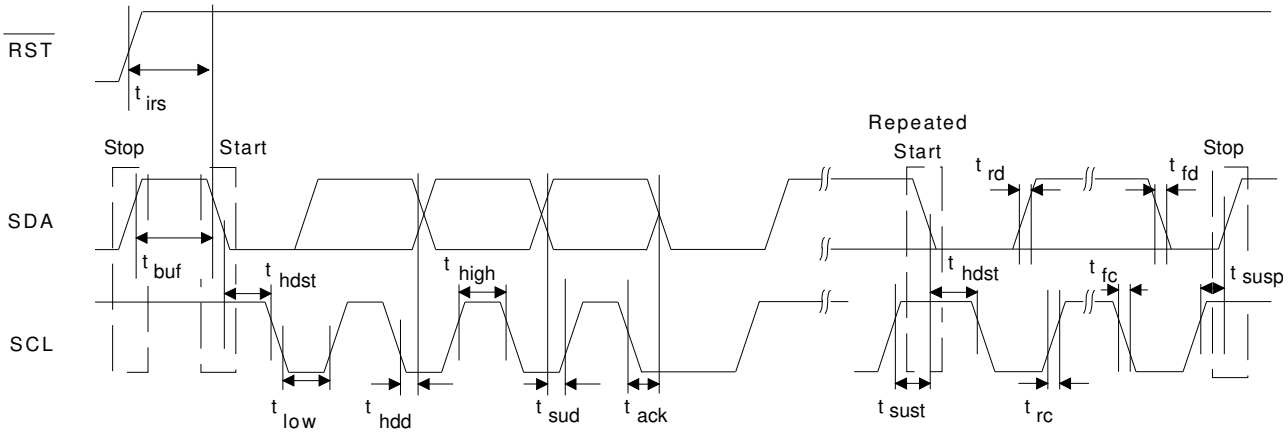


Figure 6. I²C Mode Timing

3. TYPICAL CONNECTION DIAGRAMS

3.1 Software Mode

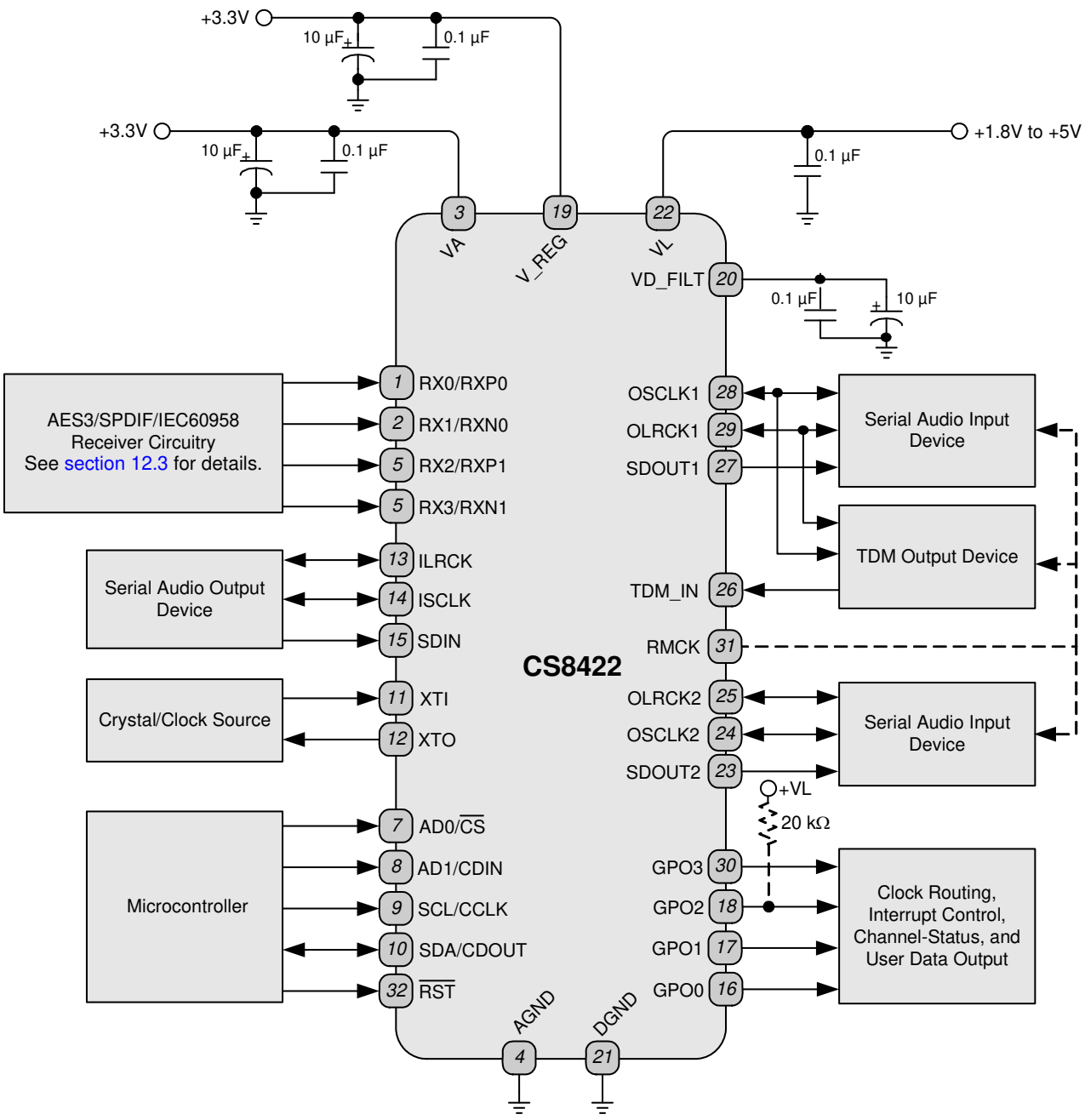


Figure 7. Typical Connection Diagram, Software Mode

3.2 Hardware Mode

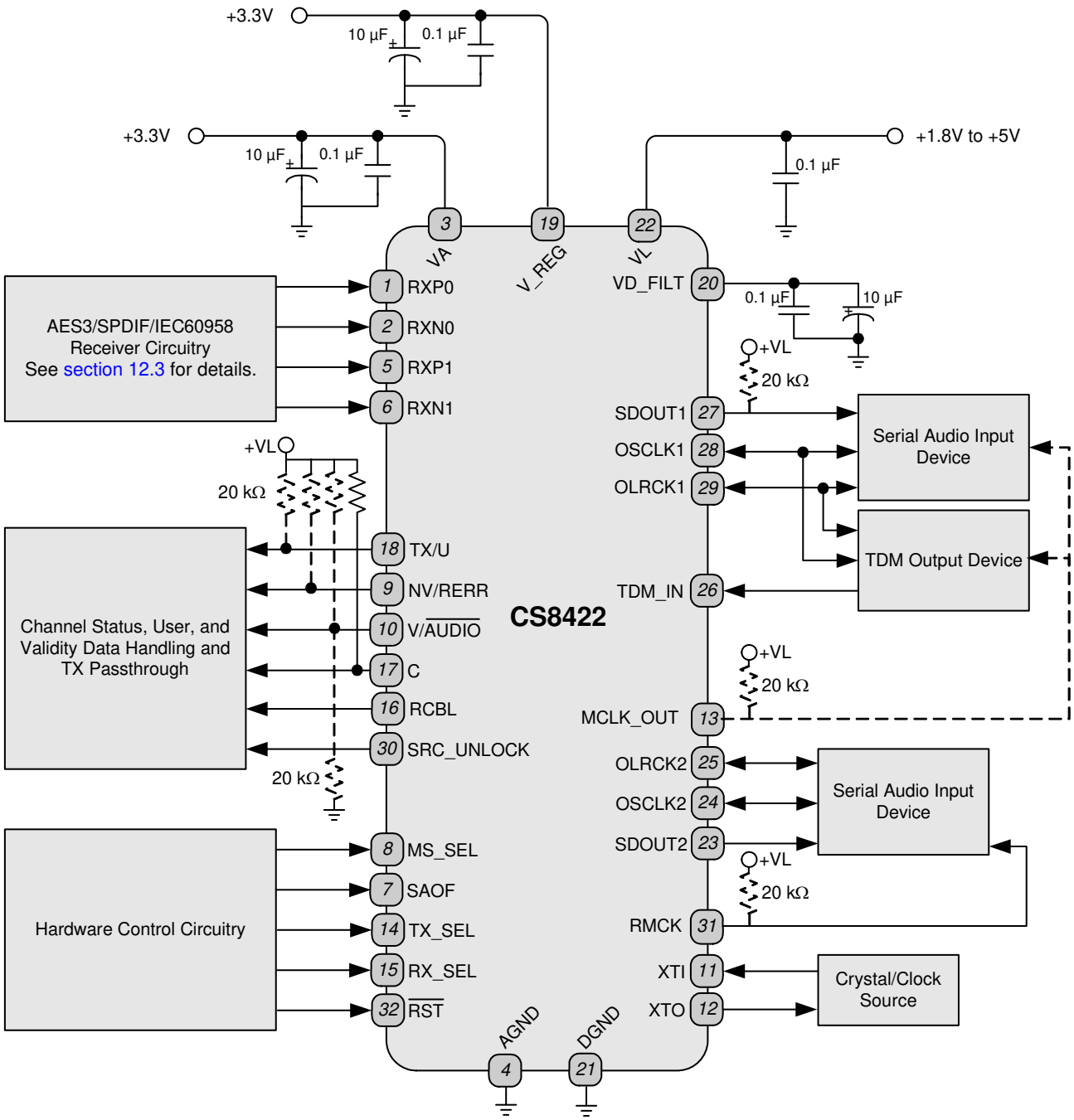


Figure 8. Typical Connection Diagram, Hardware Mode

4. OVERVIEW

The CS8422 is a 24-bit, high performance, monolithic CMOS stereo asynchronous sample rate converter with integrated digital audio interface receiver that decodes audio data according to EIAJ CP1201, IEC-60958, AES3, and S/PDIF interface standards.

Audio data is input through either a 3-wire serial audio port or the AES3-compatible digital interface receiver. Audio data is output through one of two 3-wire serial audio output ports. The serial audio ports are capable of 24, 20, 18, or 16-bit word lengths. Data in to the digital interface receiver can be up to 24-bit. Input and output data can be completely asynchronous, synchronous to an external data clock through XTI, or synchronous to the master clock recovered from the incoming S/PDIF or AES3 data.

CS8422 can be controlled either in Software Mode or in a stand-alone Hardware Mode. In Software Mode, the user can control the device through either a SPI or I²C control port.

Target applications include digital recording systems (DVD-R/RW, CD-R/RW, PVR, DAT, MD, and VTR), digital mixing consoles, high quality D/A, effects processors, and computer audio systems.

Figure 7 and Figure 8 show typical connections to the CS8422.

5. THREE-WIRE SERIAL INPUT/OUTPUT AUDIO PORT

The CS8422 provides two independent 3-wire serial audio output ports, and a 3-wire serial audio input (only available in Software Mode). The interface format should be chosen to suit the attached device either through the control port in Software Mode, or through the MS_SEL and SAOF pins in Hardware Mode. The following parameters are adjustable:

Hardware Mode

- Master or slave mode operation
- Master-mode MCLK-to-OLRCK (OLRCK1 and OLRCK2) ratios: 128, 256, and 512
- Audio data resolution of 16, 20, or 24-bits
- Left-Justified, I²S, or Right-Justified serial data formats
- Multi-channel TDM serial audio format (Serial Audio Output 1 only)

Software Mode

- Master or slave mode operation
- Master-mode MCLK-to-ILRCK and MCLK-to-OLRCK (OLRCK1 and OLRCK2) ratios: 64, 128, 192, 256, 384, 512, 768, and 1024
- Audio data resolution of 16, 18, 20, or 24-bits
- Left-Justified, I²S, or Right-Justified serial data formats
- Multi-channel TDM serial audio format
- AES3 Direct Output format

Figures 9, 10, 11, and 12 show the standard input/output formats available. The TDM serial audio format is described in Section 5.1.5 on page 27. For more information about serial audio formats, refer to the Cirrus Logic applications note AN282, “The 2-Channel Serial Audio Interface: A Tutorial”, available at *www.cirrus.com.*

5.1 Serial Port Clock Operation

5.1.1 Master Mode

When a serial port is set to master mode, its left/right clock (ILRCK, OLRCK1, or OLRCK2), and its serial bit-clock (ISCLK, OSCLK1, or OSCLK2) are outputs. If a serial output is sourced directly by the AES3 receiver, then that serial port's left/right clock and serial bit-clock will be synchronous with RMCK. If a serial port is routed to or from the sample rate converter (SRC), then that serial port's left/right clock and serial bit-clock can be synchronous with either the XTI-XTO or RMCK when it is in master mode.

If a serial output is source directly by the serial input port without the use of the SRC, then all associated clocks must be synchronous, so both serial ports must use the same master clock source. It is for this reason that, when in this mode, the serial output clock control is done through the Serial Audio Input Clock Control (07h) register.

5.1.2 Slave Mode

When a serial port is in slave mode, its left/right clock (ILRCK, OLRCK1, or OLRCK2), and its serial bit-clock (ISCLK, OSCLK1, or OSCLK2) are inputs. If the serial input or a serial output has the SRC in its data path, then the serial port's LRCK and SCLK may be asynchronous to all other serial ports. The left/right clock should be continuous, but the duty cycle can be less than 50% if enough serial clocks are present in each associated LRCK phase to clock all of the data bits.

If there are fewer SCLK periods than required to clock all the bits present in one half LRCK period in Left-Justified and I²S Modes, data will be truncated beginning with the LSB. In Right-Justified Modes, the data will be invalid.

If a serial audio output is operated in slave mode and sourced directly by the AES3 receiver or the serial input port without the use of the sample rate converter, then the OLRCK supplied to the serial audio output should be synchronous to Fsi or ILRCK to avoid skipped or repeated samples. The OSLIP bit ("Interrupt Status (14h)" on page 60) is provided to indicate when skipped or repeated samples occur.

If the input sample rate, Fsi or ILRCK, is greater than the slave-mode OLRCK frequency, then dropped samples will occur. If Fsi or ILRCK is less than the slave-mode OLRCK frequency, then samples will be repeated. In either case the OSLIP bit will be set to 1 and will not be cleared until read through the control port.

5.1.3 Hardware Mode Control

In Hardware Mode, the serial audio input port is not available. SDOUT1 is the serial data output from the sample rate converter, and SDOUT2 is the serial audio output directly from the AES3-compatible receiver. Because there is no serial audio input available in Hardware Mode, all audio data input is done through the AES3-compatible receiver. In Hardware Mode, the serial output ports are controlled through the SAOF and MS_SEL pins. See "Hardware Mode Serial Audio Port Control" on page 41 for more details.

In Hardware Mode, there are always 64 SCLK periods per LRCK period when a serial port is set to master mode.

5.1.4 Software Mode Control

In Software Mode, the CS8422 provides a serial audio input port and two serial audio output ports. Each serial port's clocking and data routing options are fully configurable as shown in Serial Audio Input Data Format (0Bh), Serial Audio Output Data Format - SDOUT1 (0Ch), and Serial Audio Output Data Format - SDOUT2 (0Dh) registers, found on pages 54, 55, and 56.