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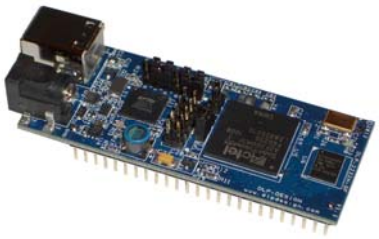
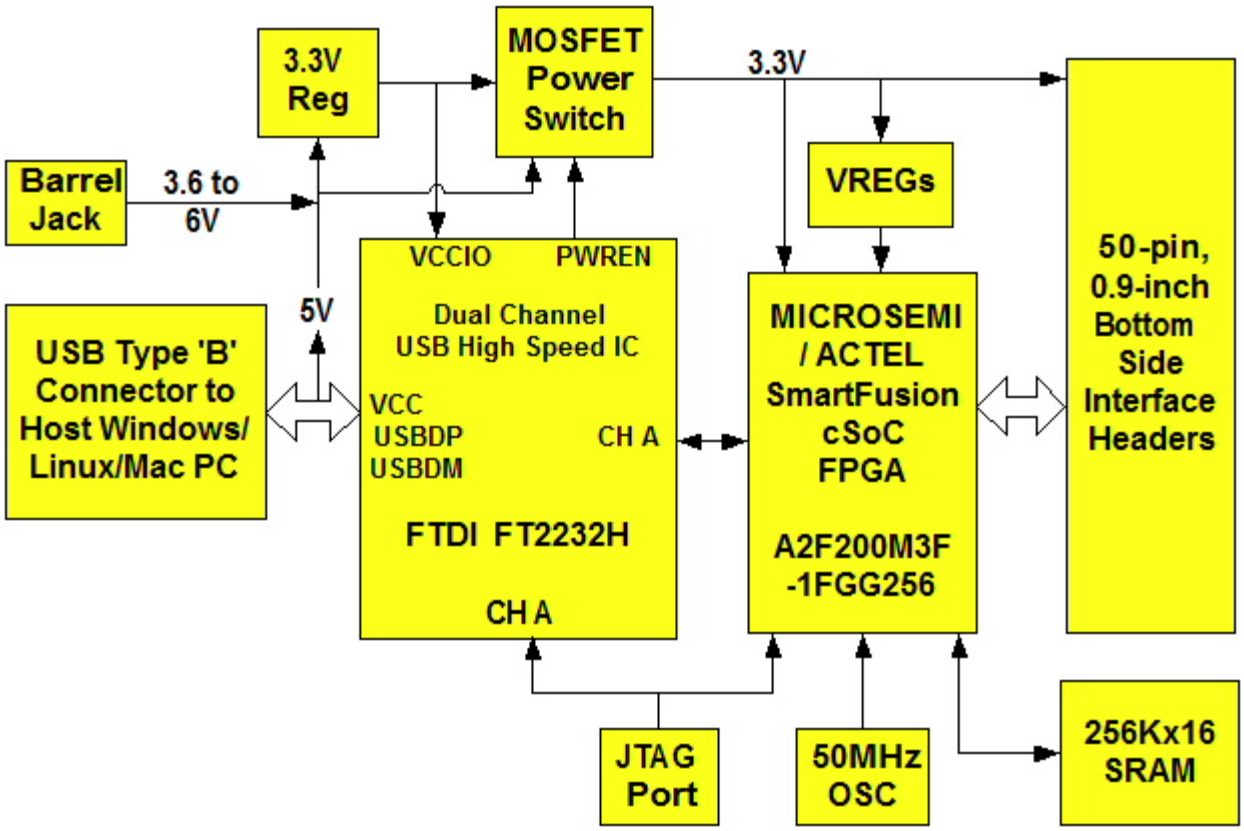


DLP-2232H-SF

LEAD FREE

USB - MICRONTROLLER - FPGA MODULE



FEATURES:

- Microsemi/Actel SmartFusion™ Customizable System-on-Chip (cSoC) FPGA
- Internal 100MHz, 32-Bit ARM® Cortex™-M3 Microcontroller Subsystem (MSS)
- Internal 100MHz RC Oscillator--1% Accurate
- 256Kbytes Embedded, Nonvolatile Flash Memory; 64Kbytes Embedded SRAM Memory
- Cypress 4-Mbit (256K x 16) SRAM Memory--PCB Supports up to 64-Mbit SRAM
- MSS Peripherals Include: UART, SPI, I^2C, Timers, RTC, 8-Channel DMA
- 10/100 Ethernet MAC with RMII Interface and External 50MHz Oscillator
- Two Configurable 8/10/12-Bit SAR ADC's with Sample Rates up to 600KSPS
- Two Configurable 8/16/24-Bit Input Sigma-Delta DAC's
- Two Active Bipolar Prescaler Analog Inputs (ABPS); Supports Voltages in Excess of 10 Volts

- Internal 2.56V Reference or Optional External Reference
- FPGA Fabric Includes 4,608 Tiles and 36,864 Bits of Block RAM
- 14 Analog Inputs; 2 Analog Outputs; 16 MSS/GPIO I/O's, 10 MSS/FPGA I/O's
- Analog Compute Engine (ACE) Supports Digital Filtering, Transformations and Threshold Flags
- Complete Combined USB Microcontroller-FPGA Reference Design Provided
- USB Port Powered or 5V External Power Barrel Jack
- USB 1.1- and 2.0-Compatible Interface
- Small Footprint: 3.0 x 1.2-Inch PCB and Standard 50-Pin, 0.9-Inch DIP Interface

APPLICATIONS:

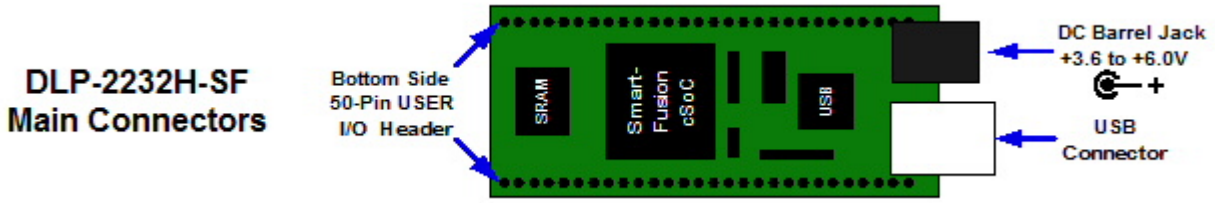
- Rapid Prototyping
- Educational Tool
- Industrial/Process Control
- Data Acquisition/Processing
- Embedded Processor

1.0 INTRODUCTION

The DLP-2232H-SF module is a low-cost, compact prototyping tool that can be used for rapid proof of concept or within educational environments. The module is based on the Microsemi SmartFusion™ cSoC microcontroller-FPGA and Future Technology Devices International's FT2232H dual-channel high-speed USB IC. The DLP-2232H-SF provides both the beginner as well as the experienced engineer with a rapid path to developing FPGA-based designs. When combined with the Libero™ SoC and SoftConsole™ IDE tools from Microsemi, this module is more than sufficient for creating anything from basic logical functions to a highly complex system controller.

The DLP-2232H-SF is fully compatible with the free Libero™ SoC and SoftConsole™ IDE tools from Microsemi. Libero™ SoC is used to configure the ARM® Cortex™-M3 Microcontroller Subsystem (MSS) and the FPGA fabric design. Libero™ supports HDL synthesis and simulation, implementation, timing verification, device fitting and JTAG programming. SoftConsole™ is based on the Eclipse IDE and is used to compile, download and debug the C/C++ source code that runs on the MSS.

The DLP-2232H-SF has on-board voltage regulators that generate all required power supply voltages from a single 5-volt source. Power for the module can be taken from either the host USB port or from a user-supplied, external 5-volt power supply via an onboard standard barrel connector:



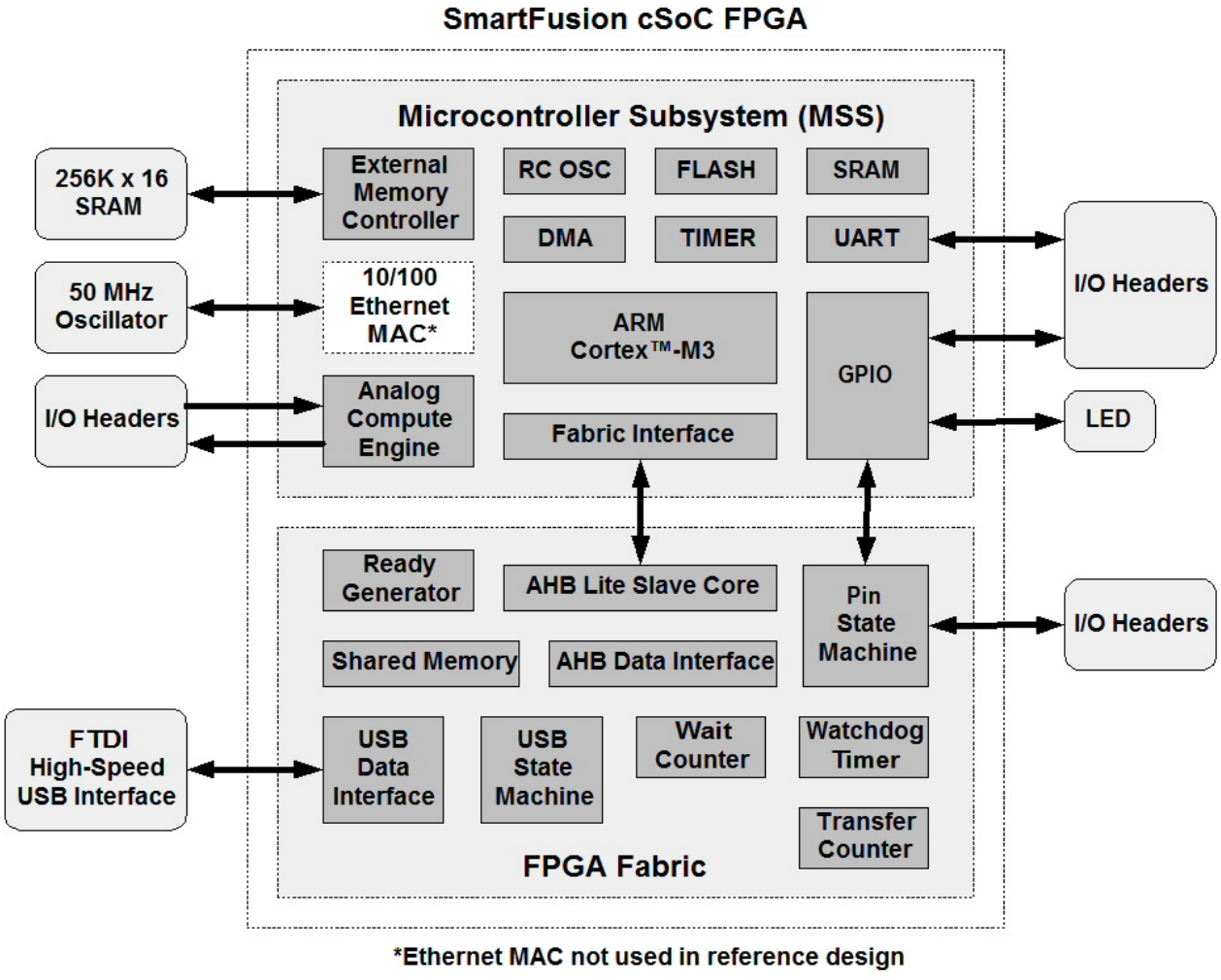
Connection to user electronics is made via a 50-pin, 0.9-inch wide, industry-standard 0.025-square inch post DIP header on the bottom of the board. The bottom-side, 50-pin header provides access to 42 of the SmartFusion™ cSoC MSS and FPGA input/output pins. This connector header mates with a user-supplied, standard, 50-pin, 0.9-inch spaced DIP socket.

DIP Socket

Other on-board features include a 256K x 16 SRAM external memory IC for use by the MSS through its External Memory Controller (EMC), a JTAG port connector for debug and programming, a JTAG mode-select header, an external battery header and a voltage-reference selection header.

2.0 REFERENCE DESIGN

A working reference design is available for the SmartFusion™ cSoC FPGA on the DLP-2232H-SF to those who purchase the module. A README file is included with the download file that explains the use of the project and the tools in detail. The hardware design is written in VHDL and built using the free Libero™ SoC tools. The software design is written in C and built using the free SoftConsole™ IDE. The reference design consists of the following blocks:



*Ethernet MAC not used in reference design

The reference design can be divided into MSS configuration and software and FPGA fabric portions. The MSS configuration uses the internal RC oscillator to derive the 100MHz clock used by the processor. It utilizes the Analog Compute Engine (ACE) to initialize both ADC's in 12-bit mode and both DAC's in 8-bit mode. ADC0 is configured to use the Programmable DMA (PDMA) controller to transfer 8,192 raw samples at 83.2 KSPS to the internal memory. ADC1 and the two DAC's are configured for single-sample operation.

The MSS uses internal Flash memory to store the executable code and the internal SRAM to store variables such as the ADC0 samples mentioned above. The External Memory Controller (EMC) is used to control the external 256K x 16 SRAM memory. It is configured for asynchronous RAM, byte enable used, half word port, with a read latency of 1. The MSS also uses the Fabric Interface configured as a master, the GPIO controller, UART 1 when debug is enabled and the timer peripheral.

The FPGA fabric design uses just over 46% of the available logic resources in the A2F200M3F device. To allow the MSS to connect to the FPGA fabric, an AHB Lite Interface Core is used. It is configured so that the MSS is master and the FPGA fabric is slave. The entire FPGA fabric design is clocked by the 50MHz clock provided by the AHB Lite Interface so that it is synchronized with the MSS.

The FPGA fabric design contains a USB Data Interface, a USB State Machine, an AHB Lite Data Interface, shared memory for communication between the FPGA and the MSS and a Pin State Machine. Several support blocks are required to count wait states and data transfers in order to generate the AHB Ready pulse due to its unique timing requirements and to provide a watchdog timer in case the MSS stops responding.

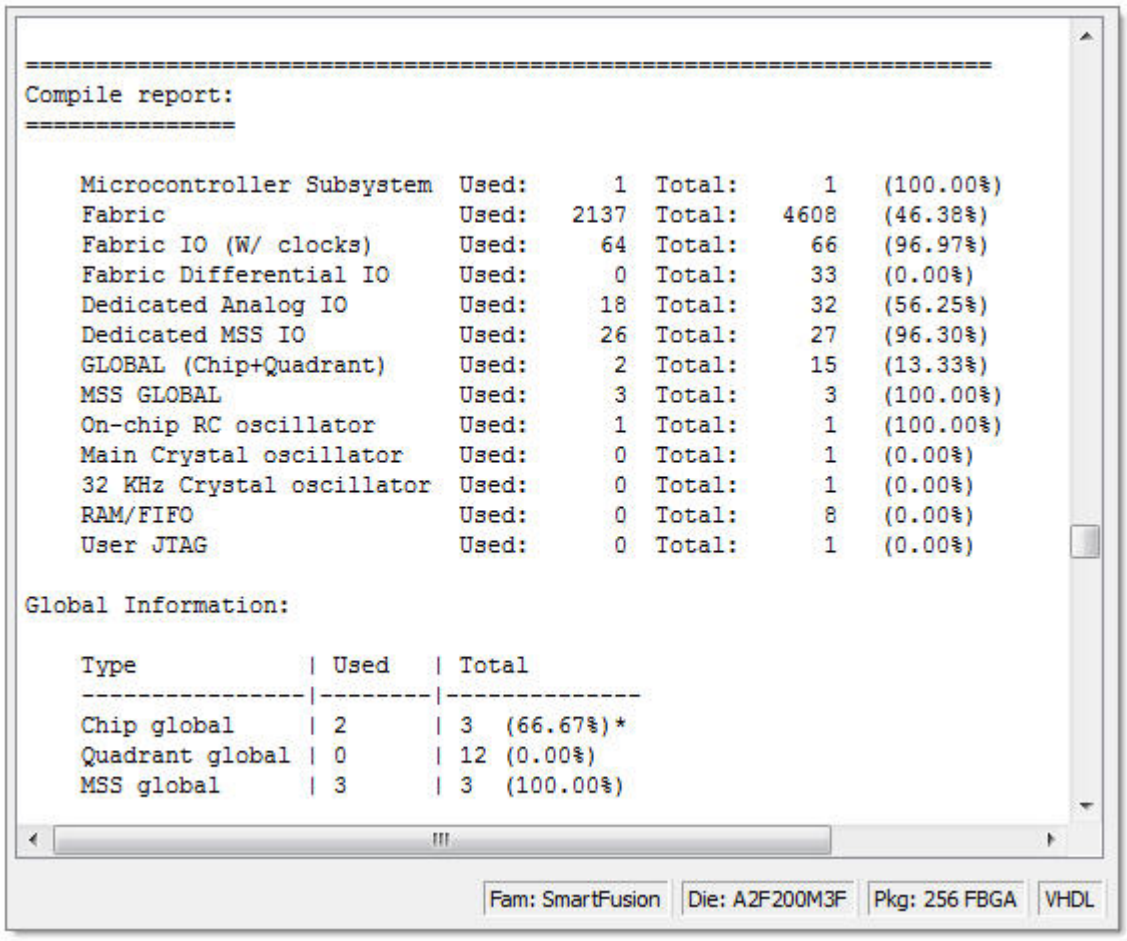
The USB interface captures, interprets and returns command and data bytes sent from the host PC through the FTDI USB interface to the FPGA. Commands include Ping, Return Status, Loopback Data, Set or Clear an I/O Pin, Read an I/O Pin, Test External Memory, Configure the DAC's and Acquire Samples from the ADC's. (Section 11 explains these in detail.)

The DLP-2232H-SF module supports user access to 43 of the SmartFusion™ cSoC pins via the J1 Connector on the bottom of the module. Of these 43 pins, 16 have analog functionality, 17 are connected to the MSS and can support GPIO or MSS functions and 10 can be connected to the FPGA fabric or the Ethernet MAC peripheral. One of the MSS pins is dedicated to the internally pulled up/ active low MSS Reset Pin. In addition, one of the MSS GPIO pins is used to control the module's D3 LED. The analog pins include 14 that can be analog inputs and 2 that can be analog outputs. Eight of the analog inputs can also be digital inputs. The functionality of these pins is configured by the project loaded into the SmartFusion™ cSoC device.

The reference design loaded into the DLP-2232H-SF module configures the user access on the J1 Connector as follows:

Of the 16 possible analog pins, 8 are configured as analog inputs and can be connected internally to the two ADC's under MSS control, 2 are analog outputs and are connected to the 2 DAC's and 6 are configured as digital inputs. Of the remaining pins, 16 are configured as MSS GPIO, 8 are configured as digital inputs, 2 are configured as digital inputs and 1 pin is used as the MSS Reset input.

The reference design occupies the following device resources on the DLP-2232H-SF module's A2F200M3F:



More reference designs are planned. Please contact DLP Design with any specific requests.

3.0 FPGA SPECIFICATIONS

The device used on the DLP-2232H-SF is the Microsemi SmartFusion™ A2F200M3F-1FGG256

- Part Number: A2F200M3F-1FGG256
- ARM® Cortex™-M3: 1
- Flash (Kbytes): 256
- SRAM (Kbytes): 64
- 10/100 Ethernet MAC: 1
- UART: 2
- I2C: 2
- SPI: 2
- ADC's (8-, 10-, 12-bit SAR): 2
- DAC's (12-Bit Sigma-Delta): 2
- FPGA System Gates: 200,000
- FPGA Tiles (D Flip-Flops): 4,608
- FPGA Block RAM Bits: 36,864

4.0 ABSOLUTE MAXIMUM RATINGS

Stresses above those listed here may cause permanent damage to the DLP-2232H-SF:

Operating Temperature: 0-70°C

Voltage on Digital Inputs with Respect to Ground: -0.5V to +4.1 V

Sink/Source Current on Any I/O: 8mA (MSS I/O) 12mA (FPGA I/O 3.3V LVTTL/LVCMOS)

5.0 WARNINGS

- Unplug from the host PC and power adapter before connecting to I/O pins on the DLP-2232H-SF.
- Isolate the bottom of the board from all conductive surfaces.
- Observe static precautions to prevent damage to the DLP-2232H-SF module.

6.0 EEPROM SETUP / MPROG

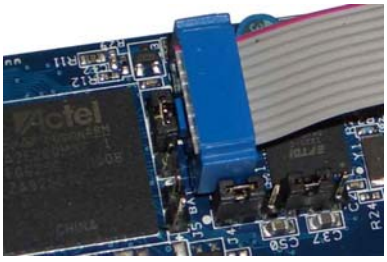
The DLP-2232H-SF has a dual-channel USB interface to the host PC. Channel A is used exclusively to connect the host PC to the FPGA fabric on the SmartFusion™ cSoC device. Channel B is connected to the SmartFusion™ device's JTAG programming port and debug port (J2) for future use. A 93LC56B EEPROM connected to the USB interface IC is used to store the USB port setup for the two channels. The parameters stored in the EEPROM include the Vendor ID (VID), Product ID (PID), serial number, description string, driver selection (VCP or D2XX) and port type (UART serial or FIFO parallel).

To use the reference design, D2XX drivers and 245 FIFO mode must be selected in the EEPROM for Channel A. Channel B is currently configured to also use the 245 FIFO mode, but it can use either the VCP or D2XX drivers as this port is not currently being utilized. The VCP drivers make the DLP-2232H-SF appear as an RS232 port to the host application. The D2XX drivers provide faster throughput, but they require working with a *.lib or *.dll library in the host application.

The operational modes and other EEPROM selections are written to the EEPROM using the MPROG utility. This utility and its manual are available for download from the bottom of the page at **www.dlpdesign.com**.

7.0 JTAG INTERFACE

To program and debug the SmartFusion™ cSoC device, a JTAG header (J2) is provided on the DLP-2232H-SF. (A FlashPro4 programming cable is required. This cable is available for purchase from Microsemi.) Connect the ribbon cable to the DLP-2232H-SF module as follows:



8.0 TEST PROGRAMMING FILE

The DLP-2232H-SF module comes pre-programmed with the reference design discussed in Section 2 of this datasheet. (This test programming file is also provided as a download from the DLP Design website to those who purchase the module.) The reference design provides access to the MSS and I/O features of the DLP-2232H-SF. The following USB command features are provided for the host PC's use:

- Ping
- Read ARM Status Registers
- Drive I/O Pins High/Low or Read their High/Low State
- Test the External Memory
- Configure the DAC Outputs
- Read the ADC Inputs

The command structure that supports these features is explained in Section 11.

9.0 USB DRIVERS

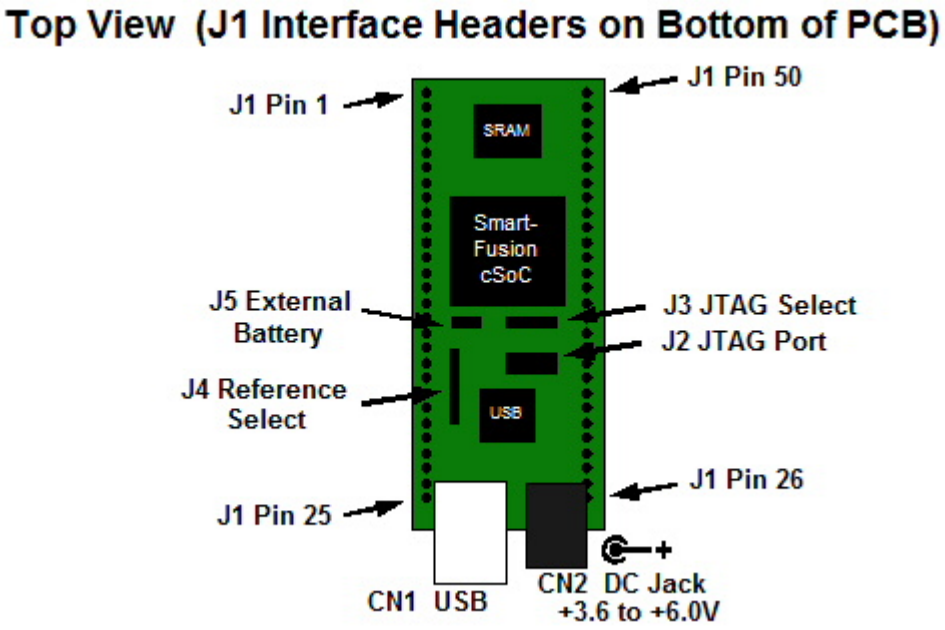
USB drivers for the following operating systems are available for download from the DLP Design website at **www.dlpdesign.com**:

OPERATING SYSTEM SUPPORT	
Windows 7 32-bit	**Windows 7 64-bit**
Windows Vista, Vista x64	**Mac OSX**
Windows XP, XP x64	**Mac OS9**
Windows Server 2008, x64	**Mac OS8**
Windows Server 2003, x64	**Linux**
Windows 2000	**Windows CE 4.2-6.0**

Note: If you are utilizing the dual-mode drivers from FTDI (CDM2.x.x) and you want to use the Virtual COM Port (VCP) drivers, then it may be necessary to disable the D2XX drivers first via Device Manager. To do so, right click on the entry under USB Controllers that appears when the DLP-2232H-SF is connected, select Properties, select the Advanced tab, check the option for Load VCP and click OK. Then unplug and replug the DLP-2232H-SF, and a COM Port should appear in Device Manager under Ports (COM & LPT).

10.0 HEADER DEFINITIONS

The DLP-2232H-SF has five user-accessible headers. The first is J1 which is located on the bottom side of the module, and the remaining four are J2 to J5, which are located on the top:



Individual header pinouts are described in the following tables:

TABLE 1				
J1: User I/O				
DLP-2232H-SF J1 Pin	**A2F200 Pin**	**A2F200 Block**	**Test App I/O Number**	**Signal Description**
J1 Pin 1	R3	MSS Analog		ABPS0: Active Bipolar Prescaler Input 0
J1 Pin 2	R11	MSS Analog		ABPS4: Active Bipolar Prescaler Input 4
J1 Pin 3	GND	Power		Ground
J1 Pin 4	R2	MSS Analog		SDD0: DAC 0 Output
J1 Pin 5	T12	MSS Analog		SDD1: DAC 1 Output
J1 Pin 6	M5	MSS Analog/ Digital In	0x03	ADC3: ADC Direct Input 3 or Digital Input
J1 Pin 7	R6	MSS Analog/ Digital In	0x01	ADC1: ADC Direct Input 1 or Digital Input
J1 Pin 8	T5	MSS Analog/ Digital In		ADC0: ADC Direct Input 0 or Digital Input
J1 Pin 9	R9	MSS Analog/ Digital In	0x07	ADC7: ADC Direct Input 7 or Digital Input
J1 Pin 10	P9	MSS Analog/ Digital In	0x06	ADC6: ADC Direct Input 6 or Digital Input
J1 Pin 11	P7	MSS Analog/ Digital In	0x02	ADC2: ADC Direct Input 2 or Digital Input
J1 Pin 12	M9	MSS Analog/ Digital In		ADC4: ADC Direct Input 4 or Digital Input

J1 Pin 13	N9	MSS Analog/ Digital In	0x05	ADC5: ADC Direct Input 5 or Digital Input
J1 Pin 14	P6	MSS Analog		CM1: Current Monitor/Comparator Input 1
J1 Pin 15	N6	MSS Analog		TM1: Current Monitor/Comparator/Temperature Input 1
J1 Pin 16	N10	MSS Analog		CM3: Current Monitor/Comparator Input 3
J1 Pin 17	P10	MSS Analog		TM3: Current Monitor/Comparator/Temperature Input 3
J1 Pin 18	GND	Power		Ground
J1 Pin 19	N16	MSS Digital	0x16	DO0/GPIO16: SPI 0 Data Output/MSS GPIO 16
J1 Pin 20	M13	MSS Digital	0x19	SS0/GPIO19: SPI 0 Slave Select/MSS GPIO 19
J1 Pin 21	M16	MSS Digital	0x17	DI0/GPIO17: SPI 0 Data Input/MSS GPIO 17
J1 Pin 22	M15	MSS Digital	0x18	CK0/GPIO18: SPI 0 Clock/MSS GPIO 18
J1 Pin 23	+5V IN	Power		+5V Input to the DLP-2232H-SF
J1 Pin 24	+5V USB	Power		+5V Supplied by Host PC USB Port
J1 Pin 25	GND	Power		Ground
J1 Pin 26	GND	Power		Ground
J1 Pin 27	K15	MSS Digital	0x29	RX1/GPIO29: UART 1 Transmit/MSS GPIO 29
J1 Pin 28	K14	MSS Digital	0x28	TX1/GPIO28: UART 1 Receive/MSS GPIO 28
J1 Pin 29	K16	MSS Digital	0x20	TX0/GPIO20: UART 0 Transmit/MSS GPIO 20
J1 Pin 30	K12	MSS Digital	0x21	RX0/GPIO21: UART 0 Receive/MSS GPIO 21
J1 Pin 31	J16	MSS Digital	0x30	SD1/GPIO30: I2C 1 Serial Data Input/Output/ MSS GPIO 30
J1 Pin 32	J14	MSS Digital	0x31	SC1/GPIO31: I2C 1 Serial Clock Output/MSS GPIO 31
J1 Pin 33	J13	MSS Digital	0x22	SD0/GPIO22: I2C 0 Serial Data Input/Output/ MSS GPIO 22
J1 Pin 34	J12	MSS Digital	0x23	SC0/GPIO23: I2C 0 Serial Clock Output/MSS GPIO 23
J1 Pin 35	L13	MSS Digital	0x27	MSS GPIO 27
J1 Pin 36	L15	MSS Digital	0x25	MSS GPIO 25
J1 Pin 37	L14	MSS Digital	0x26	MSS GPIO 26
J1 Pin 38	K4	MSS Reset		Active Low MSS Reset Input (internal pull-up)
J1 Pin 39	GND	Power		Ground
J1 Pin 40	L12	MSS Digital	0x24	MSS GPIO 24/LED D3
J1 Pin 41	E3	FPGA Fabric	0x68	FPGA Fabric I/O
J1 Pin 42	L3	FPGA Fabric	0x21	CSDV: RMII Carrier Sense/Receive Data Valid/ FPGA Fabric I/O
J1 Pin 43	K1	FPGA Fabric	0x23	MDIO: RMII Management Data Input/Output/ FPGA Fabric I/O
J1 Pin 44	K2	FPGA Fabric	0x24	MDC: RMII Management Clock/FPGA Fabric I/O
J1 Pin 45	L2	FPGA Fabric	0x20	TXEN: RMII Transmit Enable/FPGA Fabric I/O
J1 Pin 46	M1	FPGA Fabric	0x16	TXD0: RMII Transmit Data Bit 0/FPGA Fabric I/O
J1 Pin 47	M2	FPGA Fabric	0x17	TXD1: RMII Transmit Data Bit 1/Receive Data Valid/FPGA Fabric I/O
J1 Pin 48	N1	FPGA Fabric	0x19	RXD1: RMII Receive Data Bit 1/Receive Data Valid/FPGA Fabric I/O

J1 Pin 49	M3	FPGA Fabric	0x18	RXD0: RMII Receive Data Bit 0/Receive Data Valid/FPGA Fabric I/O
J1 Pin 50	L4	FPGA Fabric	0x22	RERR: RMII Receive Error/FPGA Fabric I/O

TABLE 2

J2: JTAG Port

DLP-2232H-SF J2 Pin	A2F200 Pin	A2F200 Block	Signal Description
J2 Pin 1	G15	JTAG	JTAG_TCK: JTAG Test Clock
J2 Pin 2	GND	Power	Ground
J2 Pin 3	H13	JTAG	JTAG_DOUT: JTAG Test Data Output
J2 Pin 4			Not Connected
J2 Pin 5	G14	JTAG	JTAG_TMS: JTAG Test Mode Select
J2 Pin 6	+3.3V	Power	+3.3V Power
J2 Pin 7		Power	Pull-up to +3.3V (not installed)
J2 Pin 8	G13	JTAG	JTAG_TRST: JTAG Test Reset
J2 Pin 9	H14	JTAG	JTAG_DIN: JTAG Test Data Input
J2 Pin 10	GND	Power	Ground

TABLE 3

J3: JTAG Select

DLP-2232H-SF J3 Pin	A2F200 Pin	A2F200 Block	Signal Description
J3 Pin 1	GND	Power	Pull-down to Ground
J3 Pin 2	H15	JTAG	JTAGSEL: JTAG Controller Select Input 0=Debug Cortex-M3 1=Program SmartFusion™
J3 Pin 3	+3.3V	Power	Pull-up to +3.3V

TABLE 4

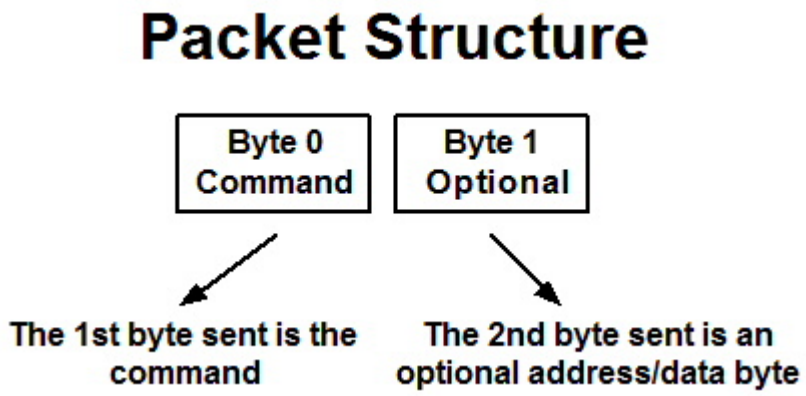
J4: Voltage Reference Input

DLP-2232H-SF J4 Pin	A2F200 Pin	A2F200 Block	Signal Description
J4 Pin 1	N12	MSS Analog	VREF_OUT: Internal Voltage Reference Output (+2.5V)
J4 Pin 2	T6	MSS Analog	VAREF0_IN: Voltage Reference Input 0
J4 Pin 3	GND	Power	Ground
J4 Pin 4	N12	MSS Analog	VREF_OUT: Internal Voltage Reference Output (+2.5V)
J4 Pin 5	T9	MSS Analog	VAREF1_IN: Voltage Reference Input 1
J4 Pin 6	GND	Power	Ground

TABLE 5			
J5: External Battery Input			
DLP-2232H-SF J5 Pin	**A2F200 Pin**	**A2F200 Block**	**Signal Description**
J5 Pin 1	P14	MSS Digital	VDDBAT: External Battery Connection to the Low-Power RTC and Battery Switch Over Circuit
J5 Pin 2	GND	Power	Pull-Down to Ground

11.0 USING THE DLP-2232H-SF

Select a power source via J1 Header Pins 23 and 24, and connect the DLP-2232H-SF to the PC to initiate the loading of USB drivers. The easiest way to do this is to connect Pins 23 and 24 to each other. This will result in operational power being taken from the host PC. Once the drivers are loaded, the DLP-2232H-SF is ready for use. (All commands issued consist of one or two bytes.)



You can either utilize the Test Application available from **www.dlpdesign.com/test.shtml** with the DLP-2232H-SF (as described in Section 12), or you can write your own program in your language of choice.

If you are using the VCP drivers, begin by opening the COM Port, and send multi-byte commands as shown in Table 6 below. There is no need to set the baud rate because the DLP-2232H-SF uses a parallel interface between the USB IC and the FPGA. (The Ping Command can be used to locate the correct COM Port used for communicating with the DLP-2232H-SF, or you can look in Device Manager to see which port was assigned by Windows.) If you are using the D2XX drivers as with the Test Application, no COM Port selection is necessary.

TABLE 6				
Command Packets				
Command Packet	**Description**	**Byte**	**Hex Value**	**Return/Comments**
FPGA Ping	Issues FPGA Ping Request	0	0x00	FPGA Ping Command - 0x4D (ASCII "M") will be returned indicating that the DLP-2232H-SF is found on the selected port.
Read Version	Accesses the Internal Version	0	0x10	Read Version/Status Registers Command
		1	0xnn	Register Address: 0xnn 0x00=Board ID 0x01=FPGA Type ID: 0xF2=A2F200M3F 0x02=Design Version ID 1 (Design Month) 0x03=Design Version ID 2 (Design Day) 0x04=Design Version ID 3 (Design Year) 0x05=Design Version ID 4 (Design Version)
Loopback	Returns the Data Byte Received	0	0x20	Loopback Command
		1	0xnn	The byte sent to the DLP-2232H-SF (0xnn) will be returned back.
Loopback Compliment	Returns the Compliment of Data Byte Received	0	0x21	Loopback Compliment Command
		1	0xnn	The byte sent to the DLP-2232H-SF (0xnn) will be complimented and returned back.
Read FPGA Input Pin	Pin Reads the State of One of the FPGA Fabric Input Pins	0	0x30	Read FPGA Input Pin Command
		1	0x01 0x02 0x03 0x05 0x06 0x07 0x21 0x23	(The FPGA fabric valid input pin numbers are described in Table 7.) FPGA Input Pin 0xnn is read and returns: 0x00=User I/O pin 0xnn is low 0x01=User I/O pin 0xnn is high
Clear FPGA Output Pin	Forces the Selected FPGA Output Pin Low	0	0x40	Clear FPGA Output Pin Command
		1	0x16 : 0x20 0x22 0x24 0x68	The FPGA fabric valid output pin numbers are described in Table 7. FPGA Output Pin 0xnn is cleared, and the specified user output pin number is returned.
Set FPGA Output	Forces the Selected FPGA Output Pin	0	0x41	Set FPGA Output Pin Command
		1	0x16 :	The FPGA fabric valid output pin numbers are described in Table 7.

Pin	High		0x20 0x22 0x24 0x68	FPGA Output Pin 0xnn is set, and the specified user output pin number is returned.
Write Shared Memory Location	Writes the Specified Shared Memory Location (shared between ARM and FPGA fabric)	0	0x5n	Write to the shared memory location "n": 0x50=Shared Memory Byte 0, To Host Status 0x51=Shared Memory Byte 1, To Host Command 0x52=Shared Memory Byte 2, To Host Data 0 0x53=Shared Memory Byte 3, To Host Data 1 0x54=Shared Memory Byte 4, From Host Status 0x55=Shared Memory Byte 5, From Host Command 0x56=Shared Memory Byte 6, From Host Data 0 0x57=Shared Memory Byte 7, From Host Data 1
		1	0xnn	Value to be written to specified location; the command byte sent is returned.
Read Shared Memory Location	Returns the Value in the Specified Shared Memory Location (shared between ARM and FPGA fabric)	0	0x6n	Reads the shared memory location "n", and the value in the specified location is returned: 0x60=Shared Memory Byte 0, To Host Status 0x61=Shared Memory Byte 1, To Host Command 0x62=Shared Memory Byte 2, To Host Data 0 0x63=Shared Memory Byte 3, To Host Data 1 0x64=Shared Memory Byte 4, From Host Status 0x65=Shared Memory Byte 5, From Host Command 0x66=Shared Memory Byte 6, From Host Data 0 0x67=Shared Memory Byte 7, From Host Data 1
ARM Ping	Issues ARM Ping Request	0	0x70	ARM Ping Command returns: 0xC3 indicates ARM Cortex-M3 is running 0xE8 indicates ARM Cortex-M3 is stopped Note: Watchdog timeout occurs after about 2 seconds of ARM core inactivity.

ARM Status Read	Returns the Specified ARM Status Register Value	0	0x8n	ARM Status Read returns the value of the following: 0x80=MSS Status Register (MSS_SR) Bit 5=PLLLOCKLOSTINT Bit 4=PLLLOCKINT Bits 3-0 same as Users Guide 0x81 =MSS Device Status Register (DEVICE_SR) 0x82=MSS PLL Status Register (MSS_CCC_SR) 0x83=MSS Soft Reset Register (SOFT_RST_CR) Bit 7=FPGA_SR Bit 6=EXT_SR Bit 5=UART_1_SR Bit 4=UART_0_SR Bits 3-0 same as Users Guide 0x84=Fabric Interface Register (FAB_IF_CR) 0x85=Fabric Interface Configuration Register (FAB_AHB_HIWORD_DR) 0x86=AHB Bus Matrix Register (AHB_MATRIX_CR) 0x87=UART 1 Line Control Register (LCR) 0x88=UART 1 Line Status Register (LSR) 0x89=GPIO 16 Configuration Register (GPIO_16_CFG) 0x8A=SW Build Number (set as #DEFINE in "main.c") Refer to the SmartFusion™ MSS Users Guide master, UART and GPIO register map for bit definitions. (Bits 7-0 match Users Guide except as noted above.)
Read ARM MSS I/O Pin	Pin Reads the State of One of the ARM MSS I/O Pins	0	0x90	Read FPGA Input Pin Command
		1	0x16 : 0x31	The ARM MSS valid I/O pin numbers are described in Table 7. The range of valid values is 16 through 31. MSS I/O Pin 0xnn is read and returns: 0x00=User I/O pin 0xnn is low 0x01=User I/O pin 0xnn is high
Clear ARM MSS I/O Pin	Clears the State of One of the ARM MSS I/O Pins	0	0xA0	Clear ARM MSS I/O Pin Command
		1	0x16 : 0x31	The ARM MSS valid I/O pin numbers are described in Table 7. The range of valid values is 16 through 31. ARM MSS Pin 0xnn is cleared. The specified user output pin number is returned.

Set ARM MSS I/O Pin	Sets the State of One of the ARM MSS I/O Pins	0	0xA1	Set ARM MSS I/O Pin Command
		1	0x16 : 0x31	The ARM MSS valid I/O pin numbers are described in Table 7. The range of valid values is 16 through 31. ARM MSS Pin 0xnn is cleared. The specified user output pin number is returned.
Test External Memory	Performs a Test on the External 265Kx16 SRAM	0	0xB0	The Test External Memory Command writes all 256K word locations with a known pattern, and then it reads all locations to verify the memory's functionality. Returns: 0x00=Memory test failed 0x01=Memory test passed
DAC 0 Configure	Loads and Enables DAC 0	0	0xC0	Configure DAC 0 Command
		1	0xnn	0xnn=Load value between 0x00 and 0xFF. DAC output range: 0-2.56V. The value 0xnn is returned. Note: DAC is configured as 8 bits in the reference design, but can be configured for 16- or 24-bit operation.
DAC 1 Configure	Loads and Enables DAC 1	0	0xC1	Configure DAC 1 Command
		1	0xnn	0xnn=Load value between 0x00 and 0xFF. DAC output range: 0-2.56V. The value 0xnn is returned. Note: DAC is configured as 8 bits in the reference design, but can be configured for 16- or 24-bit operation.
DAC 0 Disable	Turns Off DAC 0	0	0xC2	Disable DAC 0 Command
DAC 1 Disable	Turns off DAC 1	0	0xC3	Disable DAC 1 Command
ADC0 Input Single Sample (mV)	Returns mV Converted ADC Sample	0	0xD0	Single analog sample read from input ADC0 (J1 Pin 8) using convertor ADC 0. Result converted to mV. Returns 16-bit mV sample--MS byte first, followed by LS byte.

ADC4 Input Single Sample (mV)	Returns mV Converted ADC Sample	0	0xD1	Single analog sample read from input ADC4 (J1 Pin 12) using convertor ADC 1. Result converted to mV. Returns 16-bit mV sample--MS byte first, followed by LS byte.
ADC0 Input Single Sample (raw)	Returns Raw ADC Sample	0	0xD2	Single analog sample read from input ADC0 (J1 Pin 8) using convertor ADC 0. Raw count returned. Returns 12-bit raw sample right justified to 16 bits--MS byte first, followed by LS byte.
ADC4 Input Single Sample (mV)	Returns Raw ADC Sample	0	0xD3	Single analog sample read from input ADC4 (J1 Pin 12) using convertor ADC 1. Raw count returned. Returns 12-bit raw sample right justified to 16 bits--MS byte first, followed by LS byte.
ABPS0 Input Single Sample (raw)	Returns Raw ADC Sample	0	0xD4	Single analog sample read from input ABPS0 (J1 Pin 1) using convertor ADC 0. Raw count returned. Returns 12-bit raw sample right justified to 16 bits--MS byte first, followed by LS byte.
ABPS4 Input Single Sample (raw)	Returns Raw ADC Sample	0	0xD5	Single analog sample read from input ABPS4 (J1 Pin 2) using convertor ADC 1. Raw count returned. Returns 12-bit raw sample right justified to 16 bits--MS byte first, followed by LS byte.
CM1 Input Single Sample (raw)	Returns Raw ADC Sample	0	0xD6	Single analog sample read from input CM1 (J1 Pin 14) using convertor ADC 0. Raw count returned. Returns 12-bit raw sample right justified to 16 bits--MS byte first, followed by LS byte.
CM3 Input Single Sample (raw)	Returns Raw ADC Sample	0	0xD7	Single analog sample read from input CM3 (J1 Pin 16) using convertor ADC 0. Raw count returned. Returns 12-bit raw sample right justified to 16 bits--MS byte first, followed by LS byte.
TM1 Input Single Sample (raw)	Returns Raw ADC Sample	0	0xD8	Single analog sample read from input TM1 (J1 Pin 15) using convertor ADC 0. Raw count returned. Returns 12-bit raw sample right justified to 16 bits--MS byte first, followed by LS byte.

TM3 Input Single Sample (raw)	Returns Raw ADC Sample	0	0xD9	Single analog sample read from input TM3 (J1 Pin 17) using convertor ADC 0. Raw count returned. Returns 12-bit raw sample right justified to 16 bits--MS byte first, followed by LS byte.
Internal DAC0 to ADC0 Test (raw)	Returns Raw ADC Sample	0	0xDA	Single analog sample read from ADC 0 based on internal connection to DAC 0. Raw count returned. Returns 12-bit raw sample right justified to 16 bits--MS byte first, followed by LS byte.
Internal DAC1 to ADC1 Test (raw)	Returns Raw ADC Sample	0	0xDB	Single analog sample read from ADC 1 based on internal connection to DAC 1. Raw count returned. Returns 12-bit raw sample right justified to 16 bits--MS byte first, followed by LS byte.

The I/O Pin Read/Set/Clear Commands I/O number mapping to the physical I/O pins on the DLP-2232H-SF board are described in the following table:

TABLE 7					
MSS and User I/O					
Source	**I/O Code**	**J1 Pin (Bottom-Side Connector)**	**U5 Pin (SmartFusion™ Device)**	**Schematic Net Name**	**Description**
MSS (0x90, 0xA0, 0xA1)	0x16	19	N16	DO0_MSS_GPIO16	MSS multipurpose pin: SPI 0 Data Output or GPIO Bit 16. Configured as GPIO.
	0x17	21	M16	DI0_MSS_GPIO17	MSS multipurpose pin: SPI 0 Data Input or GPIO Bit 17. Configured as GPIO.
	0x18	22	M15	CK0_MSS_GPIO18	MSS multipurpose pin: SPI 0 Clock or GPIO Bit 18. Configured as GPIO.
	0x19	20	M13	SS0_MSS_GPIO19	MSS multipurpose pin: SPI 0 Slave Select or GPIO Bit 16. Configured as GPIO.
	0x20	29	K16	TX0_MSS_GPIO20	MSS multipurpose pin: UART 0 Transmit Out or GPIO Bit 20. Configured as GPIO.
	0x21	30	K12	RX0_MSS_GPIO21	MSS multipurpose pin: UART 0 Receive In or GPIO Bit 21. Configured as GPIO.
	0x22	33	J13	SD0_MSS_GPIO22	MSS multipurpose pin: I2C 0 Serial Data I/O or GPIO Bit 22. Configured as GPIO.
	0x23	34	J12	SC0_MSS_GPIO23	MSS multipurpose pin: I2C 0 Serial Clock or GPIO Bit 23. Configured as GPIO.
	0x24	40	L12	MSS_GPIO24_LEDn	MSS multipurpose pin: Connects to LED and GPIO Bit 24. Configured as GPIO. A logic "0" turns on the LED.
	0x25	36	L15	MSS_GPIO25	MSS multipurpose pin: GPIO Bit 25.
	0x26	37	L14	MSS_GPIO26	MSS multipurpose pin: GPIO Bit 26.
	0x27	35	L13	MSS_GPIO27	MSS multipurpose pin: GPIO Bit 27.
	0x28	28	K14	TX1_MSS_GPIO28	MSS multipurpose pin: UART 1 Transmit Out or GPIO Bit 28. Configured as GPIO.
	0x29	27	K15	RX1_MSS_GPIO29	MSS multipurpose pin: UART 1 Receive In or GPIO Bit 29. Configured as GPIO.
	0x30	31	J16	SD1_MSS_GPIO30	MSS multipurpose pin: I2C 1 Serial Data I/O or GPIO Bit 30. Configured as GPIO.
	0x31	32	J14	SC1_MSS_GPIO31	MSS multipurpose pin: I2C 1 Serial Clock or GPIO Bit 31. Configured as GPIO.

FPGA (0x30, 0x40, 0x41)	0x01	7	R6	ADC1	ADC Direct Input 1 configured as LVTTL Input.
	0x02	11	P7	ADC2	ADC Direct Input 2 configured as LVTTL Input.
	0x03	6	M5	ADC3	ADC Direct Input 3 configured as LVTTL Input.
	0x05	13	N9	ADC5	ADC Direct Input 5 configured as LVTTL Input.
	0x06	10	P9	ADC6	ADC Direct Input 6 configured as LVTTL Input.
	0x07	9	R9	ADC7	ADC Direct Input 7 configured as LVTTL Input.
	0X16	46	M1	TXD0_FPGA_M1	MSS multipurpose pin: MAC RMII Transmit Data Out Bit 0 or FPGA I/O. Configured as FPGA Digital Output 16.
	0x17	47	M2	TXD1_FPGA_M2	MSS multipurpose pin: MAC RMII Transmit Data Out Bit 1 or FPGA I/O. Configured as FPGA Digital Output 17.
	0x18	49	M3	RXD0_FPGA_M3	MSS multipurpose pin: MAC RMII Receive Data In Bit 0 or FPGA I/O. Configured as FPGA Digital Output 18.
	0x19	48	N1	RXD1_FPGA_N1	MSS multipurpose pin: MAC RMII Receive Data In Bit 1 or FPGA I/O. Configured as FPGA Digital Output 19.
	0x20	45	L2	TXEN_FPGA_L2	MSS multipurpose pin: MAC RMII Transmit Enable or FPGA I/O. Configured as FPGA Digital Output 20.
	0x21	42	L3	CSDV_FPGA_L3	MSS multipurpose pin: MAC RMII Carrier Sense/Receive Data Valid or FPGA I/O. Configured as FPGA Digital Input 21.
	0x22	50	L4	RERR_FPGA_L4	MSS multipurpose pin: MAC RMII Receive Error or FPGA I/O. Configured as FPGA Digital Output 22.
	0x23	43	K1	MDIO_FPGA_K1	MSS multipurpose pin: MAC RMII Management Data I/O or FPGA I/O. Configured as FPGA Digital Input 23.
	0x24	44	K2	MDC_FPGA_K2	MSS multipurpose pin: MAC RMII Management Data Clock or FPGA I/O. Configured as FPGA Digital Output 24.
	0x68	41	M3	FPGA_E3	FPGA I/O: Configured as FPGA Digital Output 68.

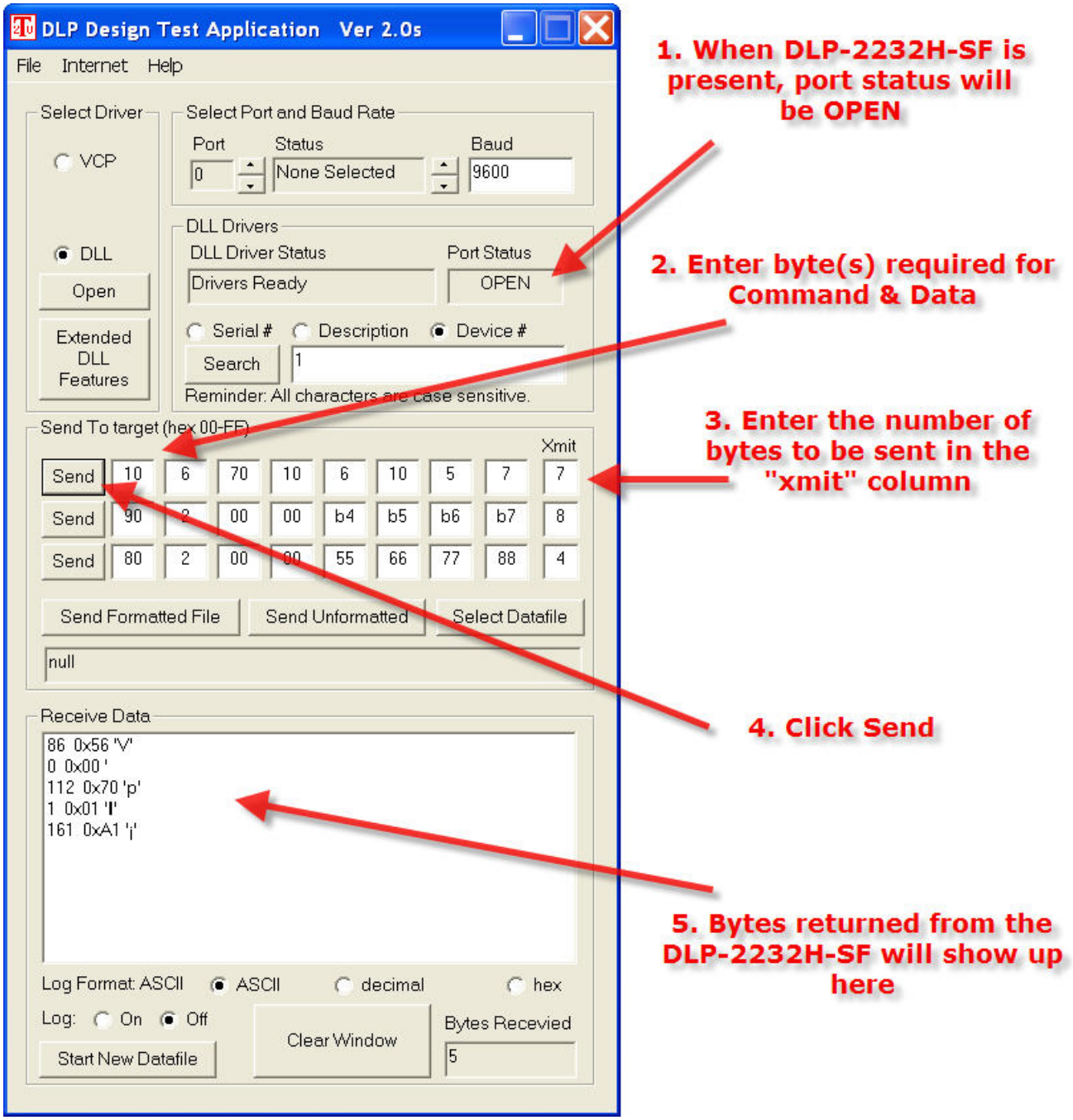
If there is a problem with the command sent, the DLP-2232H-SF module's program will return an error code to the host. The error codes always start with a hexadecimal "E". The error codes are explained in the following table:

TABLE 8			
Error Code Return Values Explained			
Error Code (Hex)	**Description**	**Source Hex Value**	**Comments**
0xE0	Invalid Register	FPGA Fabric	A valid version/status register read command (0x10) was received, but the requested register is out of range (0-5).
0xE1	Invalid Command	FPGA Fabric	An invalid command byte was sent from the host PC.
0xE2	Invalid Clear Pin Number	FPGA Fabric	A valid pin clear command (0x40) was received, but the pin specified does not match a valid pin number (see Table 1).
0xE3	Invalid Set Pin Number	FPGA Fabric	A valid pin set command (0x41) was received, but the pin specified does not match a valid pin number (see Table 1).
0xE4	Invalid Read Pin Number	FPGA Fabric	A valid pin read command (0x5x) was received, but the pin specified does not match a valid pin number (see Table 1).
0xE5	Invalid 8-Bit Shared Memory Access	FPGA Fabric	An 8-bit shared memory access was requested by the ARM MSS that specified an invalid location.
0xE6	Invalid 16-bit Shared Memory Access	FPGA Fabric	A 16-bit shared memory access was requested by the ARM MSS that specified an invalid location.
0xE7	Invalid 32-bit Shared Memory Access	FPGA Fabric	A 32-bit shared memory access was requested by the ARM MSS that specified an invalid location.
0xE8	ARM MSS Timeout	FPGA Fabric	The ARM MSS Core did not respond to the host command provided by the FPGA fabric within the 2-second limit.
0xE9	Invalid ARM Command	ARM MSS	An invalid ARM command value was specified.

12.0 USING THE DLP TEST APPLICATION (OPTIONAL)

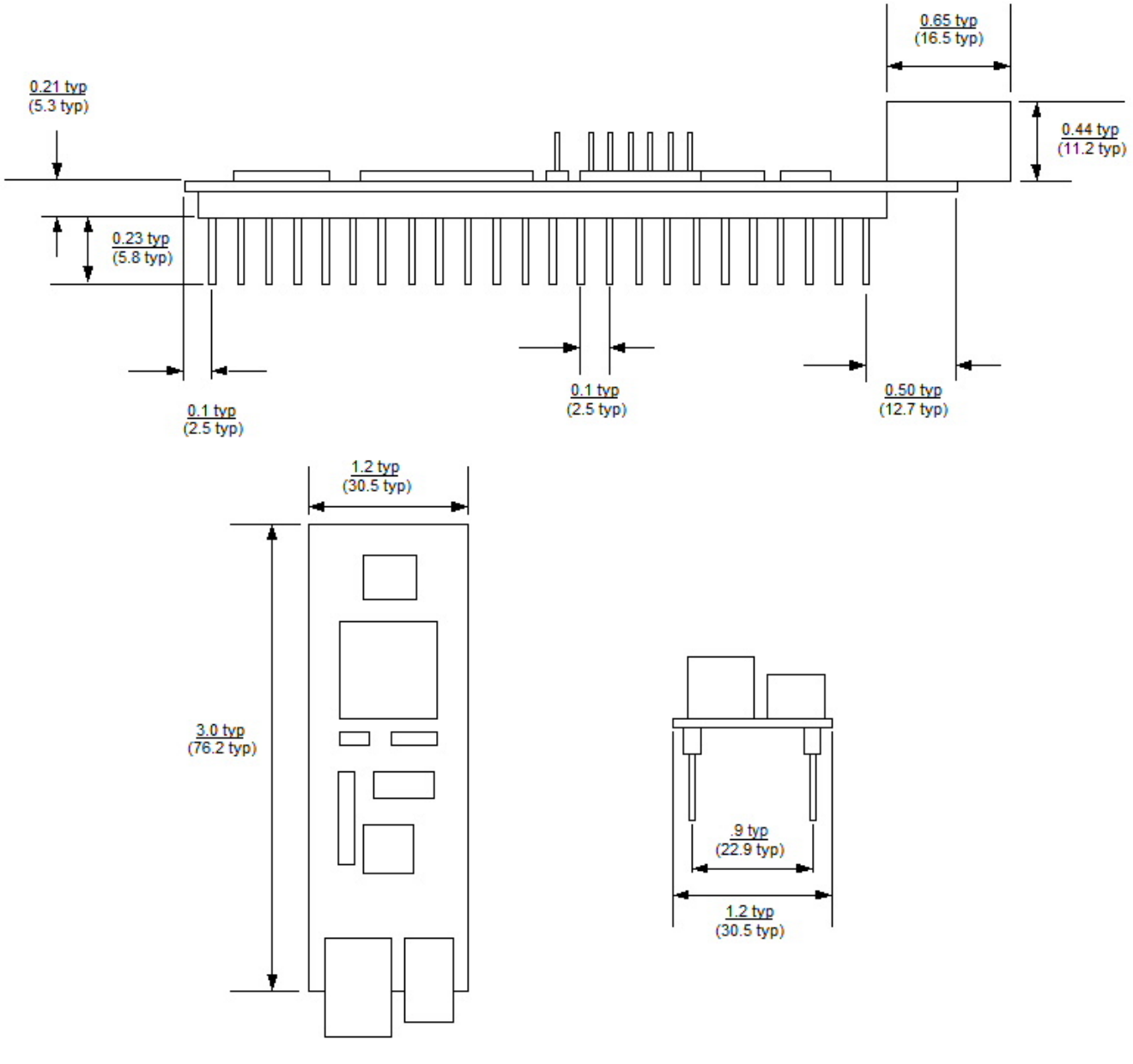
Users can either design their own host application interface to send USB commands to the DLP-2232H-SF module or utilize the test application tool available from DLP Design. The DLP Test Application is available in a free version for download from the DLP Design website at **www.dlpdesign.com/test.shtml**. Using this tool, single- and multi-byte commands can be sent to the DLP-2232H-SF board.

Once installed, the test application is used as follows:



The commands used to interface to the DLP-2232H-SF are detailed in Section 11 of this datasheet.

13.0 MECHANICAL DIMENSIONS IN INCHES (MM) (PRELIMINARY)



14.0 SCHEMATICS

Schematics for the DLP-2232H-SF are included on the last three pages.

15.0 DISCLAIMER

This product and its documentation are supplied on an as-is basis, and no warranty as to their suitability for any particular purpose is either made or implied. DLP Design, Inc. will not accept any claim for damages whatsoever arising as a result of the use or failure of this product. Your statutory rights are not affected. This product or any variant of it is not intended for use in any medical appliance, device or system in which the failure of the product might reasonably be expected to result in personal injury.

This document provides preliminary information that may be subject to change without notice.

16.0 CONTACT INFORMATION

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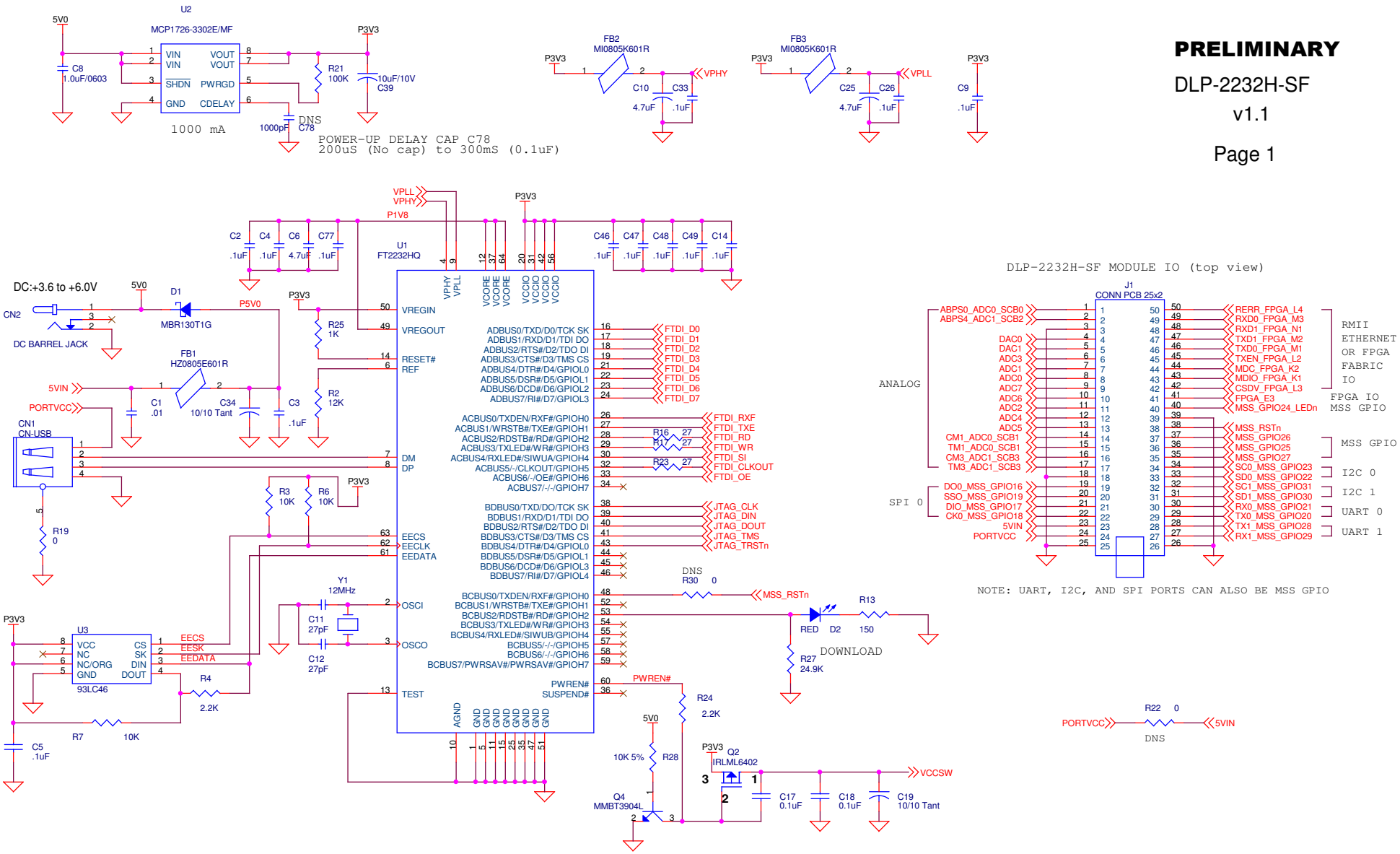
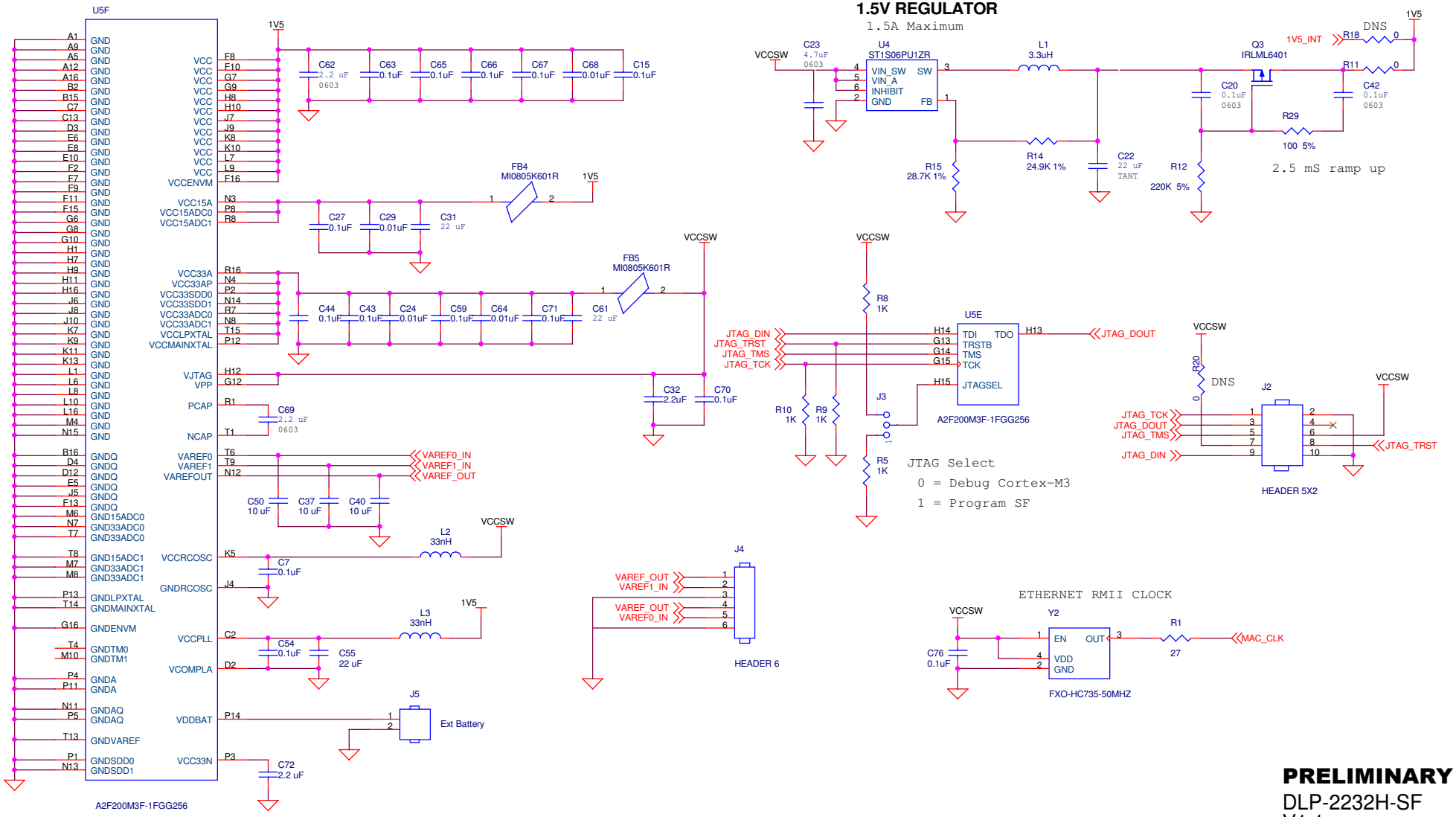
PRELIMINARY

DLP-2232H-SF

v1.1

Page 1




1.5V REGULATOR
1.5A Maximum
U5F
A2F200M3F-1FGG256
U4
ST1S06PU1ZR
VIN_SW
VIN_A
INHIBIT
GND
SW
FB
L1
3.3uH
C23
4.7uF
0603
VCCSW
1V5
1V5_INT
Q3
IRLML6401
R18
DNS
R11
C20
0.1uF
0603
C42
0.1uF
0603
R29
100 5%
2.5 mS ramp up
R15
28.7K 1%
R14
24.9K 1%
C22
22 uF
TANT
R12
220K 5%
C62
2.2 uF
0603
C63
0.1uF
C65
0.1uF
C66
0.1uF
C67
0.1uF
C68
0.01uF
C15
0.1uF
FB4
MI0805K601R
C27
0.1uF
C29
0.01uF
C31
22 uF
FB5
MI0805K601R
C44
0.1uF
C43
0.1uF
C24
0.01uF
C59
0.1uF
C64
0.01uF
C71
0.1uF
C61
22 uF
C32
2.2uF
C70
0.1uF
C69
2.2 uF
0603
C50
10 uF
C37
10 uF
C40
10 uF
L2
33nH
C7
0.1uF
L3
33nH
C54
0.1uF
C55
22 uF
J5
Ext Battery
C72
2.2 uF
R8
1K
R10
1K
R9
1K
R5
1K
J3
U5E
TDI
TDO
TRSTB
TMS
TCK
JTAGSEL
A2F200M3F-1FGG256
JTAG_DIN
JTAG_TRST
JTAG_TMS
JTAG_TCK
JTAG_DOUT
JTAG Select
0 = Debug Cortex-M3
1 = Program SF
R20
DNS
J2
HEADER 5X2
J4
HEADER 6
VAREF_OUT
VAREF1_IN
VAREF0_IN
ETHERNET RMII CLOCK
Y2
FXO-HC735-50MHZ
C76
0.1uF
R1
27
MAC_CLK
PRELIMINARY
DLP-2232H-SF
V1.1
Page 2