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dsPIC33CH Curiosity Development Board User's Guide

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Preface

NOTICE TO CUSTOMERS

All documentation becomes dated, and this manual is no exception. Microchip tools and documentation are constantly evolving to meet customer needs, so some actual dialogs and/or tool descriptions may differ from those in this document. Please refer to our website (www.microchip.com) to obtain the latest documentation available.

Documents are identified with a "DS" number. This number is located on the bottom of each page, in front of the page number. The numbering convention for the DS number is "DSXXXXXXXXA", where "XXXXXXXX" is the document number and "A" is the revision level of the document.

For the most up-to-date information on development tools, see the MPLAB® IDE on-line help. Select the Help menu, and then Topics to open a list of available on-line help files.

INTRODUCTION

This preface contains general information that will be useful to know before using the dsPIC33CH Curiosity Development Board. Topics discussed in this preface include:

- Document Layout
- Conventions Used in this Guide
- Recommended Reading
- Recommended Reading
- The Microchip WebSite
- Development Systems Customer Change Notification Service
- Customer Support
- Document Revision History

DOCUMENT LAYOUT

This user's guide provides an overview of the dsPIC33CH Curiosity Development Board. The document is organized as follows:

- **Chapter 1. "Introduction"** – This chapter introduces the dsPIC33CH Curiosity Development Board and provides a brief overview of its features.
- **Chapter 2. "Hardware"** – This chapter describes some of the noteworthy hardware features of the board.
- **Appendix A. "Schematics"** – This appendix provides schematic diagrams for the dsPIC33CH Curiosity Development Board.
- **Appendix B. "Bill of Materials (BOM)"** – This appendix provides the component list used in assembling the board.

CONVENTIONS USED IN THIS GUIDE

This manual uses the following documentation conventions:

DOCUMENTATION CONVENTIONS

Description	Represents	Examples
Arial font:		
Italic characters	Referenced books	*MPLAB® IDE User's Guide*
	Emphasized text	...is the *only* compiler...
Initial caps	A window	the Output window
	A dialog	the Settings dialog
	A menu selection	select Enable Programmer
Quotes	A field name in a window or dialog	"Save project before build"
Underlined, italic text with right angle bracket	A menu path	*File>Save*
Bold characters	A dialog button	Click **OK**
	A tab	Click the **Power** tab
N'Rnnnn	A number in verilog format, where N is the total number of digits, R is the radix and n is a digit.	4'b0010, 2'hF1
Text in angle brackets < >	A key on the keyboard	Press <Enter>, <F1>
Courier New font:		
Plain Courier New	Sample source code	`#define START`
	Filenames	`autoexec.bat`
	File paths	`c:\mcc18\h`
	Keywords	`_asm, _endasm, static`
	Command-line options	`-Opa+, -Opa-`
	Bit values	`0, 1`
	Constants	`0xFF, 'A'`
Italic Courier New	A variable argument	*`file`*`.o`, where *`file`* can be any valid filename
Square brackets [ ]	Optional arguments	`mcc18 [options]` *`file`* `[options]`
Curly braces and pipe character: { | }	Choice of mutually exclusive arguments; an OR selection	`errorlevel {0|1}`
Ellipses...	Replaces repeated text	`var_name [, var_name...]`
	Represents code supplied by user	`void main (void) { ... }`

RECOMMENDED READING

This user's guide describes how to use the dsPIC33CH Curiosity Development Board. The device-specific data sheets contain current information on programming the specific microcontroller or Digital Signal Controller (DSC) devices. The following Microchip documents are available and recommended as supplemental reference resources:

MPLAB® XC16 C Compiler User's Guide (DS50002071)

This comprehensive guide describes the usage, operation and features of Microchip's MPLAB XC16 C compiler (formerly MPLAB C30) for use with 16-bit devices.

MPLAB® X IDE User's Guide (DS50002027)

This document describes how to set up the MPLAB X IDE software and use it to create projects and program devices.

dsPIC33CH128MP508 Family Data Sheet (DS70005319)

Refer to this document for detailed information on the dsPIC33CH Dual Core Digital Signal Controllers (DSCs). Reference information found in this data sheet includes:

- Device memory maps
- Device pinout and packaging details
- Device electrical specifications
- List of peripherals included on the devices

dsPIC33/PIC24 Family Reference Manual Sections

Family Reference Manual (FRM) sections are available, which explain the operation of the dsPIC® DSC MCU family architecture and peripheral modules. The specifics of each device family are discussed in the individual family's device data sheet.

THE MICROCHIP WEBSITE

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- **General Technical Support** – Frequently Asked Questions (FAQs), technical support requests, online discussion groups, Microchip consultant program member listing
- **Business of Microchip** – Product selector and ordering guides, latest Microchip press releases, listing of seminars and events, listings of Microchip sales offices, distributors and factory representatives

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The Development Systems product group categories are:

- **Compilers** – The latest information on Microchip C compilers and other language tools. These include the MPLAB® C compiler; MPASM™ and MPLAB 16-bit assemblers; MPLINK™ and MPLAB 16-bit object linkers; and MPLIB™ and MPLAB 16-bit object librarians.
- **Emulators** – The latest information on the Microchip MPLAB REAL ICE™ in-circuit emulator.
- **In-Circuit Debuggers** – The latest information on the Microchip in-circuit debugger, MPLAB ICD 4.
- **MPLAB X IDE** – The latest information on Microchip MPLAB X IDE, the Windows® Integrated Development Environment for development systems tools. This list is focused on the MPLAB X IDE, MPLAB SIM simulator, MPLAB X IDE Project Manager and general editing and debugging features.
- **Programmers** – The latest information on Microchip programmers. These include the MPLAB PM3 device programmer and the PICkit™ 3 development programmers.

CUSTOMER SUPPORT

Users of Microchip products can receive assistance through several channels:

- Distributor or Representative
- Local Sales Office
- Field Application Engineer (FAE)
- Technical Support

Customers should contact their distributor, representative or field application engineer (FAE) for support. Local sales offices are also available to help customers. A listing of sales offices and locations is included in the back of this document.

Technical support is available through the website at: http://support.microchip.com

DOCUMENT REVISION HISTORY

Revision A (June 2018)

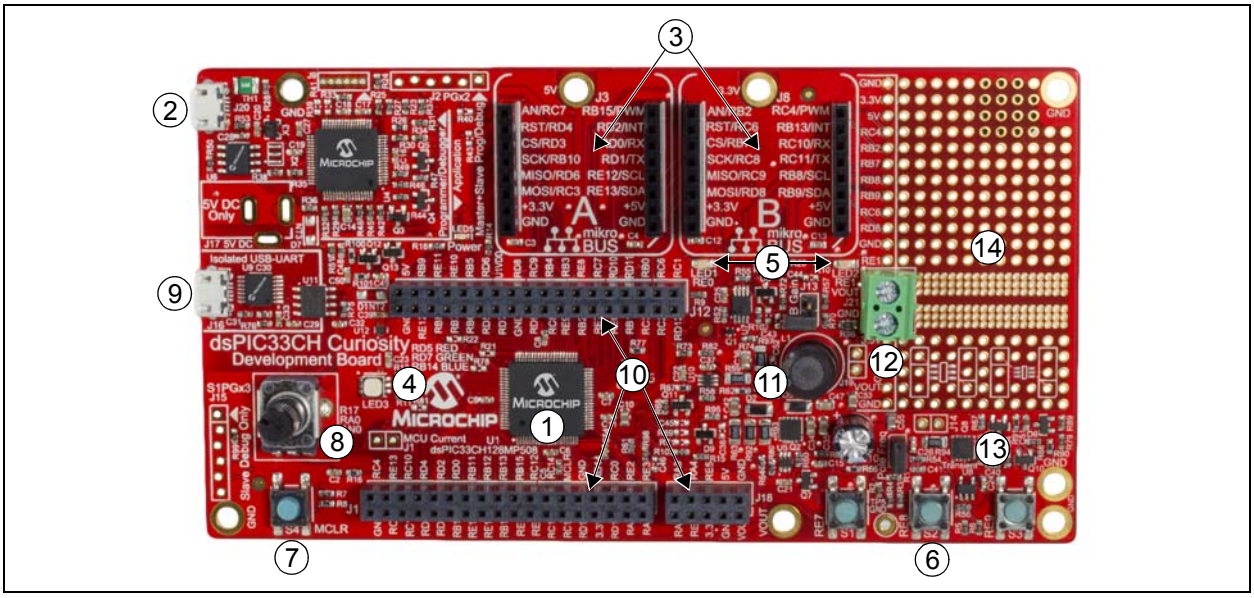
This is the initial released version of this document.

NOTES:

Chapter 1. Introduction

The dsPIC33CH Curiosity Development Board (DM330028) is intended as a cost-effective development and demonstration platform for the dsPIC33CH128MP508 family of dual core, high-performance Digital Signal Controllers. Some of the board hardware features are highlighted in Figure 1-1.

FIGURE 1-1: dsPIC33CH CURIOSITY DEVELOPMENT BOARD



Hardware Features:

1. dsPIC33CH128MP508 dual core, 16-bit DSP target device.
2. Integrated PICkit™-On-Board (PKOB) programmer/debugger.
3. 2x mikroBUS™ interfaces for hardware expansion, compatible with a wide range of existing click boards™ from MikroElektronika (www.mikroe.com).
4. 1x Red/Green/Blue (RGB) LED.
5. 2x general purpose red indicator LEDs.
6. 3x general purpose push buttons.
7. 1x $\overline{\text{MCLR}}$ Reset push button.
8. 10k potentiometer.
9. Galvanically isolated USB-UART interface, capable of up to 460,800 baud.
10. Female, 100 mil pitch, I/O pin access headers for probing and connecting to all target microcontroller GPIO pins.
11. Configurable Switch Mode Power Supply (SMPS) test circuit that can be operated in Buck, Boost, or Buck-Boost modes, using either Voltage mode or Peak Current mode control.
12. Converter output voltage screw terminal.
13. Configurable load step transient generator.
14. General purpose through-hole and SMT prototyping area.

1.1 SCHEMATICS AND BILL OF MATERIALS (BOM)

Schematics and the BOM for the dsPIC33CH Curiosity Development Board are located in **Appendix A. "Schematics"** and **Appendix B. "Bill of Materials (BOM)"**, respectively.

Chapter 2. Hardware

2.1 POWERING THE BOARD

2.1.1 USB Power

The board is intended to be primarily powered from the PKOB USB micro-B connector J20. Power is not sourced through USB connector J16, as it is part of the isolated USB-UART interface. The official *"USB 2.0 Specification"* restricts USB applications to consuming no more than 500 mA of USB VBUS power from the host. Polyfuse TH1 is rated for 500 mA to enforce the USB current restrictions and to help protect the board, or host, from damage in the event of unintended short circuits or SMPS output overloads.

When operating the board from USB power, approximately 300 mA of VBUS current is available to the SMPS circuit, as about 200 mA of the total should be reserved for use by the other non-SMPS circuitry on the board (ex: primarily U1, U4, U11, R17, LED5, etc.).

2.1.2 External Power

An external DC wall cube may optionally be connected if a DC barrel jack is installed in the unpopulated footprint J17. If an external wall cube is used, it should be well regulated and rated for 5.0V, ≤1.5A, with center pin positive. Compared to operating from USB power, powering the board with an external wall cube enables more power to be sourced by the SMPS circuit on the board. It is not necessary to use an external power supply for standard operation at lower current levels (e.g., SMPS circuit output load power of about <1.2W).

When the board is powered through J17, the polyfuse TH1 is bypassed, and therefore, it is recommended to use a wall cube with internal short circuit and overload protection (≤1.5A) to minimize the risk of circuit damage in the event of unintended short circuits. Additionally, if an external wall cube is used, it is recommended to cut a trace (NT2 on the top of the PCB) and populate D1 with a ≥1A rated Schottky diode (SOD-123). This will prevent any USB VBUS "backdrive" current from flowing out of the wall cube and into the attached host via J20. USB VBUS backdrive currents may not necessarily be destructive (when limited in current level), but are a USB compliance violation. They can interfere with the host operation, especially when the host is unpowered. This scenario can be avoided, however, via D1.

2.2 USING THE PROGRAMMED DEMO FIRMWARE

The development board comes programmed with some basic demo firmware, which exercises several of the board hardware features. For details on how to use the programmed demo firmware, please refer to the documentation associated with the source code for the demo, which can be obtained from:

www.microchip.com/dspic33chcuriosity

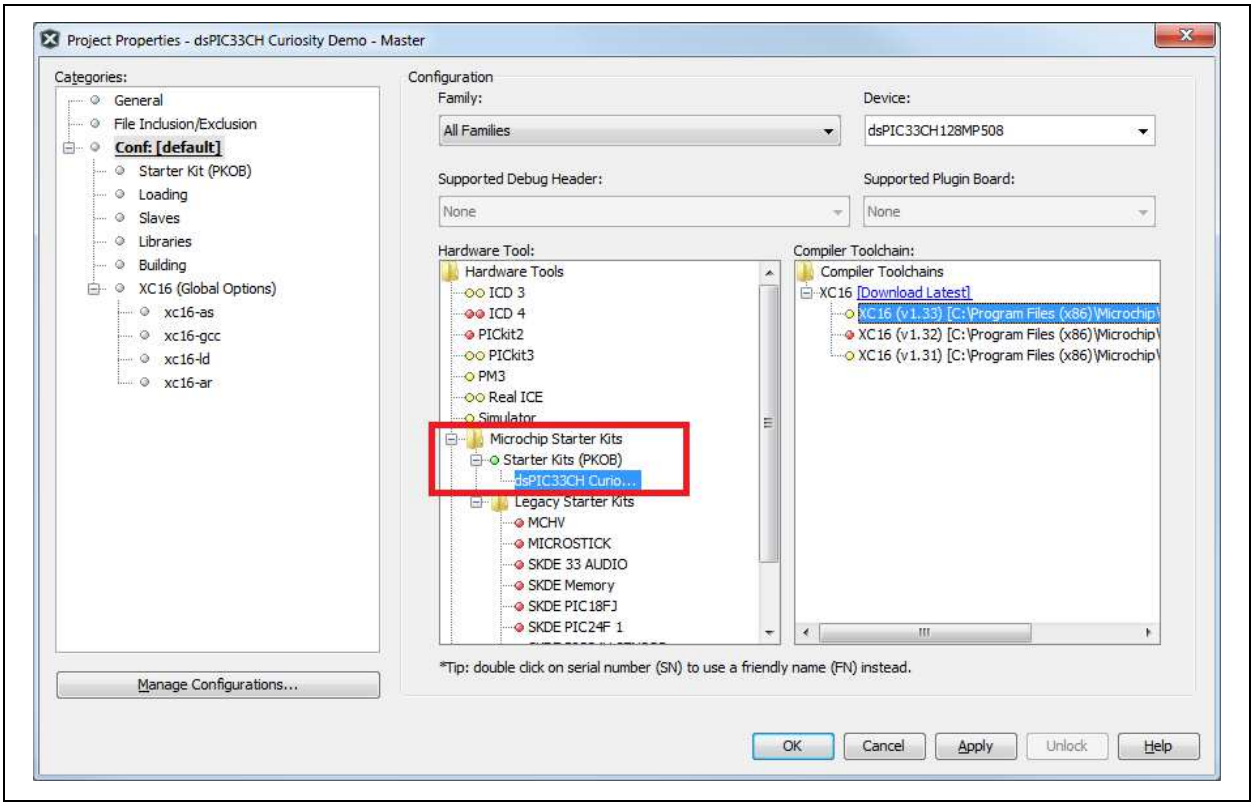
2.3 REPROGRAMMING AND DEBUGGING THE dsPIC33CH128MP508 DEVICE (U1)

The board has a PICkit-On-Board (PKOB) programmer/debugger circuit, which can be used to program and debug both the Master and Slave cores in the dsPIC33CH128MP508 target device (U1). Alternatively, an external programmer/debugger tool can be connected to the board via the 6-pin inline connector J2, using a male-male 100 mil pitch 6-pin header.

During simultaneous "dual debug" of both the Master and Slave cores, two debugger tools are required. During simultaneous dual debug operation, the PKOB circuit can be used to debug the Master core, while an external programmer/debugger tool should be connected via the 6-pin 100 mil pitch connector J15 using a male-male header. Two programmer/debugger tools are only required when performing dual core simultaneous debug operations. When programming or debugging only a single core (either Master or Slave) at a time, the on-board PKOB circuit is sufficient.

The PKOB circuit should automatically enumerate and be recognized by the MPLAB® X IDE v4.10 or later, when the Curiosity Board is connected to the host via the USB micro-B connector J20. No custom USB driver installation is necessary as the PKOB circuit relies on standard OS provided HID drivers, and therefore, driver installation should be fully automatic. When plugged in, the PKOB programmer/debugger tool can be selected from the MPLAB X project properties page by selecting the device under: *Hardware Tools>Microchip Starter Kits>Starter Kits (PKOB)>dsPIC33CH Curio…*, as shown in Figure 2-1.

FIGURE 2-1: dsPIC33CH CURIOSITY PKOB TOOL SELECTION



2.4 USING THE ISOLATED USB-UART INTERFACE

The board implements a galvanically isolated USB-UART interface based around the MCP2221A chip. The MCP2221A implements the standard Communication Device Class (CDC) – Abstract Control Model (ACM) protocol, and therefore, can use standard USB drivers that are provided with modern Windows®, Mac® and Linux® operating systems. Under most operating systems, the USB driver installation will be fully automatic. Under certain older operating systems, or if the device is attached to an older than Windows 10 machine without an active internet connection, manual installation of the drivers may be necessary. In this case, the driver package can be downloaded from:

www.microchip.com/mcp2221a

Details on how to access the serial port from Mac and Linux operating systems can also be found in the associated collateral for the MCP2221A. Under Windows, after successful USB driver installation, the device will appear as a “COMx” port object, which standard serial terminal programs can open/read/write to and from.

2.5 CIRCUIT DETAILS

Some of the circuit blocks in the schematics may not have immediately obvious purpose or method of operation. This section highlights some of these circuit elements and provides an explanation for their intent and function.

2.5.1 Jumpers/Headers/Connectors

J1 – This is an unpopulated 2-pin, 100 mil jumper header, which may optionally be used to insert a current meter in series with the U1 V_{DD} current path to measure the microcontroller current consumption. In order to measure the U1 current, the trace on the bottom of the PCB, that shorts the two pins of J1, should be cut and a 2-pin jumper should be soldered into J1.

J2 – This is an unpopulated 6-pin staggered header interface, which can optionally be used to connect an external programmer/debugger tool to the target microcontroller U1. Ordinarily, it is not necessary to use J2, since the integrated programmer/debugger (PKOB) circuit connects to the same U1 program/debug interface pins.

J3 – This is a female header that implements the mikroBUS Interface A, which can be used to attach hardware daughter boards to expand the functionality of the development board.

J8 – This is a female header that implements the mikroBUS Interface B, which can be used to attach hardware daughter boards to expand the functionality of the development board.

J10 – This jumper sets the -3 dB low-pass filter breakpoint frequency of the RC network, composed of R54 + C26/C41. When the jumper is open, the low-pass filter frequency is around 15.9 kHz, but with the jumper capped, it is around 1.4 kHz. When a sufficiently high-frequency PWM waveform is generated on RC5, the low-pass filter can smooth it into a near DC value, which is buffered by op amp U8, providing a software controlled DAC capability.

J11 – This is a female I/O pin access header used for accessing the U1 microcontroller I/O pins.

J12 – This is a female I/O pin access header used for accessing the U1 microcontroller I/O pins.

J13 – This jumper sets the effective resistor divider feedback ratio for the SMPS output voltage when it is measured by the U1 ADC. When the SMPS is used to generate relatively low voltages (ex: 0V-6.5V), it is suggested to keep J13 capped to maximize feedback circuit sensitivity. When the SMPS will be used to generate voltages above 6.5V, J13 should be opened to ensure the feedback voltage stays within the input sensing range of the ADC.

J14 – This is an unpopulated 2-pin jumper location that can be used to disconnect the SMPS transient generator circuitry from the output of the SMPS circuit. In order to disconnect the transient generator circuit, it is suggested to populate J14 with a 2-pin jumper header and to cut the trace (NT5) on the bottom of the PCB linking the pins of J14.

J15 – This is an unpopulated 6-pin staggered header interface that can optionally be used to connect an external programmer/debugger tool to the target microcontroller U1 when performing dual simultaneous debug of both the Master and Slave cores. The J15 header connects to the Slave debug port, S1PGx3, and is only intended for use during dual debug operations. For single core debug of either the Master or Slave, either J2 or the PKOB circuit should be used. The holes for J15 are slightly staggered, which provides some friction retention force, without requiring physical soldering, when a straight male-male or right angle male-male header is installed in J15.

J16 – This is a standard female USB micro-B connector, which connects to the MCP2221A USB-UART converter chip. This USB interface is a data interface only, as it is galvanically isolated from the rest of the application circuitry and does not supply power to the rest of the board.

J17 – This is an unpopulated footprint that may optionally be used to install a standard DC barrel jack for externally powering the board from a regulated 5.0V wall cube.

J18 – This is a female I/O pin access header for accessing certain U1 microcontroller I/O pins, along with the various power rails implemented on the development board.

J19 – This is an unpopulated 2-pin jumper header, that may optionally be used as an attachment point for connecting an external frequency response analyzer tool, for measuring the SMPS control loop phase/gain characteristics. The 20 Ohm load resistor (R96) is connected directly across the J19 pins.

J20 – This is a standard female USB micro-B connector that is intended to be used to power the board and provide a USB communication path when using the integrated programmer/debugger (PKOB) circuit.

J21 – This is a 2-pin screw terminal that provides access to the SMPS VOUT and GND nets. This is a convenient place for attaching external loads that may be powered by the SMPS circuit.

2.5.2 SMPS Hardware Overcurrent Protection

The components, Q11, C22, R67, U10, and the high-side current sense resistors, R59 + R74, implement a crude form of hardware-based overcurrent protection. In a normal/real application SMPS design, overcurrent protection is often provided through the use of comparator(s), which would typically be implemented using the comparators and DACs inside the microcontroller. However, during initial firmware development, the code for enabling the DACs + comparators may not have been written and debugged yet, at the time of, say, accidentally dropping an oscilloscope ground lead onto the demo board. This could result in an unanticipated random short circuit. In these scenarios, the hardware overcurrent protection circuit implemented by Q11, U10 and surrounding components can potentially help protect the circuit from damage.

During an overcurrent condition, when the current through R59 + R74 starts to exceed approximately 1.2A (ex: 600 mV sense voltage), the base of Q11 will become forward biased and it will begin to turn on. This will quickly charge the capacitor C22 to the Schmitt trigger V_{IH} input logic high threshold of the U10 logic chip (which is configured as a Schmitt trigger OR gate). Once the V_{IH} level is reached, the U10 output will go high (independent of the RC14_S1PWM7H signal), thus turning off the high-side P-channel MOSFET Q6.

At this point, the current through Q6 will drop to zero, Q11 will turn off, but C22 will remain charged near the V_{IH} level until it is eventually bled down to the V_{IL} level through R67. The U10 output will not immediately switch back on due to the Schmitt trigger hysteresis voltage between the V_{IH} and V_{IL} input thresholds of U10. It takes approximately 40% of an RC time constant (between C22 + R67) for the V_{IL} threshold to be reached, which enforces a minimum Q6 off time of roughly 80 µs. This delay is sufficient for the L1 inductor current to drop all the way to zero due to the energy loss in the diodes D2, D5 and the resistance in the freewheeling current path.

Therefore, even during short-circuit conditions with improperly implemented firmware control signals, the average current can be maintained at a reasonably safe level. Once the firmware for enabling and using the internal U1 comparators and DACs has been developed/debugged, it is expected that the Q11 and related hardware overcurrent protection components would be omitted, since they would become somewhat redundant in the final application design.

2.5.3 SMPS Hardware Overvoltage Protection

The components, Q7, C15, R64, R65, R66 and U5, implemented a hardware-based output overvoltage protection feature in a manner similar to the hardware overcurrent protection circuit. When a conventional boost converter is operated open loop without enough load on the output, the output voltage can theoretically rise to an indeterminate high level, which can potentially avalanche the output Schottky diode, the boost MOSFET or the output capacitors.

When the output voltage rises above approximately 16V, the output of the resistor divider (R65 + R66) will become high enough to begin forward biasing the Q7 base and turning on the transistor. This will quickly discharge C15 from 3.3V down to the V_{IL} Schmitt trigger input threshold of the Schmitt AND gate implemented by U5. This overrides the PWM control signal and shuts down Q2 until such time as the output overvoltage condition has decayed away, and enough time has elapsed for R64 to charge C15 back up to the V_{IH} Schmitt trigger input threshold of U5 (automatically re-enabling PWM activity on Q2).

In a typical/real SMPS application, the closed-loop output feedback control loop would normally be responsible for preventing output overvoltage conditions from occurring. However, during initial firmware development, the closed-loop control algorithms may not yet be fully implemented and operational (or may be halted from normal operation, for example, due to hitting a debug breakpoint in the firmware). In these scenarios, the hardware output overvoltage protection circuitry can help to prevent potential circuit damage.

2.5.4 PWM DAC/DC Bias Generator

The RC5_S1PWM2L net is intended to be driven with a fixed frequency PWM waveform. The low-pass filter, consisting of R54 + C26 (and C41 when jumper J10 is capped), averages the PWM waveforms, and for a high PWM frequency, generates an adjustable DC voltage. Op amp U8 buffers the DC voltage, providing a low-impedance firmware adjustable DAC, where the output voltage is based on the PWM duty cycle provided to the circuit.

2.5.5 Transient Load Tester Circuit

The MOSFET Q8 and surrounding components implement an adjustable constant-current sink that can be periodically pulsed on for a few milliseconds at a time to generate momentary SMPS output load transient pulses. During control loop firmware development, it is often desirable to study the control system behavior in response to large signal step changes.

By monitoring the SMPS output voltage waveforms in response to the load step transient event, one can get an idea of the real world output voltage undershoot during the transient and the subsequent overshoot that will occur after the transient load is rapidly removed. Additionally, the transient response recovery waveform shapes can also provide hints as to likely control loop stability and approximate phase margin.

Load step transient response curves exhibiting damped sinusoidal oscillating output voltage, that takes a long time to recover to steady-state DC values, implies a control loop with low phase margin, while an over damped RC-like recovery waveform implies higher phase margin.

When the RC13_TRANSIENT logic signal is driven high, the MOSFET Q8 will begin to turn on through the gate resistor R79. However, as the gate voltage rises, current will begin to flow through the MOSFET and current sense resistor R94, which will create a voltage that is sensed by Q9. When the voltage at the base of Q9 is sufficient to turn it on, it will begin sinking current from the gate of Q8, preventing the gate voltage from rising further and maintaining MOSFET Q8 in the linear region, where it behaves like a voltage controlled constant-current sink.

Components, R83 and C40, provide compensation for the MOSFET Q8 gate waveform to ensure small signal stable regulation of the constant current. The relative sizes of R79 and R87 set the DC gain of the constant-current regulation control loop.

The value of current sense resistor R94 sets the current limit, but it is made adjustable by biasing the base of Q9, up or down, via the resistor dividers R84 and R85. When the S1PWM2L_DAC_ISET DC voltage level is high (e.g., near 3.3V), Q9 will always be turned on, even with no current through R94 due to the resistor divider output (of R84 + R85) being higher than the turn-on voltage of the BJT Q9. Conversely, when the S1PWM2L_DAC_ISET DC voltage is low (e.g., near 0.0V), this decreases the voltage appearing on the Q9 base, requiring larger currents through R94 before the MOSFET Q8 gate voltage becomes limited.

Adjusting the PWM waveform duty cycle on RC5_S1PWM2L by +1.0% alters the Q8 constant-current sink value by approximately -12 mA. At 50% PWM duty cycle, the approximate current sink level is around 390 mA, but will vary somewhat between boards and at different ambient temperatures, as these will affect the Q9 turn-on voltage. For exact current sink values, it is necessary to use closed-loop control by measuring the RA2_TRANSIENTFB current sense voltage with the ADC at run time. Then, using the resulting value to fine-tune adjust the PWM duty cycle on RC5_S1PWM2L.

Since Q8 is driven in the linear region during the transient pulse, the instantaneous power dissipation within the MOSFET can be quite high, potentially up to 15W if the circuit is configured for 15V output and 1A pulse load current. This power dissipation level cannot be sustained indefinitely without a substantial heat sink, but for short pulses (ex: ≤100 ms based on the safe operating area graph in the MCP87130T MOSFET data sheet), the thermal inertia of the MOSFET die and package allow the junction temperature to stay below the 150ºC maximum of the device. However, in between pulses, enough time must be allowed for the die and package to cool back to room temperature, before the next pulse, in order to ensure reliable operation of the circuit. It is therefore recommended to control RC13_TRANSIENT, so as to generate short pulses (ex: ≤10 ms) with long off times between pulses (ex: pulse rate of ~5 Hz).

In the event of improper firmware control of the RC13_TRANSIENT net (e.g., DC logic high or high time pulses > 10 ms), Q8 would potentially experience high sustained power dissipation, and unless protected somehow, would be vulnerable to thermal failure. To prevent this scenario, components, Q10, R88, C51, R90 and R91, implement a crude maximum on-time restricting sub-circuit, which is intended to limit the Q8 on time to roughly 10 ms maximum.

When RC13_TRANSIENT goes high, C51 begins charging through R88 and will eventually reach approximately 2x the VBE forward voltage necessary to turn on Q10. At this point, the output voltage of the resistor dividers, R90 and R91, rises high enough that Q10 begins turning on, sinking current/voltage away from the gate of Q8 and eventually turning off the MOSFET Q8. When RC13_TRANSIENT is eventually driven logic low, C51 discharges through R90 and R91, resetting the circuit automatically.

2.6 LOW-SIDE CURRENT SENSING

During Buck mode operation, it is sometimes desirable to be able to measure the current during the off time of MOSFET Q6 if implementing some form of “peak valley” or Average Current mode control algorithm. Low-side current sensing during the MOSFET off time is possible via the current sense resistors, R63, R92 and R93. However, the voltage developed across the current sense resistors will be a negative voltage with respect to ground. The signal is therefore connected to the inverting input of one of the PGAs in the microcontroller, which can then be used to invert and amplify the negative voltage into a positive voltage that can be measured by the ADC or used by a comparator inside the device.

When supplying a negative input voltage to the PGA, it is important to maintain the I/O pin voltage within the absolute maximum ratings from the device data sheet, which allows for negative voltages only within V_{SS} to (V_{SS} – 300 mV) range. Therefore, Schottky diode D9 and resistor R95 are used to clamp the negative voltages to within the 0V to -300 mV range. However, it is important to be aware that the inverting inputs to the PGAs on the device have approximately 10k typical input impedance from the device data sheet, and therefore, the resistance of R95 will reduce the gain of the amplifier for a given PGA setting. Such that, in this configuration, the firmware should not rely on the absolute output voltage of the PGA to reflect the true current through the sense resistors, unless the overall gain of the complete circuit is directly measured and factored into the computations in the firmware.

2.7 HIGH-SIDE CURRENT SENSING

The SMPS on-time current can be measured by the voltage developed across the high-side current sense resistors, R59 and R74. However, the ISENSEH signal is referenced to the +5V input rail of the SMPS circuit (not to ground), which prevents it from being measured directly by the ADC or comparators in the microcontroller U1. Therefore, the ISENSEH voltage signal is level shifted (to be ground referenced) and amplified by the components, U7A, Q1, R52 and R98, with an effective gain of 3.3.

Components, R97 and R102, add a small DC bias (approximately -71 mV, before level shifter gain or about +235 mV at RA3_ISENSEH), which appears at the RA3_ISENSEH microcontroller pin as an intentional offset error in the current measurement. This intentional DC biasing ensures that the current sense voltage signal is always within the U1 comparator input sensing range and the internal DAC reachable range, even when the Q6 current is exactly 0.0 mA with realistic comparator and DAC offset voltages.

The final output voltage on RA3_ISENSEH is related to the Q6 current approximately, as shown in Equation 2-1 and Equation 2-2 (where RA3_ISENSEH is the voltage in volts measurable with the microcontroller ADC; V_{IN} is the +5V rail input voltage, which may be ~4.6V under load during operation and IQ6 is the current through the MOSFET Q6 in amps). Equation 2-1 and Equation 2-2 were derived by simplifying and substituting resistor values into Equation 2-3 through Equation 2-6, which in turn, were derived from the schematic implementation.

EQUATION 2-1:

$$RA3\_ISENSEH \cong 0.04877 \bullet V_{IN} + 1.626 \bullet IQ6$$

EQUATION 2-2:

$$IQ6 \cong \frac{RA3\_ISENSEH - 0.04877 \bullet V_{IN}}{1.626}$$

EQUATION 2-3:

$$Rsense = \left(\frac{1}{R59} + \frac{1}{R74}\right)^{-1} = 0.5\ Ohms$$

EQUATION 2-4:

$$ISENSEH\_BIASED = (V_{IN} - IQ6 \bullet Rsense)\ \frac{R102}{(R102 + R97)}$$

EQUATION 2-5:

$$RA3\_ISENSEH = \frac{R98}{R52}\ (V_{IN} - ISENSEH\_BIASED)$$

EQUATION 2-6:

$$RA3\_ISENSEH = \frac{R98}{R52}\left[V_{IN} - \left(\frac{(V_{IN} - IQ6 \bullet Rsense)(R102)}{R102 + R97}\right)\right]$$

Appendix A. Schematics

The schematics for the dsPIC33CH Curiosity Development Board (DM330028) are shown in Figure 1 through Figure 4.

FIGURE A-1: dsPIC33CH CURIOSITY BOARD SCHEMATIC REV. 1.0 (SHEET ONE OF FOUR)

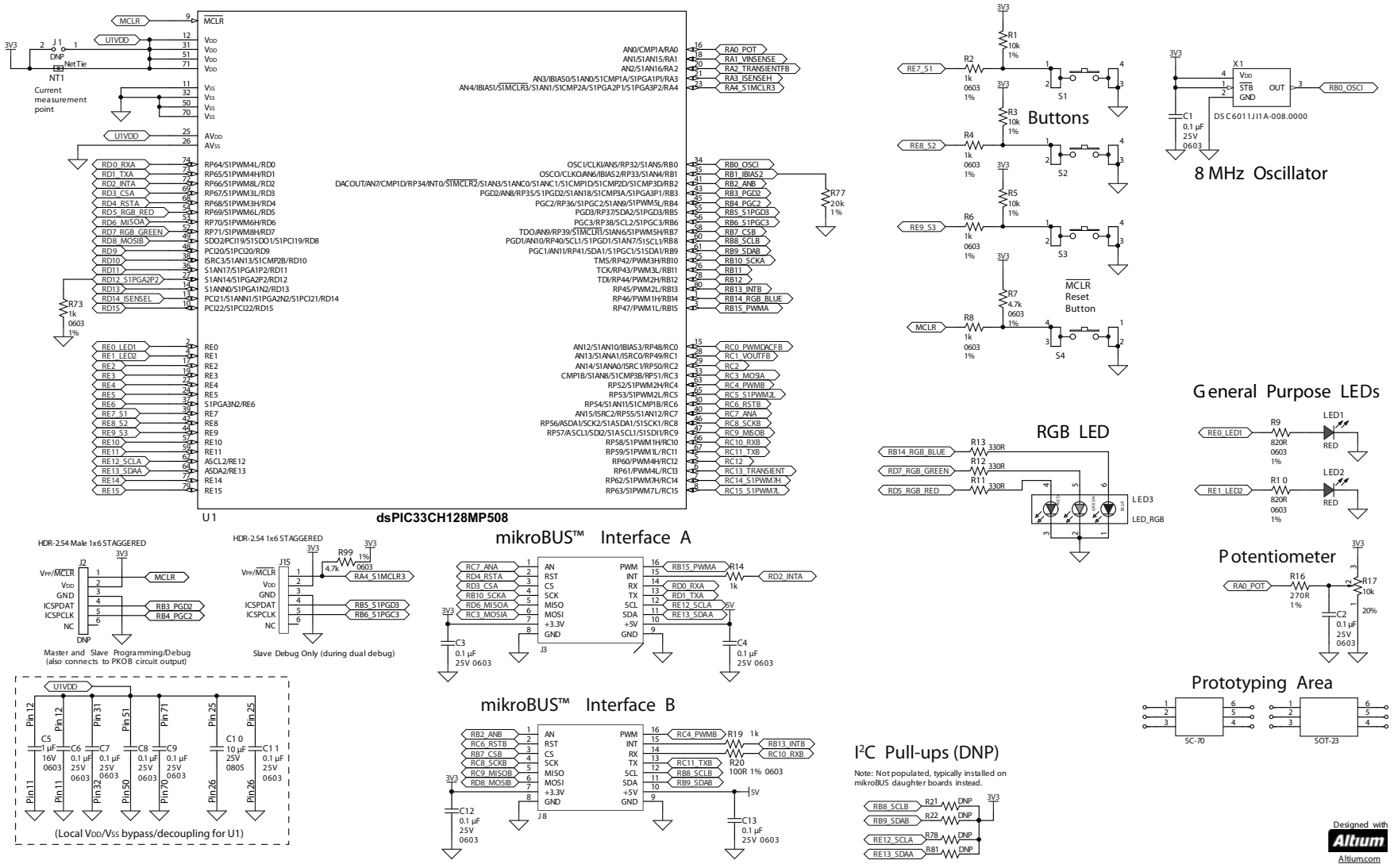
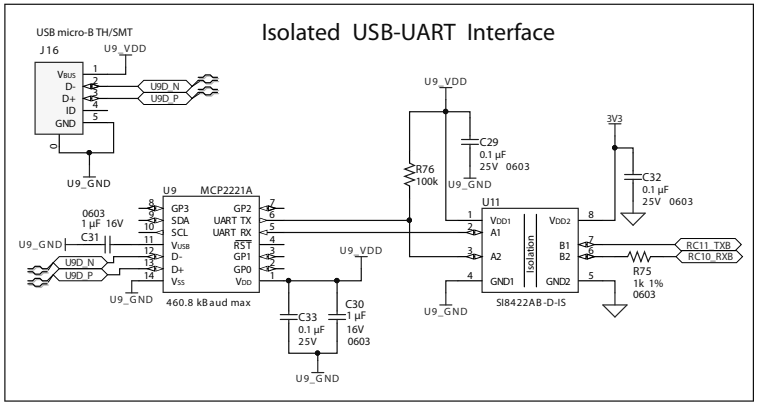
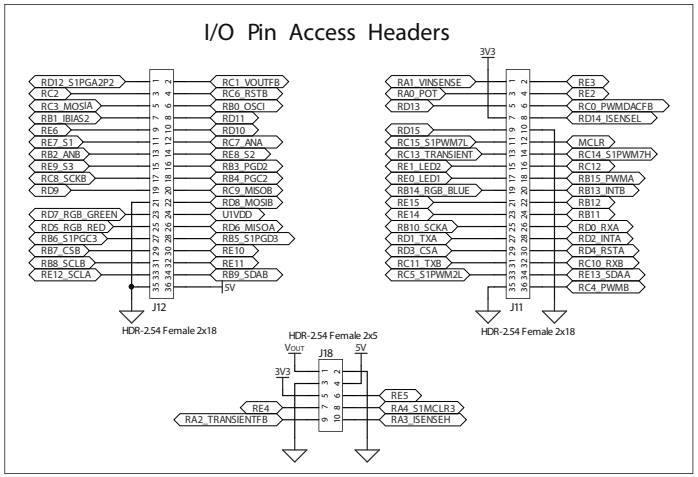


FIGURE A-2: dsPIC33CH CURIOSITY BOARD LAYOUT SCHEMATIC REV. 1.0 (SHEET TWO OF FOUR)





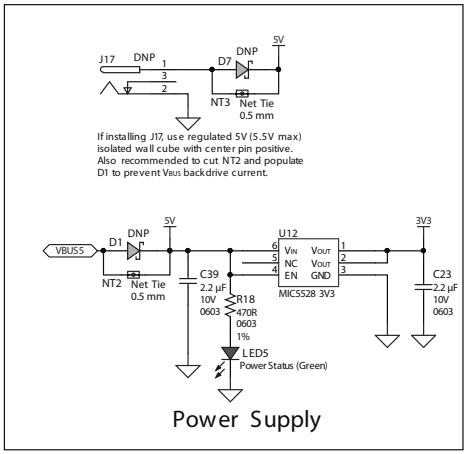


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FIGURE A-3: dsPIC33CH CURIOSITY BOARD LAYOUT SCHEMATIC REV. 1.0 (SHEET THREE OF FOUR)

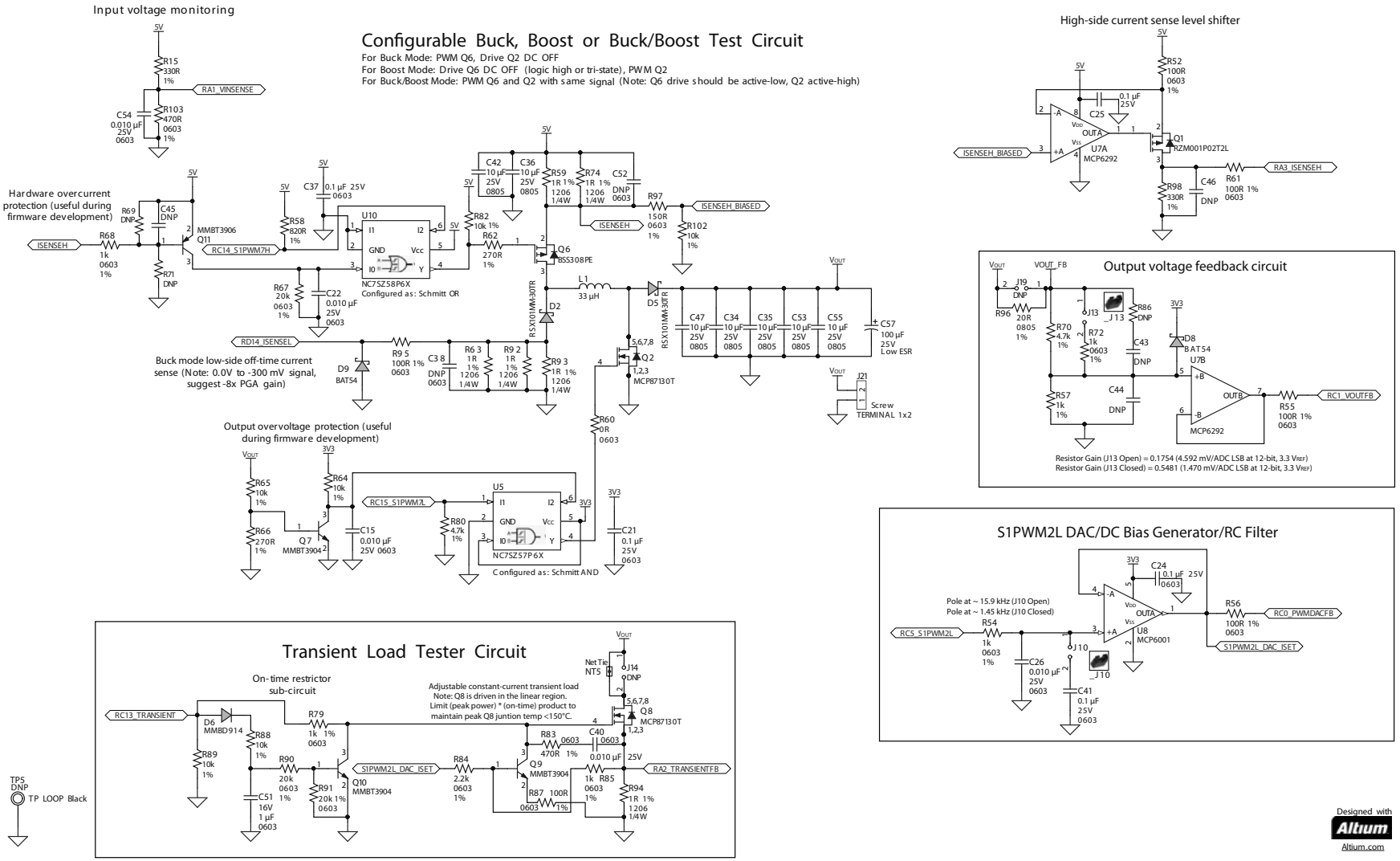

FIGURE A-4: dsPIC33CH CURIOSITY BOARD LAYOUT SCHEMATIC REV. 1.0 (SHEET FOUR OF FOUR)