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FAIRCHILD SEMICONDUCTOR™

October 1986
Revised July 2003

DM74AS651 • DM74AS652
Octal Bus Transceiver and Register

General Description

These devices incorporate an octal transceiver and an octal D-type register configured to enable transmission of data from bus to bus or internal register to bus. The DM74AS651 offers 64-Industrial grade product guaranteeing performance from –40°C to +85°C.

These bus transceivers feature totem-pole 3-STATE outputs designed specifically for driving highly-capacitive or relatively low-impedance loads. The high-impedance state and increased high-logic-level drive provide these devices with the capability of being connected directly to and driving the bus lines in a bus-organized system without need for interface or pull-up components. They are particularly attractive for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The registers in the DM74AS651 and DM74AS652 are edge-triggered D-type flip-flops. On the positive transition of the clock (CAB or CBA), the input data is stored.

The SAB and SBA control pins are provided to select whether real-time data or stored data is transferred. A LOW input level selects real-time data and a HIGH level selects stored data. The select controls have a “make before break” configuration to eliminate a glitch which would normally occur in a typical multiplexer during the transition between stored and real-time data.

The Enable (GAB and $\overline{G}$BA) control pins provide four modes of operation; real-time data transfer from bus A-to-B, real-time data transfer from bus B-to-A, real-time bus A and/or B data transfer to internal storage, or internal stored data transfer to bus A and/or B.

Features

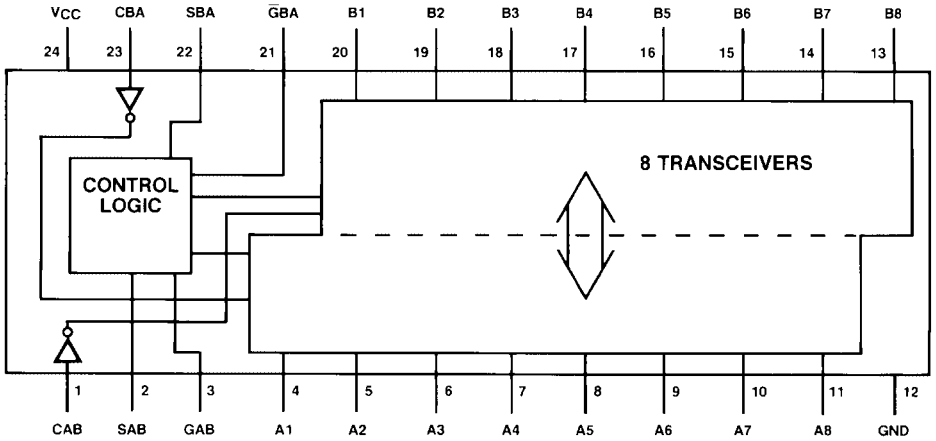
- Switching specifications at 50 pF
- Switching specifications guaranteed over full temperature and V_{CC} range
- Advanced oxide-isolated, ion-implanted Schottky TTL process
- 3-STATE buffer-type outputs drive bus lines directly
- Guaranteed performance over industrial temperature range (–40°C to +85°C) in 64-grade products

Ordering Code:

Order Number	Package Number	Package Description
DM74AS651WM	M24B	24-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
DM74AS651NT	N24C	24-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
DM74AS652WM	M24B	24-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
DM74AS652NT	N24C	24-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter “X” to the ordering code.

Connection Diagram



Function Table

INPUTS						DATA I/O (Note 1)		OPERATION OR FUNCTION	
GAB	$\overline{G}$BA	CAB	CBA	SAB	SBA	A1 THRU A8	B1 THRU B8	DM74AS651	DM74AS652
L	H	H or L	H or L	X	X	Input	Input	Isolation	Isolation
L	H	↑	↑	X	X			Store A and B Data	Store A and B Data
L	L	X	X	X	L	Output	Input	Real Time $\overline{B}$ Data to A Bus	Real Time B Data to A Bus
L	L	X	H or L	X	H			Stored $\overline{B}$ Data to A Bus	Stored B Data to A Bus
H	H	X	X	L	X	Input	Output	Real Time $\overline{A}$ Data to B Bus	Real Time A Data to B Bus
H	H	H or L	X	H	X			Stored $\overline{A}$ Data to B Bus	Stored A Data to B Bus
H	L	H or L	H or L	H	H	Output	Output	Stored $\overline{A}$ Data to B Bus & Stored $\overline{B}$ Data to A Bus	Stored A Data to B Bus & Stored B Data to A Bus
X	H	↑	H or L	X	X	Input	Unspecified (Note 1)	Store A, Hold B	Store A, Hold B
H	H	↑	↑	X (Note 2)	X	Input	Output	Store A in both registers	Store A in both registers
L	X	H or L	↑	X	X	Unspecified (Note 1)	Input	Hold A, Store B	Hold A, Store B
L	L	↑	↑	X	X (Note 2)	Output	Input	Store B in both registers	Store B in both registers

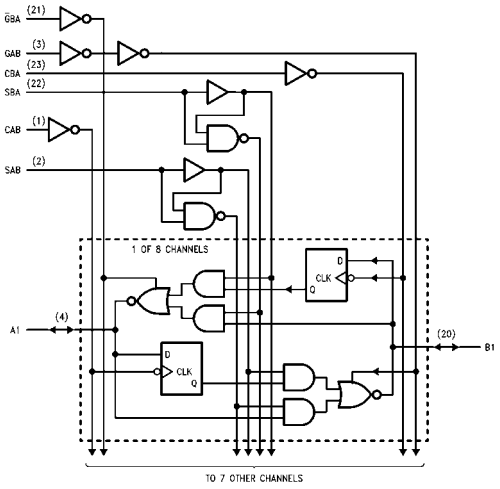
H = HIGH Level
L = LOW Level
X = Irrelevant
↑ = LOW-to-HIGH Transition

Note 1: The data output functions may be enabled or disabled by various signals at the GAB and $\overline{G}$BA inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every LOW-to-HIGH transition on the clock inputs.

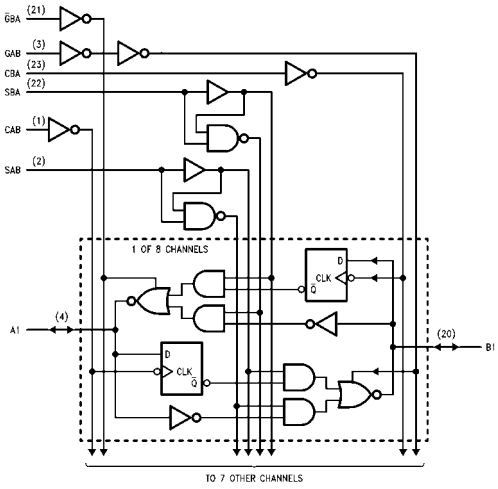
Note 2: If the select control is LOW, the clocks can occur simultaneously. If the select control is HIGH, the clocks must be staggered in order to load both registers.

Logic Diagrams

DM74AS651

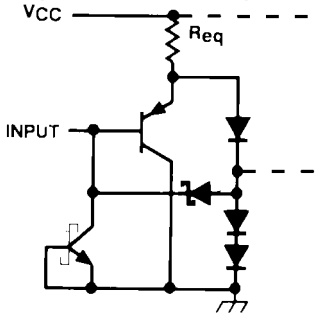


DM74AS652

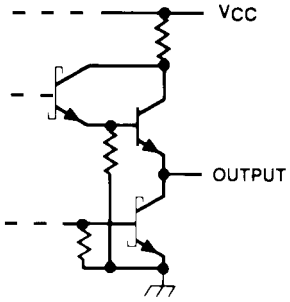


Schematics of Inputs and Outputs

Equivalent of All Other Inputs



Typical of All DM74AS651, DM74AS652 Outputs



Absolute Maximum Ratings(Note 3)

Supply Voltage	7V
Input Voltage	
Control Inputs	7V
I/O Ports	5.5V
Operating Free Air Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Typical θ_{JA}	
N Package	41.1°C/W
M Package	81.5°C/W

Note 3: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Recommended Operating Conditions

Symbol	Parameter		Min	Nom	Max	Units
V_{CC}	Supply Voltage		4.5	5	5.5	V
V_{IH}	HIGH Level Input Voltage		2			V
V_{IL}	LOW Level Input Voltage				0.8	V
I_{OH}	HIGH Level Output Current				−15	mA
I_{OL}	LOW Level Output Current				48	mA
f_{CLK}	Clock Frequency		0		90	MHz
t_{WCLK}	Width of Enable Pulse	HIGH	5			ns
		LOW	6			
t_{SU}	Data Setup Time		6			ns
t_H	Data Hold Time		0			ns
T_A	Operating Free Air Temperature		0		70	°C

Electrical Characteristics

over recommended operating free air temperature range. All typical values are measured at V_{CC} = 5V, T_A = 25°C.

Symbol	Parameter	Conditions			Min	Typ	Max	Units
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18 mA					−1.2	V
V_{OH}	HIGH Level Output Voltage	V_{CC} = 4.5V		I_{OH} = Max	2			V
				I_{OH} = −3 mA	2.4	3.2		
		V_{CC} = 4.5V to 5.5V		I_{OH} = −2 mA	V_{CC} − 2			
V_{OL}	LOW Level Output Voltage	V_{CC} = 4.5V, I_{OL} = Max				0.35	0.5	V
I_I	Input Current at Max Input Voltage	V_{CC} = 5.5V	V_I = 7V	Control Inputs			0.1	mA
			V_I = 5.5V	A or B Ports			0.1	
I_{IH}	HIGH Level Input Current	V_{CC} = 5.5V, V_{IH} = 2.7V		Control Inputs			20	µA
				A or B Ports			70	
I_{IL}	LOW Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V		Control Inputs			−0.5	mA
				A or B Ports			−0.75	
I_O	Output Drive Current	V_{CC} = 5.5V, V_O = 2.25V			−30		−112	mA
I_{CC}	Supply Current	V_{CC} = 5.5V	DM74AS651	Outputs HIGH		110	185	mA
				Outputs LOW		120	195	
				Outputs Disabled		130	195	
			DM74AS652	Outputs HIGH		120	195	
				Outputs LOW		130	211	
				Outputs Disabled		130	211	

DM74AS651 Switching Characteristics

Symbol	Parameter	Conditions	From	To	Min	Max	Units
f_{MAX}	Maximum Clock Frequency	V_{CC} = 4.5V to 5.5V			90		MHz
t_{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	$R_1 = R_2 = 500\Omega$ C_L = 50 pF	CBA or CAB	A or B	2	8.5	ns
t_{PHL}	Propagation Delay Time HIGH-to-LOW Level Output				2	9	ns
t_{PLH}	Propagation Delay Time LOW-to-HIGH Level Output		A or B	B or A	2	8	ns
t_{PHL}	Propagation Delay Time HIGH-to-LOW Level Output				1	7	ns
t_{PLH}	Propagation Delay Time LOW-to-HIGH Level Output		SBA or SAB (Note 4)	A or B	2	11	ns
t_{PHL}	Propagation Delay Time HIGH-to-LOW Level Output				2	9	ns
t_{PZH}	Output Enable Time to HIGH Level Output		Enable $\overline{G}$BA	A	2	10	ns
t_{PZL}	Output Enable Time to LOW Level Output				3	16	ns
t_{PHZ}	Output Disable Time from HIGH Level Output				2	9	ns
t_{PLZ}	Output Disable Time from LOW Level Output				2	9	ns
t_{PZH}	Output Disable Time to HIGH Level Output		Enable GAB	B	3	11	ns
t_{PZL}	Output Disable Time to LOW Level Output				3	16	ns
t_{PHZ}	Output Disable Time from HIGH Level Output				2	10	ns
t_{PLZ}	Output Disable Time from LOW Level Output				2	11	ns

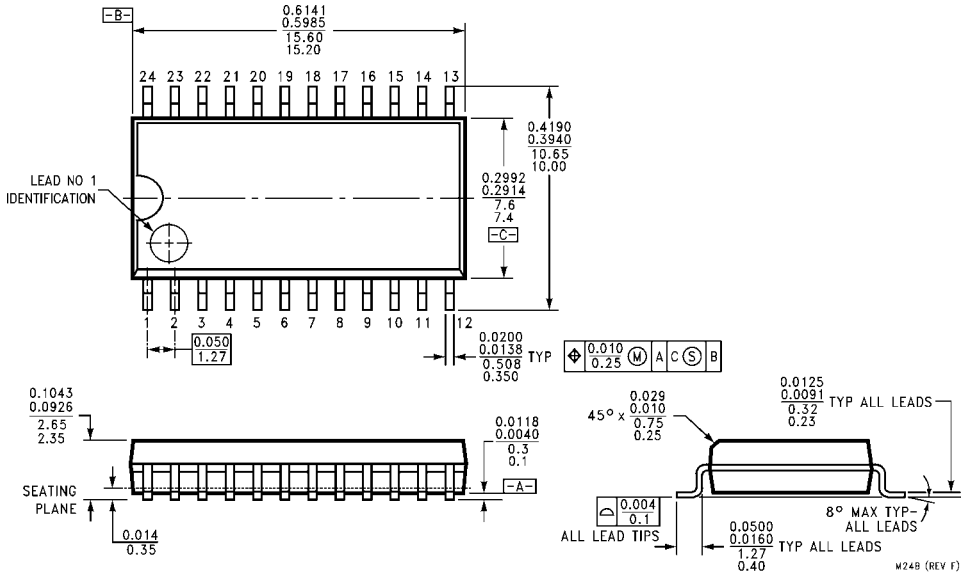
Note 4: These parameters are measured with the internal output state of the storage register opposite to that of the bus input.

DM74AS652 Switching Characteristics

Symbol	Parameter	Conditions	From	To	Min	Max	Units
f_{MAX}	Maximum Clock Frequency	V_{CC} = 4.5V to 5.5V			90		MHz
t_{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	$R_1 = R_2 = 500\Omega$ C_L = 50 pF	CBA or CAB	A or B	2	8.5	ns
t_{PHL}	Propagation Delay Time HIGH-to-LOW Level Output				2	9	ns
t_{PLH}	Propagation Delay Time LOW-to-HIGH Level Output		A or B	B or A	2	9	ns
t_{PHL}	Propagation Delay Time HIGH-to-LOW Level Output				1	7	ns
t_{PLH}	Propagation Delay Time LOW-to-HIGH Level Output		SBA or SAB (Note 5)	A or B	2	11	ns
t_{PHL}	Propagation Delay Time HIGH-to-LOW Level Output				2	9	ns
t_{PZH}	Output Enable Time to HIGH Level Output		Enable $\overline{G}$BA	A	2	10	ns
t_{PZL}	Output Enable Time to LOW Level Output				3	16	ns
t_{PHZ}	Output Disable Time from HIGH Level Output				2	9	ns
t_{PLZ}	Output Disable Time from LOW Level Output				2	9	ns
t_{PZH}	Output Disable Time to HIGH Level Output		Enable GAB	B	3	11	ns
t_{PZL}	Output Disable Time to LOW Level Output				3	16	ns
t_{PHZ}	Output Disable Time from HIGH Level Output				2	10	ns
t_{PLZ}	Output Disable Time from LOW Level Output				2	11	ns

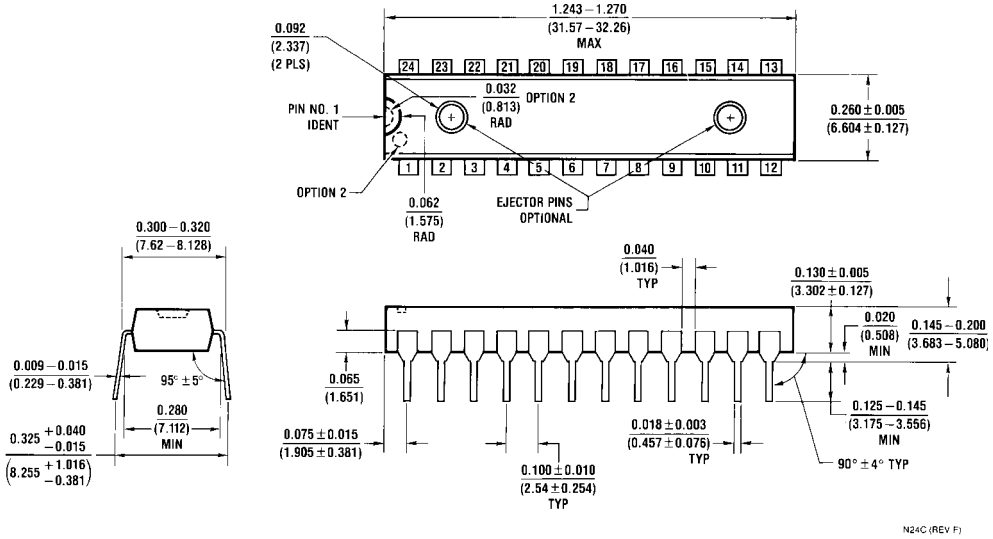
Note 5: These parameters are measured with the internal output state of the storage register opposite to that of the bus input.

Physical Dimensions inches (millimeters) unless otherwise noted



24-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
Package Number M24B

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



24-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
Package Number N24C

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