Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

FAIRCHILD SEMICONDUCTOR™

August 1986
Revised April 2000

DM74S174 • DM74S175
Hex/Quad D Flip-Flop with Clear

General Description

These positive-edge-triggered flip-flops utilize TTL circuitry to implement D-type flip-flop logic. All have a direct clear input, and the quad (DM74S175) versions feature complementary outputs from each flip-flop.

Information at the D inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock input is at either the HIGH or LOW level, the D input signal has no effect at the output.

Features

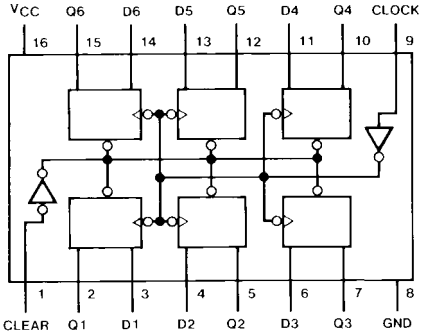
- DM74S174 contain six flip-flops with single-rail outputs.
- DM74S175 contain four flip-flops with double-rail outputs.
- Buffered clock and direct clear inputs
- Individual data input to each flip-flop
- Applications include:
  - Buffer/storage registers
  - Shift registers
  - Pattern generators
- Typical clock frequency 110 MHz
- Typical power dissipation per flip-flop 75mW

Ordering Code:

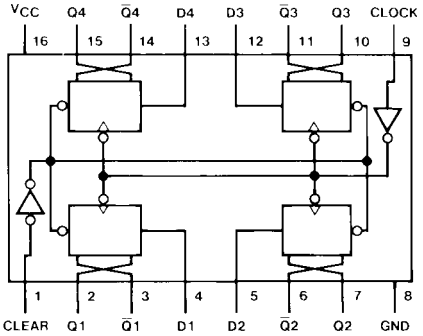
Order Number	Package Number	Package Description
DM74S174N	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide
DM74S175N	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

Connection Diagrams

DM74S174



DM74S175



Function Table (Each Flip-Flop)

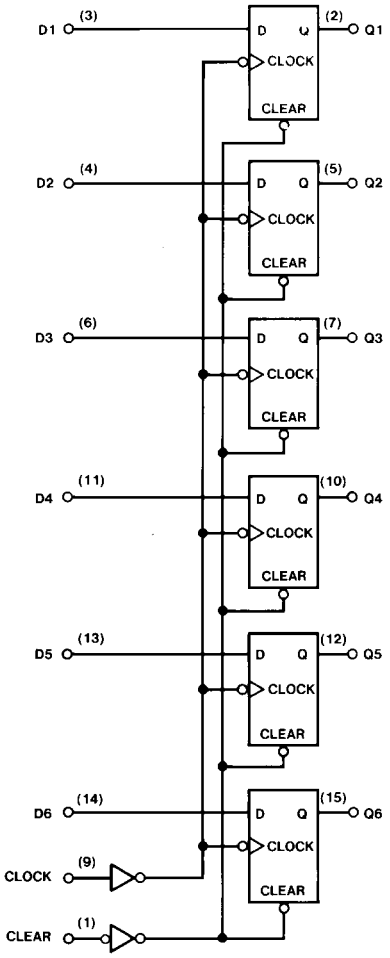
Inputs			Outputs	
Clear	**Clock**	**D**	**Q**	**$\overline{Q}$ (Note 1)**
L	X	X	L	H
H	↑	H	H	L
H	↑	L	L	H
H	L	X	Q_0	$\overline{Q}_0$

H = HIGH Level (steady state)
L = LOW Level (steady state)
X = Don't Care
↑ = Transition from LOW-to-HIGH level
Q_0 = The level of Q before the indicated steady-state input conditions were established.

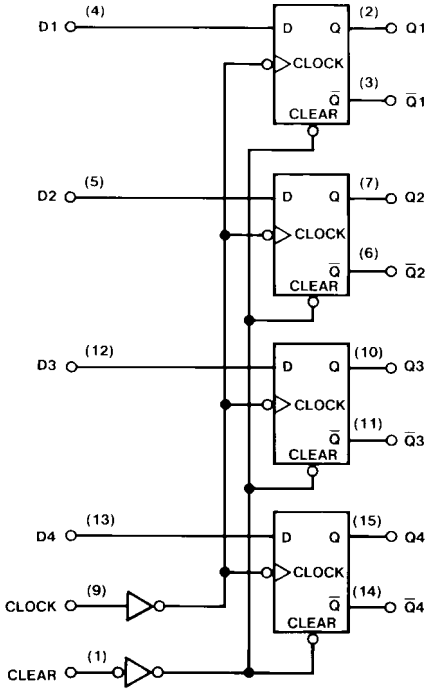
Note 1: DM74S175 only.

Logic Diagrams

DM74S174



DM74S175



Absolute Maximum Ratings(Note 2)

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note 2: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Recommended Operating Conditions

Symbol	Parameter		Min	Nom	Max	Units
V_{CC}	Supply Voltage		4.75	5	5.25	V
V_{IH}	HIGH Level Input Voltage		2			V
V_{IL}	LOW Level Input Voltage				0.8	V
I_{OH}	HIGH Level Output Current				−1	mA
I_{OL}	LOW Level Output Current				20	mA
f_{CLK}	Clock Frequency (Note 3)		0	110	75	MHz
f_{CLK}	Clock Frequency (Note 4)		0	90	65	MHz
t_W	Pulse Width	Clock	7			ns
	(Note 3)	Clear	10			
	Pulse Width	Clock	9			
	(Note 4)	Clear	12			
t_{SU}	Data Setup Time (Note 3)		5			ns
	Data Setup Time (Note 4)		7			
t_H	Data Hold Time (Note 3)		3			ns
	Data Hold Time (Note 4)		5			
t_{REL}	Clear Release Time (Note 3)		5			ns
	Clear Release Time (Note 4)		7			
T_A	Free Air Operating Temperature		0		70	°C

Note 3: C_L = 15 pF, R_L = 280Ω, T_A = 25°C and V_{CC} = 5V.

Note 4: C_L = 50 pF, R_L = 280Ω, T_A = 25°C and V_{CC} = 5V.

Electrical Characteristics

over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 5)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA			−1.2	V
V_{OH}	HIGH Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min	2.7	3.4		V
V_{OL}	LOW Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max			0.5	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V			1	mA
I_{IH}	HIGH Level Input Current	V_{CC} = Max, V_I = 2.7V			50	μA
I_{IL}	LOW Level Input Current	V_{CC} = Max, V_I = 0.5V			−2	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 6)	−40		−100	mA
I_{CC}	Supply Current (DM74S174)	V_{CC} = Max (Note 7)		90	144	mA
I_{CC}	Supply Current (DM74S175)	V_{CC} = Max (Note 7)		60	96	mA

Note 5: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 6: Not more than one output should be shorted at a time, and the duration should not exceed one second.

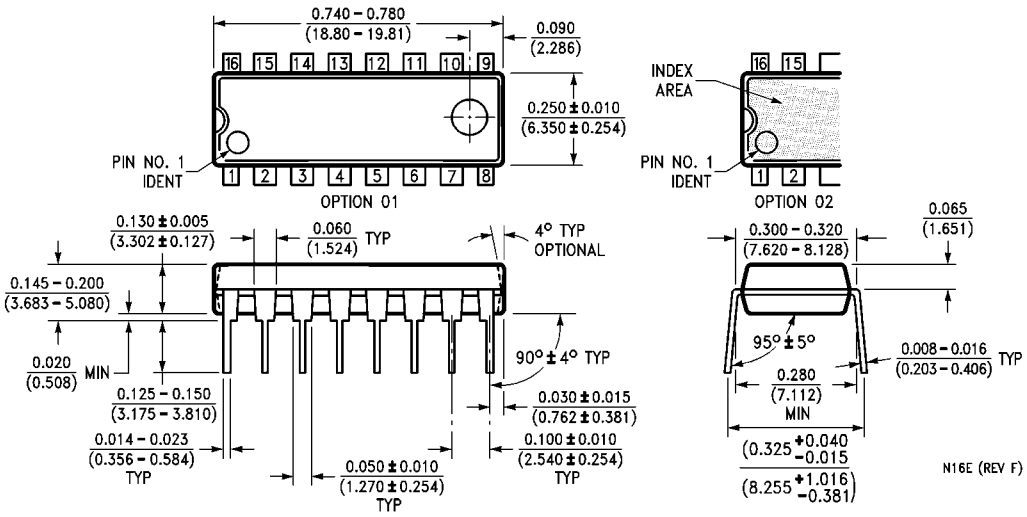
Note 7: With all outputs OPEN and 4.5V applied to all DATA and CLEAR inputs, I_{CC} is measured after a momentary ground, then 4.5V applied to the CLOCK input.

Switching Characteristics

at V_{CC} = 5V and T_A = 25°C

Symbol	Parameter	From (Input) To (Output)	R_L = 280Ω				Units
			C_L = 15 pF		C_L = 50 pF		
			Min	Max	Min	Max	
f_{MAX}	Maximum Clock Frequency		75		65		MHz
t_{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	Clock to Output		12		15	ns
t_{PHL}	Propagation Delay Time HIGH-to-LOW Level Output	Clock to Output		17		21	ns
t_{PLH}	Propagation Delay Time LOW-to-HIGH Level Output (DM74S175 Only)	Clear to $\overline{Q}$		15		18	ns
t_{PHL}	Propagation Delay Time HIGH-to-LOW Level Output	Clear to Q		22		23	ns

Physical Dimensions inches (millimeters) unless otherwise noted



16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide
Package Number N16E