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FAIRCHILD SEMICONDUCTOR™

August 1986
Revised May 2000

DM74S373 • DM74S374
3-STATE Octal D-Type Transparent Latches and Edge-Triggered Flip-Flops

General Description

These 8-bit registers feature totem-pole 3-STATE outputs designed specifically for driving highly-capacitive or relatively low-impedance loads. The high-impedance state and increased high-logic-level drive provide these registers with the capability of being connected directly to and driving the bus lines in a bus-organized system without need for interface or pull-up components. They are particularly attractive for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight latches of the DM74S373 are transparent D-type latches meaning that while the enable (G) is HIGH the Q outputs will follow the data (D) inputs. When the enable is taken LOW the output will be latched at the level of the data that was set up.

The eight flip-flops of the DM74S374 are edge-triggered D-type flip-flops. On the positive transition of the clock, the Q outputs will be set to the logic states that were set up at the D inputs.

Schmitt-trigger buffered inputs at the enable/clock lines simplify system design as ac and dc noise rejection is improved by typically 400 mV due to the input hysteresis. A buffered output control input can be used to place the eight outputs in either a normal logic state (HIGH or LOW logic levels) or a high-impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly.

The output control does not affect the internal operation of the latches or flip-flops. That is, the old data can be retained or new data can be entered even while the outputs are OFF.

Features

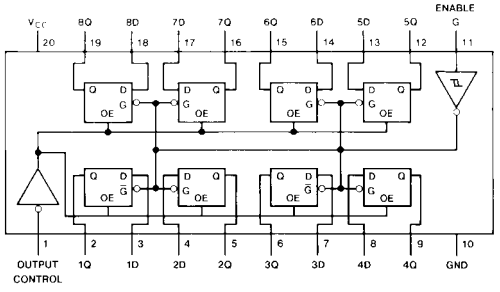
- Choice of 8 latches or 8 D-type flip-flops in a single package
- 3-STATE bus-driving outputs
- Full parallel-access for loading
- Buffered control inputs
- P-N-P input reduce D-C loading on data lines

Ordering Code:

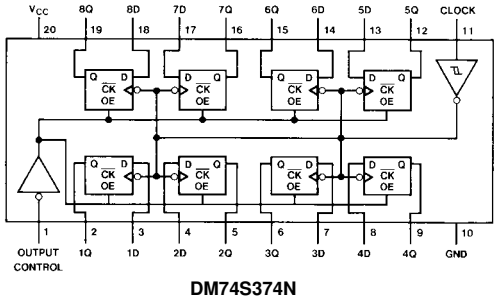
Order Number	Package Number	Package Description
DM74S373WM	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide
DM74S373N	N20A	20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide
DM74S374WM	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide
DM74S374N	N20A	20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Connection Diagrams



DM74S373N



DM74S374N

Truth Tables

DM74S373

Output Control	Enable G	D	Output
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

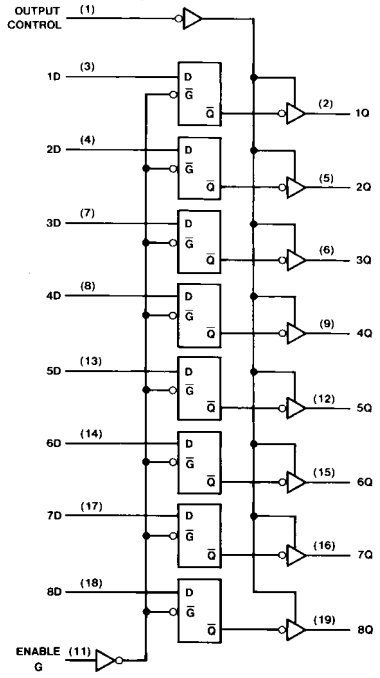
DM74S374

Output Control	Clock	D	Output
L	↑	H	H
L	↑	L	L
L	L	X	Q_0
H	X	X	Z

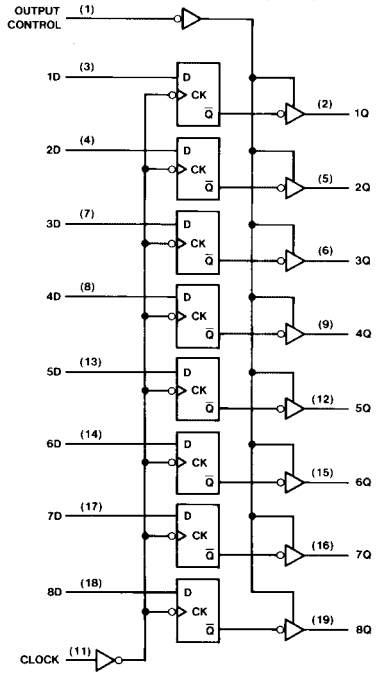
H = HIGH Level (Steady State)
L = LOW Level (Steady State)
X = Don't Care
Z = High Impedance State
↑ = Transition from LOW-to-HIGH level,
Q_0 = The level of the output before steady-state input conditions were established.

Logic Diagrams

74S373
Transparent Latches



74S374
Positive-Edge-Triggered Flip-Flops



Absolute Maximum Ratings(Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

DM74S373 Recommended Operating Conditions

Symbol	Parameter		Min	Nom	Max	Units
V_{CC}	Supply Voltage		4.75	5	5.25	V
V_{IH}	HIGH Level Input Voltage		2			V
V_{IL}	LOW Level Input Voltage				0.8	V
I_{OH}	HIGH Level Output Current				−6.5	mA
I_{OL}	LOW Level Output Current				20	mA
t_W	Pulse Width (Note 2)	Enable HIGH	6			ns
		Enable LOW	7.3			
t_W	Pulse Width (Note 3)	Enable HIGH	15			ns
		Enable LOW	15			ns
t_{SU}	Data Setup Time (Note 4)(Note 5)		0↓			ns
t_H	Data Hold Time (Note 4)(Note 5)		10↓			ns
T_A	Free Air Operating Temperature		0		70	°C

Note 2: C_L = 15 pF, R_L = 280Ω, T_A = 25°C and V_{CC} = 5V.

Note 3: C_L = 50 pF and R_L = 280Ω, T_A = 25°C and V_{CC} = 5V.

Note 4: The symbol (↓) indicates the falling edge of the clock pulse is used for reference.

Note 5: T_A = 25°C and V_{CC} = 5V.

DM74S373 Electrical Characteristics

over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 6)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.2	V
V_{OH}	HIGH Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4	3.2		V
V_{OL}	LOW Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max				0.5	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	HIGH Level Input Current	V_{CC} = Max, V_I = 2.7V				50	µA
I_{IL}	LOW Level Input Current	V_{CC} = Max, V_I = 0.5V				−250	µA
I_{OZH}	Off-State Output Current with HIGH Level Output Voltage Applied	V_{CC} = Max, V_O = 2.4V V_{IH} = Min, V_{IL} = Max				50	µA
I_{OZL}	Off-State Output Current with LOW Level Output Voltage Applied	V_{CC} = Max, V_O = 0.5V V_{IH} = Min, V_{IL} = Max				−50	µA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 7)		−40		−100	mA
I_{CC}	Supply Current	V_{CC} = Max	Outputs HIGH or LOW		105	160	mA
			Outputs Disabled			190	

Note 6: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 7: Not more than one output should be shorted at a time, and the duration should not exceed one second.

DM74S373 Switching Characteristics

at V_{CC} = 5V and T_A = 25°C

Symbol	Parameter	From (Input) To (Output)	R_L = 280Ω				Units
			C_L = 15 pF		C_L = 50 pF		
			Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	Data to Any Q		12		14	ns
t_{PHL}	Propagation Delay Time HIGH-to-LOW Level Output	Data to Any Q		12		16	ns
t_{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	Enable to Any Q		14		14	ns
t_{PHL}	Propagation Delay Time HIGH-to-LOW Level Output	Enable to Any Q		18		21	ns
t_{PZH}	Enable Time to HIGH Level Output	Output Control to Any Q		15		17	ns
t_{PZL}	Output Enable Time to LOW Level Output	Output Control to Any Q		18		23	ns
t_{PHZ}	Output Disable Time to HIGH Level Output (Note 8)	Output Control to Any Q		9			ns
t_{PLZ}	Output Disable Time to LOW Level Output (Note 8)	Output Control to Any Q		12			ns

Note 8: C_L = 5 pF

DM74S374 Recommended Operating Conditions

Symbol	Parameter		Min	Nom	Max	Units
V_{CC}	Supply Voltage		4.75	5	5.25	V
V_{IH}	HIGH Level Input Voltage					V
V_{IL}	LOW Level Input Voltage				0.8	V
I_{OH}	HIGH Level Output Current				−6.5	mA
I_{OL}	LOW Level Output Current				20	mA
f_{CLK}	Clock Frequency (Note 9)		0		75	MHz
f_{CLK}	Clock Frequency (Note 10)		0		75	MHz
t_W	Pulse Width (Note 9)	Clock HIGH	6			ns
		Clock LOW	7.3			
	Pulse Width (Note 10)	Clock HIGH	15			
		Clock LOW	15			
t_{SU}	Data Setup Time (Note 11)(Note 12)		5↑			ns
t_H	Data Hold Time (Note 11)(Note 12)		2↑			ns
T_A	Free Air Operating Temperature		0		70	°C

Note 9: C_L = 15 pF, R_L = 280Ω, T_A = 25°C and V_{CC} = 5V.

Note 10: C_L = 50 pF, R_L = 280Ω, T_A = 25°C and V_{CC} = 5V.

Note 11: The symbol (↑) indicates the rising edge of the clock pulse is used for reference.

Note 12: T_A = 25°C and V_{CC} = 5V.

DM74S374 Electrical Characteristics

over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 13)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.2	V
V_{OH}	HIGH Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4	3.2		V
V_{OL}	LOW Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max				0.5	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_H	HIGH Level Input Current	V_{CC} = Max, V_I = 2.7V				50	µA
I_{IL}	LOW Level Input Current	V_{CC} = Max, V_I = 0.5V				−250	µA
I_{OZH}	Off-State Output Current with HIGH Level Output Voltage Applied	V_{CC} = Max, V_O = 2.4V V_{IH} = Min, V_{IL} = Max				50	µA
I_{OZL}	Off-State Output Current with LOW Level Output Voltage Applied	V_{CC} = Max, V_O = 0.5V V_{IH} = Min, V_{IL} = Max				−50	µA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 14)		−40		−100	mA
I_{CC}	Supply Current	V_{CC} = Max	Outputs HIGH			110	mA
			Outputs LOW		90	140	
			Outputs Disabled			160	

Note 13: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 14: Not more than one output should be shorted at a time, and the duration should not exceed one second.

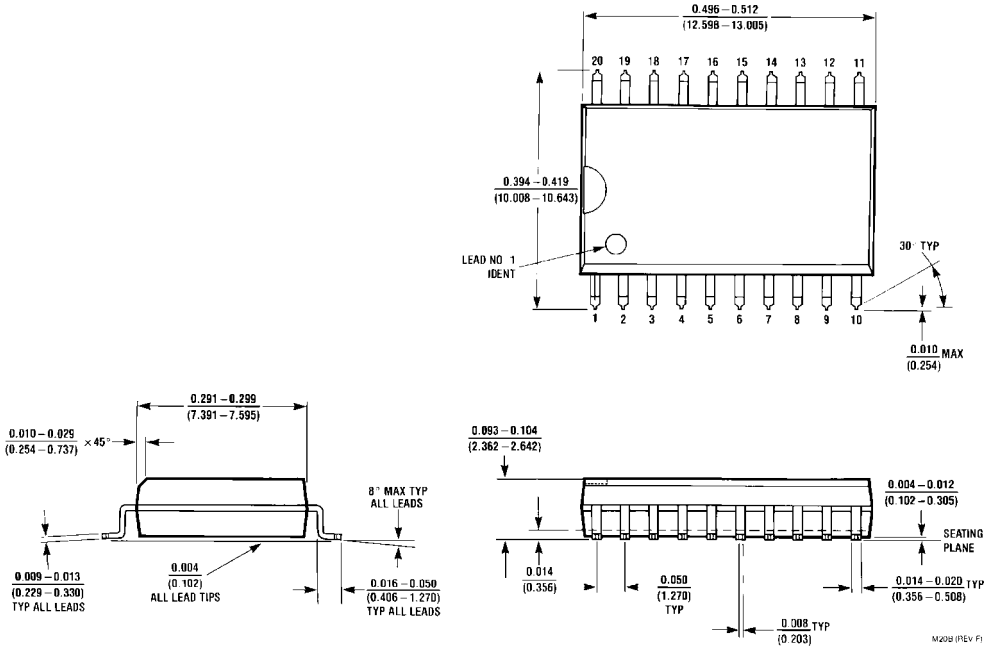
DM74S374 Switching Characteristics

at V_{CC} = 5V and T_A = 25°C

Symbol	Parameter	From (Input) To (Output)	R_L = 280Ω				Units
			C_L = 15 pF		C_L = 50 pF		
			Min	Max	Min	Max	
f_{MAX}	Maximum Clock Frequency			75		75	MHz
t_{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	Clock to Any Q		15		15	ns
t_{PHL}	Propagation Delay Time HIGH-to-LOW Level Output	Clock to Any Q		17		20	ns
t_{PZH}	Output Enable Time to HIGH Level Output	Output Control to Any Q		15		17	ns
t_{PZL}	Output Enable Time to LOW Level Output	Output Control to Any Q		18		23	ns
t_{PHZ}	Output Disable Time from HIGH Level Output (Note 15)	Output Control to Any Q		9			ns
t_{PLZ}	Output Disable Time from LOW Level Output (Note 15)	Output Control to Any Q		12			ns

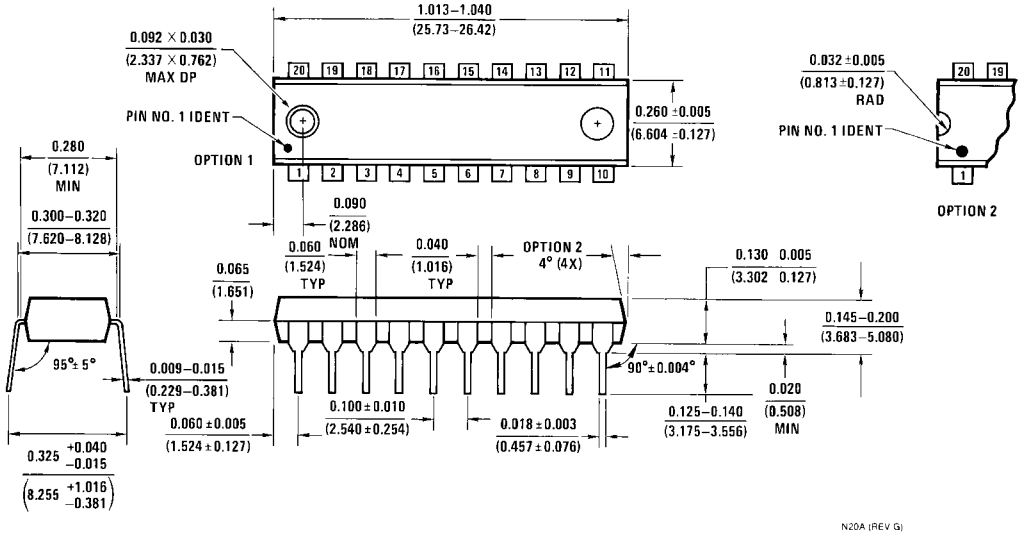
Note 15: C_L = 5 pF

Physical Dimensions inches (millimeters) unless otherwise noted



20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide
Package Number M20B

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide
Package Number N20A