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# **DMA56105**

## Silicon PNP epitaxial planar type

For digital circuits
DMA26105 in SMini5 type package

#### ■ Features

- $\bullet$  High forward current transfer ratio  $h_{FE}$  with excellent linearity
- $\bullet$  Low collector-emitter saturation voltage  $V_{\text{CE}(\text{sat})}$
- Halogen-free / RoHS compliant (EU RoHS / UL-94 V-0 / MSL: Level 1 compliant)
- Marking Symbol: K1

#### ■ Basic Part Number

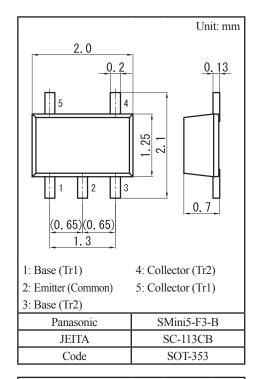
Dual DRA2114T (Common emitter)

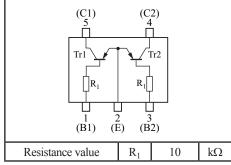
#### ■ Packaging

DMA561050R Embossed type (Thermo-compression sealing): 3 000 pcs / reel (standard)

### ■ Absolute Maximum Ratings $T_a = 25$ °C

	Parameter	Symbol Rating		Unit
Tr1 Tr2	Collector-base voltage (Emitter open)	V <sub>CBO</sub>	-50	V
	Collector-emitter voltage (Base open)	V <sub>CEO</sub>	-50	V
	Collector current	$I_{C}$	-100	mA
Overall	Total power dissipation	$P_{T}$	150	mW
	Junction temperature	T <sub>j</sub>	150	°C
	Operating ambient temperature	T <sub>opr</sub>	-40 to +85	°C
	Storage temperature	T <sub>stg</sub> -55 to +150		°C



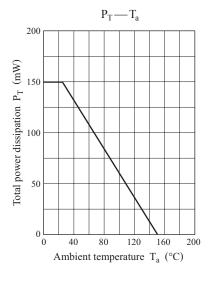


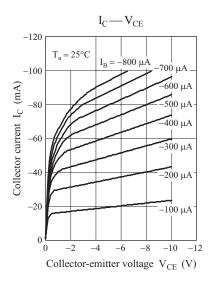
#### ■ Electrical Characteristics $T_a = 25$ °C±3°C

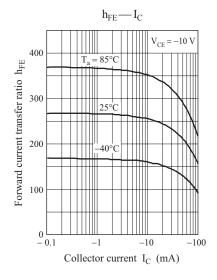
Parameter	Symbol	Conditions	Min	Тур	Max	Unit
Collector-base voltage (Emitter open)	V <sub>CBO</sub>	$I_{\rm C} = -10 \mu\text{A}, I_{\rm E} = 0$	-50			V
Collector-emitter voltage (Base open)	V <sub>CEO</sub>	$I_C = -2 \text{ mA}, I_B = 0$	-50			V
Collector-base cutoff current (Emitter open)	$I_{CBO}$	$V_{CB} = -50 \text{ V}, I_E = 0$			-0.1	μΑ
Collector-emitter cutoff current (Base open)	I <sub>CEO</sub>	$V_{CE} = -50 \text{ V}, I_{B} = 0$			-0.5	μΑ
Emitter-base cutoff current (Collector open)	$I_{EBO}$	$V_{EB} = -6 \text{ V}, I_C = 0$			-0.01	mA
Forward current transfer ratio	$h_{\mathrm{FE}}$	$V_{CE} = -10 \text{ V}, I_{C} = -5 \text{ mA}$	160		460	_
h <sub>FE</sub> ratio *1	h <sub>FE</sub> (Small/Large)	$V_{CE} = -10 \text{ V}, I_{C} = -5 \text{ mA}$	0.50	0.99		_
Collector-emitter saturation voltage	V <sub>CE(sat)</sub>	$I_C = -10 \text{ mA}, I_B = -0.5 \text{ mA}$			-0.25	V
Input voltage (ON)	V <sub>I(on)</sub>	$V_{CE} = -0.2 \text{ V}, I_{C} = -5 \text{ mA}$	-1.2			V
Input voltage (OFF)	V <sub>I(off)</sub>	$V_{CE} = -5 \text{ V}, I_{C} = -100  \mu\text{A}$			-0.4	V
Input resistance	$R_1$		-30%	10	+30%	kΩ

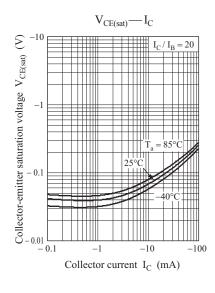
Note) 1. Measuring methods are based on JAPANESE INDUSTRIAL STANDARD JIS C 7030 measuring methods for transistors.

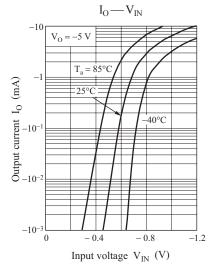
2. \*1: Ratio between 2 elements

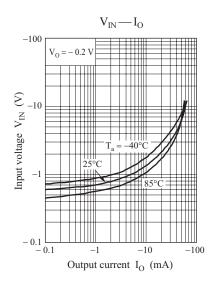






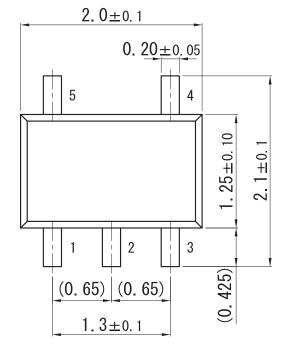


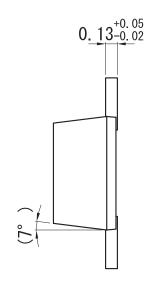


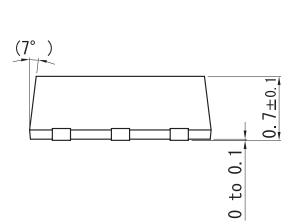


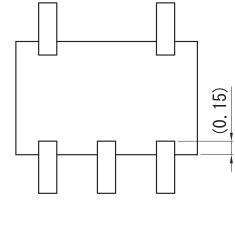
## SMini5-F3-B

Unit: mm

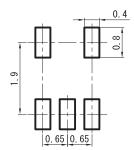








### ■ Land Pattern (Reference) (Unit: mm)



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