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Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832

Email & Skype: info@chipsmall.com Web: www.chipsmall.com

Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China











COMPLEMENTARY PAIR ENHANCEMENT MODE MOSFET

Product Summary

Device	V _{(BR)DSS}	R _{DS(on)} max	I _D Max T _A = +25°C
Q2	30V	8.5A	
QZ	307	$32mΩ @ V_{GS} = 4.5V$	7.2A
Q1	-30V	$39m\Omega$ @ V_{GS} = -10 V	-7A
Qi		53 m Ω @ V _{GS} = -4.5V	-5.6A

Description and

This MOSFET has been designed to minimize the on-state resistance (R_{DS(on)}) and yet maintain superior switching performance, making it ideal for high efficiency power management applications.

Applications

- **Power Management Functions**
- Analog Switch
- Load Switch

Features

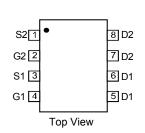
- Low On-Resistance
- Low Input Capacitance
- Fast Switching Speed
- Low Input/Output Leakage
- Complementary Pair MOSFET
- Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)
- Halogen and Antimony Free. "Green" Device (Note 3)
- Qualified to AEC-Q101 Standards for High Reliability

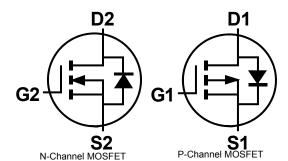
Mechanical Data

- Case: SO-8
- Case Material: Molded Plastic, "Green" Molding Compound UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals Connections: See Diagram
- Terminals: Finish Matte Tin annealed over Copper lead frame Solderable per MIL-STD-202, Method 208 @3
- Weight: 0.072 grams (approximate)









Ordering Information (Note 4)

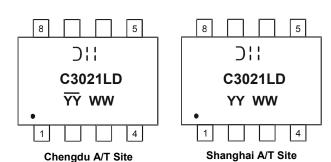
Part Number	Case	Packaging		
DMC3021LSD-13	SO-8	2500/Tape & Reel		

SO-8

Notes:

- 1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS) & 2011/65/EU (RoHS 2) compliant.
- 2. See http://www.diodes.com/quality/lead_free.html for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
- 3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
- 4. For packaging details, go to our website at http://www.diodes.com/products/packages.html.

Marking Information



⊃¦¦ = Manufacturer's Marking C3021LD = Product Type Marking Code YYWW = Date Code Marking YY or \overline{YY} = Year (ex: 14 = 2014) WW = Week (01 - 53)

YY = Date Code Marking for SAT (Shanghai Assembly/ Test site) YY = Date Code Marking for CAT (Chengdu Assembly/ Test site)



Char	Symbol	Value	Unit
Drain-Source Voltage	V _{DSS}	30	V
Gate-Source Voltage	V_{GSS}	±20	V
Continuous Drain Current (Note 5)	I _D	8.5 7.1	А
Pulsed Drain Current (Note 6)	I _{DM}	26	Α

Maximum Ratings P-CHANNEL – Q1 (@T_A = +25°C, unless otherwise specified.)

Char	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	-30	V
Gate-Source Voltage	V _{GSS}	±20	V
Continuous Drain Current (Note 5)	I _D	-7.0 -4.5	А
Pulsed Drain Current (Note 6)	I _{DM}	-25	Α

Thermal Characteristics (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Value	Unit
Power Dissipation (Note 5)	P _D	2.5	W
Thermal Resistance, Junction to Ambient (Note 5)	$R_{\theta JA}$	50	°C/W
Operating and Storage Temperature Range	T _J , T _{STG}	-55 to +150	°C

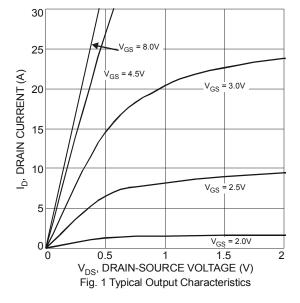
Electrical Characteristics N-CHANNEL – Q2 (@T_A = +25°C, unless otherwise specified.)

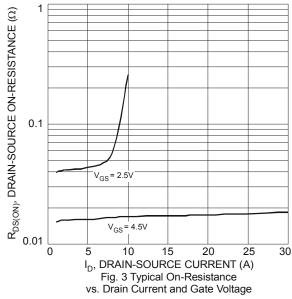
Characteristic	Symbol	Min	Тур	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 7)						
Drain-Source Breakdown Voltage	BV _{DSS}	30	_	_	V	$V_{GS} = 0V, I_D = 250\mu A$
Zero Gate Voltage Drain Current T _J = +25°C	I _{DSS}	_	_	1.0	μA	V _{DS} = 30V, V _{GS} = 0V
Gate-Source Leakage	I _{GSS}	_	_	±100	nA	$V_{GS} = \pm 20V, V_{DS} = 0V$
ON CHARACTERISTICS (Note 7)						
Gate Threshold Voltage	$V_{GS(th)}$	1	1.45	2.1	V	$V_{DS} = V_{GS}$, $I_C = 250\mu A$
Static Drain-Source On-Resistance	D	_	14	21	mΩ	V_{GS} = 10V, I_C = 7A
Static Dialit-Source Off-Nesistatice	R _{DS (ON)}		18	32	11122	$V_{GS} = 4.5V, I_C = 5.6A$
Forward Transfer Admittance	Y _{fs}	_	8.1	_	S	$V_{DS} = 5V, I_{C} = 7A$
Diode Forward Voltage (Note 7)	V_{SD}	_	0.7	1.0	V	$V_{GS} = 0V, I_{S} = 1A$
DYNAMIC CHARACTERISTICS (Note 8)				_		
Input Capacitance	C _{iss}	_	767	_	pF	V 40V V 0V
Output Capacitance	Coss	_	110	_	pF	$V_{DS} = 10V, V_{GS} = 0V,$ f = 1.0MHz
Reverse Transfer Capacitance	Crss	_	105	_	pF	1 - 1.01/11/2
Gate Resistance	Rg	_	1.4	_	Ω	V_{DS} = 0V, V_{GS} = 0V, f = 1MHz
Total Gate Charge (V _{GS} = 4.5V)	Qg	_	7.8	_	nC	
Total Gate Charge (V _{GS} = 10V)	Q_g	_	16.1	_	nC	V _{DS} = 15V, I _D = 9A
Gate-Source Charge	Q_{gs}	_	1.8	_	nC	VDS - 15V, ID - 9A
Gate-Drain Charge	Q_{gd}	_	2.5	_	nC	
Turn-On Delay Time	t _{D(on)}	_	5.0	_	ns	
Turn-On Rise Time	t _r	_	4.5	_	ns	V _{GS} = 10V, V _{DS} = 15V,
Turn-Off Delay Time	t _{D(off)}	_	26.3	_	ns	$R_G = 6\Omega$, $I_D = 1A$
Turn-Off Fall Time	t _f	_	8.55	_	ns]

Notes:

- 5. Device mounted on FR-4 PCB, with minimum recommended pad layout.
- 6. Repetitive rating, pulse width limited by junction temperature.
- 7. Short duration pulse test used to minimize self-heating effect.
- 8. Guaranteed by design. Not subject to production testing.







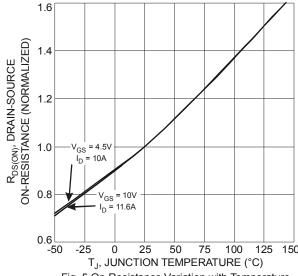
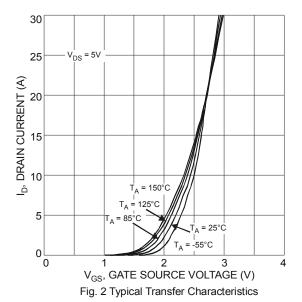


Fig. 5 On-Resistance Variation with Temperature



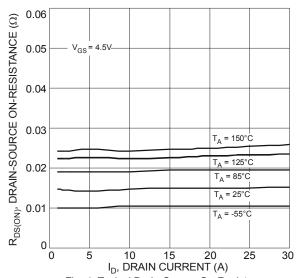


Fig. 4 Typical Drain-Source On-Resistance vs. Drain Current and Temperature

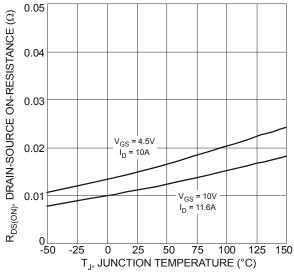


Fig. 6 On-Resistance Variation with Temperature



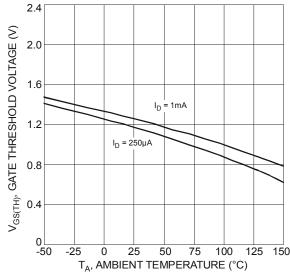
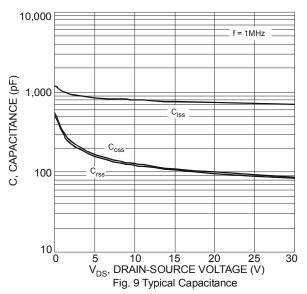
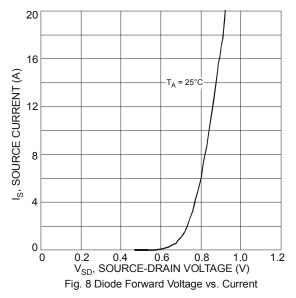
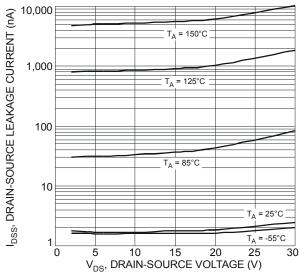


Fig. 7 Gate Threshold Variation vs. Ambient Temperature







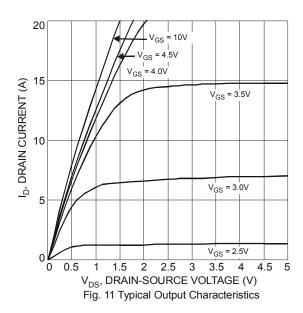


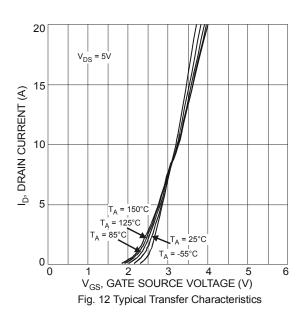
Electrical Characteristics P-CHANNEL – Q1 (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Тур	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 7)						
Drain-Source Breakdown Voltage	BV _{DSS}	-30	_	_	V	$V_{GS} = 0V, I_D = -250\mu A$
Zero Gate Voltage Drain Current T _J = +25°C	I _{DSS}	_	_	-1.0	μΑ	V _{DS} = -30V, V _{GS} = 0V
Gate-Source Leakage	I _{GSS}		_	±100	nA	$V_{GS} = \pm 20V, V_{DS} = 0V$
ON CHARACTERISTICS (Note 7)						·
Gate Threshold Voltage	$V_{GS(th)}$	-1	-1.7	-2.2	V	$V_{DS} = V_{GS}, I_{D} = -250 \mu A$
Static Drain-Source On-Resistance	D-s (s)		30	39	mΩ	$V_{GS} = -10V$, $I_D = -4.3A$
Static Dialii-Source Off-Resistance	R _{DS(ON)}	_	42	53	11122	$V_{GS} = -4.5V, I_D = -3.7A$
Forward Transfer Admittance	Y _{fs}		7	_	S	$V_{DS} = -5V, I_D = -4.3A$
Diode Forward Voltage (Note 7)	V_{SD}	_	-0.75	-1.0	V	V _{GS} = 0V, I _S = -1.7A
DYNAMIC CHARACTERISTICS (Note 8)						
Input Capacitance	C _{iss}	_	1002	_	pF	101/11/ 01/
Output Capacitance	Coss		125	_	pF	$V_{DS} = -10V, V_{GS} = 0V,$ - f = 1.0MHz
Reverse Transfer Capacitance	C _{rss}	_	118	_	pF	1 - 1.000112
Gate Resistance	Rg	_	13	_	Ω	$V_{DS} = 0V$, $V_{GS} = 0V$, $f = 1MHz$
Total Gate Charge (V _{GS} = 4.5V)	Qg	_	10.1	_	nC	
Total Gate Charge (V _{GS} = 10V)	Qg	_	21.1	_	nC	\\ - 15\\ \ - 60
Gate-Source Charge	Q _{gs}	_	2.8	_	nC	$-V_{DS} = -15V, I_{D} = -6A$
Gate-Drain Charge	Q _{gd}	_	3.2	_	nC	
Turn-On Delay Time	t _{D(on)}		10.1	_	ns	
Turn-On Rise Time	t _r		6.5	_	ns	V _{GS} = -10V, V _{DS} = -15V,
Turn-Off Delay Time	t _{D(off)}	_	50.1	_	ns	$R_G = 6\Omega$, $I_D = -1A$
Turn-Off Fall Time	t _f		22.2	_	ns	

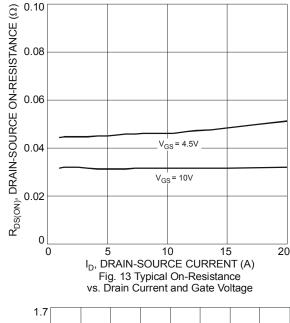
Notes: 7. Short duration pulse test used to minimize self-heating effect.

^{8.} Guaranteed by design. Not subject to production testing.









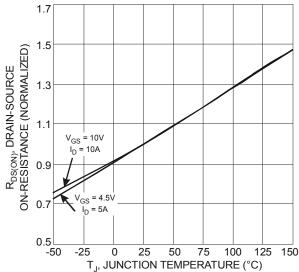


Fig. 15 On-Resistance Variation with Temperature

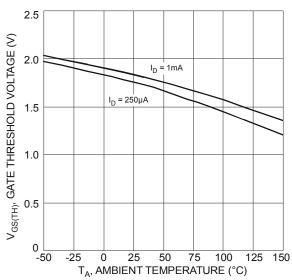


Fig. 17 Gate Threshold Variation vs. Ambient Temperature

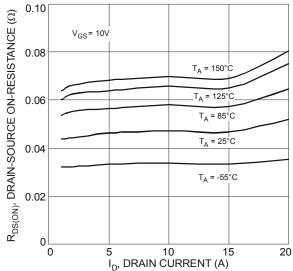


Fig. 14 Typical Drain-Source On-Resistance vs. Drain Current and Temperature

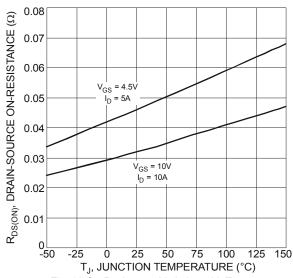


Fig. 16 On-Resistance Variation with Temperature

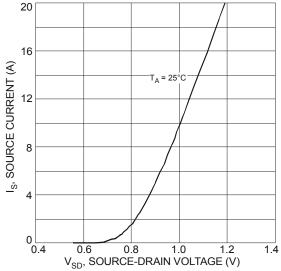
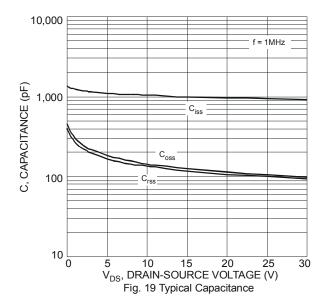
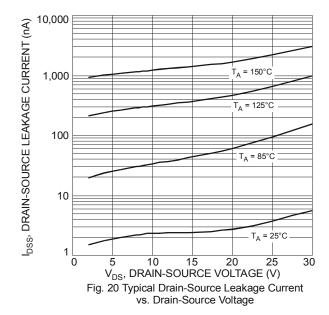


Fig. 18 Diode Forward Voltage vs. Current

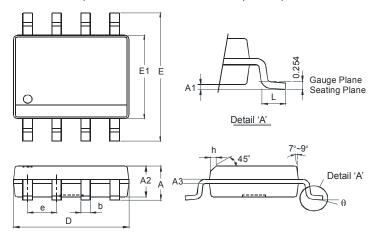






Package Outline Dimensions

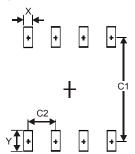
Please see AP02002 at http://www.diodes.com/datasheets/ap02002.pdf for latest version.



SO-8						
Dim	Min	Max				
Α	-	1.75				
A1	0.10	0.20				
A2	1.30	1.50				
А3	0.15	0.25				
b	0.3	0.5				
D	4.85	4.95				
Е	5.90	6.10				
E1	3.85	3.95				
е	1.27 Typ					
h	-	0.35				
L	0.62	0.82				
θ	0°	8°				
All Dimensions in mm						

Suggested Pad Layout

Please see AP02001 at http://www.diodes.com/datasheets/ap02001.pdf for latest version.



Dimensions	Value (in mm)		
X	0.60		
Υ	1.55		
C1	5.4		
C2	1.27		



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