Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

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Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

Product Summary

Device	BV_{DSS}	$R_{DS(ON)}$ MAX	I_D T_A = +25°C
Q1 & Q4	100V	160mΩ @ V_{GS} = 10V	2.9A
		200mΩ @ V_{GS} = 4.5V	2.6A
Q2 & Q3	-100V	250mΩ @ V_{GS} = -10V	-2.3A
		300mΩ @ V_{GS} = -4.5V	-2.1A

Features

- Low On-Resistance
- Low Input Capacitance
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**
- **Qualified to AEC-Q101 Standards for High Reliability**

Description

This new generation MOSFET is designed to minimize the on-state resistance ($R_{DS(ON)}$) and yet maintain superior switching performance, making it ideal for high-efficiency power management applications.

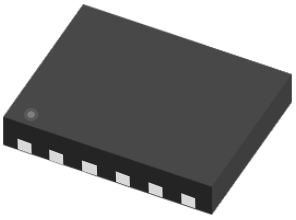
Mechanical Data

- Case: V-DFN5045-12
- Case Material: Molded Plastic, "Green" Molding Compound. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminal Connections: See Diagram
- Terminals: Finish – NiPdAu over Copper Leadframe. Solderable per MIL-STD-202, Method 208 e4
- Weight: 0.056 grams (Approximate)

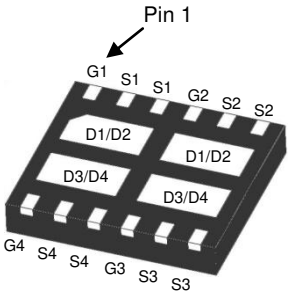
Applications

- High-Efficiency Bridge Rectifiers

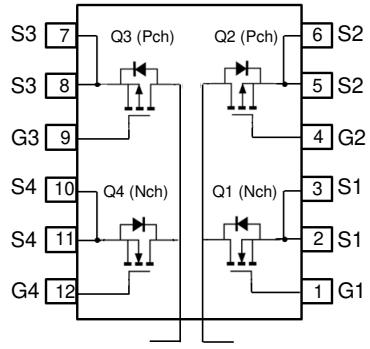
V-DFN5045-12



Top View



Bottom View



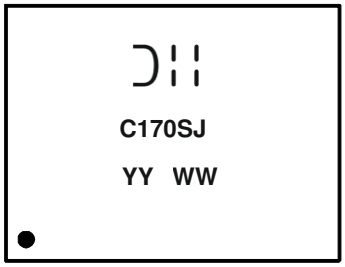
Internal Schematic

Ordering Information (Note 4)

Part Number	Case	Tape Width	Packaging
DMHC10H170SFJ-13	V-DFN5045-12	12mm	3,000/Tape & Reel

Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS) & 2011/65/EU (RoHS 2) compliant.
2. See http://www.diodes.com/quality/lead_free.html for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
4. For packaging details, go to our website at http://www.diodes.com/products/packages.html.

Marking Information



=Manufacturer's Marking
C170SJ = Product Type Marking Code
YYWW = Date Code Marking
YY = Last Two Digits of Year (ex: 16 = 2016)
WW = Week Code (01 to 53)

Maximum Ratings Q1 & Q4 N-Channel (@T_A = +25°C, unless otherwise specified.)

Characteristic			Symbol	Value	Unit
Drain-Source Voltage			V_{DSS}	100	V
Gate-Source Voltage			V_{GSS}	±20	V
Continuous Drain Current (Note 5) V_{GS} = 10V	Steady State	T_A = +25°C T_A = +70°C	I_D	2.9 2.3	A
Maximum Body Diode Forward Current (Note 5)			I_S	2.5	A
Pulsed Drain Current (10µs pulse, Duty Cycle = 1%)			I_{DM}	13	A

Maximum Ratings Q2 & Q3 P-Channel (@T_A = +25°C, unless otherwise specified.)

Characteristic			Symbol	Value	Unit
Drain-Source Voltage			V_{DSS}	-100	V
Gate-Source Voltage			V_{GSS}	±20	V
Continuous Drain Current (Note 5) V_{GS} = -10V	Steady State	T_A = +25°C T_A = +70°C	I_D	-2.3 -1.9	A
Maximum Body Diode Forward Current (Note 5)			I_S	-2.4	A
Pulsed Drain Current (10µs pulse, Duty Cycle = 1%)			I_{DM}	-11	A

Thermal Characteristics (@T_A = +25°C, unless otherwise specified.)

Characteristic		Symbol	Value	Unit
Total Power Dissipation (Note 5)	T_A = +25°C	P_D	2.1	W
Thermal Resistance, Junction to Ambient (Note 5)		$R_{\theta JA}$	60	°C/W
Thermal Resistance, Junction to Case (Note 5)		$R_{\theta JC}$	6	
Operating and Storage Temperature Range		T_J, T_{STG}	-55 to +150	°C

Note: 5. Device mounted on FR-4 substrate PC board, 2oz copper, with 1inch square copper pad layout.

Electrical Characteristics Q1 & Q4 N-Channel (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 6)						
Drain-Source Breakdown Voltage	BV_{DSS}	100	—	—	V	V_{GS} = 0V, I_D = 250µA
Zero Gate Voltage Drain Current	I_{DSS}	—	—	1	µA	V_{DS} = 80V, V_{GS} = 0V
Gate-Source Leakage	I_{GSS}	—	—	±100	nA	V_{GS} = ±20V, V_{DS} = 0V
ON CHARACTERISTICS (Note 6)						
Gate Threshold Voltage	$V_{GS(TH)}$	1.0	2.0	3.0	V	V_{DS} = V_{GS}, I_D = 250µA
Static Drain-Source On-Resistance	$R_{DS(ON)}$	—	111	160	mΩ	V_{GS} = 10V, I_D = 5A
		—	121	200		V_{GS} = 4.5V, I_D = 5A
Diode Forward Voltage	V_{SD}	—	0.9	1.0	V	V_{GS} = 0V, I_S = 10A
DYNAMIC CHARACTERISTICS (Note 7)						
Input Capacitance	C_{iss}	—	1,167	—	pF	V_{DS} = 25V, V_{GS} = 0V, f = 1.0MHz
Output Capacitance	C_{oss}	—	36	—		
Reverse Transfer Capacitance	C_{rss}	—	25	—		
Gate Resistance	R_G	—	1.3	—	Ω	V_{DS} = 0V, V_{GS} = 0V, f = 1.0MHz
Total Gate Charge (V_{GS} = 4.5V)	Q_g	—	4.9	—	nC	V_{DS} = 80V, I_D = 12.8A
Total Gate Charge (V_{GS} = 10V)	Q_g	—	9.7	—		
Gate-Source Charge	Q_{gs}	—	2.0	—		
Gate-Drain Charge	Q_{gd}	—	2.0	—		
Turn-On Delay Time	$t_{D(ON)}$	—	10.5	—	ns	V_{DD} = 50V, R_G = 25Ω, I_D = 12.8A
Turn-On Rise Time	t_R	—	11.1	—		
Turn-Off Delay Time	$t_{D(OFF)}$	—	42.6	—		
Turn-Off Fall Time	t_F	—	12.8	—		
Body Diode Reverse Recovery Time	t_{RR}	—	30.3	—	ns	V_{GS} = 0V, I_S = 12.8A, dI/dt = 100A/µs
Body Diode Reverse Recovery Charge	Q_{RR}	—	35.2	—	nC	V_{GS} = 0V, I_S = 12.8A, dI/dt = 100A/µs

Electrical Characteristics Q2 & Q3 P-Channel (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 6)						
Drain-Source Breakdown Voltage	BV_{DSS}	-100	—	—	V	V_{GS} = 0V, I_D = -250µA
Zero Gate Voltage Drain Current	I_{DSS}	—	—	1	µA	V_{DS} = -80V, V_{GS} = 0V
Gate-Source Leakage	I_{GSS}	—	—	±100	nA	V_{GS} = ±20V, V_{DS} = 0V
ON CHARACTERISTICS (Note 6)						
Gate Threshold Voltage	$V_{GS(TH)}$	-1.0	-1.6	-3.0	V	V_{DS} = V_{GS}, I_D = -250µA
Static Drain-Source On-Resistance	$R_{DS(ON)}$	—	191	250	mΩ	V_{GS} = -10V, I_D = -5A
		—	213	300		V_{GS} = -4.5V, I_D =-5A
Diode Forward Voltage	V_{SD}	—	-0.9	-1.2	V	V_{GS} = 0V, I_S = -5A
DYNAMIC CHARACTERISTICS (Note 7)						
Input Capacitance	C_{iss}	—	1,239	—	pF	V_{DS} = -25V, V_{GS} = 0V, f = 1.0MHz
Output Capacitance	C_{oss}	—	42	—		
Reverse Transfer Capacitance	C_{rss}	—	28	—		
Gate Resistance	R_g	—	13	—	Ω	V_{DS} = 0V, V_{GS} = 0V, f = 1.0MHz
Total Gate Charge (V_{GS} = -4.5V)	Q_g	—	8.4	—	nC	V_{DS} = -60V, I_D = -5A
Total Gate Charge (V_{GS} = -10V)	Q_g	—	17.5	—		
Gate-Source Charge	Q_{gs}	—	2.8	—		
Gate-Drain Charge	Q_{gd}	—	3.2	—		
Turn-On Delay Time	$t_{D(ON)}$	—	9.1	—	ns	V_{DD} = -50V, R_g = 9.1Ω, I_D = -5A
Turn-On Rise Time	t_R	—	14.9	—		
Turn-Off Delay Time	$t_{D(OFF)}$	—	57.4	—		
Turn-Off Fall Time	t_F	—	34.4	—		
Body Diode Reverse Recovery Time	t_{RR}	—	25.2	—	ns	V_{GS} = 0V, I_S = -5A, di/dt = 100A/µs
Body Diode Reverse Recovery Charge	Q_{RR}	—	24.5	—	nC	V_{GS} = 0V, I_S = -5A, di/dt = 100A/µs

Notes: 6. Short duration pulse test used to minimize self-heating effect.
7. Guaranteed by design. Not subject to production testing.

Typical Characteristics - N-CHANNEL

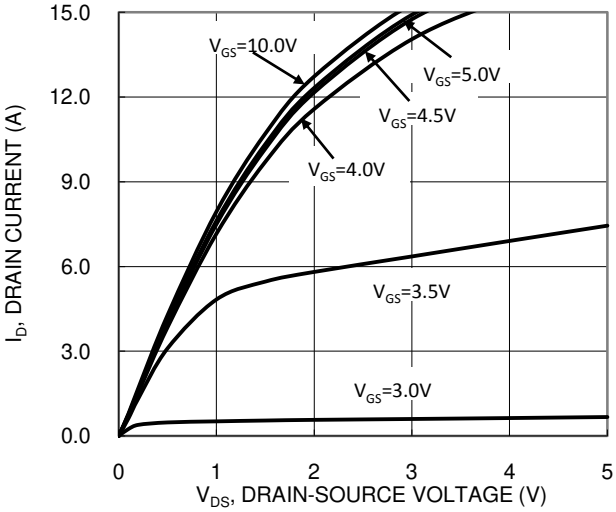


Figure 1. Typical Output Characteristic

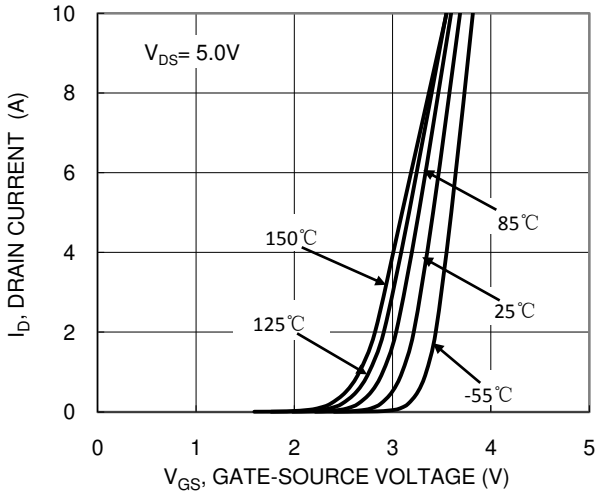


Figure 2. Typical Transfer Characteristic

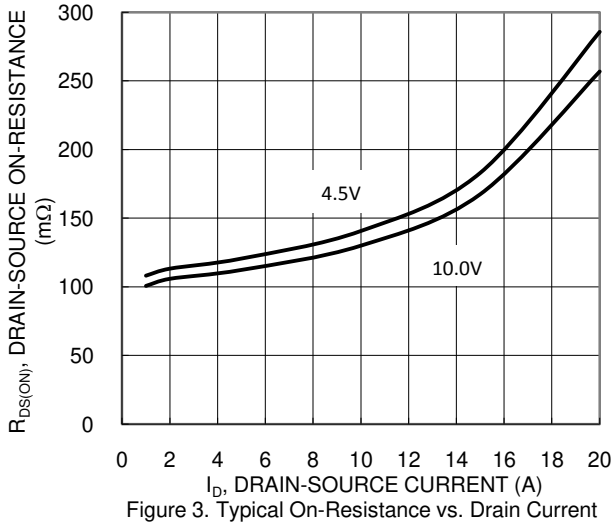


Figure 3. Typical On-Resistance vs. Drain Current and Gate Voltage

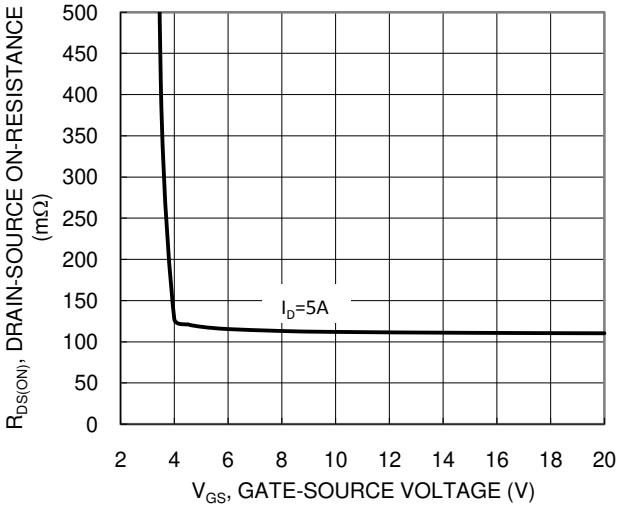


Figure 4. Typical Transfer Characteristic

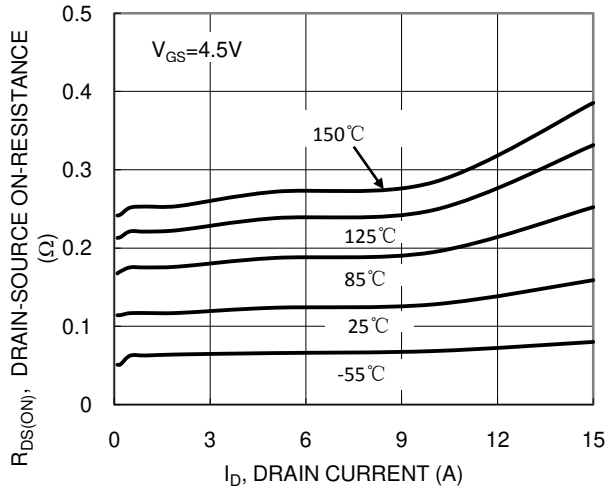


Figure 5. Typical On-Resistance vs. Drain Current and Temperature

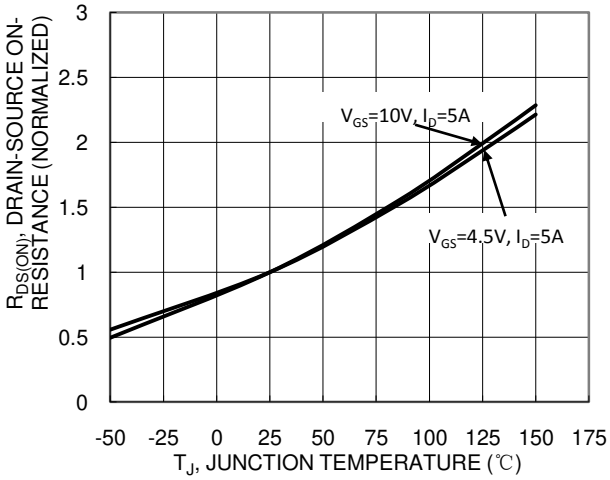


Figure 6. On-Resistance Variation with Temperature

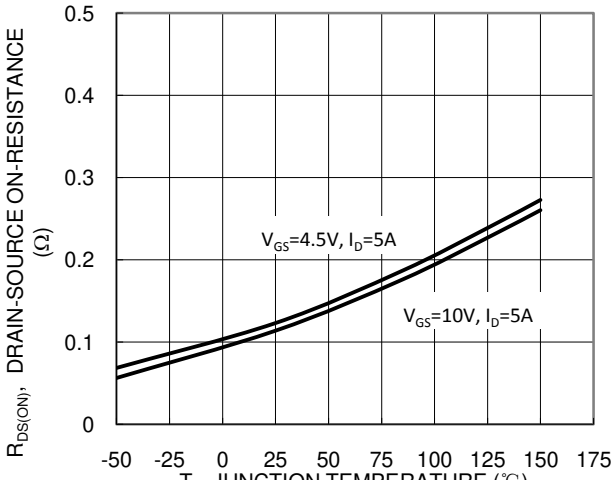


Figure 7. On-Resistance Variation with Temperature

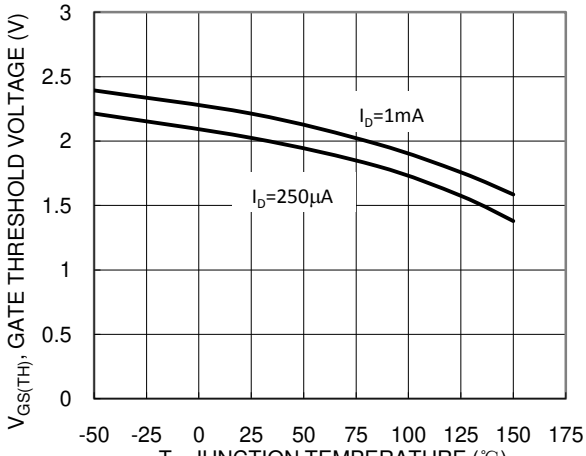


Figure 8. Gate Threshold Variation vs. JunctionTemperature

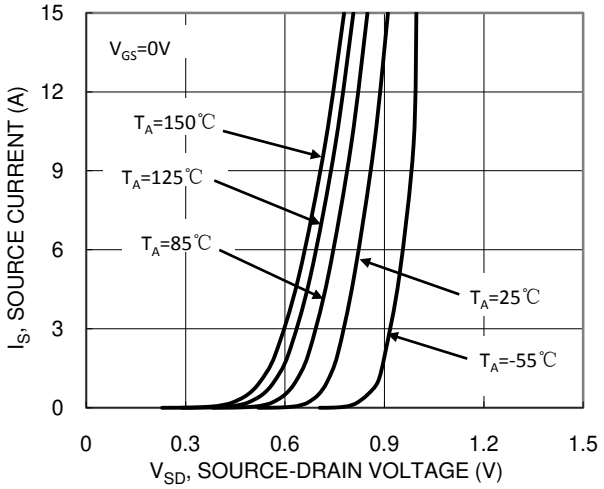


Figure 9. Diode Forward Voltage vs. Current

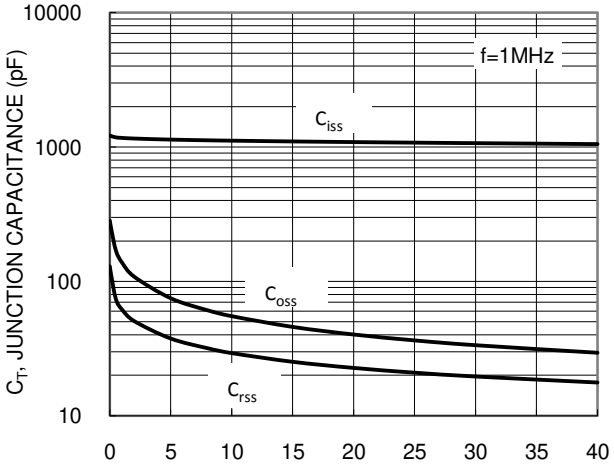


Figure 10. Typical Junction Capacitance

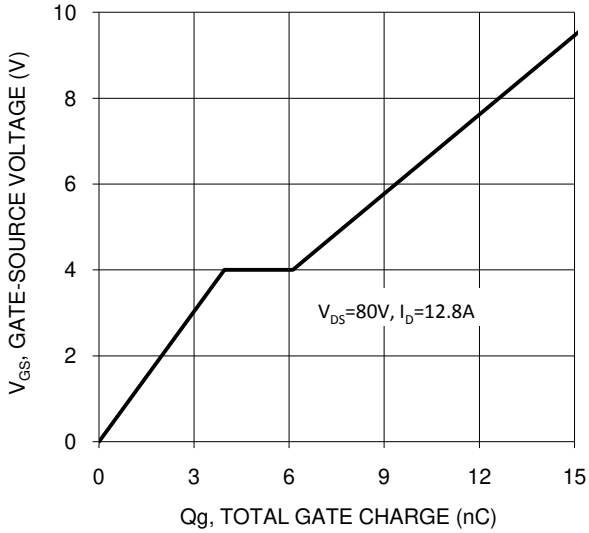


Figure 11. Gate Charge

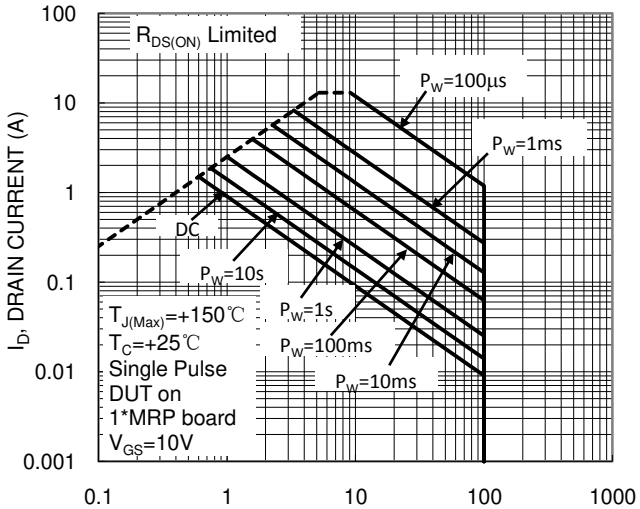


Figure 12. SOA, Safe Operation Area

Typical Characteristics - P-CHANNEL

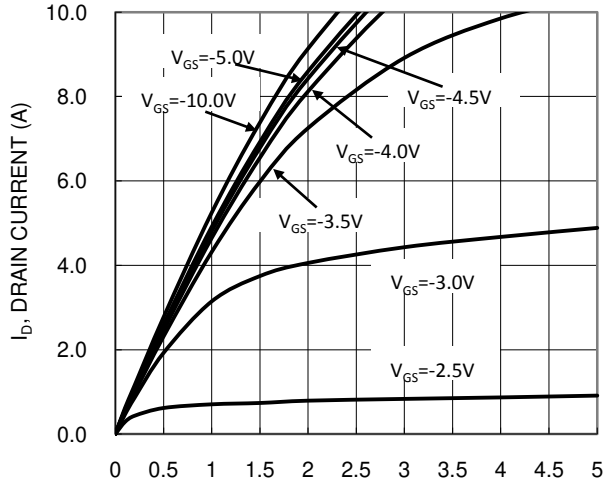


Figure 13. Typical Output Characteristic

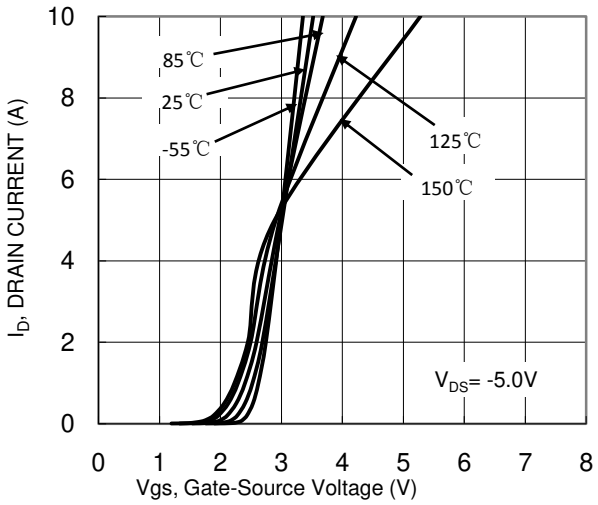


Fig.14 Typical Transfer Characteristic

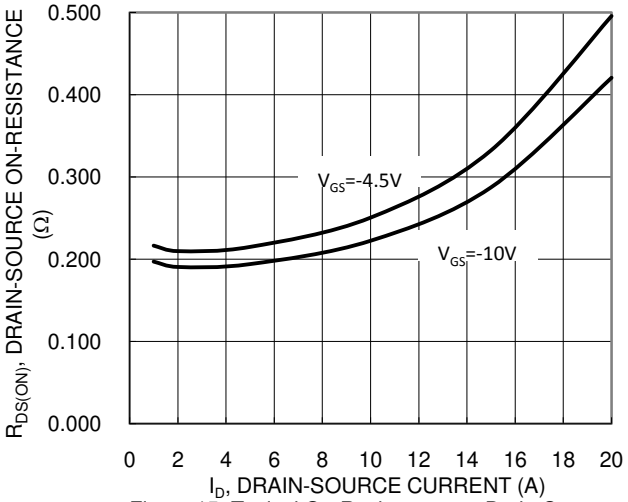


Figure 15. Typical On-Resistance vs. Drain Current and Gate Voltage

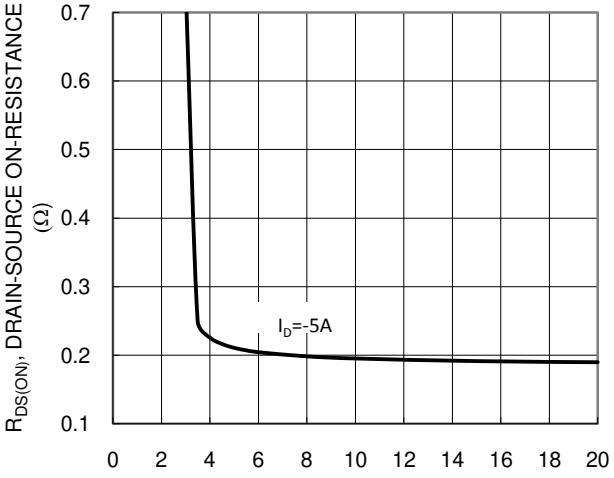


Figure 16. Typical Transfer Characteristic

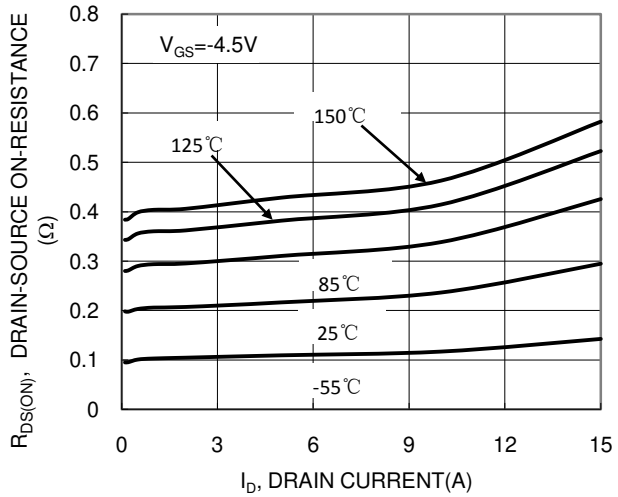


Figure 17. Typical On-Resistance vs. Drain Current and Temperature

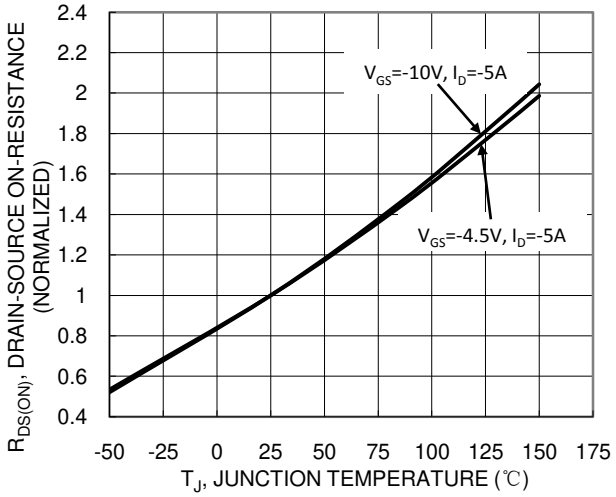


Figure 18. On-Resistance Variation with Temperature

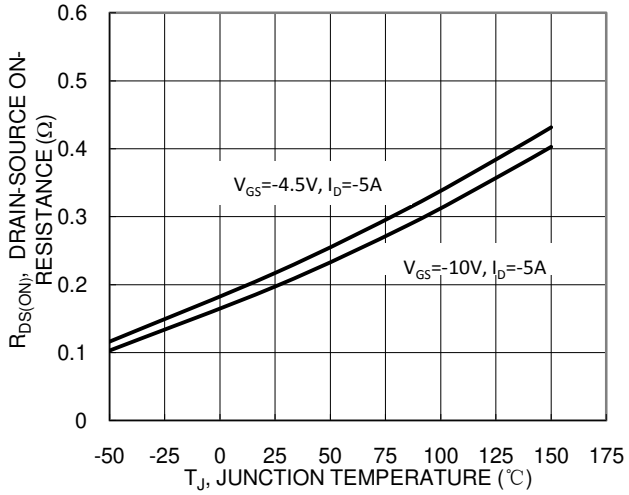


Figure 19. On-Resistance Variation with Temperature

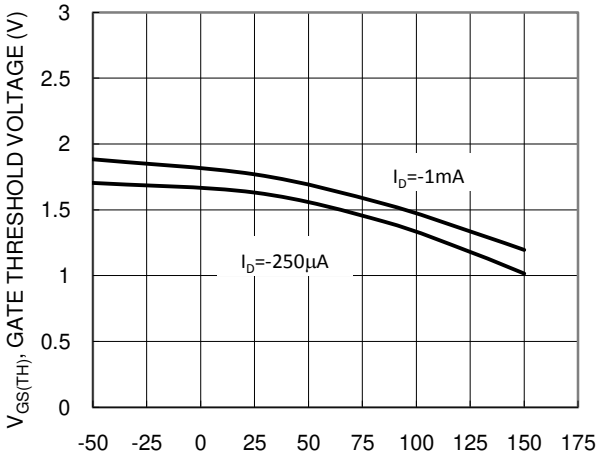


Figure 20. Gate Threshold Variation vs. Junction Temperature

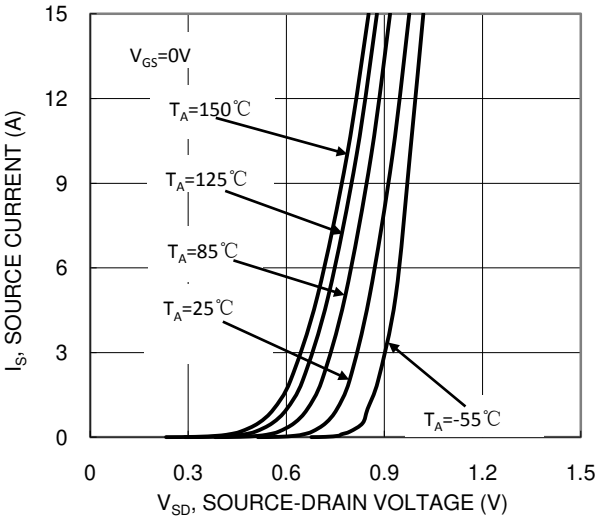


Figure 21. Diode Forward Voltage vs. Current

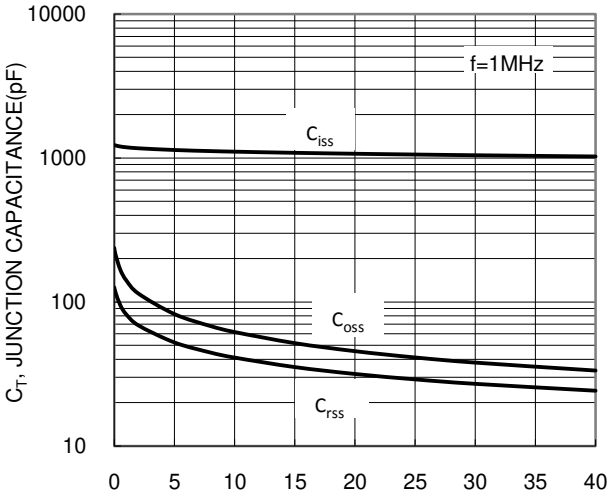


Figure 22. Typical Junction Capacitance

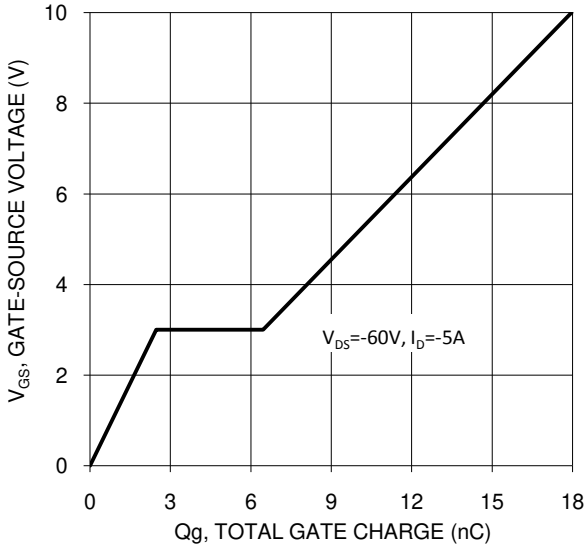


Figure 23. Gate Charge

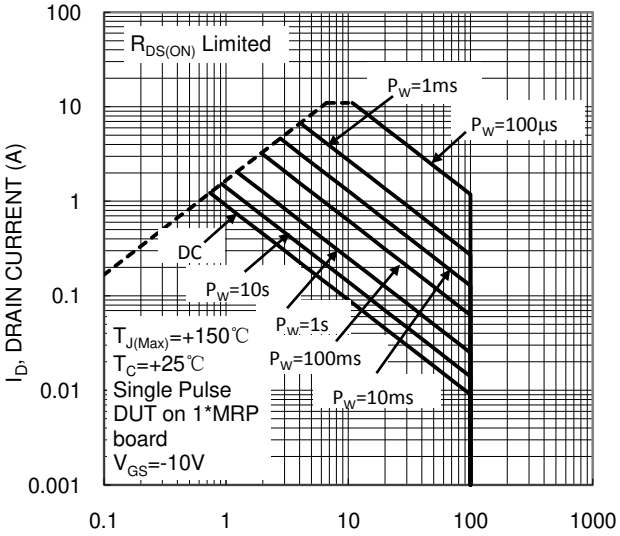


Figure 24. SOA, Safe Operation Area

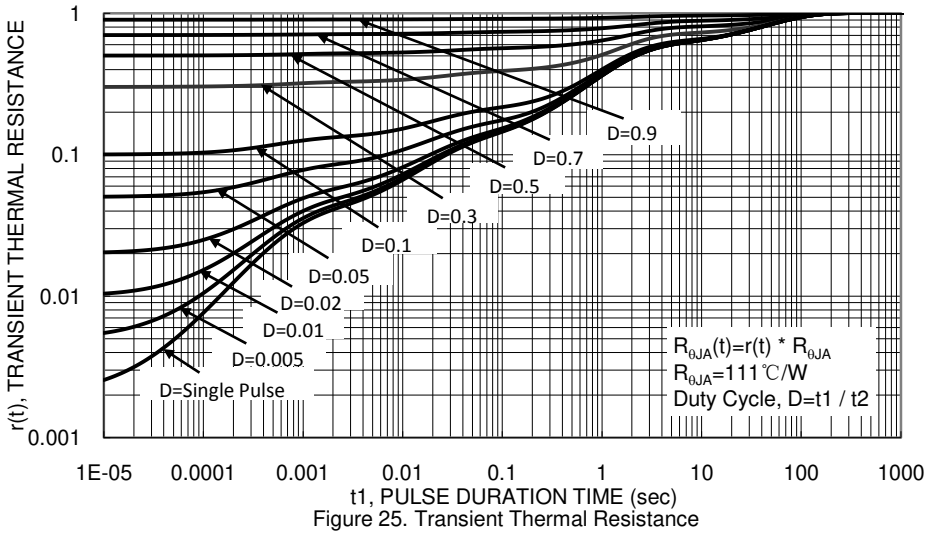
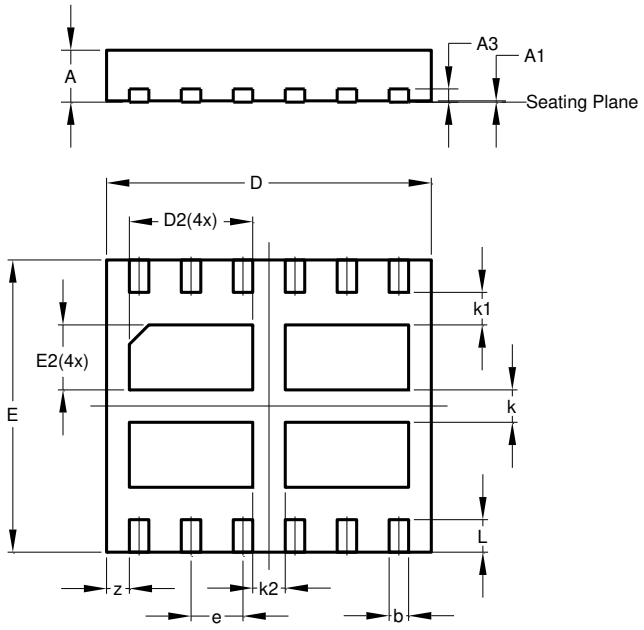


Figure 25. Transient Thermal Resistance

Package Outline Dimensions

Please see AP02001 at http://www.diodes.com/_files/datasheets/ap02001.pdf for the latest version.

V-DFN5045-12

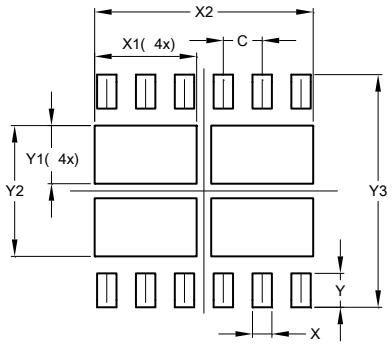


V-DFN5045-12			
Dim	**Min**	**Max**	**Typ**
A	0.75	0.85	0.80
A1	0.00	0.05	0.02
A3	-	-	0.203
b	0.25	0.35	0.30
D	4.95	5.05	5.00
D2	1.80	2.00	1.90
E	4.45	4.55	4.50
E2	0.90	1.10	1.00
e	-	-	0.80
k	-	-	0.50
k1	-	-	0.50
k2	-	-	0.50
L	0.45	0.55	0.50
z	-	-	0.35
All Dimensions in mm			

Suggested Pad Layout

Please see AP02001 at http://www.diodes.com/_files/datasheets/ap02001.pdf for the latest version.

V-DFN5045-12



Dimensions	Value (in mm)
C	0.800
X	0.400
X1	2.100
X2	4.500
Y	0.700
Y1	1.200
Y2	2.700
Y3	4.800