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DMN6040SVTQ

60V N-CHANNEL ENHANCEMENT MODE MOSFET

Product Summary

V _{(BR)DSS}	R _{DS(ON)} Max	I _D T _A = +25°C
60V	44mΩ @ V _{GS} = 10V	5.0A
607	60mΩ @ V _{GS} = 4.5V	4.3A

Features and Benefits

- 100% Unclamped Inductive Switch (UIS) Test in Production
- Low Input Capacitance
- Low On-Resistance
- Fast Switching Speed
- Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)
- Halogen and Antimony Free. "Green" Device (Note 3)
- Qualified to AEC-Q101 standards for High Reliability
- PPAP Capable (Note 4)

Description and Applications

This new generation MOSFET is designed to minimize the on-state resistance (R_{DS(ON)}), yet maintain superior switching performance, making it ideal for high efficiency power management applications.

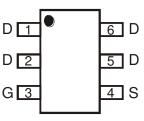
- DC-DC Converters
- Power Management Functions
- Backlighting

Mechanical Data

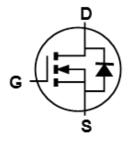
- Case: TSOT26
- Case Material: Molded Plastic, "Green" Molding Compound.
 UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminal Connections: See Diagram
- Terminals: Finish Tin Finish Annealed over Copper Leadframe.
 Solderable per MIL-STD-202, Method 208 (§3)
- Weight: 0.013 grams (Approximate)







Top View Pin Configuration



Equivalent Circuit

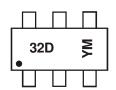
Ordering Information (Note 5)

Part Number	Case	Packaging
DMN6040SVTQ-7	TSOT26	3,000/Tape & Reel
DMN6040SVTQ-13	TSOT26	10,000/Tape & Reel

Notes:

- 1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS) & 2011/65/EU (RoHS 2) compliant.
- 2. See http://www.diodes.com/quality/lead_free.html for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
- 3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
- 4. Automotive products are AEC-Q101 qualified and are PPAP capable. Please refer to http://www.diodes.com/quality/product_compliance_definitions/.
- 5. For packaging details, go to our website at http://www.diodes.com/products/packages.html.

Marking Information



32D = Product Type Marking Code YM = Date Code Marking Y = Year (ex: X = 2010) M = Month (ex: 9 = September)

Date Code Key

Year	2010		2017	2018	20	19 20	020	2021	2022	2023	2024	2025
Code	Χ		Е	F	G	i	Н	1	J	K	Г	М
Month	Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec
Code	1	2	3	4	5	6	7	8	9	0	N	D



Maximum Ratings (@T_A = +25°C, unless otherwise specified.)

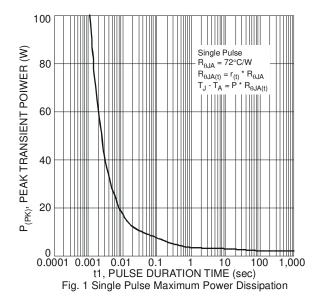
Characteristic	Symbol	Value	Units		
Drain-Source Voltage	V_{DSS}	60	V		
Gate-Source Voltage	V_{GSS}	±20	V		
Continuous Drain Current (Note 7) V 10V	Steady State	$T_A = +25$ °C $T_A = +70$ °C	I _D	5.0 4.0	А
Continuous Drain Current (Note 7) V _{GS} = 10V	t<10s	$T_A = +25^{\circ}C$ $T_A = +70^{\circ}C$	I _D	6.3 5.0	А
Continuous Dunin Comment (Note 7) V	Steady State	$T_A = +25$ °C $T_A = +70$ °C	I _D	4.3 3.4	Α
Continuous Drain Current (Note 7) V _{GS} = 5V	t<10s	$T_A = +25$ °C $T_A = +70$ °C	I _D	5.4 4.3	А
Maximum Body Diode Forward Current (Note 7)	Is	2.1	Α		
Pulsed Drain Current (10µs Pulse, Duty Cycle = 1%)	I _{DM}	30	Α		
Avalanche Current (Note 8) L = 0.1mH	I _{AR}	14.2	Α		
Avalanche Energy (Note 8) L = 0.1mH	E _{AR}	10	mJ		

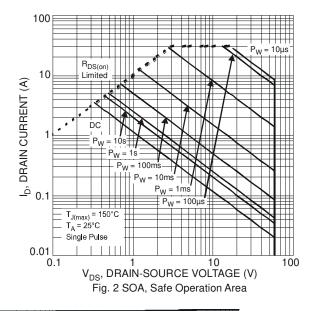
Thermal Characteristics (@T_A = +25°C, unless otherwise specified.)

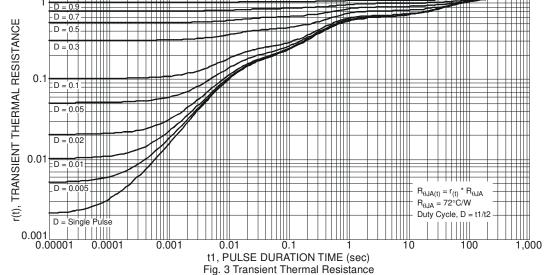
Characteristic		Symbol	Value	Units	
Total Power Dissipation (Note 6)	$T_A = +25^{\circ}C$	P _D	1.2	W	
Total Fower Dissipation (Note 6)	$T_A = +70^{\circ}C$	PD	0.75		
Thermal Resistance, Junction to Ambient (Note 6)	Steady State	В	106	°C/W	
Thermal Resistance, Junction to Ambient (Note 6)	t<10s	$R_{\theta JA}$	69	°C/W	
Total Power Dissipation (Note 7)	$T_A = +25^{\circ}C$	P_D	1.8	W	
Total Fower Dissipation (Note 7)	$T_A = +70^{\circ}C$	r _D	1.1		
Thermal Resistance, Junction to Ambient (Note 7)	Steady State	D	68	°C/W	
Themai hesistance, bunction to Ambient (Note 1)	t<10s	R _{eja}	44	°C/W	
Thermal Resistance, Junction to Case (Note 7)		$R_{ heta JC}$	20	°C/W	
Operating and Storage Temperature Range		T _J , T _{STG}	-55 to +150	°C	

- 6. Device mounted on FR-4 substrate PC board, 2oz copper, with minimum recommended pad layout. 7. Device mounted on FR-4 substrate PC board, 2oz copper, with 1inch square copper plate.
- 8. IAR and EAR rating are based on low frequency and duty cycles to keep $T_J = +25$ °C.











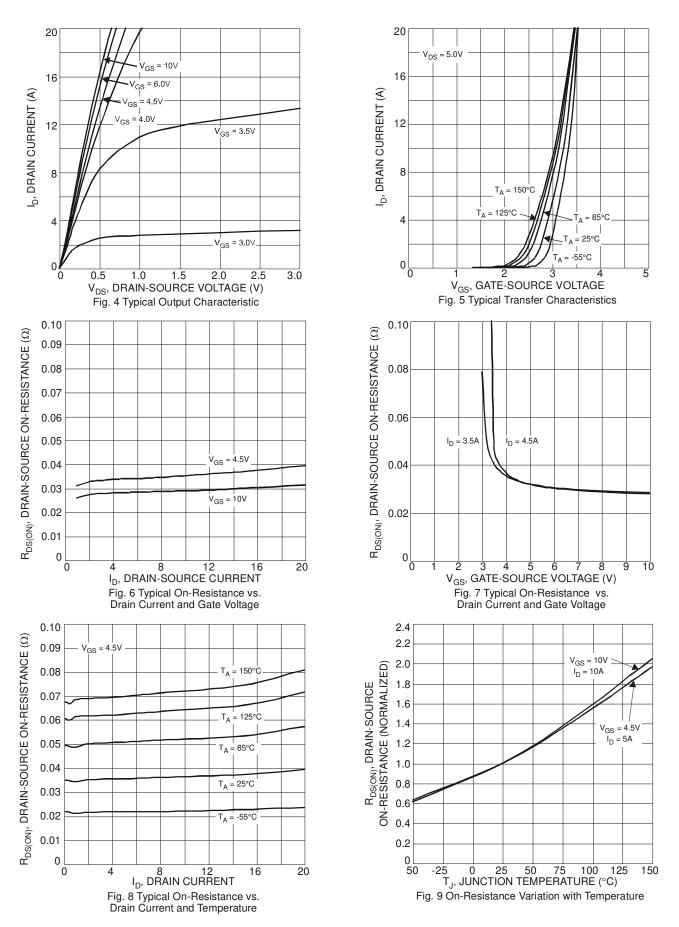
Electrical Characteristics @TA = 25°C unless otherwise specified

Characteristic	Symbol	Min	Тур	Max	Unit	Test Condition	
OFF CHARACTERISTICS (Note 9)							
Drain-Source Breakdown Voltage	BV _{DSS}	60	_	_	V	$V_{GS} = 0V, I_D = 250\mu A$	
Zero Gate Voltage Drain Current	I _{DSS}	_	_	100	nA	$V_{DS} = 60V, V_{GS} = 0V$	
Gate-Source Leakage	I _{GSS}	_	_	±100	nA	$V_{GS} = \pm 20V, V_{DS} = 0V$	
ON CHARACTERISTICS (Note 9)							
Gate Threshold Voltage	V _{GS(TH)}	1		3	V	$V_{DS} = V_{GS}, I_D = 250 \mu A$	
Static Drain-Source On-Resistance	D		30	44	mΩ	$V_{GS} = 10V, I_D = 4.3A$	
Static Diain-Source Off-Nesistance	R _{DS(ON)}		35	60	11152	$V_{GS} = 4.5V, I_D = 4A$	
Forward Transfer Admittance	Y _{FS}		4.5	_	S	$V_{DS} = 10V, I_D = 4.3A$	
Diode Forward Voltage	V_{SD}	_	0.7	1.2	V	$V_{GS} = 0V, I_{S} = 1A$	
DYNAMIC CHARACTERISTICS (Note 10)							
Input Capacitance	CISS		1,287	_		V _{DS} = 25V, V _{GS} = 0V f = 1.0MHz	
Output Capacitance	Coss		57	_	pF		
Reverse Transfer Capacitance	C _{RSS}		44	_		1 = 1.0IVII IZ	
Gate Resistance	Rg	_	1.2	_	Ω	$V_{DS} = 0V, V_{GS} = 0V, f = 1.0MHz$	
Total Gate Charge (V _{GS} = 10V)	Q_{G}	_	22.4				
Total Gate Charge (V _{GS} = 4.5V)	Q_{G}	_	10.4	_	nC	V 20V L 4.0A	
Gate-Source Charge	Q _{GS}	_	4.9	_	110	$V_{DS} = 30V, I_{D} = 4.3A$	
Gate-Drain Charge	Q_{GD}	_	3.0	_			
Turn-On Delay Time	t _{D(ON)}	_	6.6	_			
Turn-On Rise Time	t _R	_	8.1	_		$V_{GS} = 10V, V_{DD} = 30V, R_{G} = 6\Omega,$	
Turn-Off Delay Time	t _{D(OFF)}	_	20.1		ns	$I_D = 4.3A$	
Turn-Off Fall Time	t _F		4.0				
Body Diode Reverse Recovery Time	t _{RR}	_	18		ns	I _S = 4.3A, dI/dt = 100A/µs	
Body Diode Reverse Recovery Charge	Q _{RR}	_	11.9		nC	I _S = 4.3A, dI/dt = 100A/µs	

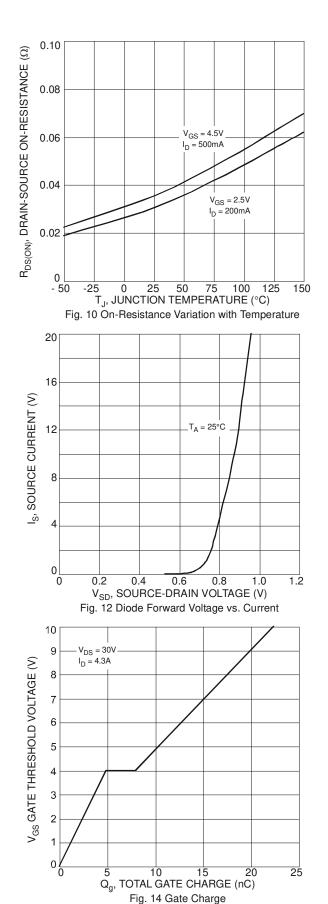
Notes:

^{9.} Short duration pulse test used to minimize self-heating effect. 10. Guaranteed by design. Not subject to product testing.









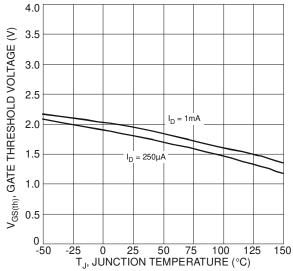
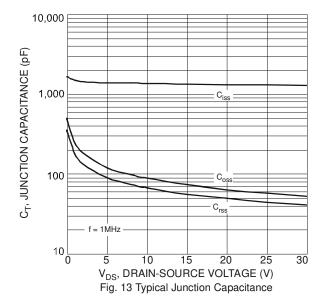


Fig. 11 Gate Threshold Variation vs. Ambient Temperature

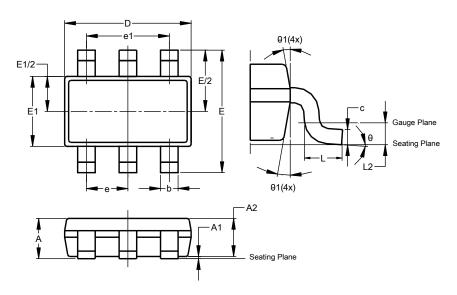




Package Outline Dimensions

Please see AP02002 at http://www.diodes.com/datasheets/ap02002.pdf for the latest version.

TSOT26

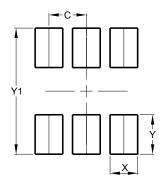


TSOT26							
Dim	Min Max Typ						
Α	-	1.00	-				
A1	0.010	0.100	_				
A2	0.840	0.900	-				
D	2.800	3.000	2.900				
Е	2	.800 BS	С				
E1	1.500 1.700 1.600						
p	0.300	0.450	-				
С	0.120	0.200	_				
е	0.950 BSC						
e1	1	.900 BS	C				
L	0.30	0.50					
L2	0.250 BSC						
θ	0°	8°	4°				
θ1	4°	12°	_				
All Dimensions in mm							

Suggested Pad Layout

Please see AP02001 at http://www.diodes.com/datasheets/ap02001.pdf for the latest version.

TSOT26



Dimensions	Value (in mm)
С	0.950
Х	0.700
Υ	1.000
Y1	3.199



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