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**DMP21D0UFB**

**20V P-CHANNEL ENHANCEMENT MODE MOSFET**

**Product Summary**

$V_{(BR)DSS}$	$R_{DS(on) Max}$	$I_D Max$ @ $T_A = 25^\circ C$ (Note 4)
-20V	495m $\Omega$ @ $V_{GS} = -4.5V$	-0.77A
	690m $\Omega$ @ $V_{GS} = -2.5V$	-0.67A
	960m $\Omega$ @ $V_{GS} = -1.8V$	-0.57A

**Description and Applications**

This MOSFET has been designed to minimize the on-state resistance ( $R_{DS(on)}$ ) and yet maintain superior switching performance, making it ideal for high efficiency power management applications.

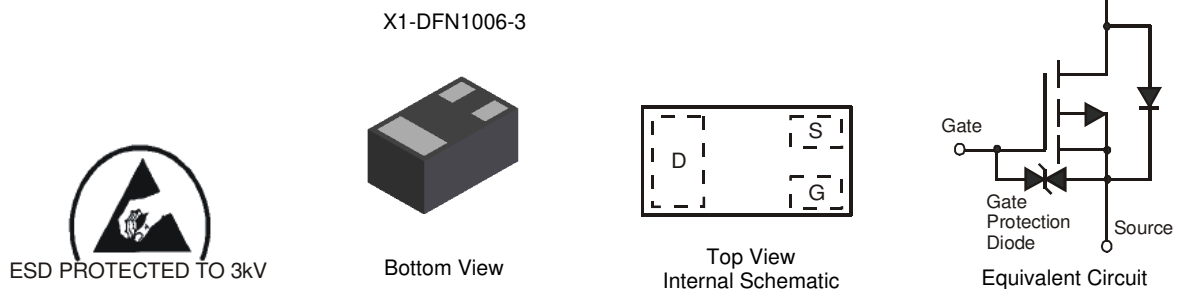
- Portable electronics

**Features and Benefits**

- Footprint of just 0.6mm<sup>2</sup> – thirteen times smaller than SOT23
- Low Gate Threshold Voltage
- Fast Switching Speed
- **Totally Lead-Free & Fully RoHS compliant (Note 1)**
- **Halogen and Antimony Free. "Green" Device (Note 2)**
- **ESD Protected Gate 3KV**
- **Qualified to AEC-Q101 Standards for High Reliability**

**Mechanical Data**

- Case: X1-DFN1006-3
- Case Material: Molded Plastic, "Green" Molding Compound. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals: Finish – NiPdAu over Copper leadframe. Solderable per MIL-STD-202, Method 208
- Weight: 0.001 grams (approximate)



**Ordering Information** (Note 3)

Part Number	Marking	Reel size (inches)	Tape width (mm)	Quantity per reel
DMP21D0UFB-7B	NG	7	8	10,000

- Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS) & 2011/65/EU (RoHS 2) compliant.
  2. Halogen and Antimony free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
  3. For packaging details, go to our website at <http://www.diodes.com>.

**Marking Information**

DMP21D0UFB-7B



NG = Product Type Marking Code

Top View  
Bar Denotes Gate  
and Source Side

**Maximum Ratings** @ $T_A = 25^\circ\text{C}$  unless otherwise specified

Characteristic			Symbol	Value	Unit
Drain-Source Voltage			$V_{DSS}$	-20	V
Gate-Source Voltage			$V_{GSS}$	$\pm 8$	V
Continuous Drain Current	Steady State	$T_A = 25^\circ\text{C}$ (Note 4)	$I_D$	-0.77	A
		$T_A = 85^\circ\text{C}$ (Note 4)		-0.55	
		$T_A = 25^\circ\text{C}$ (Note 5)		-1.17	
Pulsed Drain Current (Note 6)			$I_{DM}$	-5.0	A

**Thermal Characteristics** @ $T_A = 25^\circ\text{C}$  unless otherwise specified

Characteristic	Symbol	Value	Unit
Power Dissipation (Note 4)	$P_D$	0.43	W
Power Dissipation (Note 5)	$P_D$	0.99	W
Thermal Resistance, Junction to Ambient (Note 4)	$R_{\theta JA}$	293	$^\circ\text{C/W}$
Thermal Resistance, Junction to Ambient (Note 5)	$R_{\theta JA}$	126	$^\circ\text{C/W}$
Operating and Storage Temperature Range	$T_J, T_{STG}$	-55 to +150	$^\circ\text{C}$

**Thermal Characteristics**

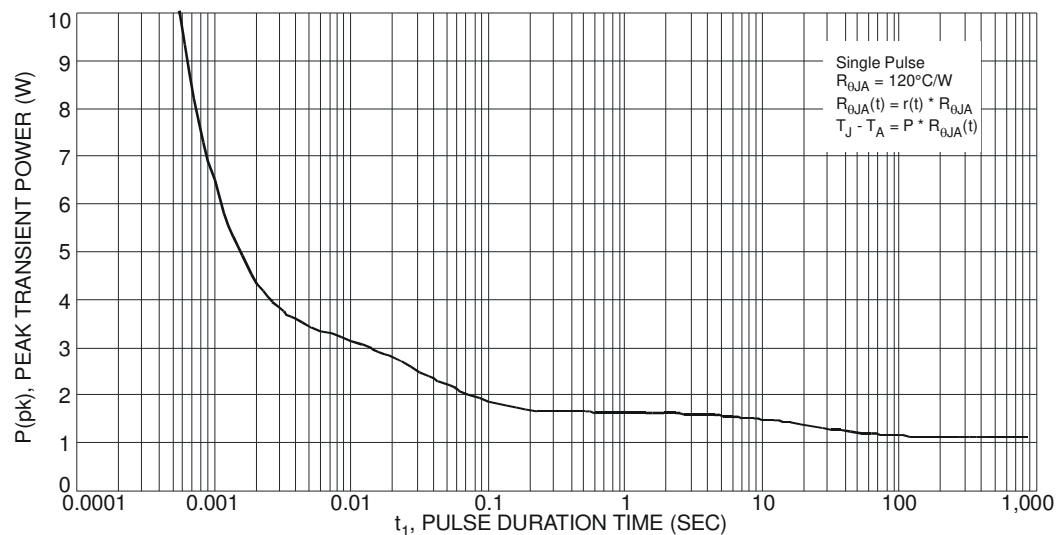


Fig. 1 Single Pulse Maximum Power Dissipation

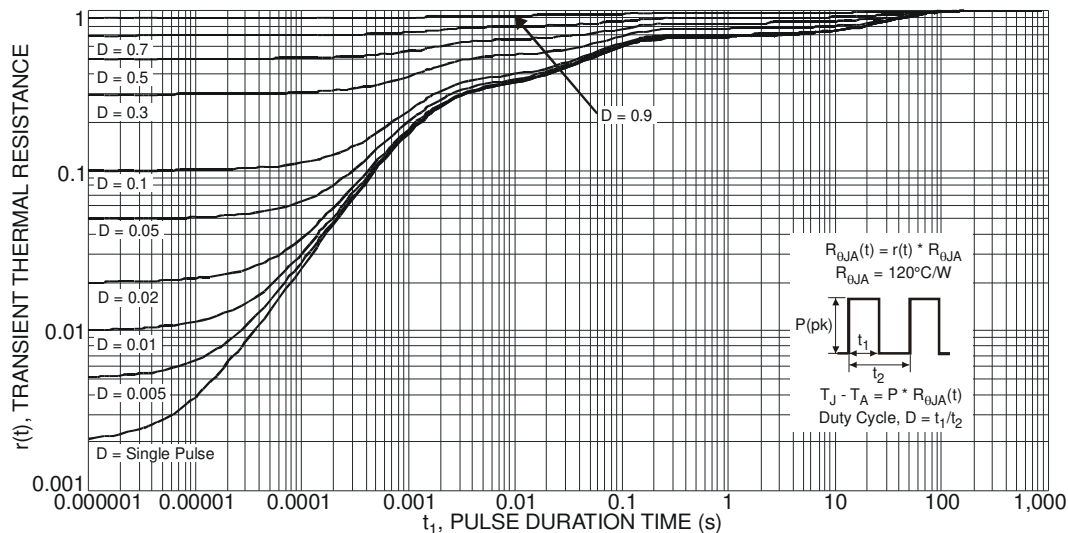


Fig. 2 Transient Thermal Response

**Electrical Characteristics** @T<sub>A</sub> = 25°C unless otherwise specified

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
<b>OFF CHARACTERISTICS (Note 7)</b>						
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	20	-	-	V	V <sub>GS</sub> = 0V, I <sub>D</sub> = -250μA
Zero Gate Voltage Drain Current T <sub>J</sub> = 25°C	I <sub>DSS</sub>	-	-	-1	μA	V <sub>DS</sub> = -20V, V <sub>GS</sub> = 0V
Gate-Source Leakage	I <sub>GSS</sub>	-	-	±10	μA	V <sub>GS</sub> = ±8V, V <sub>DS</sub> = 0V
<b>ON CHARACTERISTICS (Note 7)</b>						
Gate Threshold Voltage	V <sub>GS(th)</sub>	-	-0.7	-	V	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = -250μA
Static Drain-Source On-Resistance	R <sub>DS(ON)</sub>	-	-	495	mΩ	V <sub>GS</sub> = -4.5V, I <sub>D</sub> = -400mA
				690		V <sub>GS</sub> = -2.5V, I <sub>D</sub> = -300mA
				960		V <sub>GS</sub> = -1.8V, I <sub>D</sub> = -100mA
Forward Transfer Admittance	Y <sub>fs</sub>	50	-	-	mS	V <sub>DS</sub> = -3V, I <sub>D</sub> = -300mA
Diode Forward Voltage	V <sub>SD</sub>	-	-	-1.2	V	V <sub>GS</sub> = 0V, I <sub>S</sub> = -300mA
<b>DYNAMIC CHARACTERISTICS</b>						
Input Capacitance	C <sub>iSS</sub>	-	76.5	-	pF	V <sub>DS</sub> = -10V, V <sub>GS</sub> = 0V, f = 1.0MHz
Output Capacitance	C <sub>oSS</sub>	-	13.7	-	pF	
Reverse Transfer Capacitance	C <sub>rSS</sub>	-	10.7	-	pF	
Gate Resistance	R <sub>g</sub>	-	195	-	Ω	V <sub>DS</sub> = 0V, V <sub>GS</sub> = 0V, f = 1MHz
Total Gate Charge	Q <sub>g</sub>	-	1.5	-	nC	V <sub>GS</sub> = -8V, V <sub>DS</sub> = -15V, I <sub>D</sub> = -1A
Total Gate Charge	Q <sub>g</sub>	-	1.0	-	nC	V <sub>GS</sub> = -4.5V, V <sub>DS</sub> = -15V, I <sub>D</sub> = -1A
Gate-Source Charge	Q <sub>gs</sub>	-	0.2	-	nC	
Gate-Drain Charge	Q <sub>gd</sub>	-	0.3	-	nC	
Turn-On Delay Time	t <sub>D(on)</sub>	-	7.1	-	ns	V <sub>DS</sub> = -10V, -I <sub>D</sub> = 1A V <sub>GS</sub> = -4.5V, R <sub>G</sub> = 6Ω
Turn-On Rise Time	t <sub>r</sub>	-	8.0	-	ns	
Turn-Off Delay Time	t <sub>D(off)</sub>	-	31.7	-	ns	
Turn-Off Fall Time	t <sub>f</sub>	-	18.5	-	ns	

- Notes: 4. Device mounted on FR-4 substrate PC board, 2oz copper, with minimum recommended pad layout  
 5. Device mounted on FR-4 substrate PC board, 2oz copper, with thermal vias to bottom layer 1inch square copper plate  
 6. Device mounted on minimum recommended pad layout test board, 10 s pulse duty cycle = 1%.  
 7. Short duration pulse test used to minimize self-heating effect.

**Typical Characteristics**

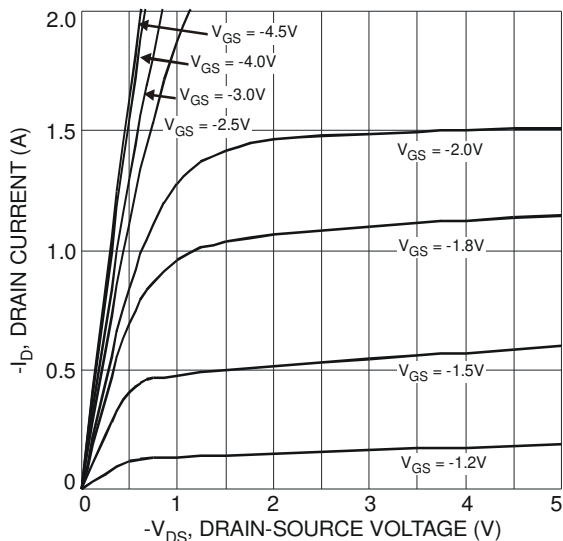


Fig. 3 Typical Output Characteristic

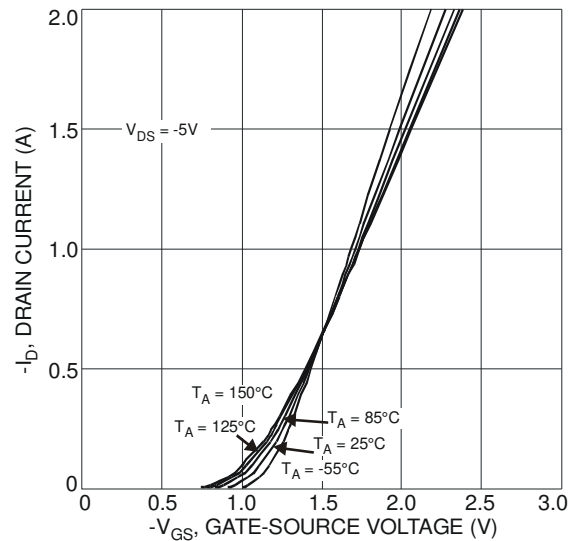


Fig. 4 Typical Transfer Characteristic

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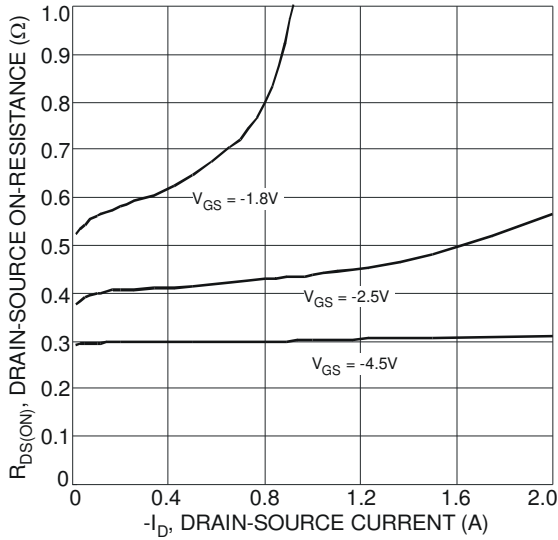


Fig. 5 Typical On-Resistance vs. Drain Current and Gate Voltage

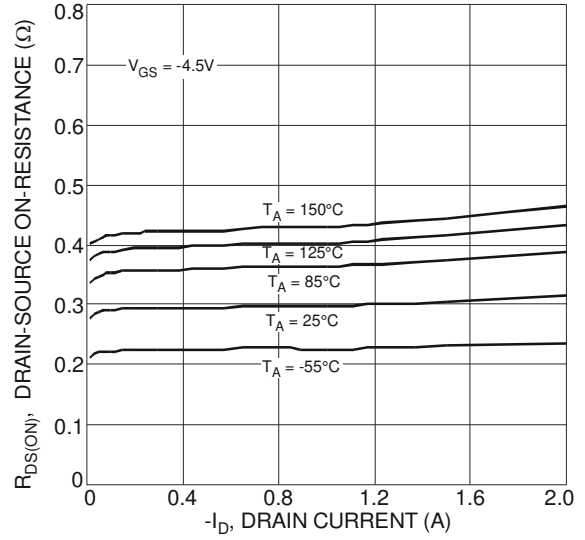


Fig. 6 Typical On-Resistance vs. Drain Current and Temperature

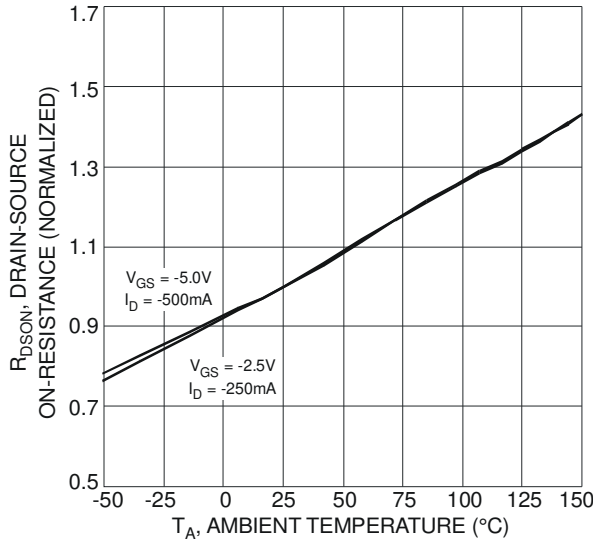


Fig. 7 On-Resistance Variation with Temperature

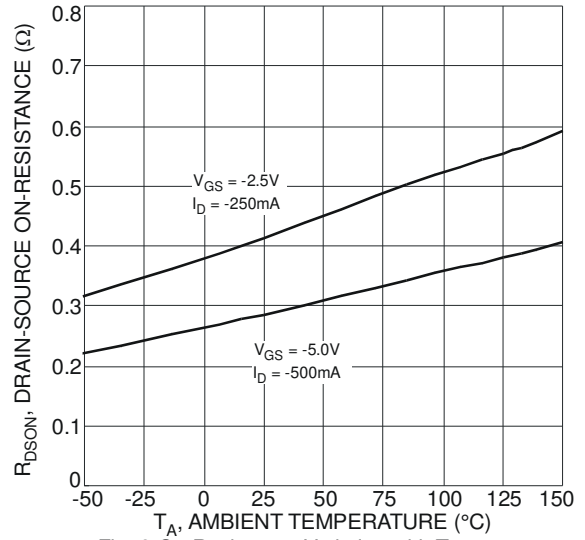


Fig. 8 On-Resistance Variation with Temperature

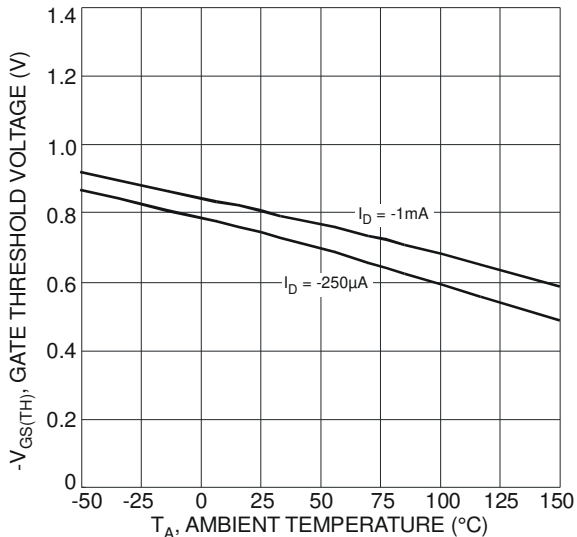


Fig. 9 Gate Threshold Variation vs. Ambient Temperature

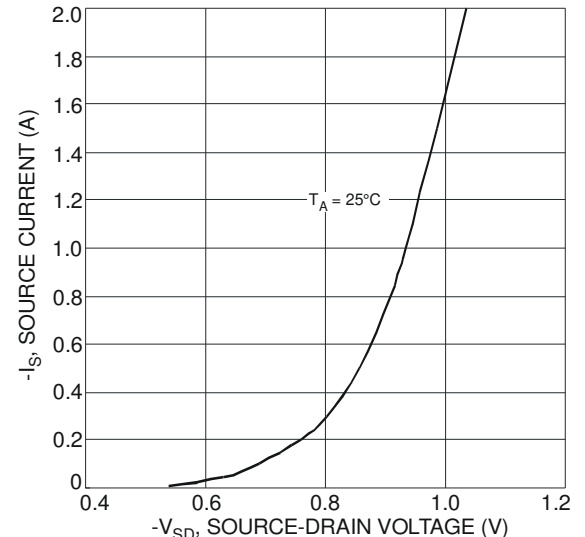


Fig. 10 Diode Forward Voltage vs. Current

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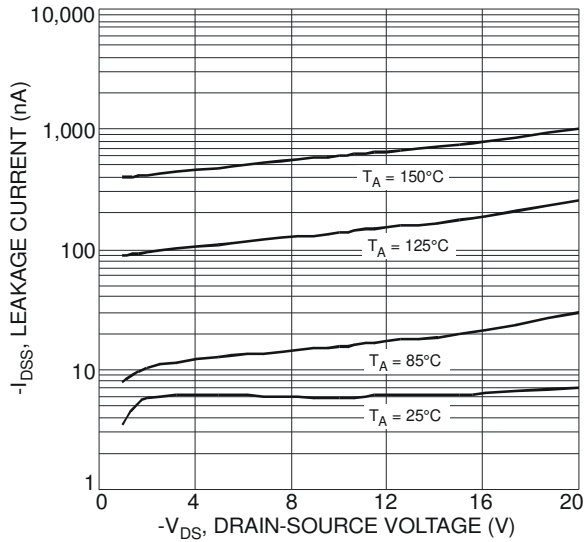


Fig. 11 Typical Leakage Current vs. Drain-Source Voltage

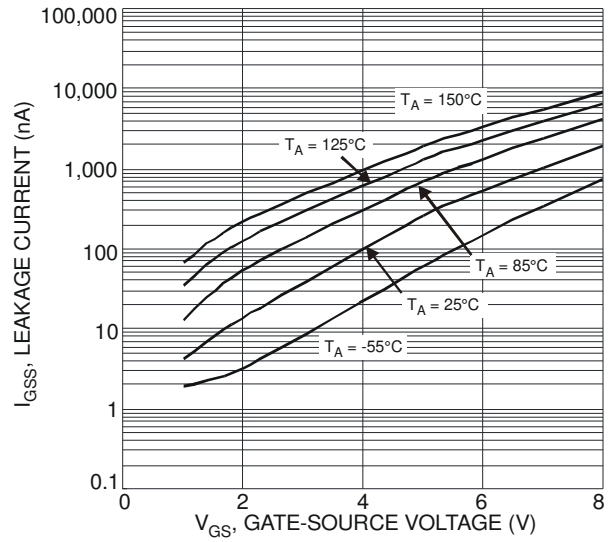


Fig. 12 Leakage Current vs. Gate-Source Voltage

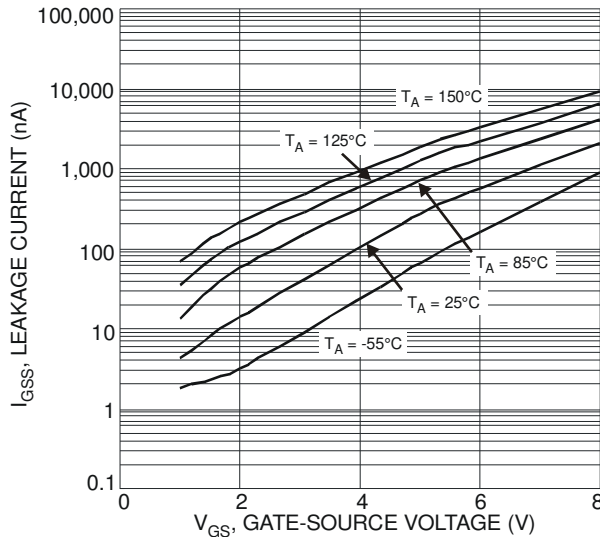


Fig. 13 Leakage Current vs. Gate-Source Voltage

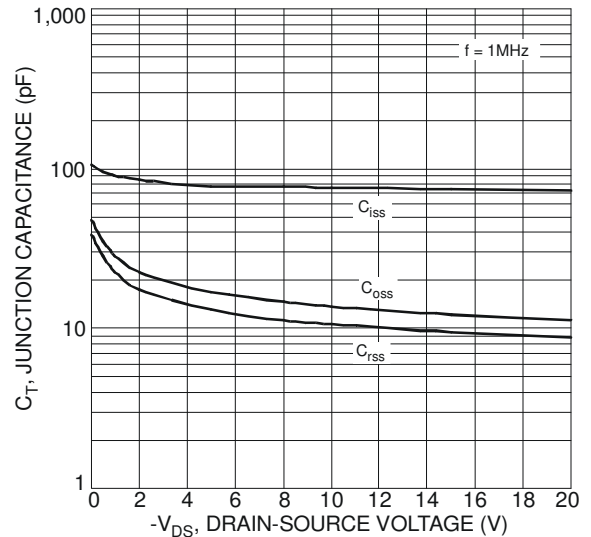


Fig. 14 Typical Junction Capacitance

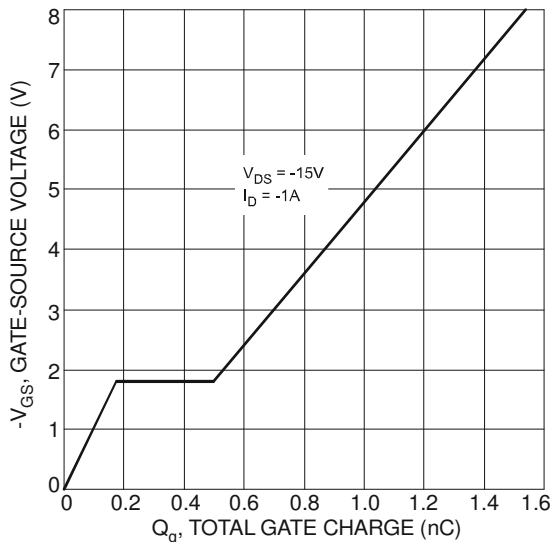
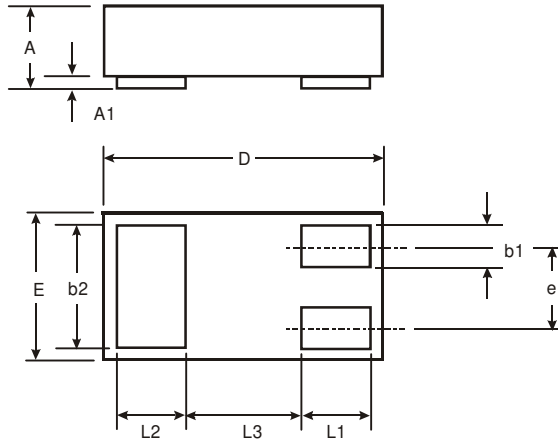


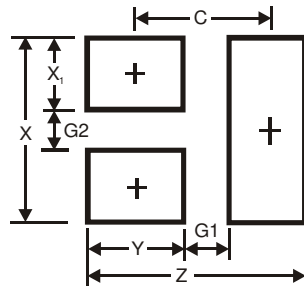
Fig. 15 Gate-Charge Characteristics

**Package Outline Dimensions**



X1-DFN1006-3			
Dim	Min	Max	Typ
A	0.47	0.53	0.50
A1	0	0.05	0.03
b1	0.10	0.20	0.15
b2	0.45	0.55	0.50
D	0.95	1.075	1.00
E	0.55	0.675	0.60
e	—	—	0.35
L1	0.20	0.30	0.25
L2	0.20	0.30	0.25
L3	—	—	0.40
All Dimensions in mm			

**Suggested Pad Layout**



Dimensions	Value (in mm)
Z	1.1
G1	0.3
G2	0.2
X	0.7
X1	0.25
Y	0.4
C	0.7

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