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Product Summary

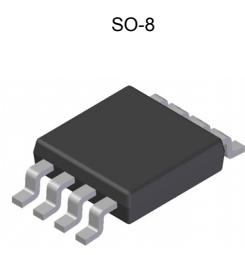
$V_{(BR)DSS}$	$R_{DS(on)}$ max	I_D $T_A = +25^\circ C$
-30V	65m Ω @ $V_{GS} = -10V$	-4.4A
	115m Ω @ $V_{GS} = -4.5V$	-3.2A

Description

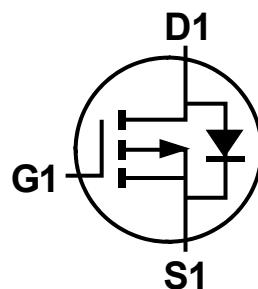
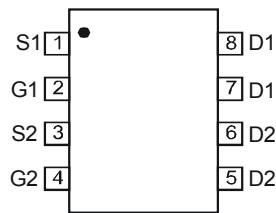
This new generation MOSFET has been designed to minimize the on-state resistance ($R_{DS(ON)}$) and yet maintain superior switching performance, making it ideal for high efficiency power management applications.

Applications

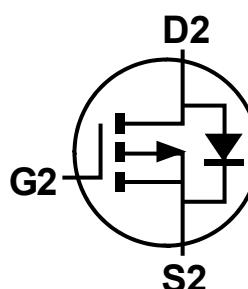
- Power Management Functions
- Analog Switch
- Load Switch
- Boost Switch



TOP VIEW



P-Channel MOSFET



P-Channel MOSFET

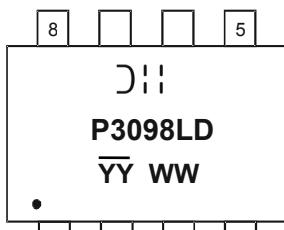
Ordering Information (Note 4)

Part Number	Case	Packaging
DMP3098LSD-13	SO-8	2,500/Tape & Reel

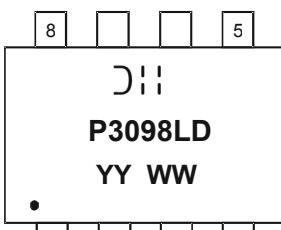
Notes:

- No purposely added lead. Fully EU Directive 2002/95/EC (RoHS) & 2011/65/EU (RoHS 2) compliant.
- See http://www.diodes.com/quality/lead_free.html for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
- Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
- For packaging details, go to our website at <http://www.diodes.com/products/packages.html>.

Marking Information



Chengdu A/T Site



Shanghai A/T Site

DII = Manufacturer's Marking
P3098LD = Product Type Marking Code

YYWW = Date Code Marking

YY or YY = Year (ex: 14 = 2014)

WW = Week (01 - 53)

YY = Date Code Marking for SAT (Shanghai Assembly/ Test site)

YY = Date Code Marking for CAT (Chengdu Assembly/ Test site)

Maximum Ratings (@ $T_A = +25^\circ\text{C}$, unless otherwise specified.)

Characteristic		Symbol	Value	Units
Drain-Source Voltage		V_{DSS}	-30	V
Gate-Source Voltage		V_{GSS}	± 20	V
Drain Current (Note 5)	Steady State	I_D	-4.4 -3.3	A
Pulsed Drain Current (Note 6)		I_{DM}	-15	A

Thermal Characteristics

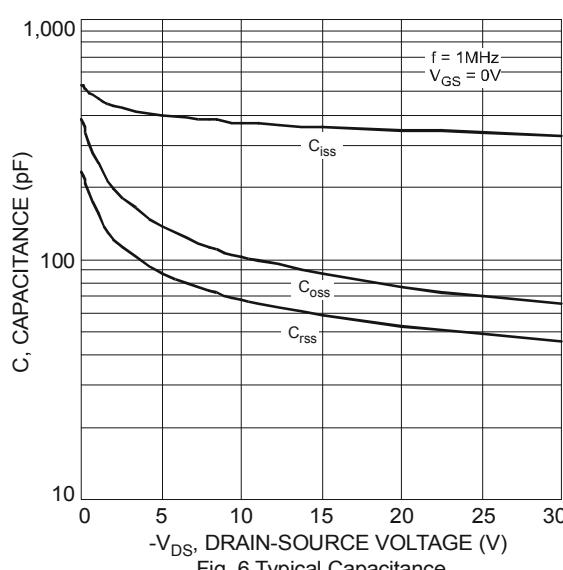
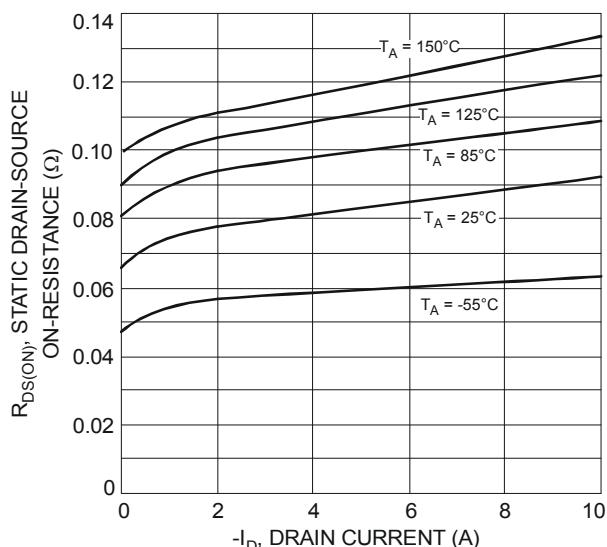
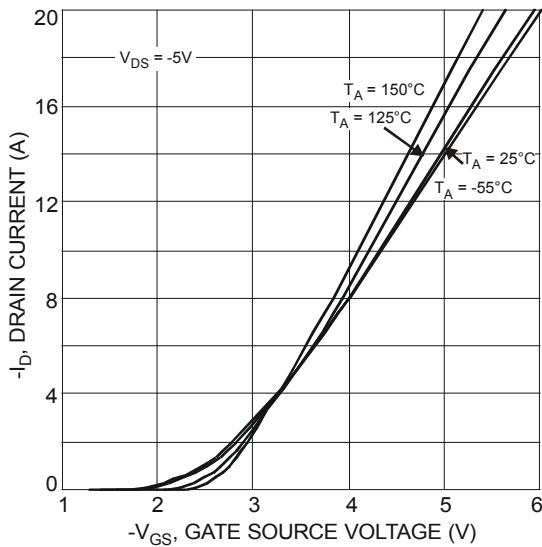
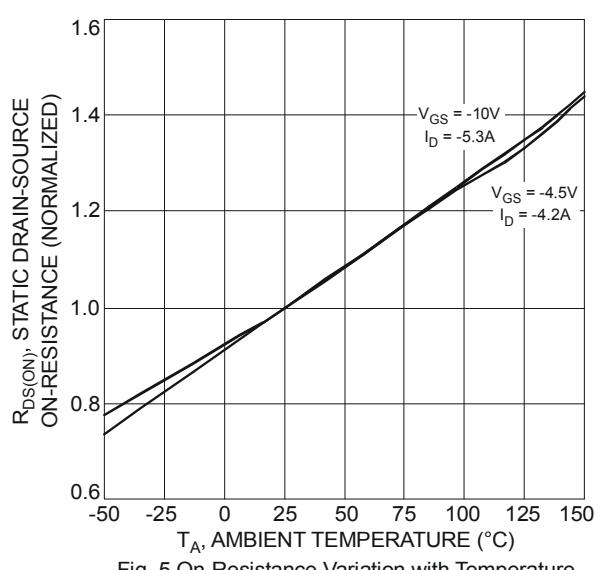
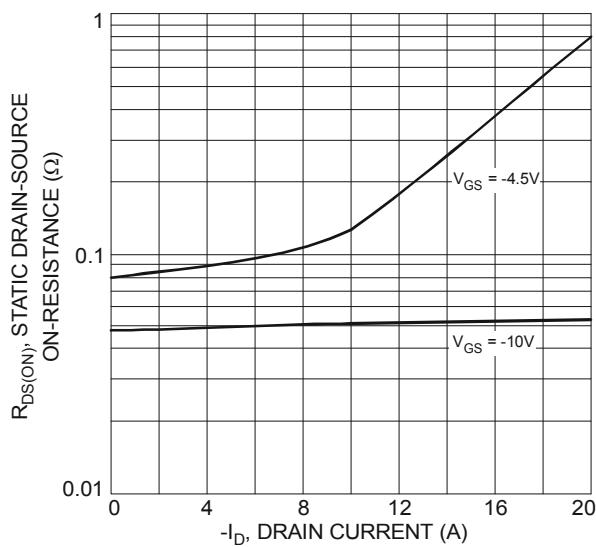
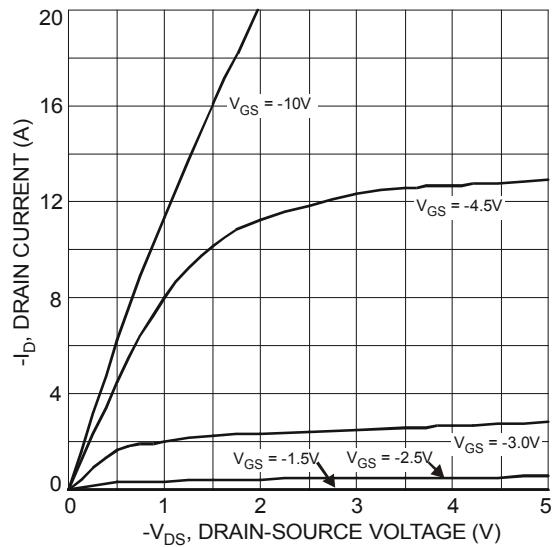
Characteristic	Symbol	Value	Unit
Total Power Dissipation (Note 5)	P_D	1.8	W
Thermal Resistance, Junction to Ambient (Note 5)	$R_{\theta JA}$	70	°C/W
Operating and Storage Temperature Range	T_J, T_{STG}	-55 to +150	°C

Electrical Characteristics (@ $T_A = +25^\circ\text{C}$, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 7)						
Drain-Source Breakdown Voltage	BV_{DSS}	-30	—	—	V	$V_{GS} = 0\text{V}, I_D = -250\mu\text{A}$
Zero Gate Voltage Drain Current	I_{DSS}	—	—	-1	μA	$V_{DS} = -30\text{V}, V_{GS} = 0\text{V}$
Gate-Source Leakage	I_{GSS}	—	—	± 100	nA	$V_{GS} = \pm 20\text{V}, V_{DS} = 0\text{V}$
ON CHARACTERISTICS (Note 7)						
Gate Threshold Voltage	$V_{GS(\text{th})}$	-1	1.7	-2.1	V	$V_{DS} = V_{GS}, I_D = -250\mu\text{A}$
Static Drain-Source On-Resistance	$R_{DS(\text{ON})}$	—	56 98	65 115	$\text{m}\Omega$	$V_{GS} = -10\text{V}, I_D = -5.0\text{A}$ $V_{GS} = -4.5\text{V}, I_D = -4.0\text{A}$
Forward Transconductance	g_{fs}	—	5.2	—	S	$V_{DS} = -10\text{V}, I_D = -5.0\text{A}$
Diode Forward Voltage (Note 7)	V_{SD}	-0.5	—	-1.2	V	$V_{GS} = 0\text{V}, I_S = -2.6\text{A}$
DYNAMIC CHARACTERISTICS						
Input Capacitance	C_{iss}	—	336	—	pF	$V_{DS} = -25\text{V}, V_{GS} = 0\text{V}$ $f = 1.0\text{MHz}$
Output Capacitance	C_{oss}	—	70	—	pF	
Reverse Transfer Capacitance	C_{rss}	—	49	—	pF	$V_{DS} = -15\text{V}, V_{GS} = 0\text{V}, f = 1.0\text{MHz}$
Gate Resistance	R_G	—	4.6	—	Ω	
SWITCHING CHARACTERISTICS						
Total Gate Charge	Q_g	—	4.0 7.8	—	nC	$V_{DS} = -15\text{V}, V_{GS} = -4.5\text{V}, I_D = -5.0\text{A}$ $V_{DS} = -15\text{V}, V_{GS} = -10\text{V}, I_D = -5.0\text{A}$
Gate-Source Charge	Q_{gs}	—	1.0	—		$V_{DS} = -15\text{V}, V_{GS} = -4.5\text{V}, I_D = -5.0\text{A}$
Gate-Drain Charge	Q_{gd}	—	2.5	—	ns	$V_{DS} = -15\text{V}, V_{GS} = -4.5\text{V}, I_D = -5.0\text{A}$
Turn-On Delay Time	$t_{d(\text{on})}$	—	6.0	—		$V_{DS} = -15\text{V}, V_{GS} = -10\text{V}, I_D = -1\text{A}, R_G = 6.0\Omega$
Rise Time	t_r	—	5.0	—		
Turn-Off Delay Time	$t_{d(\text{off})}$	—	17.6	—		
Fall Time	t_f	—	9.5	—		

Notes:

5. Device mounted on 2 oz. 1" x 1" Copper pads on 2" x 2" FR-4 PCB.
6. Pulse width $\leq 10\mu\text{s}$, Duty Cycle $\leq 1\%$.
7. Short duration pulse test used to minimize self-heating effect.



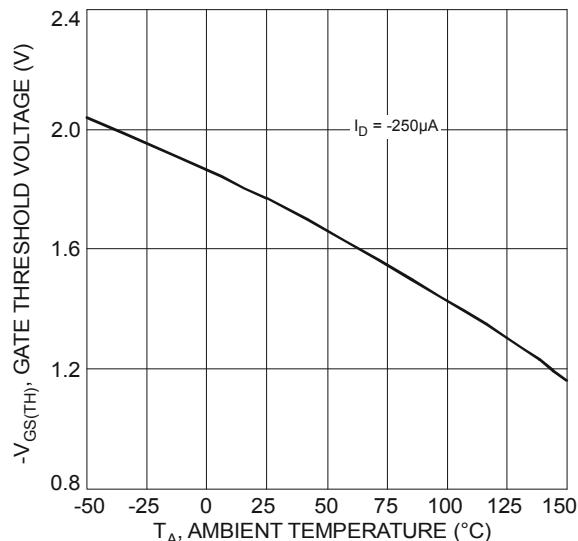


Fig. 7 Gate Threshold Variation vs. Ambient Temperature

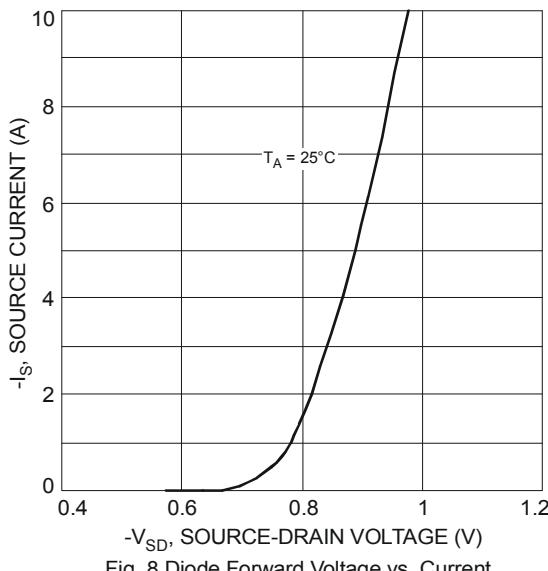
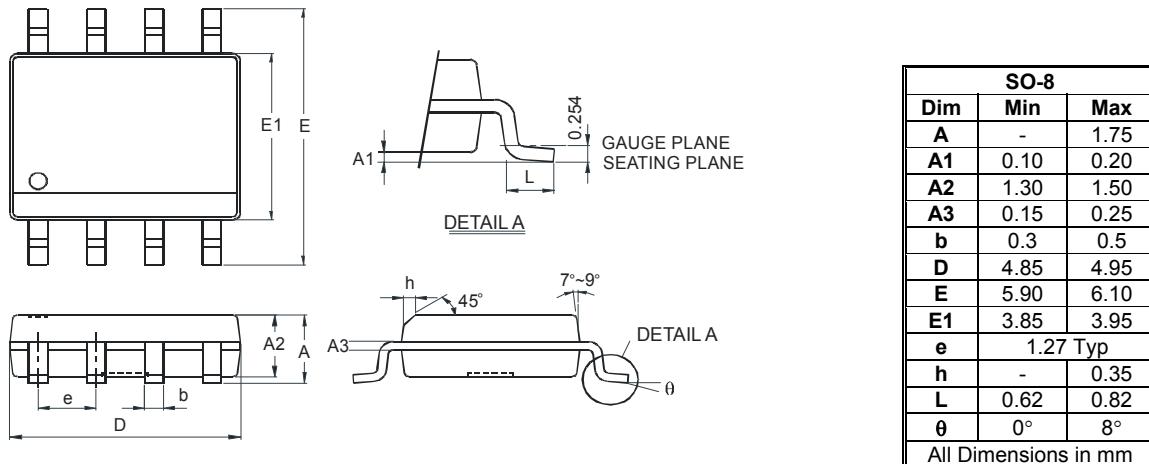


Fig. 8 Diode Forward Voltage vs. Current

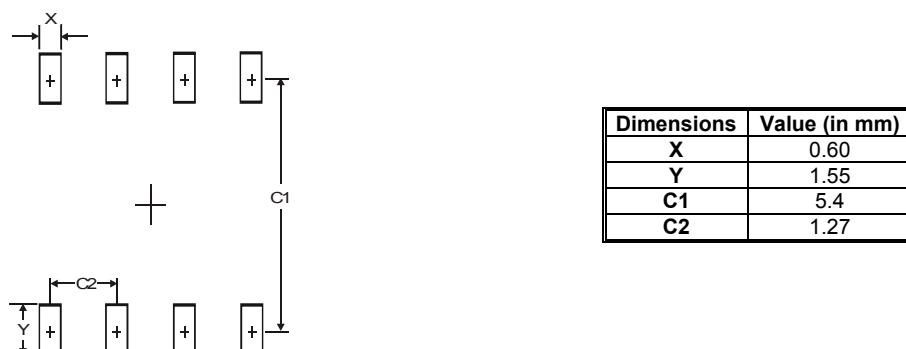
Package Outline Dimensions

Please see AP02002 at <http://www.diodes.com/datasheets/ap02002.pdf> for latest version.



Suggested Pad Layout

Please see AP02001 at <http://www.diodes.com/datasheets/ap02001.pdf> for the latest version.



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