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DP8160G

60A DC-DC Intelligent dPOL

Bel Power Solutions **DP8160G** is a second generation intelligent, fully programmable multi-phase step-down point-of-load DC-DC converter integrating digital power conversion and intelligent power management. It works with the DM7300 Series Digital Power Managers (DPM) which provides for synchronizing all system Power-On-Load regulators, for an elegant, flexible, low noise power system solution.

All key parameters, sequencing, tracking, fault protection, and compensation parameters of the DP8160G are all programmable via Bel Power Solutions I^2C based GUI. All settings can be changed by a user at any time during product development and service. Once programmed, the DPM remembers all settings and configures the DP8160G through a self-clocking single wire communication bus.

FLASH memory in the DPM allows changes to be made without the need to solder or rewire the regulator.

Key Features & Benefits

- Wide input voltage range: 8V–14V
- Programmable key features
- A voltage out range of 0.7V–2.75V at 0 to 60A.
- Efficiency greater than 92% with a built in heat sink.
- Three phase 500 kHz switching for low ripple noise.
- Flexible Fault Response features
- Multiple turn-on/off slew rates and delays
- Digital Filter Compensation
- Synchronous operation with other supplies
- Real time performance monitoring
- GUI based configuration for short development time.
- Low height of 1.1” suitable for 1U high enclosures
- Approved to the latest edition and amendment of ITE Safety standards, UL/CSA 60950-1 and IEC60950-1

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1. ORDERING INFORMATION

DP	81	60	G	-	zz
Product Family	**Series**	**Output Current**	**RoHS Compliance**	**Dash**	**Packaging Option**[1]
d-pwer®	Intelligent dPOL Converter	60 A	**G -** RoHS compliant for all six substances		**T050** - 50pc Tray **Sample** quantity orders have no suffix.

Example:
DP8160G-T050: A 50-piece tray of RoHS compliant dPOL converters. Each dPOL converter is labelled DP8160G.

Reference Documents

- DM7300 Digital Power Manager Data Sheet
- DM7300 Digital Power Manager Programming Manual
- I^2C Graphical User Interface
- DM00056-KIT USB to I^2C Adapter Kit. User Manual

2. ABSOLUTE MAXIMUM RATINGS

Stresses in excess of the absolute maximum ratings may cause performance degradation, adversely affect long-term reliability and cause permanent damage to the converter.

PARAMETER	CONDITIONS / DESCRIPTION	MIN	MAX	UNITS
Inductor Temperature	Input Voltage applied	-40	125	°C
Input Voltage	250ms Transient		15	VDC

3. ELECTRICAL SPECIFICATIONS

Specifications apply at the input voltage from 8V to 14V, output load from 0 to 60A, ambient temperature from -40°C to 85°C, and default performance parameters settings unless otherwise noted.

3.1. INPUT SPECIFICATIONS

PARAMETER	CONDITIONS / DESCRIPTION	MIN	NOM	MAX	UNITS
Input Voltage (V_{IN})		8		14	VDC
Input Current (at no load)	V_{IN} = 12 V, V_{OUT} = 2.0 V		290		mADC

[1] Packaging option is used only for ordering and not included in the part number printed on the dPOL converter label.

3.2. OUTPUT SPECIFICATIONS [2]

PARAMETER	CONDITIONS / DESCRIPTION	MIN	NOM	MAX	UNITS
Output Voltage Range (V_{OUT})	Programmable within range[3]	0.7		2.75	VDC
	Resolution				mV
Output Voltage Setpoint Resolution			2.5 mV (1LSB)		
Output Voltage Setpoint Accuracy	2ND V_O Loop Enabled		±(0.6% + 5 mV)		
Output Current (I_{OUT})	$V_{IN\ MIN}$ to $V_{IN\ MAX}$	-50		60	ADC
Line Regulation	$V_{IN\ MIN}$ to $V_{IN\ MAX}$		±0.3		$\%V_{OUT}$
Load Regulation	0 to $I_{OUT\ MAX}$		±0.3		$\%V_{OUT}$
Dynamic Regulation Peak Deviation Settling Time	50% - 75% load step, Slew rate 1A/µs F_{SW} = 0.5 MHz to 10% of peak deviation		75 35		mV µs
Output Voltage Peak-to-Peak Ripple and Noise BW=20MHz Full Load	V_{IN} = 12V, V_{OUT} = 0.75V		15		mV
	V_{IN} = 12V, V_{OUT} = 1.0V		20		mV
	V_{IN} = 12V, V_{OUT} = 1.8V		25		mV
	V_{IN} = 12V, V_{OUT} = 2.5V		30		mV
Efficiency F_{SW} = 500 kHz Full Load Room temperature	V_{IN} = 12V, V_{OUT} = 0.75V		82.3		%
	V_{IN} = 12V, V_{OUT} = 1.0V		85.5		%
	V_{IN} = 12V, V_{OUT} = 1.2V		87.4		%
	V_{IN} = 12V, V_{OUT} = 1.5V		89.3		%
	V_{IN} = 12V, V_{OUT} = 1.8V		90.6		%
	V_{IN} = 12V, V_{OUT} = 2.5V		92.5		%
Temperature Coefficient	V_{IN} = 12V, V_{OUT} = 2.5V, I_{OUT} = 0.5*$I_{OUT\ MAX}$		TBD		ppm/°C
Switching Frequency	Default		500		kH
	Programmable	500		500	kH
Duty Cycle	Default		16.7		%
	Programmable, 1.56% steps	3.125		98	%

3.3. PROTECTION SPECIFICATIONS

PARAMETER	CONDITIONS/DESCRIPTION	MIN	NOM	MAX	UNITS
OUTPUT OVERCURRENT PROTECTION					
Type	Default		Non-Latching, 130ms period		
	Programmable		Latching/Non-Latching		
Threshold	Default		132		$\%I_{OUT}$
	Programmable in 11 steps	35.2		132	$\%I_{OUT}$
Threshold Accuracy		-20		+20	$\%I_{OCP.SET}$
OUTPUT OVERVOLTAGE PROTECTION					
Type	Default		Non-Latching, 130ms period		
	Programmable		Latching/Non-Latching		
Threshold	Default		130		$\%V_{O.SET}$
	Programmable in 10% steps	110[4]		130	$\%V_{O.SET}$
Threshold Accuracy	Measured at $V_{O.SET}$ = 2.5V	-2		2	$\%V_{OVP.SET}$
Delay	From instant when threshold is exceeded until the turn-off command is generated		6		µs
Turn Off Behavior[5]	Default		Catastrophic Off		
	Programmable to		Critical Off / Catastrophic Off		

[2] Characteristics assume external output capacitance consisting of 4 x 22 µF and 1 x 47 uf ceramic XR7 and 4 x 330µF 20 mOhm solid electrolytic capacitors unless noted otherwise.
[3] DP8160G is a step-down converter, thus the output voltage is always lower than the input voltage.
[4] Minimum OVP threshold is 0.5V
[5] Sequenced Off: The turn-off follows the turn-off delay and slew-rate settings; Critical Off: At turn-off both low and high switches are immediately disabled; Catastrophic Off: At turn-off the high side switch is disabled and the low side switch is enabled.

OUTPUT UNDERVOLTAGE PROTECTION					
Type	Default Programmable		Non-Latching, 130ms period Latching/Non-Latching		
Threshold	Default		75		$\%V_{O.SET}$
	Programmable in 5% steps	75		90	$\%V_{O.SET}$
Threshold Accuracy	Measured at $V_{O.SET}$=2.5V	-2		2	$\%V_{UVP.SET}$
Delay	From instant when threshold is exceeded until the turn-off command is generated		6		µs
Turn Off Behavior[5]	Default Programmable to		Sequenced Off Sequenced / Critical Off		
OVERTEMPERATURE PROTECTION					
Type	Default Programmable		Non-Latching, 130ms period Latching/Non-Latching		
Turn Off Threshold	Temperature is increasing		130		°C
Turn On Threshold	Temperature is decreasing after the module was shut down by OTP		120		°C
Threshold Accuracy		-5		5	°C
Delay	From instant when threshold is exceeded until the turn-off command is generated		6		µs
Turn Off Behavior[5]	Default Programmable to		Sequenced Off Sequenced / Critical Off		
TRACKING PROTECTION (WHEN ENABLED)					
Type	Default Programmable		Disabled Latching/Non-Latching, 130ms		
Threshold	Enabled during output voltage ramping up			±250	mVDC
Threshold Accuracy		-50		50	mVDC
Delay	From instant when threshold is exceeded until the turn-off command is generated		6		µs
OVERTEMPERATURE WARNING					
Threshold	Always enabled, reported in Status register		120		°C
Threshold Accuracy		-5		+5	°C
Hysteresis			3		°C
Delay	From instant when threshold is exceeded until the warning signal is generated		6		µs
POWER GOOD SIGNAL (PG PIN)					
Logic	V_{OUT} is inside the PG window V_{OUT} is outside the PG window		High Low		
Lower Threshold	Default		90		$\%V_{O.SET}$
	Programmable in 5% steps	90		95	$\%V_{O.SET}$
Upper Threshold	Default		110		$\%V_{O.SET}$
	Programmable in 5% steps	105		110	$\%V_{O.SET}$
Threshold Accuracy	Measured at $V_{O.SET}$=2.5V	-2		2	$\%V_{O.SET}$
PG On Delay[6]	Default		0		ms
	Programmable to		0, 10, 50, 150		ms
PG Off Delay	Default		PG disabled when Vo reaches low threshold		
	Programmable same as PG On Delay		PG disabled at turn-off command (Reset function)		

[6] From instant when threshold is exceeded until status of PG signal changes high

3.4. FEATURE SPECIFICATIONS [7]

PARAMETER	CONDITIONS / DESCRIPTION	MIN	NOM	MAX	UNITS
CURRENT SHARE					
Type			Active, Single Line		
Maximum Number of Modules Connected in Parallel			4		
Current Share Accuracy	$I_{OUT} \geq 20\%\ I_{OUT\ NOM}$			±20	$\%I_{OUT}$
INTERLEAVE					
Interleave (Phase Shift)	Default		0		Degree
	Programmable in 22.5° steps	0		337.5	Degree
SEQUENCING					
Turn ON Delay	Default		0		ms
	Programmable in 1ms steps	0		255	ms
Turn OFF Delay	Default		0		ms
	Programmable in 1ms steps	0		63	ms
TRACKING					
Turn ON Slew Rate	Default		0.05		V/ms
	Programmable in 7 steps	0.05		5.0[8]	V/ms
Turn OFF Slew Rate	Default		-0.05		V/ms
	Programmable in 7 steps	-0.05		-5.0[8]	V/ms
OPTIMAL VOLTAGE POSITIONING					
Load Regulation	Default		0		mV/A
	Programmable in 7 steps	0		1.3	mV/A
FEEDBACK LOOP COMPENSATION					
Proportional	Programmable	0.01		2	
Integral	Programmable	1		100	µs
Differential	Programmable	1		100	µs
Differential Roll-Off	Programmable	1		100	µs
MONITORING					
Voltage Monitoring Accuracy	12 Bit Resolution over 0.5…2.75V	-0.5		0.5	%
Current Monitoring Accuracy	$20\%\ I_{OUT\ NOM} < I_{OUT} < I_{OUT\ NOM}$	-20		+20	$\%I_{OUT}$
Temperature Monitoring Accuracy	Junction temperature of dPOL controller	-5		+5	°C
REMOTE VOLTAGE SENSE (+VS AND -VS PINS)[9]					
Voltage Drop Compensation	Between +VS and VOUT			300	mV
Voltage Drop Compensation	Between -VS and PGND			100	mV

[7] Timing based functions such as Turn ON Delay are clock count based and subject to the accuracy limits of the SD signal.
[8] Achieving fast slew rates under specific line and load conditions may require feedback loop adjustment.
[9] If the voltage sense outputs are connected remotely, it is recommended to place a 0.01-0.1µF ceramic capacitor between +VS and –VS pins as close to the dPOL converter as possible. The capacitor improves noise immunity of the dPOL converter.

3.5. SIGNAL SPECIFICATIONS

PARAMETER	CONDITIONS/DESCRIPTION	MIN	NOM	MAX	UNITS
VDD	Internal supply voltage	3.15	3.3	3.45	V
Logic In Max	Pull Up Logic max safe input			VDD+.4	V
SYNC/DATA Line (SD pin)					
ViL_sd	LOW level input voltage	-0.5		0.3 x VDD	V
ViH_sd	HIGH level input voltage	0.75 x VDD		VDD + 0.5	V
Vhyst_sd	Hysteresis of input Schmitt trigger	0.25 x VDD		0.45 x VDD	V
VoL	LOW level sink current @ 0.5V	16		60	mA
Tr_sd	Maximum allowed rise time 10/90%VDD			300	ns
Cnode_sd	Added node capacitance		5	10	pF
Ipu_sd	Pull-up current source at Vsd=0V	0.25		0.75	mA
Freq_sd	SD signal lock range	475		525	kHz
Tsynq	Sync pulse duration	22		28	% of clock cycle
T0	Data=0 pulse duration	72		78	% of clock cycle
Inputs: ADDR0...ADDR4, EN, IM					
ViL_x	LOW level input voltage	-0.5		0.25	V
ViH_x	HIGH level input voltage	0.5 x VDD - 0.25		VDD+0.5	V
RdnL_ADDR	External pull down resistance ADDRX forced low	6		14	kΩ
Power Good and OK Inputs/Outputs					
Iup_PG	Pull-up current source input forced low PG	30		100	µA
Iup_OK	Pull-up current source input forced low OK	85		250	µA
ViL_x	LOW level input voltage	-0.5		0.3 x VDD	V
ViH_x	HIGH level input voltage	0.7 x VDD		VDD+0.5	V
Vhyst_x	Hysteresis of input Schmitt trigger	0.1 x VDD		0.3 x VDD	V
IoL	LOW level sink current at 0.5V	2			mA
Current Share Bus (CS pin)					
Iup_CS	Pull-up current source at VCS = 0V	0.84		2.5	mA
ViL_CS	LOW level input voltage	-0.5		0.3 x VDD	V
ViH_CS	HIGH level input voltage	0.75 x VDD		VDD+0.5	V
Vhyst_CS	Hysteresis of input Schmitt trigger	0.25 x VDD		0.45 x VDD	V
IoL	LOW level sink current at 0.5V	16			mA
Tr_CS	Maximum allowed rise time 10/90% VDD			100	ns

4. PIN ASSIGNMENTS AND DESCRIPTIONS

PIN NAME	PIN NUMBER	PIN TYPE	BUFFER TYPE	PIN DESCRIPTION	NOTES
OK	3	I/O	PU	Fault/Status Condition	Connect to OK pin of the DPM and any other dPOLs of the same group.
SD	5	I/O	PU	Sync/Data Line	Connect to SD pin of DPM
PG	4	I/O	PU	Power Good	Pin stat reflected in Status Register.
CS	6	I/O	PU	Current Share	Connect to CS pins of other dPOLs connected in parallel. Leave floating if not on shared bus.
ADDR4	16	I	PU	dPOL Address Bit 4	Tie to GND for 0 or leave floating for 1
ADDR3	15	I	PU	dPOL Address Bit 3	Tie to GND for 0 or leave floating for 1
ADDR2	14	I	PU	dPOL Address Bit 2	Tie to GND for 0 or leave floating for 1
ADDR1	9	I	PU	dPOL Address Bit 1	Tie to GND for 0 or leave floating for 1
ADDR0	1	I	PU	dPOL Address Bit 0	Tie to GND for 0 or leave floating for 1
-VS	10	I	A	Negative Voltage Sense	Connect to the negative point close to the load or PGND
+VS	11	I	A	Positive Voltage Sense	Connect to the positive point close to the load or VOUT
VOUT	18, 20, 22,24	P		Output Voltage	
PGND	7, 8, 17, 19, 21, 23	P		Power Ground	
VIN	12, 13	P		Input Voltage	

Legend: I=input, O=output, I/O=input/output, P=power, A=analog, PU=internal pull-up

5. TYPICAL PERFORMANCE CHARACTERISTICS

5.1. DISSIPATION AND EFFICIENCY CURVES

Figure 1. Efficiency at Vin = 8V

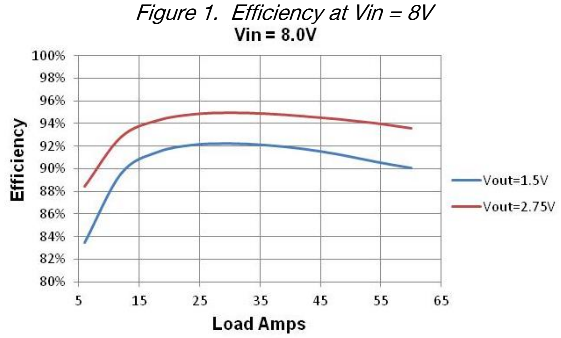


Figure 2. Power Dissipation at Vin = 8V

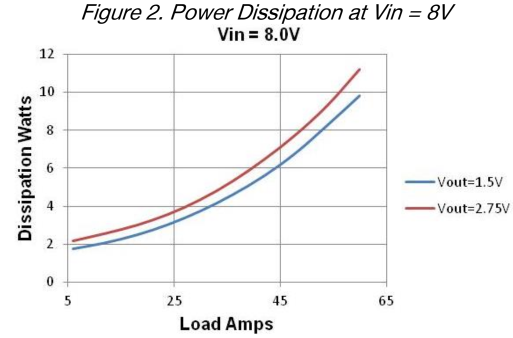


Figure 3. Efficiency vs Load at Vin = 12V

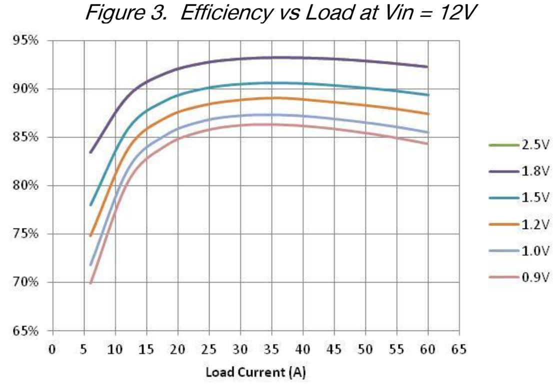
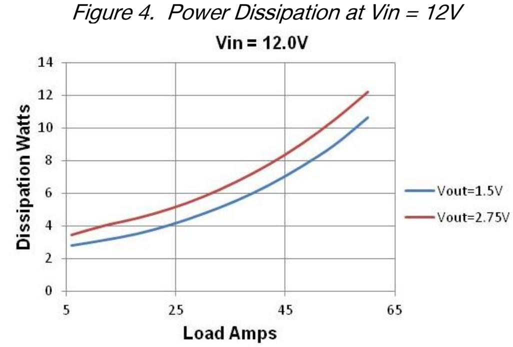
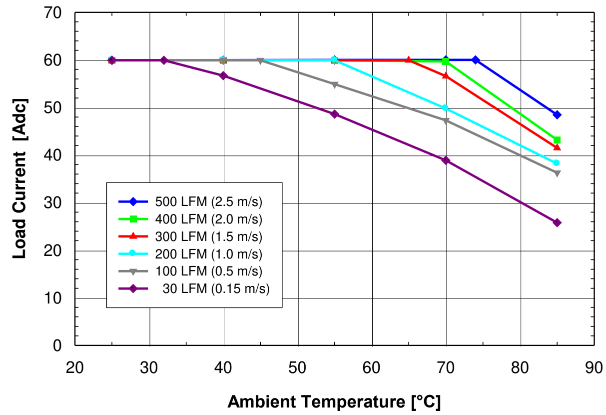


Figure 4. Power Dissipation at Vin = 12V



5.2. THERMAL DERATING

Figure 5. Thermal Derating Curves. Vin=12V, Vout=2.5V



6. PROGRAMMABLE FEATURES

Performance parameters of DP8160G dPOL converters are programmed by the system DPM over a self-clocking single wire bus as need. Each parameter is stored in FLASH memory in the DPM and loaded into volatile memory registers in the dPOL control chip detailed in Table 1. Setup registers 00h through 14h are programmed at the system power-up. When the input voltage is removed, the dPOL controller's default values are restored.

Table 1. DP8160G Memory Registers

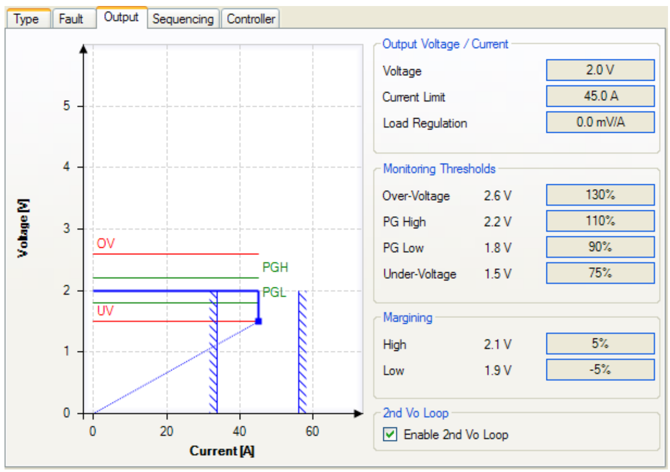
CONFIGURATION REGISTERS		
Name	**Register**	**Address**
PC1	Protection Configuration 1	0x00
PC2	Protection Configuration 2	0x01
PC3	Protection Configuration 3	0x02
TC	Tracking Configuration	0x03
INT	Interleave and Frequency Configuration	0x04
DON	Turn-On Delay	0x05
DOF	Turn-Off Delay	0x06
VLC	Voltage Loop Configuration	0x07
CLS	Current Limit Set-point	0x08
DCL	Duty Cycle Limit	0x09
PC4	Protection Configuration 4	0x0A
V1H	Output Voltage Setpoint 1 (Low Byte)	0x0B
V1L	Output Voltage Setpoint 1 (High Byte)	0x0C
V2H	Output Voltage Setpoint 2 (Low Byte)	0x0D
V2L	Output Voltage Setpoint 2 (High Byte)	0x0E
V3H	Output Voltage Setpoint 3 (Low Byte)	0x0F
V3L	Output Voltage Setpoint 3 (High Byte)	0x10
CP	Controller Proportional Coefficient	0x11
CI	Controller Integral Coefficient	0x12
CD	Controller Derivative Coefficient	0x13
B1	Controller Derivative Roll-Off Coefficient	0x14
STATUS REGISTERS		
Name	**Register**	**Address**
RUN	Run enable / status	0x15
ST	Status	0x16
MONITORING REGISTERS		
Name	**Register**	**Address**
VOH	Output Voltage High Byte (Monitoring)	0x17
VOL	Output Voltage Low Byte (Monitoring)	0x27
IO	Output Current (Monitoring)	0x18
TMP	Temperature (Monitoring)	0x19

DP8160G converters can be programmed using the Graphical User Interface or directly via the I²C bus by using high and low level commands as described in the “DPM Programming Manual”.
DP8160G parameters can be reprogrammed at any time during the system operation and service except for the digital filter coefficients, the switching frequency and the duty cycle limit, that can only be changed when the dPOL output is turned off.

6.1. OUTPUT VOLTAGE

The output voltage can be programmed in the GUI Output Configuration window shown in the Figure 6 or directly via the I²C bus by writing into the VOS register shown in Figure 7.

Figure 6. Output Configuration Window



Note that the GUI shows the effect of setting PG, OV and UV limits as both values and graphical limit bars. Vertical hashed lines are error bars for the Overcurrent (OC) limit.

6.1.1.Output Voltage Setpoint

The output voltage programming range is from 0.7 V to 2.75 V. The resolution is constant across the range and is 2.5 mV. A Total of 3 registers are provided: one should be used for the normal setpoint voltage; the other two can be used to define a low/high margining voltage setpoint. Note that each register is 16bit wide and that the high byte needs always to be written / read first. The writing of the low byte triggers the refresh of the whole 16bit register (the high byte is written to a shadow register).
Unlike other configuration registers, the dPOL controller's VOS registers are dynamic. Changes to VOS values can be made while the output is enabled over the I²C bus through register bypass commands and the dPOL will change its output immediately.

Figure 7. Output Voltage Setpoint Register VOS

VOS: Output Voltage Set-Point
Address: 0x0B … 0x10

	Coefficient	Addr	Bits	Default
V1H	First Vo Setpoint High Byte	0x0B	8	
V1L	First Vo Setpoint Low Byte	0x0C	8	
V2H	Second Vo Setpoint High Byte	0x0D	8	
V2L	Second Vo Setpoint Low Byte	0x0E	8	
V3H	Third Vo Setpoint High Byte	0x0F	8	
V3L	Third Vo Setpoint Low Byte	0x10	8	

Mapping:
- 12 bit data word, left aligned
- 1LSB = 2.5mV

Note:
- all registers are readable and writeable
- always write and read the high byte first

6.1.2.Output Voltage Margining

If the output voltage needs to be varied by a certain percentage, the margining function can be utilized. The margining can be programmed in the dPOL Configuration window or directly via the I²C bus using high level commands as described in the "DM7300 Digital Power Manager Programming Manual".
In order to properly margin dPOLs that are connected in parallel, the dPOLs must be members of one of the Parallel Buses. Refer to the GUI System Configuration Window shown in Figure 46.

6.1.3.Output Load Regulation Control

Load Regulation provides for dynamic output voltage change proportional to load current. This feature helps to improve step load response by changing the VI characteristic slope at the point of regulation. This parameter can be programmed in the GUI Output Configuration window shown in Figure 6 or directly via the I²C bus. In the DP8160G Load Regulation can be set to one of eight values: 0, 0.12, 0.24, 0.37, 0.49, 0.61, 0.73, or 0.86 mV/A.

Figure 8. Concept of Optimal Voltage Positioning

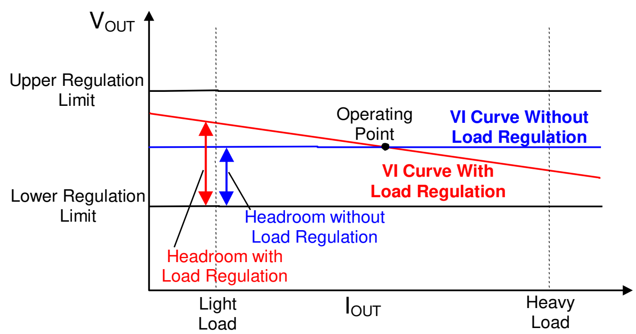


Figure 8 shows a DP8160G dPOL with 0 mv/A (load current) regulation setting. Alternating high and low output load currents causes large transients in Vout to appear with each change.

Figure 9. Transient Response without Optimal Voltage Positioning

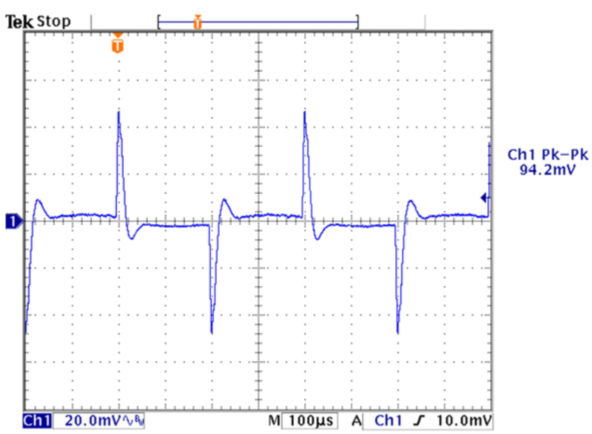
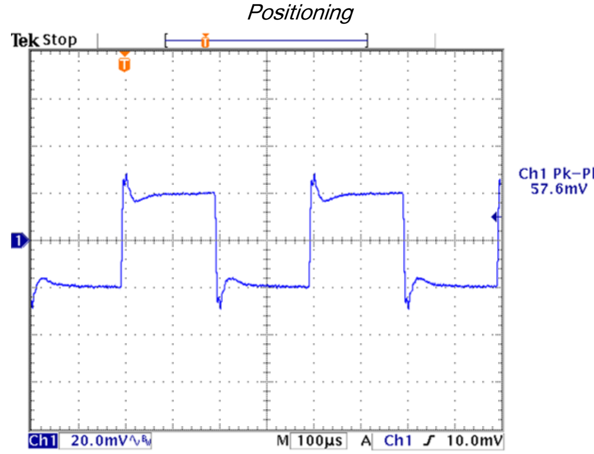


Figure 10. Transient Response with Optimal Voltage Positioning



As the Load Regulation parameter is increased, step offsets in output voltage begin to appear, as shown in Figure 9.

The Load Regulation parameter is an important part of Current Sharing. It is used to set one dPOL as a "master", by assigning a lower mV/A load regulation than all other dPOLs which share the load as "slaves". The dPOL with the lowest Regulation parameter sets the effective overall regulation. (See Current Sharing elsewhere in this document.)

6.2. SEQUENCING AND TRACKING

Turn-on delay, turn-off delay, and rising and falling output voltage slew rates can be programmed in the GUI Sequencing/Tracking window shown in Figure 11 or directly via the I²C bus by writing into the DON, DOF, and TC registers, respectively. The registers are shown in Figure 12, Figure 14, and Figure 15.

Figure 11. Sequencing/Tracking Window

6.2.1.Turn-On Delay

Turn-on delay is defined as an interval from the application of the Turn-On command until the output voltage starts ramping up.

Figure 12. Turn-On Delay Register DON

DON: Turn-On Delay Configuration
Address: 0x05

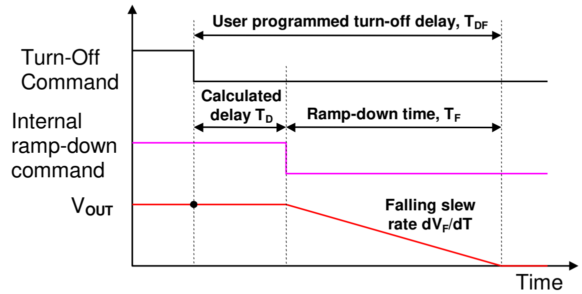
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
DON7	**DON6**	**DON5**	**DON4**	**DON3**	**DON2**	**DON1**	**DON0**
Bit 7							Bit 0

Bit 7:0	**DON[7:0]**: Turn-On delay in ms 0x00 = 0ms (default) 0x01 = 1ms … 0xFF = 255ms

6.2.2.Turn-Off Delay

Turn-off delay is defined as an interval from the application of the Turn-Off command until the output voltage reaches zero (if the falling slew rate is programmed) or until both high side and low side switches are turned off (if the slew rate is not programmed). Therefore, for the slew rate controlled turn-off the ramp-down time is included in the turn-off delay as shown in Figure 13.

Figure 13. Relationship between Turn-Off Delay and Falling Slew Rate



As it can be seen from the figure, the internally calculated delay T_D is determined by the equation below.

$$T_D = T_{DF} - \frac{V_{OUT}}{dV_F / dT}$$

For proper operation T_D shall be greater than zero. The appropriate value of the turn-off delay needs to be programmed to satisfy the condition.

If the falling slew rate control is not utilized, the turn-off delay only determines an interval from the application of the Turn-Off command until both high side and low side switches are turned off. In this case, the output voltage ramp-down process is determined by load parameters.

Figure 14. Turn-Off Delay Register DOF

DOF: Turn-Off Delay Configuration
Address: 0x06

U	U	R/W-0	R/W-0	R/W-1	R/W-0	R/W-1	R/W-1
---	---	**DOF5**	**DOF4**	**DOF3**	**DOF2**	**DOF1**	**DOF0**
Bit 7							Bit 0

Bit 7:6	**Unimplemented:** read as ‘0’
Bit 5:0	**DOF[5:0]**: Turn-Off delay in ms 0x00 = 0ms 0x01 = 1ms … 0x0B = 11ms (default) … 0x3F = 63ms

6.3. TURN-ON/OFF CONTROL

Once delays are accounted for, turn-on and turn-off characteristics are simply a function of slew rates, which are selectable.

6.3.1.Rising and Falling Slew Rates

Output voltage ramp up (and down) control is accomplished by programming the rising and falling slew rates of the output voltage, supported in the GUI as shown in Figure 11, which is implemented by the DPM through writing data to the TC register, Figure 15.

To achieve programmed slew rates, the output voltage is being changed in 10mV steps where duration of each step determines the slew rate. For example, ramping up a 1.0V output with a slew rate of 0.5V/ms will require 100 steps duration of 20µs each.

Duration of each voltage step is calculated by dividing the master clock frequency generated by the DPM. Since all dPOLs in the system are synchronized to the master clock, the matching of voltage slew rates of different outputs is very accurate as it can be seen in Figure 16 and Figure 21.

During the turn on process, a dPOL not only delivers current required by the load (I_{LOAD}), but also charges the load capacitance. The charging current can be determined from the equation:

$$I_{CHG} = C_{LOAD} \times {dV_R}/{dt}$$

Where, C_{LOAD} is load capacitance, dV_R/dt is rising voltage slew rate, and I_{CHG} is charging current.

Figure 15. Tracking Configuration Register TC

TC: Tracking Configuration
Address: 0x03

U	R/W-0	R/W-0	R/W-1	R/W-1	R/W-1	R/W-0	R/W-0
---	**R2**	**R1**	**R0**	**SC**	**F2**	**F1**	**F0**
Bit 7							Bit 0

Bit 7	**Unimplemented**: read as ‘0’
Bit 6:4	**R[2:0]**: Vo rising slew rate 0 = 0.05 V/ms (default when in bus terminator mode) 1 = 0.1 V/ms (default) 2 = 0.2 V/ms 3 = 0.25 V/ms 4 = 0.5 V/ms 5 = 1.0 V/ms 6 = 2.0 V/ms 7 = Reserved
Bit 3	**SC**: Turn-off slew rate control 0 = disabled 1 = enabled (default)
Bit 2:0	**F[2:0]**: Vo falling slew rate 0 = -0.05 V/ms 1 = -0.1 V/ms 2 = -0.2 V/ms 3 = -0.25 V/ms (default when in bus terminator mode) 4 = -0.5 V/ms (default) 5 = -1.0 V/ms 6 = -2.0 V/ms 7 = -Reserved

When selecting the rising slew rate, a user needs to ensure that

$$I_{LOAD} + I_{CHG} < I_{OCP}$$

Where I_{OCP} is the overcurrent protection threshold of the DP8160. If the condition is not met, then the overcurrent protection will be triggered during the turn-on process. To avoid this, dV_R/dt and the overcurrent protection threshold should be programmed to meet the condition above.

6.3.2. Delay and Slew Rate Combination

The effect of setting slew rates and turn on/off delays is illustrated in the following sets of figures.

Figure 16. Tracking Turn-On. Rising Slew Rate is Programmed at 0.5V/ms. Vin=12V

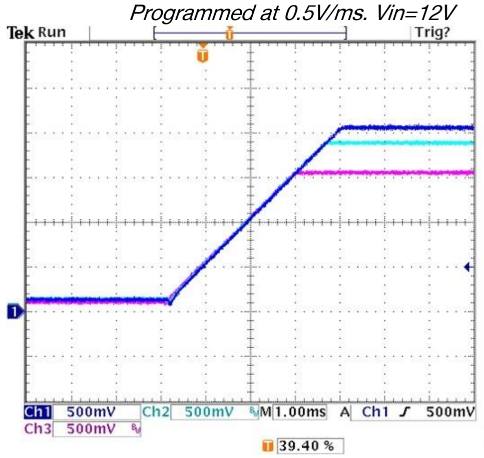


Figure 17. Turn-On with Slew Rates Programmed as follows V1 at 1.0V/ms, V2 at 0.5V/ms, V3 at0.2V/ms. Vin=12V

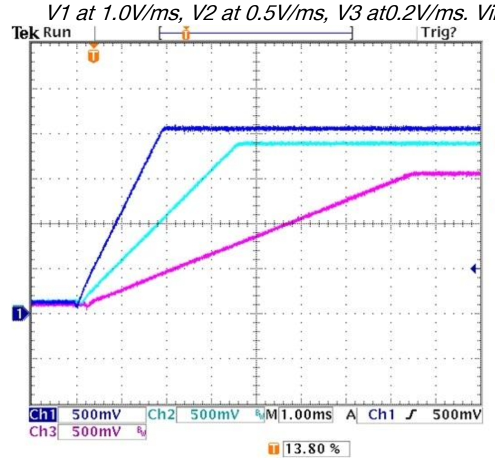


Figure 18. Turn On with Sequencing and Tracking. Rising Slew Rate Programmed at 0.5V/ms, V1 and V2 delays are programmed at 5ms. Vin=12V

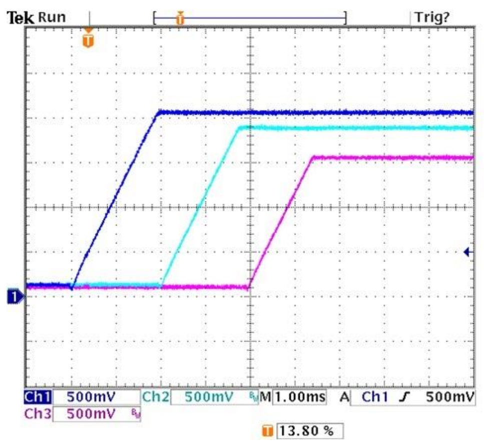
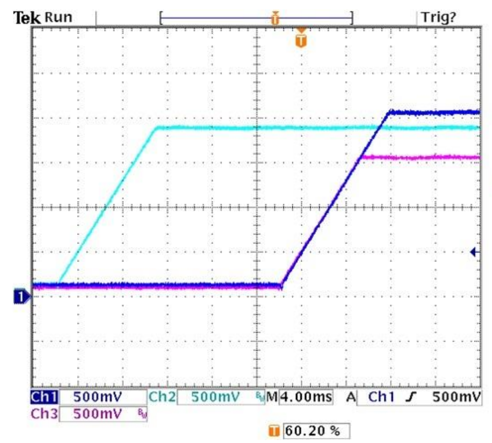


Figure 19. Two outputs delayed 5ms. All slew rates at 0.5V/ms



6.3.3.Pre-Bias

In some applications, power may "leak" from a powered circuit to an unpowered bus, typically through ESD protection diodes. The d-pwer® controller in the DP7120 holds off turn on its output until the desired ramp up point crosses the pre-bias point, as seen in Figure 20.

Figure 20. Turn On into Prebiased Load. V1 and V2 are Prebiased by V3 via a Diode. Vin=12V

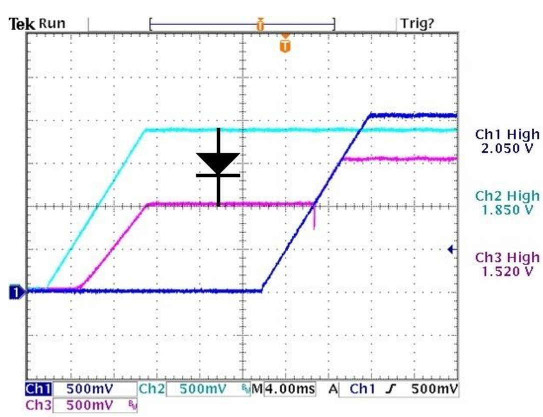


Figure 20 was captured with an actual system where a diode was added to pre-bias a 1.5V bus from a 1.85V bus in order to simulate the effect of current leakage through protection circuits of unpowered logic connected to powered logic outputs (a common source of pre-bias in power systems).

6.4. TURN-OFF CHARACTERISTICS

Turn of captures show that combining turn off delays and ramp rates. Note that while turnoff delays have a lower upper time limit as compared to turn on delays, all ramp down rates are available independently to turn on and off.

Figure 21. Tracking Turn-Off. Falling Slew Rate is Programmed at 0.5V/ms. Vin=12V

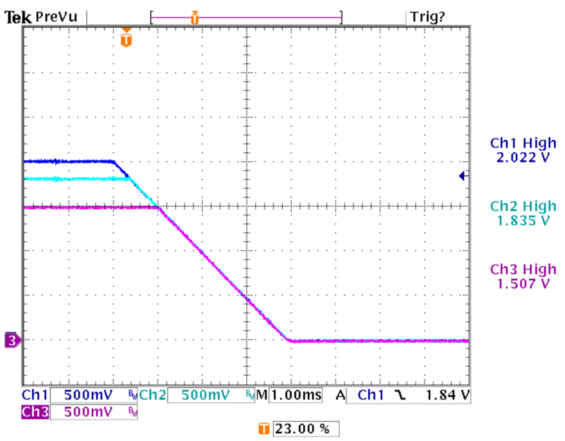
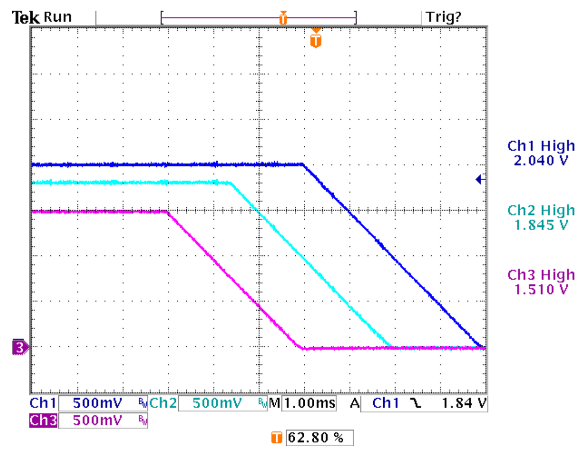


Figure 22. Turn-Off with Tracking and Sequencing. Falling Slew Rate is Programmed at 0.5V/ms. Vin=12V



6.5. FAULTS, ERRORS AND WARNINGS

All dPOL series converters have a comprehensive set of programmable fault and error protection functions that can be classified into three groups based on their effect on system operation: warnings, faults, and errors. These are *warnings*, *errors* and *faults*. Warnings include Thermal (Overtemperature limit near) and Power Good (a warning in a negative sense.)
Faults in dP series POLs include overcurrent protection, overvoltage, overtemperature and tracking failure detection. Errors include only undervoltage. Control of responses to Faults and Errors are distributed between different dPOL registers and are configurable in the GUI.
Thresholds of overcurrent, over- and undervoltage protections, and Power Good limits can be programmed in the GUI Output Configuration window or directly via the I²C bus by writing into the CLS and PC2 registers shown in Figure 24 and Figure 23.

Figure 23. Protection Configuration Register PC2

PC2: Protection Configuration Register 2 [1)]
Address: 0x01

U	U	R/W-0	R/W-0	R/W-1	R/W-0	R/W-0	R/W-0
---	**---**	**PGHL**	**PGLL**	**OVPL1**	**OVPL0**	**UVPL1**	**UVPL0**
Bit 7							Bit 0

Bit7:6	**Unimplemented**: read as ‘0’
Bit 5	**PGHL**: Power Good High Level 1 = 105% of Vo 0 = 110% of Vo (default)
Bit 4	**PGLL**: Power Good Low Level 1 = 95% of Vo 0 = 90% of Vo (default)
Bit 3:2	**OVPL**: Over Voltage Protection Level 00 = 110% of Vo 01 = 120% of Vo 10 = 130% of Vo (default) 11 = 130% of Vo
Bit 1:0	**UVPL**: Under Voltage Protection Level 00 = 75% of Vo (default) 01 = 80% of Vo 10 = 85% of Vo 11 = 90% of Vo

[1)] This register can only be written when PWM is not active (RUN[RUN] is ‘0’)

Note that the overvoltage and undervoltage protection thresholds and Power Good limits are defined as percentages of the output voltage. Therefore, the absolute levels of the thresholds change when the output voltage setpoint is changed either by output voltage adjustment or by margining.
Overcurrent limits are set either in the GUI POL Output configuration dialog or in the dPOL's CLS register as shown in Figure 24.
Note that the CLS register includes bits which control the Regulation option settings. When writing into this register be careful to not change Regulation by accident.

Figure 24. Current Limit Setpoint Register CLS

CLS: Current Limit Setting
Address: 0x08

R/W-0	R/W-0	R/W-0	R/W-1	R/W-1	R/W-0	R/W-1	R/W-1
LR2	**LR1**	**LR0**	**TCE**	**CL3**	**CL2**	**CL1**	**CL0**
Bit 7							Bit 0

Bit 7:5	**LR[2:0]**: Load Regulation setting 0 = 0 V/A/Ω (default) 1 = 0.39 V/A/Ω 2 = 0.78 V/A/Ω 3 = 1.18 V/A/Ω 4 = 1.57 V/A/Ω 5 = 1.96 V/A/Ω 6 = 2.35 V/A/Ω 7 = 2.75 V/A/Ω
Bit 4	**TCE**: Temperature Compensation for Current Limitation Enable 0 = disabled 1 = enabled (default)
Bit 3:0	**CLS[3:0]**: Current Limit set-point when Vo Stationary or Falling 0x0 = 37% 0x1 = 47% … 0xB = 140% (default) values higher than 0xB are translated to 0xB (140%)

6.5.1.Warnings

This group includes Overtemperature Warning and Power Good Signal. The warnings do not turn off dPOLs but rather generate signals that can be transmitted to a host controller via the I^2C bus.

6.5.1.1. Overtemperature Warning

The Overtemperature Warning is generated when temperature of the controller exceeds 120°C. The Overtemperature Warning changes the PT bit of the status register ST. When the temperature falls below 117°C, the PT bit is cleared and the Overtemperature Warning is removed.

6.5.1.2. Power Good

Power Good (PG) is an open collector output that is pulled low, if the output voltage is outside of the Power Good window. The window is formed by the Power Good High threshold that is programmable at 105 or 110% of the output voltage and the Power Good Low threshold that can be programmed at 90 or 95% of the output voltage.
The Power Good protection is only enabled after the output voltage reaches its steady state level. A programmable delay can be set between 0 and 150ms to delay the release of the PG pin after the voltage has reached the steady state level (see Figure 11). This allows using the PG pin to reset load circuits properly. The Power Good protection remains active during margining voltage transitions. The threshold will vary proportionally to the voltage change (see Figure 25).
The Power Good Warning pulls the PG pin low and changes the PG bit of the status register ST to 0. When the output voltage returns within the Power Good window, the PG pin is released high, the PG bit is cleared and the Power Good Warning is removed. The Power Good pin can also be pulled low by an external circuit to initiate the Power Good Warning.
At turn-off the PG pin can be programmed to either be pulled low immediately following the turn-off command, or then when the voltage actually starts to ramp down (Reset vs. Power Good functionality in Figure 11).

Note: To retrieve status information, Status Monitoring in the GUI dPOL Group Configuration Window should be enabled (refer to Digital Power Manager Data Sheet). The DPM will retrieve the status information from each dPOL on a continuous basis.

6.5.2.Faults

This group includes overcurrent, overtemperature, undervoltage, and tracking protections. Triggering any protection in this group will turn off the dPOL. For UV and OT faults the turn-off can be programmed to sequenced or critical turn-off behavior:

6.5.2.1. Overcurrent Protection

Overcurrent protection is active whenever the output voltage of the dPOL exceeds the prebias voltage (if any). When the output current reaches the OC threshold, the POL control chip asserts an OC fault. The dPOL sets the OC bit in the register ST to 0. Both high side and low side switches of the dPOL are turned off instantly (fast turn-off).
Current sensing is across the dPOLs choke. To compensate for copper winding $T_{C,}$ compensation is added to keep the OC threshold approximately constant at temperatures above room temperature. Note that the temperature compensation can be disabled in the dPOL Configure Output window or directly via the I^2C by writing into the CLS register. However, it is recommended to keep the temperature compensation enabled.

6.5.2.2. Undervoltage Protection

The undervoltage protection is only active during steady state operation of the dPOL to prevent nuisance tripping. If the output voltage decreases below the UV threshold and there is no OC fault, the UV fault signal is generated, the dPOL turns off, and the UV bit in the register ST is changed to 0. The dPOL switch-off can be programmed to follow a sequenced or critical turn-off.

6.5.2.3. Overtemperature Protection

Overtemperature protection is active whenever the dPOL is powered up. If temperature of the controller exceeds 120°C, the OT fault is generated, dPOL turns off, and the OT bit in the register ST is changed to 0. The dPOL switch-off can be programmed to follow a sequenced or critical turn-off.
If non-latching OTP is programmed, the dPOL will restart as soon as the temperature of the controller decreases below the Overtemperature Warning threshold of 110°C.

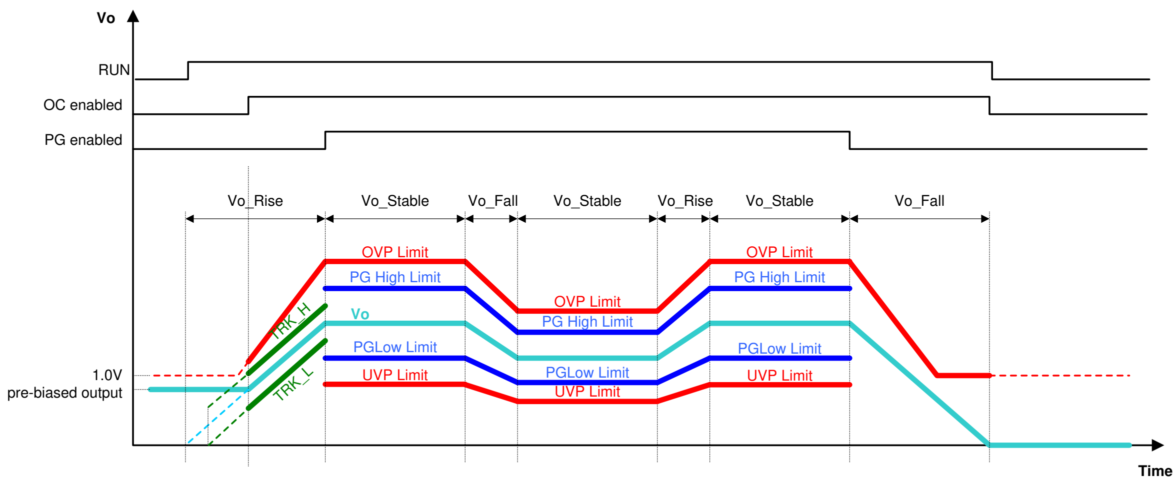
6.5.2.4. Tracking Protection

Ramp up and down operations are under control by the dPOL. Tracking protection, however, is active only when the output voltage is ramping up. The purpose of the protection is to ensure that the voltage differential between multiple rails being tracked does not exceed 250mV. This protection eliminates the need for external clamping diodes between different voltage rails which are frequently recommended by ASIC manufacturers.
When the tracking protection is enabled, the dPOL continuously compares actual value of the output voltage to its programmed value as defined by the output voltage and its rising slew rate. If absolute value of the difference exceeds 250mV, the tracking fault signal is generated, the dPOL turns off, and the TR bit in the register ST is changed to 0. Both high side and low side switches of the dPOL are turned off instantly (fast turn-off).
The tracking protection can be disabled, if it contradicts requirements of a particular system (for example turning into high capacitive load where rising slew rate is not important). It can be disabled in the dPOL Configure Fault window or directly via the I²C bus by writing into the PC1 register.

6.5.3.Faults and Margining

As noted earlier, UV and OV protection settings are a percentage of Vout. As Vout ramps between nominal, low or high margin values, UVP and OVP limits adjust accordingly. This is illustrated in Figure 25. The middle plot of Vo (Vout) level is the result of a Low Margining command. Note that Tracking is not re-enabled during changes to Vout from margining commands.

Figure 25. Protections Enable Conditions



6.5.4.Errors

This protection group includes only overvoltage protection.

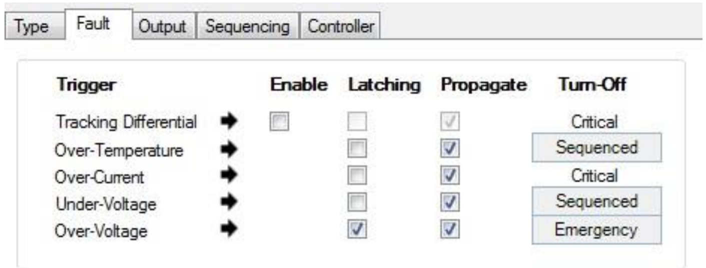
6.5.4.1. Overvoltage Protection

The overvoltage protection is set as a percentage of Vout. It is active whenever the output voltage of the dPOL exceeds the pre-bias voltage (if any). If the output voltage exceeds the overvoltage protection threshold, the overvoltage error signal is generated, the dPOL turns off, and the OV bit in the register ST is changed to 0. The high side switch is turned off instantly, and simultaneously the low side switch is turned on to ensure reliable protection of sensitive loads. The low side switch provides low impedance path to quickly dissipate energy stored in the output filter and achieve effective voltage limitation. The OV threshold can be programmed from 110% to 130% of the output voltage setpoint, but not lower than 0.5V. Also the OV threshold will always be at least 0.25V above the setpoint.

6.5.5.Fault and Error Latching

The user has the option of setting up any protection option as either latching/non-latching and propagating or non-propagating.
Propagation and Latching for each dPOL is set up in the GUI Device / Configure / Faults dialog for dPOL, as shown in Figure 26, and readable the dPOL register ST1 (Figure 27).

Figure 26. dPOL Fault Management Window



If the non-latching protection is selected, a dPOL will attempt to restart every 130ms until the condition that triggered the protection is removed. When restarting, the output voltages follow tracking and sequencing settings.
If the latching type is selected, a dPOL will turn off and stay off. The dPOL can be turned on after 130ms, if the condition that caused the fault is removed and the respective bit in the ST register was cleared, or the Turn On command was recycled, or the input voltage was recycled.

Figure 27. Protection Configuration Register PC1

PC1: Protection Configuration Register 1
Address: 0x00

R/W-0	R/W-1	R/W-0	R/W-0	R/W-0	R/W-0	R/W-1	R/W-1
TRE	**PVE**	**TRC**	**OTC**	**OCC**	**UVC**	**OVC**	**PVC**
Bit 7							Bit 0

Bit 7	TRE: Tracking fault enable 1 = enabled 0 = disabled
Bit 6	PVE: Phase voltage error enable 1 = enabled 0 = disabled
Bit 5	TRC: Tracking Fault Protection Configuration 1 = latching 0 = non-latching
Bit 4	OTC: Over Temperature Protection Configuration 1 = latching 0 = non-latching
Bit 3	OCC: Over Current Protection Configuration 1 = latching 0 = non- latching
Bit 2	UVC: Under Voltage Protection Configuration 1 = latching 0 = non- latching
Bit 1	OVC: Over Voltage Protection Configuration 1 = latching 0 = non- latching
Bit 0	PVC: Phase Voltage Protection Configuration 1 = latching 0 = non- latching

6.5.6.Fault and Error Turn Off Control

In the GUI dPOL Fault dialog is a column of spin controls which set the Turn-Off style OT, UV and OV events. The choices are defined as:
Sequenced: Outputs shut down according to ramp down rate control settings. This is the method used when a dPOL is told to do a normal, controlled shut down.

Critical: Both high side and low side switches of the dPOL are turned off instantly

Emergency: The high side switch is turned off instantly, and simultaneously the low side switch is turned on to ensure reliable protection of sensitive loads

6.5.7. Fault and Error Status

The status of each protection circuit is stored in the ST register shown in Figure 28.
When Status monitoring is enabled for a group, the DPM will read this register and make the information available for uses such as GUI Monitor display.

Figure 28. Protection Status Register ST

ST: Status register
Address: 0x16

R-1	R-0	R/W-1[1)]	R/W-1[1)]	R/W-1[1)]	R/W-1[1)]	R/W-1[1)]	R/W-1[1)]
TW	**PG**	**TR**	**OT**	**OC**	**UV**	**OV**	**PV**
Bit 7							Bit 0

Bit 7	**TW**: Temperature Warning
Bit 6	**PG**: Power Good Warning (high and low)
Bit 5	**TR**: Tracking Fault
Bit 4	**OT**: Over Temperature Fault
Bit 3	**OC**: Over Current Fault
Bit 2	**UV**: Under Voltage Fault
Bit 1	**OV**: Over Voltage Error
Bit 0	**PV**: Phase Voltage Error

Note: an activated fault is encoded as ‘0’
[1)] Writing a ‘1’ into a fault/error bit clears a latching fault/error

6.5.8. Fault and Error Propagation

The feature adds flexibility to the fault management scheme by giving users control over propagation of fault signals within and outside of the system. The propagation means that a fault in one dPOL can be programmed to turn off other dPOLs and devices in the system, even if they are not directly affected by the fault.

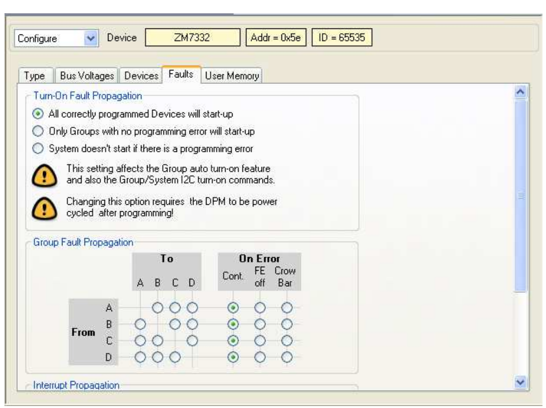
6.5.8.1. Fault Propagation

When propagation is enabled, the faulty dPOL pulls its OK pin low. This signals to the DPM and any other dPOL connected to that signal, that the dPOL has a Fault or Error condition. A low OK line initiates turn-off of other dPOLs connected to the same OK line with the same turn-off behavior as the faulty dPOL. The turn-off type is encoded into the OK line when it transitions from high to low.

6.5.9. Grouping of dPOLs

Interconnecting dPOL OK lines a dPOLs can be arranged in several groups to simplify fault management. A group of dPOLs is defined as a number of dPOLs with interconnected OK pins. A group can include from 1 to 32 dPOLs. If fault propagation within a group is desired, the propagation bit needs to be checked in the GUI Fault Management Window. The parameters can also be programmed directly via the I²C bus by writing into the PC3 register shown in Figure 30.
In order for a particular Fault or Error to propagate through the OK line to other groups, Propagation needs to be checked in the GUI dPOL **Configure / Fault** Management Window shown in Figure 29.

Figure 29. Fault and Error Propagation Window



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Note that the turn-off type of the fault as it propagates through the DPM will remain unchanged. Propagation options for dPOLs can be read or set in the dPOL PC3 register shown in Figure 30.

Figure 30. Protection Configuration Register PC3

PC3: Protection Configuration Register 3
Address: 0x02

U	U	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
---	**---**	**TRP**	**OTP**	**OCP**	**UVP**	**OVP**	**PVP**
Bit 7							Bit 0

Bit 7:6	**Unimplemented**: Read as '0'
Bit 5	**TRP**: Tracking Protection Propagation 0 = disabled 1 = enabled
Bit 4	**OTP**: Over Temperature Protection Propagation 0 = disabled 1 = enabled
Bit 3	**OCP**: Over Current Protection Propagation 0 = disabled 1 = enabled
Bit 2	**UVP**: Under Voltage Protection Propagation 0 = disabled 1 = enabled
Bit 1	**OVP**: Over Voltage Protection Propagation 0 = disabled 1 = enabled
Bit 0	**PVP**: Phase Voltage Protection Propagation 0 = disabled 1 = enabled

6.5.10. Front End and Crowbar

As shown in the propagation dialog, if an error is propagated, the DPM can be configured to generate commands to turn off a front end (a DC-DC converter generating the intermediate bus voltage) or trigger crowbar protection to accelerate removal of the IBV voltage. (The two options are independent of inter-group propagation, and may require some external hardware to interface to the IBV or crow-bar SCR device.

6.5.11. Propagation Examples

Understanding Fault and Error propagation is easier with the following examples.
The First example is of of non-propagation from a dPOL, as shown in Figure 31. An undervoltage error shuts down the Vo, but since propagation was not enabled, OK-A is not pulled down and Vo2 stays up.

Figure 31. No Group Fault Propagation

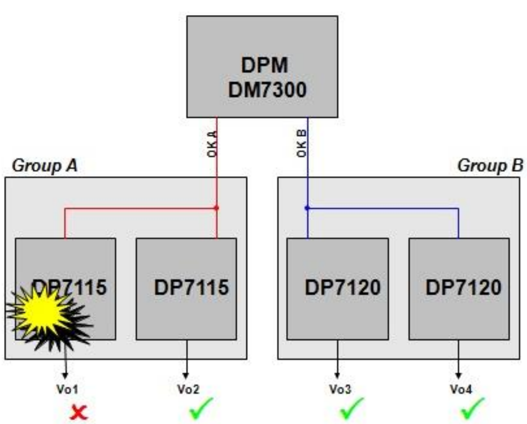

Figure 32. Turn-On into UVP on V3. The UV Fault is programmed to be Non-Latching. Ch1 - Vo1, Ch2 - Vo2 (Group A), Ch3 - Vo3 (Group B). Vo4 not shown.

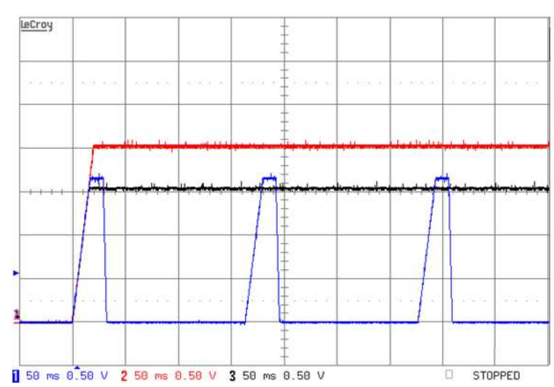

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Figure 32 shows a scope capture an actual system when undervoltage error detection is set to not propagate.
In this example, the dPOL connected to scope Ch 1 encounters the undervoltage fault after turn-on. Because fault propagation is not enabled for this POL, it alone turns off and generates the UV fault signal. Because a UV fault triggers the sequenced turn-off, the dPOL meets its turn-off delay and falling slew rate settings during the turn-off process as shown in the trace for Ch1. Since the UV fault is programmed to be non-latching, the dPOL will attempt to restart every 130 ms, repeating the process described above until the condition causing the undervoltage is removed. The 130ms hiccup interval is guaranteed regardless of the turn-off delay setting.
The next example is intra-group propagation, the dPOL propagates its fault or error events. Here fault propagation between POLs is enabled. The dPOL powering output Vo1 again encounters an undervoltage error. It pulls its OK line low. Since the dPOL powering output Vo2 (Ch3 in the picture) belongs to the same group (A in this case), pulling down OK-A tells that dPOL to execute a regular turn-off.

Figure 33. Intra Group Fault Propagation

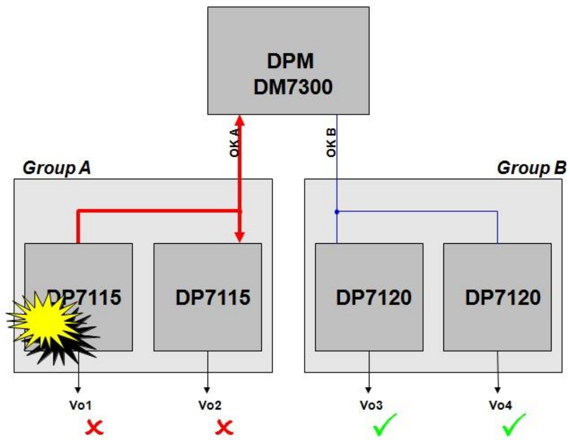
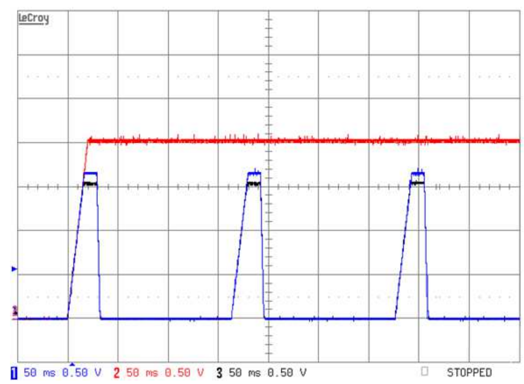


Figure 34. Turn-On into UVP on V3. The UV Fault is programmed to be Non-Latching and Propagate From Group C to Group A. Ch1 - V3(Group c), Ch2 - V2, Ch3 - V1 (Group A)



Since both Vo1 and Vo2 have the same delay and slew rate settings they will continue to turn off and on synchronously every 130ms as shown in Figure 34 until the condition causing the undervoltage is removed.
Note that the dPOL powering the output Vo2 (Ch3) actually reaches its voltage set point before the error in Vo1 is detected.
The turn-off type of a POL fault/error as propagated by the faulty dPOL via the OK line is propagated through the DPM to other dPOLs connected to other Groups (per configuration in Figure 29) through its connection to their OK line or lines.
This behavior assures that all dPOLs configured to be affected through Group linkages will switch off with the same turn-off type.

6.5.12. Protection Summary

A summary of protection support, their parameters and features are shown in Table 2.

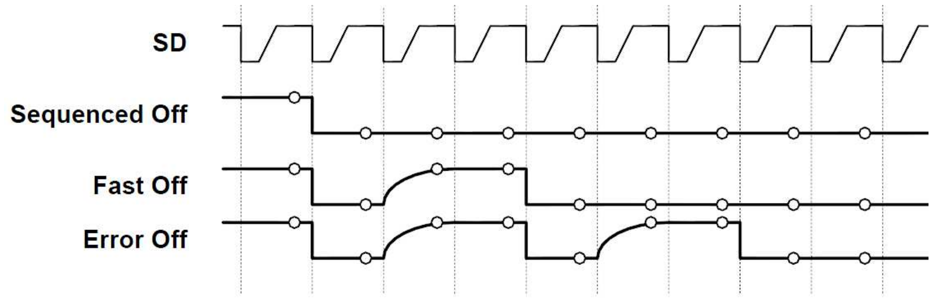
Table 2. Summary of Protection Parameters and Features

CODE	NAME	TYPE	WHEN ACTIVE	TURN OFF	LOW SIDE SWITCH	PROPAGATION	DISABLE
TW	Temperature Warning	Warning	Whenever V_{IN} is applied	No	N/A	Status Bit	No
PG	Power Good	Warning	During steady state	No	N/A	PG	No
TR	Tracking	Fault	During ramp up	Fast	Off	Critical	Yes
OT	Overtemperature	Fault	Whenever V_{IN} is applied	Regular	Off	Sequenced or Critical	No
OC	Overcurrent	Fault	When V_{OUT} exceeds prebias	Fast	Off	Critical	No
UV	Undervoltage	Fault	During steady state	Regular	Off	Sequenced or Critical	No
OV	Overvoltage	Error	When V_{OUT} exceeds prebias	Fast	On	Critical or Emergency	No

6.6. OK FAULT AND ERROR CODING

d-pwer® dPOLs have an additional functionality added to the OK line signal. The OK line is used to propagate and receive information from other devices in the power system belonging to the same group as to the kind of turn-off procedure a device has initiated because of a fault.
Figure 35 shows the three types of OK encoding. The bubbles show when the SD and OK line logic levels are sampled by dPOL and DPM logic.

Figure 35. OK Severity Encoding Waveforms



Note that the OK line state changes are always executed by dPOLs at the negative edge of the SD line.
The chart shows shut down response types as the user can select the kind of response desired for each type of Fault or Error (within the limits of choice provided for each type of Fault or Error). All dPOL devices in the same Group are expected to trigger the same turn-off procedure in order to maintain overall tracking of output voltages in the system. And when fault propagation is set to go from one group to another, the encoding is passed along un-changed.

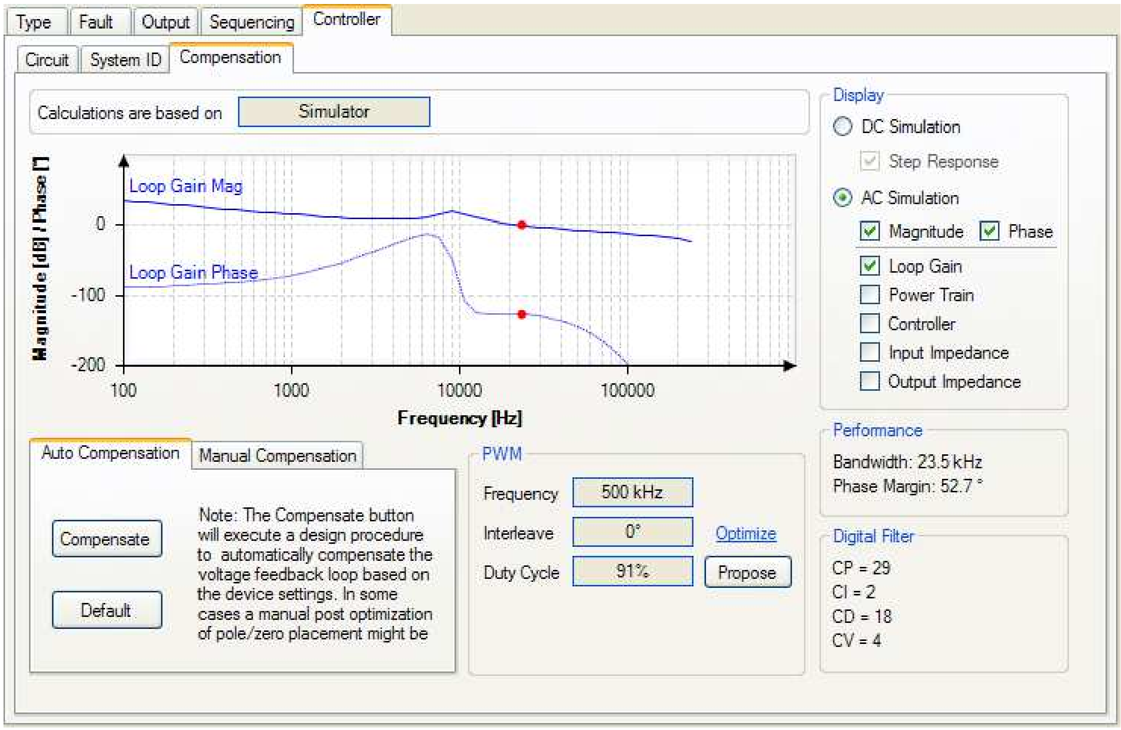
6.7. SWITCHING AND COMPENSATION

d-pwer® dPOLs utilize the digital PWM controller. The controller enables users to program most of the performance parameters, such as switching frequency, PWM duty cycle and limiting, interleave and feedback loop compensation.

6.7.1.Switching Frequency

The switching frequency for the DP8160G is fixed at 500kHz. Although the controller itself will honor selection of other frequencies through direct access via the I²C bus, *this is not recommended*. The GUI only supports the one PWM frequency.
Each dPOL is equipped with a PLL that locks to the 500 KHzSD signal which is generated by the DPM. This sets up for switching actions to be synchronous to the falling edge of SD by all dPOLs, which are thereby kept coordinated to each other.
Although synchronized to SD, switching frequency selection is independent for each dPOL, with the exception of shared load bus groups, where dPOLs attached to a shared load bus are forced to use the same frequency by the GUI.

Figure 36. PWM Controller Window



6.7.2.Interleave

Within the same PWM dialog is the switching Interleave control. Interleave is defined as a phase delay between the synchronizing slope of the master clock on the SD pin and the start of each dPOL PWM cycle. This parameter can be programmed in the dPOL Controller Configure Compensation window or directly via the I²C bus by writing into the INT register in 22.5° steps.

Figure 37. Interleave Configuration Register INT

INT: Interleave Configuration
Address: 0x04

R	R	R/W-0	U	R/W-0	R/W-0	R/W-0	R/W-0
PHS1	**PHS0**	**FRQ**	**---**	**INT3**	**INT2**	**INT1**	**INT0**
Bit 7							Bit 0

Bit 7:6	**PHS[1:0]**: Phase selection 0 = Single phase (PWM0) 1 = Dual phase (PWM0 and PWM2) 2 = Triple phase (PWM0, PWM1 and PWM2) 3 = Quad phase (PWM0, PWM1, PWM2 and PMW3)
Bit 5	**FRQ**: PWM frequency selection 0 = 500 kHz (default) 1 = 1000 kHz
Bit 4	**Unimplemented**: Read as '0'
Bit 3:0	**INT[3:0]**: PWM interleave phase with respect to SD line 0x00 = 0° phase lag 0x01 = 22.5° phase lag 0x02 = 45° phase lag … 0x1F = 337.5° phase lag

6.7.3. Interleave and Input Bus Noise

When a dPOL turns on its high side switch there is an inrush of current. If no interleave is programmed, inrush current spikes from all dPOLs in the system reflect back into the input source at the same time, adding together as shown in Figure 38.

Figure 38. Input Voltage Noise, No Interleave

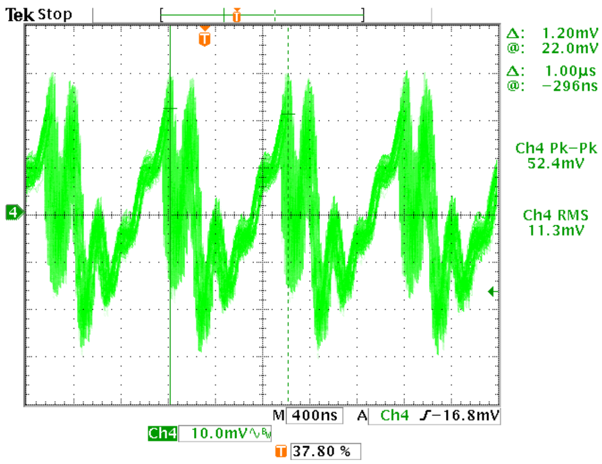


Figure 39. Input Voltage Noise with Interleave

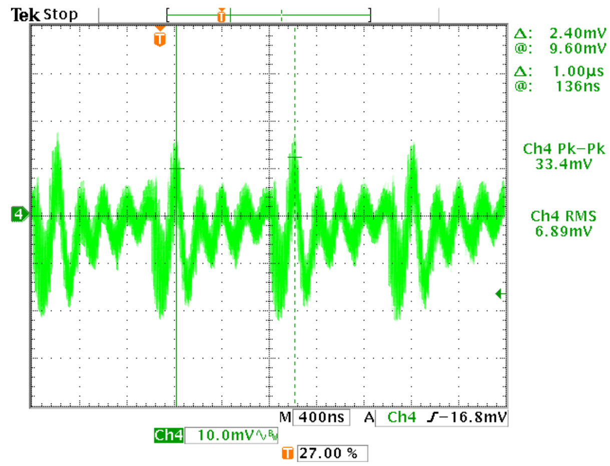


Figure 39 shows the input voltage noise of the three-output system with programmed interleave. Instead of all three dPOLs switching at the same time as in the previous example, the dPOLs V1, V2, and V3 switch at 67.5°, 180°, and 315°, respectively. Noise is spread evenly across the switching cycle resulting in more than 1.5 times reduction. To achieve similar noise reduction without the interleave will require the addition of an external LC filter.

Similar noise reduction can be achieved on the output of dPOLs connected in parallel. Figure 40 and Figure 41 show the output noise of two dPOLs connected in parallel without and with a 180° interleave, respectively. Resulting noise reduction is more than 2 times and is equivalent to doubling switching frequency or adding extra capacitance on the output of the dPOLs.

Figure 40. Output Voltage Noise, Full Load, No Interleave

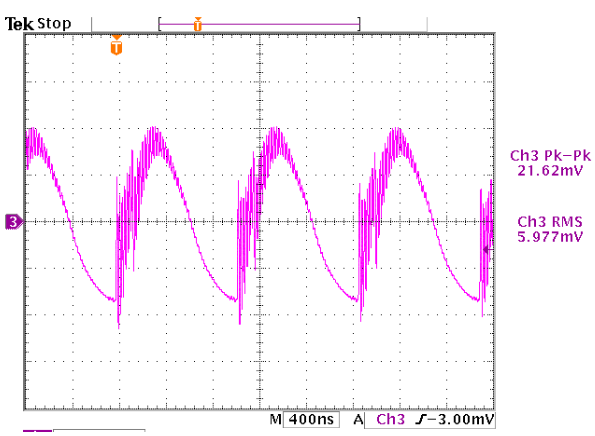
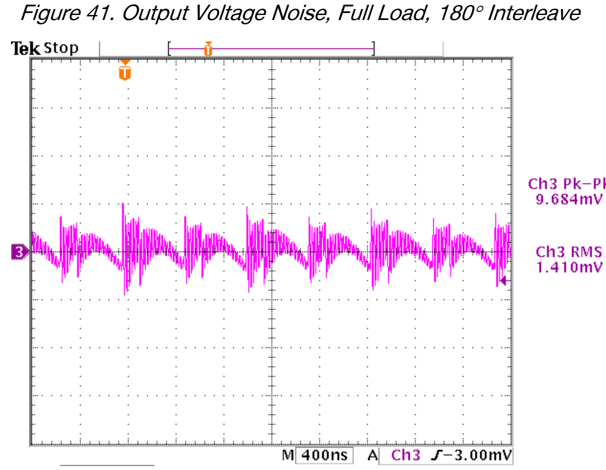


Figure 41. Output Voltage Noise, Full Load, 180° Interleave



6.7.4. Duty Cycle Limit

The DP8160G is a step-down converter therefore V_{OUT} is always less than V_{IN}. The relationship between the two parameters is characterized by the duty cycle and can be estimated from the following equation:

$$DC = \frac{V_{OUT}}{V_{IN.MIN}},$$