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19-5664; Rev 1; 12/10

DALLAS SEMICONDUCTOR MAXIM

Parallel-Interface Elapsed Time Counter

General Description

The DS1318 parallel-interface elapsed time counter (ETC) is a 44-bit counter that maintains the amount of time that the device operates from main and/or backup power or during an external event. The internal frequency of the counter clock is 4.096kHz, which provides a 244µs resolution and a maximum count of over 136 years. A built-in power-sense circuit detects power failures, automatically switches to the backup supply, and controls the timer. If an external event timer is desired, the control input EXT can control the counter operation. An open-drain output provides an interrupt, and a square-wave output provides a programmable square wave. The DS1318 is accessed through a byte-wide parallel interface, and operates over the industrial temperature range.

Applications

Power Meters

Industrial Controls

Servers

Features

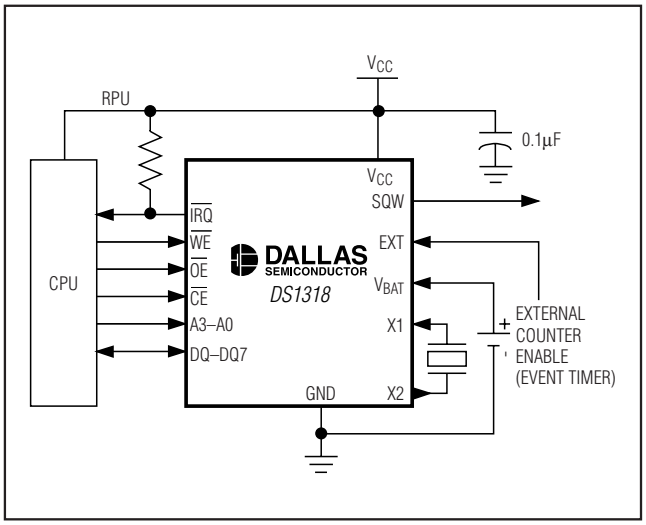
- **Byte-Wide Parallel Interface**
- **44-Bit Binary Counter Provides Timer with 244µs Resolution**
- **Automatic Power-Fail Detect and Switch Circuitry Selects Power Source from the Primary Power and the Battery, and Write Protects the Internal Registers**
- **Internal Power-Fail Circuit Allows Timer to Provide Primary or Battery Operation Times**
- **Timer can Alternately Provide an Event Timer of Either an Active-High or Active-Low Pulse**
- **Interrupt Output Generated Periodically or When the Upper 32 Bits of the Counter Match an Alarm Register**
- **Square-Wave Output with 16 Selectable Frequencies from 32.768kHz to 0.5Hz**
- **+3.3V Operation**
- **Industrial Temperature Range: -40°C to +85°C**
- **Underwriters Laboratories (UL) Recognized**

Ordering Information

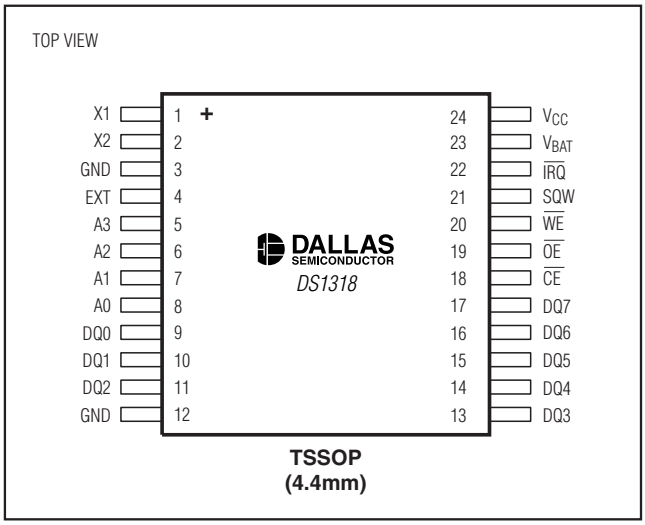
PART	TEMP RANGE	PIN-PACKAGE
DS1318E+	-40°C to +85°C	24 TSSOP
DS1318E+T&R	-40°C to +85°C	24 TSSOP

+Denotes a lead(Pb)-free/RoHS-compliant package.
T&R = Tape and reel.

Typical Operating Circuit



Pin Configuration



TSSOP
(4.4mm)

Parallel-Interface Elapsed Time Counter

ABSOLUTE MAXIMUM RATINGS

Voltage Range on any Pin Relative to Ground .....-0.3V to +6.0V
Operating Temperature Range .....-40°C to +85°C
Storage Temperature Range .....-55°C to +125°C
Lead Temperature (soldering, 10s) .....+260°C
Soldering Temperature (reflow) .....+260°C

PACKAGE THERMAL CHARACTERISTICS (Note 1)

TSSOP (multilayer board)
Junction-to-Ambient Thermal Resistance (θ_{JA}) .....72°C/W
Junction-to-Case Thermal Resistance (θ_{JC}) .....13°C/W

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maxim-ic.com/thermal-tutorial**.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS

(V_{CC} = $V_{CC(MIN)}$ to $V_{CC(MAX)}$, T_A = -40°C to +85°C, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	V_{CC}	(Note 3)	3.0	3.3	3.6	V
Battery Voltage	V_{BAT}	(Note 3)	1.6	3.3	3.7	V
Logic 1 Voltage	V_{IH}	(Note 3)	0.7 x V_{CC}		V_{CC} + 0.5	V
Logic 0 Voltage	V_{IL}	(Note 3)	-0.5		+0.3 x V_{CC}	V

DC ELECTRICAL CHARACTERISTICS

(**V_{CC} = $V_{CC(MIN)}$ to $V_{CC(MAX)}$**, T_A = -40°C to +85°C, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Logic 0 Output Current (V_{OL} = 0.15 x V_{CC})	I_{OL}		3			mA
Logic 1 Output Current (V_{OH} = 0.85 x V_{CC})	I_{OH}		1			mA
SQW, INT Logic 0 Output (V_{OL} = 0.15 x V_{CC})	I_{OLSI}		5			mA
Input Leakage	I_{LI}	(Note 4)			1	µA
I/O Leakage	I_{LO}	(Note 5)	-1		+1	µA
Active Supply Current	I_{CCA}	(Note 6)			10	mA
Standby Current	I_{CCS}	(Note 7)		100	150	µA
Battery Input-Leakage Current	I_{BATLKG}			10	100	nA
Power-Fail Voltage	V_{PF}	(Note 3)	2.70		2.97	V

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 0V, V_{BAT} = 3.7V, T_A = -40°C to +85°C, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Battery Input Current (ENOSC = 1)	I_{BAT}	(Note 8)		750	1100	nA
Battery Input Current (ENOSC = 0)	I_{BATDR}	(Note 8)			100	nA

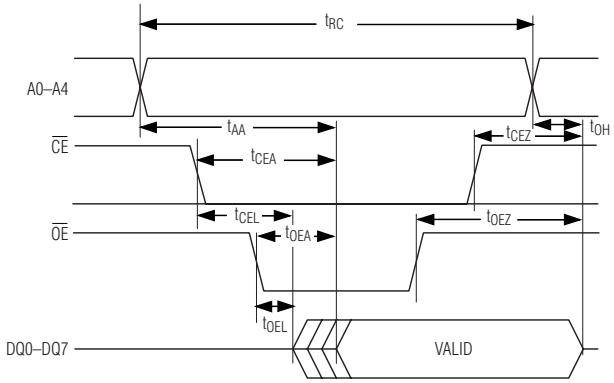
AC ELECTRICAL CHARACTERISTICS

(V_{CC} = $V_{CC(MIN)}$ to $V_{CC(MAX)}$, T_A = -40°C to +85°C, unless otherwise noted.) (Note 2)

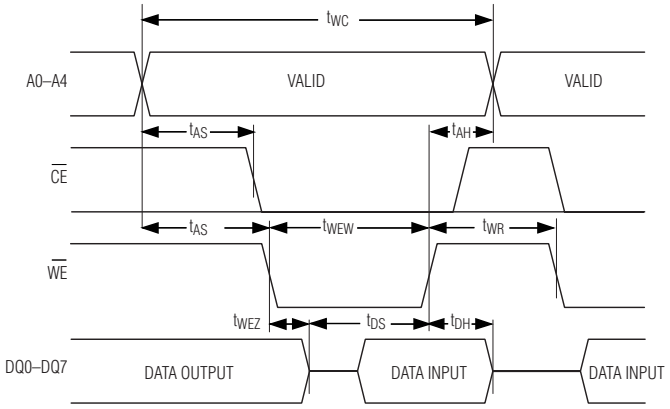
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Read Cycle Time	t_{RC}		80			ns
Address Access Time	t_{AA}				80	ns
$\overline{CE}$ to DQ Low-Z	t_{CEL}		0			ns
$\overline{CE}$ Access Time	t_{CEA}				80	ns
$\overline{CE}$ Data Off-Time	t_{CEZ}				30	ns
$\overline{OE}$ to DQ Low-Z	t_{OEL}		0			ns
$\overline{OE}$ Access Time	t_{OEA}				70	ns
$\overline{OE}$ Data Off-Time	t_{OEZ}				30	ns
Output Hold from Address	t_{OH}		5			ns
Write Cycle Time	t_{WC}		80			ns
Address Setup Time	t_{AS}		0			ns
$\overline{WE}$ Pulse Width	t_{WEW}		40			ns
$\overline{CE}$ Pulse Width	t_{CEW}		70			ns
Data Setup Time	t_{DS}		40			ns
Data Hold Time	t_{DH}		0			ns
Address Hold Time	t_{AH}		0			ns
$\overline{WE}$ Data Off-Time	t_{WEZ}				30	ns
Write Recovery Time	t_{WR}		10			ns
Oscillator Stop Flag (OSF) Delay	t_{OSF}	(Note 9)		4		ms

Parallel-Interface Elapsed Time Counter

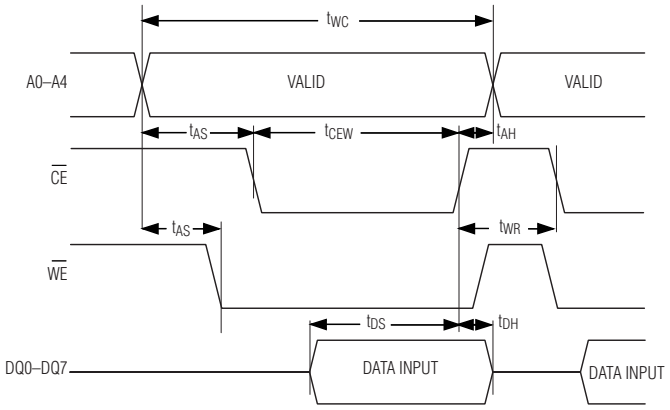
Read Cycle Timing



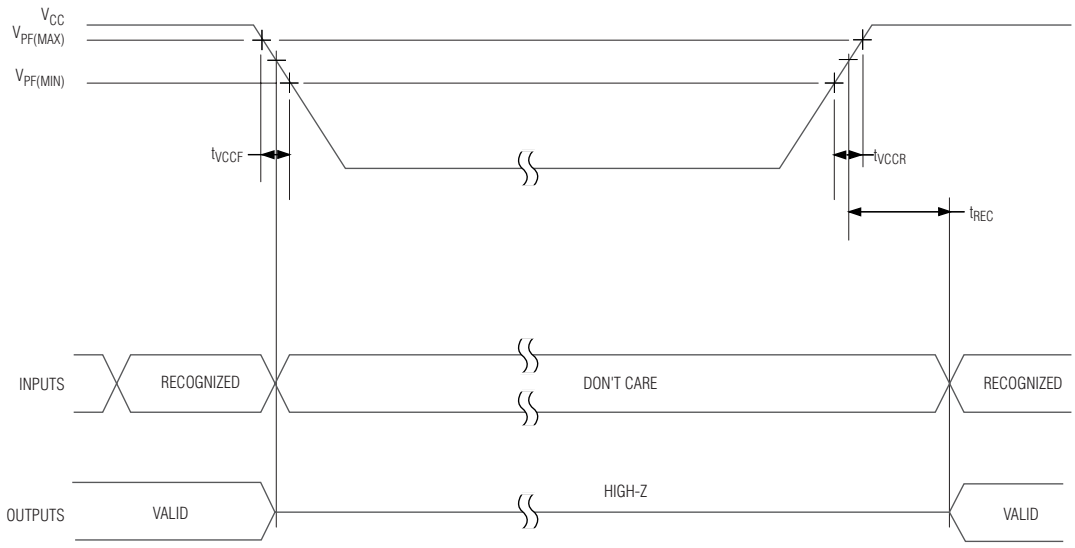
Write Cycle Timing, Write-Enable Controlled



Write Cycle Timing, Chip-Enable Controlled



Power-Up/Power-Down Timing



POWER-UP/POWER-DOWN CHARACTERISTICS

(T_A = -40°C to +85°C) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Recovery at Power-Up	t_{REC}	(Note 10)			150	ms
V_{CC} Fall Time; $V_{PF(MAX)}$ to $V_{PF(MIN)}$	t_{VCCF}		300			µs
V_{CC} Rise Time; $V_{PF(MIN)}$ to $V_{PF(MAX)}$	t_{VCCR}		0			µs

CAPACITANCE

(T_A = +25°C)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Capacitance on All Input Pins	C_{IN}				10	pF
Capacitance on $\overline{IRQ}$, SQW, and DQ Pins	C_{IO}				10	pF

Parallel-Interface Elapsed Time Counter

AC TEST CONDITIONS

PARAMETER	TEST CONDITION
Input Pulse Levels	0 to 2.7V
Output Load Including Scope and Jig	25pF + 1TTL Gate
Input and Output Timing Measurement Reference Levels	V_{CC} / 2
Input-Pulse Rise and Fall Times	4ns

WARNING:

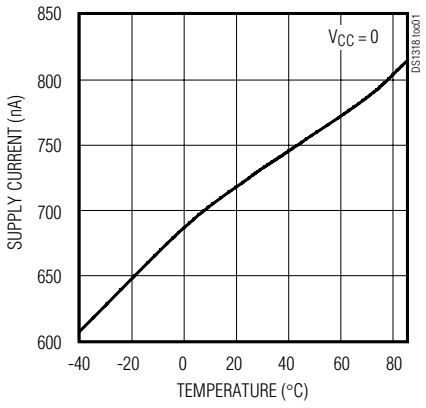
Under no circumstances are negative undershoots, of any amplitude, allowed when device is in write protection.

Note 2: Limits at -40°C are guaranteed by design and not production tested.
Note 3: All voltages are referenced to ground.
Note 4: $\overline{OE}$, $\overline{CE}$, $\overline{WE}$, EXT, and A3–A0.
Note 5: DQ7–DQ0, SQW, and $\overline{IRQ}$, when the outputs are high impedance.
Note 6: Outputs open.
Note 7: Specified with parallel bus inactive.
Note 8: Measured with a 32,768kHz crystal attached to the X1 and X2 pins.
Note 9: The parameter t_{OSF} is the period of time that the oscillator must be stopped for the OSF flag to be set over the voltage range of $0V \le V_{CC} \le V_{CC(MAX)}$ and $1.3V \le V_{BAT} \le 3.7V$.
Note 10: This delay applies only if the oscillator is enabled and running. If the ENOSC bit is 0, t_{REC} is disabled, and the device is immediately accessible. If $\overline{CE}$ and $\overline{OE}$ are low on power-up, the DQ outputs are active. Valid data out is not available until after t_{REC}.

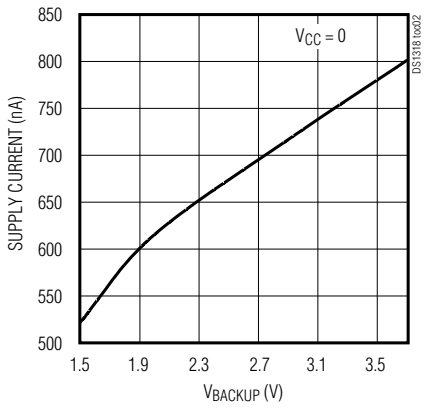
Typical Operating Characteristics

(V_{CC} = +3.3V, T_A = +25°C, unless otherwise noted.)

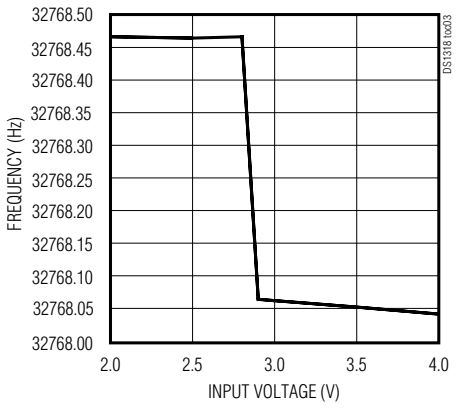
I_{BAT} vs. TEMPERATURE
V_{BAT} = 3.0V



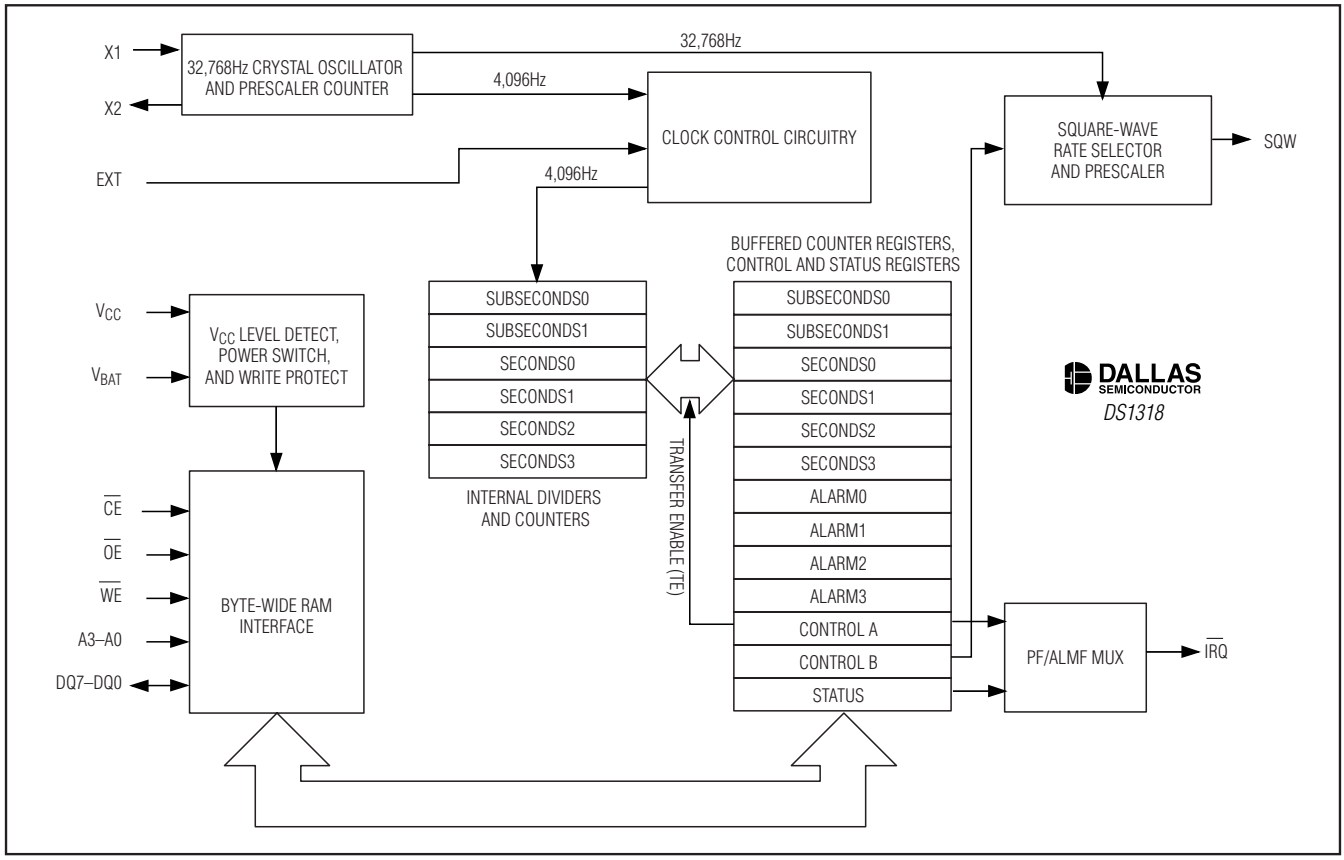
I_{BAT} vs. V_{BAT}



OSCILLATOR FREQUENCY vs. VOLTAGE



Functional Diagram



Parallel-Interface Elapsed Time Counter

Pin Description

PIN	NAME	FUNCTION
1	X1	Connections for Standard 32.768kHz Quartz Crystal. The internal oscillator circuitry is designed for operation with a crystal having a 12.5pF specified load capacitance (C_L). X1 is the input to the oscillator and can optionally be connected to an external 32.768kHz oscillator. The output of the internal oscillator, X2, is left unconnected if an external oscillator is connected to X1.
2	X2	
3, 12	GND	Ground. This pin must be connected to ground for proper operation.
4	EXT	External Counter-Enable Input
5–8	A3–A0	Address Bus Inputs
9, 10, 11, 13–17	DQ0–DQ7	Bidirectional Data Pins
18	$\overline{CE}$	Chip-Enable Input, Active Low
19	$\overline{OE}$	Output-Enable Input, Active Low
20	$\overline{WE}$	Write-Enable Input, Active Low
21	SQW	Square-Wave Output
22	$\overline{IRQ}$	Interrupt Output. This active-low open-drain pin requires a pullup resistor.
23	V_{BAT}	Battery/Backup Power-Supply Input
24	V_{CC}	DC Power for Primary Power Supply

Table 1. Operation Modes for Power-Supply Conditions

V_{CC}	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	DQ0–DQ7	A0–A4	MODE	POWER
$V_{CC} > V_{PF}$	V_{IH}	X	X	High-Z	X	Deselect	Standby
	V_{IL}	X	V_{IL}	D_{IN}	A_{IN}	Write	Active
	V_{IL}	V_{IL}	V_{IH}	D_{OUT}	A_{IN}	Read	Active
	V_{IL}	V_{IH}	V_{IH}	High-Z	A_{IN}	Read	Active
$V_{SO} < V_{CC} < V_{PF}$	X	X	X	High-Z	X	Deselect	CMOS Standby
$V_{CC} < V_{SO} < V_{PF}$	X	X	X	High-Z	X	Data	Battery Current

Detailed Description

The parallel-interface ETC contains a 44-bit up counter that maintains the amount of time the counter is enabled. The resolution of the timer is 244µs. A control register selects which events enable and disable the counter. The counter is double-buffered into two register sets, and the TE bit controls the updating of the user-readable copy.

The counter can be used to maintain the cumulative amount of time the primary power source or the battery powers the device. In this mode, the counter starts when the internal power-switching circuit enables the selected power source and stops when the circuit enables the other source.

The counter can also be used as an external event timer. In this mode, the counter starts when the signal EXT toggles to the active sate and stops when it toggles to the inactive state. The active state of the EXT signal is configurable as high or low. EXT is ignored and the counter is disabled while the device is in power fail.

The interrupt output pin provides two maskable interrupt sources. A 32-bit alarm register allows an interrupt to be generated whenever the upper 32 bits of the counter match the alarm register. A periodic interrupt can also be generated from once every 244µs to once every 1/12,097,152Hz (24.27 days). The alarm and interrupt output operate when the device is operating from either supply.

Table 1 shows the factors that control the device operation. V_{SO} is the battery switchover voltage and is the lesser of V_{BAT} and V_{PF}. While the device is operating from the battery with the oscillator running, the battery

Table 2. Crystal Specifications*

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Nominal Frequency	f_O		32.768		kHz
Series Resistance	ESR			50	kΩ
Load Capacitance	C_L		12.5		pF

**The crystal, traces, and crystal input pins should be isolated from RF generating signals. Refer to* Application Note 58: Crystal Considerations for Dallas Real-Time Clocks *for additional specifications.*

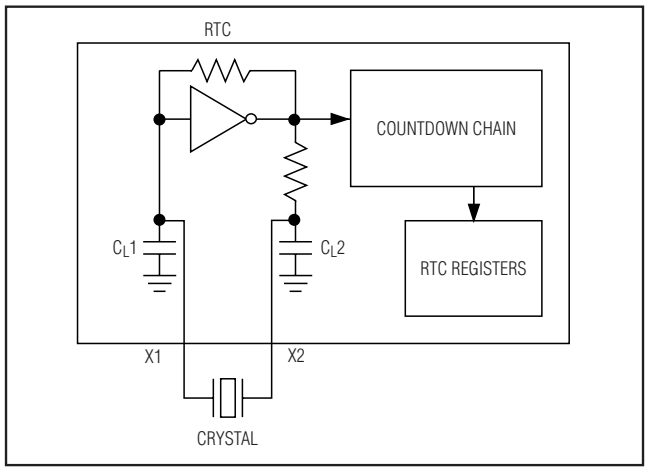


Figure 1. Oscillator Circuit Showing Internal Bias Network

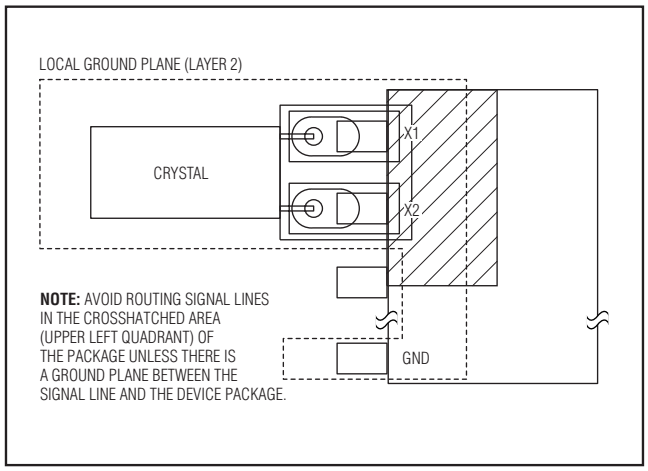


Figure 2. Layout Example

input current is I_{BAT}. The oscillator consumes most of the current. If the oscillator is disabled, the data in the registers remain static, and the battery input current is I_{BATDR}, which is primarily due to the leakage of the static memory cells.

The DS1318 uses a standard parallel byte-wide interface to access the register map. Table 1 summarizes the modes of operation at various power-supply conditions.

Oscillator Circuit

The DS1318 uses an external 32.768kHz crystal. The oscillator circuit does not require any external resistors or capacitors to operate. Table 2 specifies several crystal parameters for the external crystal, and Figure 1 shows a functional schematic of the oscillator circuit. An enable bit in the control register controls the oscillator. Oscillator startup times are highly dependent upon crystal characteristics, PC board leakage, and layout. High ESR and excessive capacitive loads are the major contributors to long startup times. A circuit using a crystal with the recommended characteristics and proper layout usually starts within one second.

An external 32.768kHz oscillator can also drive the DS1318. In this configuration, the X1 pin is connected to the external oscillator signal and the X2 pin is left unconnected.

Clock Accuracy

The accuracy of the clock is dependent upon the accuracy of the crystal and the accuracy of the match between the capacitive load of the oscillator circuit and the capacitive load for which the crystal was trimmed. Additional error is added by crystal frequency drift caused by temperature shifts. External circuit noise coupled into the oscillator circuit can result in the clock running fast. Figure 2 shows a typical PC board layout for isolation of the crystal and oscillator from noise. Refer to *Application Note 58: Crystal Considerations with Dallas Real-Time Clocks* for more detailed information.

Parallel-Interface Elapsed Time Counter

Table 3. Address Map

ADDRESS	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	FUNCTION	RANGE
00h	SS3	SS2	SS1	SS0	0	0	0	SQWS	Subseconds0	00–F0h
01h	SS11	SS10	SS9	SS8	SS7	SS6	SS5	SS4	Subseconds1	00–FFh
02h	S7	S6	S5	S4	S3	S2	S1	S0	Seconds0	00–FFh
03h	S15	S14	S13	S12	S11	S10	S9	S8	Seconds1	00–FFh
04h	S23	S22	S21	S20	S19	S18	S17	S16	Seconds2	00–FFh
05h	S31	S30	S29	S28	S27	S26	S25	S24	Seconds3	00–FFh
06h	ALM7	ALM6	ALM5	ALM4	ALM3	ALM2	ALM1	ALM0	Alarm0	00–FFh
07h	ALM15	ALM14	ALM13	ALM12	ALM11	ALM10	ALM9	ALM8	Alarm1	00–FFh
08h	ALM23	ALM22	ALM21	ALM20	ALM19	ALM18	ALM17	ALM16	Alarm2	00–FFh
09h	ALM31	ALM30	ALM29	ALM28	ALM27	ALM26	ALM25	ALM24	Alarm3	00–FFh
0Ah	TE	ENOSC	CCFG1	CCFG0	EPOL	SQWE	PIE	AIE	ControlA	00–FFh
0Bh	PRS3	PRS2	PRS1	PRS0	SRS3	SRS2	SRS1	SRS0	ControlB	00–FFh
0Ch	OSF	UIP	0	0	0	0	PF	ALMF	Status	—

Note: *Unless otherwise specified, the state of the registers is not defined when power is first applied.*

Counter Operation

The binary time information is obtained by reading the appropriate register bytes. Registers 02h through 05h contain the time in seconds from an arbitrary reference time determined by the user. Registers 00h and 01h contain the fractional seconds count. A buffered copy of the clock registers (A0–A5), updated every 244µs, allows the user to read and write the registers while the internal registers continue to increment. However, it is possible to read or write inconsistent data, or for a write to corrupt the current buffered read copy, if an update occurs during the read or write. Several methods may be used to ensure that the data is accurate.

The clock registers can be read, with the least-significant byte (LSB) being read once at the beginning and again after the other registers have been read (i.e., A2–A5, A2). If the LSB register data has changed, the registers should be re-read until the LSB register data matches. If the subseconds0 register is used, the user never has more than 244µs to read all the registers before a mismatch occurs. In addition, if the routine used to read the registers takes approximately 1.95ms to read the registers, it is possible that the subseconds0 register could roll over to the same value as previously read.

Other methods use the TE and UIP bits to synchronize accessing the clock registers to ensure that the data are valid. These methods are discussed in later sections.

Alarm

To use the alarm function, the user writes registers 06h through 09h with a time in seconds. When the current time in seconds becomes equal to the alarm value, the ALMF bit in the status register (0Ch) is set to 1. If the AIE bit in control register A is set to 1 by the user, then the $\overline{IRQ}$ pin is driven low when the ALMF bit is set to 1. The alarm and $\overline{IRQ}$ output operate when the device is running from either supply.

Periodic Flag

Writing a non-zero value into the periodic flag rate-select bits in control register B enables the periodic flag operation. The periodic flag is set to logic 1 when the internal counter reaches the selected value. Writing the PF bit to 0 resets the periodic flag. If the flag is not reset, it remains high. Once the PF bit is set, the internal counter continues counting, and attempts to set the PF bit again when the count again matches the selected rate value. Clearing the PF bit has no effect on the internal counter. If the PIE bit in control register A is set to 1, the $\overline{IRQ}$ output goes low when the PF bit is set. The periodic flag and $\overline{IRQ}$ output operates when the device is running from either supply.

Note that writing to the subseconds or seconds registers affects the setting of the PF flag and $\overline{IRQ}$ output. The square-wave output uses a separate prescaler and is not affected by changes to the subseconds or seconds bits.

Control Register A (0Ah)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
TE	ENOSC	CCFG1	CCFG0	EPOL	SQWE	PIE	AIE

Special-Purpose Registers

The DS1318 has three additional registers (control A, control B, and status) that control the clock, alarms, square wave, and interrupt output. The subseconds0 register has a square-wave synchronization (SQWS) bit in the bit 0 location. Writing the SQWS bit to 1 clears the square-wave prescaler and holds it in reset. Only the frequencies below 4096Hz are reset. Writing the bit back to 0 takes the prescaler out of reset and starts the square wave running.

Bit 7: Transfer Enable (TE). When TE is set to logic 1, the DS1318 continues to update the user copy of the time value as it receives 4,096Hz clock pulses from the oscillator. To ensure reading valid time data from the part, the user should set TE to logic 0 before reading registers 00–05h. TE must be enabled (logic 1) for at least 244µs to ensure that a transfer occurs. Note that because of the 244µs restriction, sequential values of the subseconds0 register cannot be read when TE is used.

It is possible that TE could be set to logic 0 while a transfer is taking place. In that case, the buffered data could be invalid. To prevent this, the UIP bit, described later, should be used. To write data to the clock registers, the user should set TE to logic 0, write the registers, and set TE to logic 1.

Bit 6: Enable Oscillator (ENOSC). When ENOSC is set to logic 1, the DS1318 crystal oscillator becomes enabled. Actual startup time for the oscillator depends on many external variables and is not a specified parameter.

Bits 5, 4: Clock Configuration 1, 0 (CCFG1, CCFG0). These bits determine which of the four possible modes the DS1318 uses to clock its timekeeping registers:

CCFG1	CCFG0	MODE
0	0	Always clocks the registers (normal mode)
0	1	Clocks when the EXT pin is “active” and V_{CC} is greater than V_{PF} (event-timer mode, depends on EPOL bit)
1	0	Clocks registers when part is running on V_{CC}
1	1	Clocks registers when part is running on V_{BAT}

Bit 3: External Polarity (EPOL). This bit controls the polarity on the EXT pin input when the CCFG1 and CCFG0 bits are equal to 0 and 1, respectively. When EPOL is set to logic 1, the registers count when the EXT pin is 1. When EPOL is set to logic 0, the registers count when the EXT pin is logic 0.

Bit 2: Square-Wave Enable (SQWE). When SQWE is set to logic 1, a frequency determined by the SRSx bits in control register B (0Bh) is output on the SQW pin. When SQWE is logic 0, the SQW pin is always 0. When the part is in power-fail, the SQW pin is always high-impedance. The square-wave output uses a separate prescaler from the one used by PF, $\overline{IRQ}$, UIP, and the up counter. The SQWS bit in control register A can be used to synchronize the square-wave output to within 244µs of the other events.

Bit 1: Periodic Interrupt Enable (PIE). When PIE is set to logic 1, the DS1318 sets the $\overline{IRQ}$ pin low whenever the PF flag is set to 1. When PIE is 0, the PF flag does not affect the $\overline{IRQ}$ pin.

Bit 0: Alarm Interrupt Enable (AIE). When AIE is set to logic 1, the DS1318 sets the $\overline{IRQ}$ pin low whenever the ALMF flag is set to 1. When AIE is 0, the ALMF flag does not affect the $\overline{IRQ}$ pin.

Parallel-Interface Elapsed Time Counter

Control Register B (0Bh)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
PRS3	PRS2	PRS1	PRS0	SRS3	SRS2	SRS1	SRS0

Bits 7 to 4: Periodic Rate Select (PRS3–PRS0). When the oscillator is enabled (ENOSC = 1) the PF flag is set at the rates determined by the following table:

Periodic Flag Frequency When ENOSC = 1

PRS3	PRS2	PRS1	PRS0	PERIODIC FLAG FREQUENCY
0	0	0	0	Periodic Flag Not Set
0	0	0	1	4096Hz
0	0	1	0	2048Hz
0	0	1	1	1024Hz
0	1	0	0	512Hz
0	1	0	1	256Hz
0	1	1	0	128Hz
0	1	1	1	8Hz
1	0	0	0	4Hz
1	0	0	1	2Hz
1	0	1	0	1Hz
1	0	1	1	1/64Hz (Once per 1.067 Minutes)
1	1	0	0	1/4096Hz (Once per 1.138 Hours)
1	1	0	1	1/65536Hz (Once per 1.318 Days)
1	1	1	0	1/524288Hz (Once per 0.8669 Weeks)
1	1	1	1	1/2097152Hz (Once per 24.27 Days)

Bits 3 to 0: Square-Wave Rate Select (SRS3–SRS0). When the oscillator is enabled (ENOSC = 1) and running, and the square-wave pin is enabled (SQWE = 1), the SQW pin outputs a square-wave signal determined by the SRS bits according to the following table:

Square-Wave Output Frequency When SQWE = 1, ENOSC = 1

SRS3	SRS2	SRS1	SRS0	SQUARE-WAVE OUTPUT FREQUENCY (Hz)
0	0	0	0	32,768
0	0	0	1	8192
0	0	1	0	4096
0	0	1	1	2048
0	1	0	0	1024
0	1	0	1	512
0	1	1	0	256
0	1	1	1	128
1	0	0	0	64
1	0	0	1	32
1	0	1	0	16
1	0	1	1	8
1	1	0	0	4
1	1	0	1	2
1	1	1	0	1
1	1	1	1	0.5

Status Register (0Ch)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
OSF	UIP	0	0	0	0	PF	ALMF

Bit 7: Oscillator Stop Flag (OSF). A logic 1 in this bit indicates that the oscillator either is or was stopped for some period of time and may be used to judge the validity of the timekeeping data. This bit is set to logic 1 any time the oscillator stops. The following are examples of conditions that can cause the OSF bit to be set:

1) The first time power is applied.
2) The voltage present on both V_{CC} and V_{BAT} is insufficient to support oscillation.
3) The ENOSC bit is turned off in battery-backed mode.
4) External influences on the crystal (i.e., noise, leakage, etc.)

Any write to the status register while this flag is active clears the bit to 0.

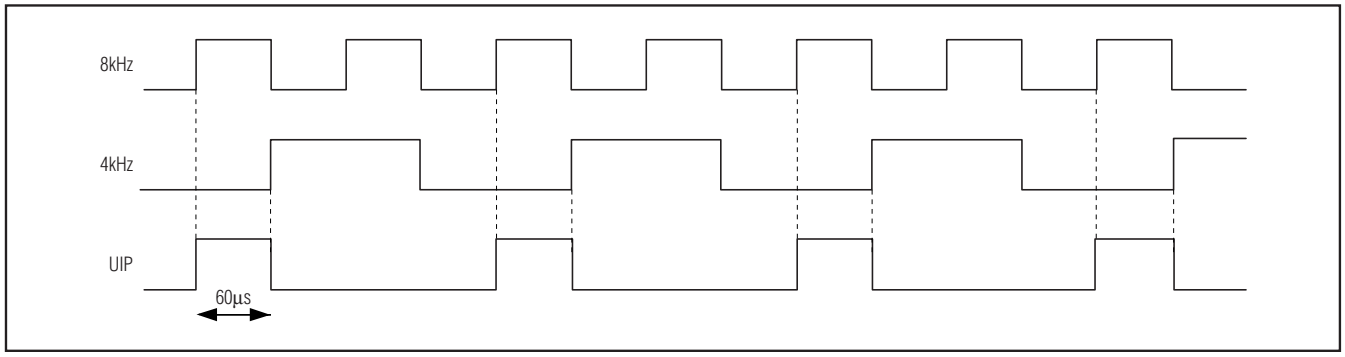
Bit 6: Update-In-Progress Flag (UIP). A logic 1 in the update-in-progress bit indicates that the internal clock registers may be in the process of updating the user registers. Writing to any seconds or subseconds registers when this bit is logic 1 may cause a collision with the internal update and corrupt one or more of the user registers until the next update occurs. If the UIP bit is read and is logic 0, the user has at least 60µs to write to the device without the possibility of causing a collision with the internal update. The internal timekeeping update is gated by the falling edge of UIP.

Reading the subseconds and or seconds registers while UIP is logic 1 may result in reading inconstant values. If the UIP bit is read and is logic 0, the user has at least 60µs to read from the device without the possibility of getting inconstant values.

Bit 1: Periodic Flag (PF). The periodic flag bit is set to 1 at the rate determined by the PRS bits in register 0Bh. If the PF bit is already 1 when the selected frequency attempts to set it to 1 again, no change occurs. The user must clear the PIF flag faster than the part attempts to set it to see the desired PF rate. If the PIE bit in register 0Ah is also set to logic 1, the $\overline{IRQ}$ pin is driven low in response to PF transitioning to 1. Any write to the status register while this flag is active clears the bit to 0.

Bit 0: Alarm Flag (ALMF). A logic 1 in the alarm flag bit indicates that the contents of the seconds registers matched the contents of the alarm registers. If the AIE bit in register 0Ah is also set to logic 1, the $\overline{IRQ}$ pin is driven low in response to ALMF transitioning to 1. Any write to the status register while this flag is active clears the bit to 0.

UIP vs. Update Timing



Parallel-Interface Elapsed Time Counter

Chip Information

PROCESS: CMOS

SUBSTRATE CONNECTED TO GROUND

Package Information

For the latest package outline information and land patterns, go to **www.maxim-ic.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
24 TSSOP	U24+2	21-0066	90-0118

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	2/04	Initial release	—
1	12/10	Added the UL recognized bullet to the *Features* section; added lead(Pb)-free parts to the *Ordering Information* table; updated the *Absolute Maximum Ratings* section to include lead temperature and soldering temperature information; added the *Package Thermal Characteristics* section; changed the battery voltage parameter symbol from V_{CC} to V_{BAT} in the *Recommended DC Operating Conditions* table; changed V_{BACKUP} to V_{BAT} in the *DC Electrical Characteristics* table globals and Note 9; added the *Package Information* table	1, 2, 3, 5, 6, 14