Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

Rev 0; 10/08

XFP Laser Control and Digital Diagnostic IC

General Description

The DS1862A is a closed-loop laser-driver control IC with built-in digital diagnostics designed for XFP MSA. The laser control function incorporates automatic power control (APC) and allows extinction ratio control though a temperature-indexed lookup table (LUT). The DS1862A monitors up to seven analog inputs, including temperature and monitor diode (MD) current, which are used to regulate the laser bias current and extinction ratio. Warning and alarm thresholds can be programmed to generate an interrupt if monitored signals exceed tolerance. Calibration is also provided internally using independent gain and offset scaling registers for each of the monitored analog signals. Settings such as programmed calibration data are stored in password-protected EEPROM memory. Programming is accomplished through an I²C-compatible interface, which can also be used to access diagnostic functionality.

Applications

Laser Control and Monitoring 10Gbps Optical Transceiver Modules (XFP)

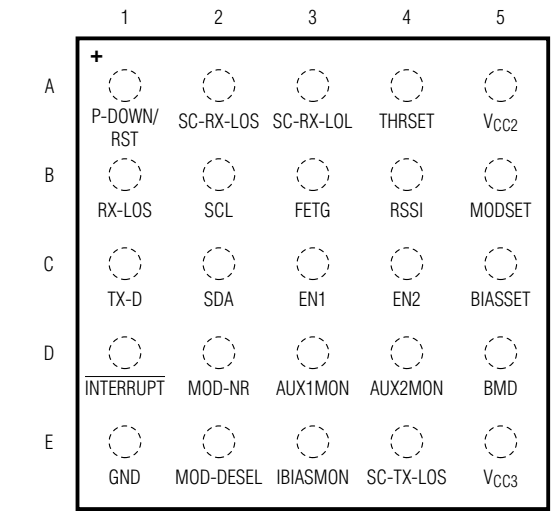
Laser Control and Monitoring

Digital Diagnostics in Optical Transmission

Features

- **Implements XFP MSA Requirements for Digital Diagnostics, Serial ID, and User Memory**
- **I²C-Compatible Serial Interface**
- **Automatic Power Control (APC)**
- **Extinction Ratio Control with Lookup Table**
- **Seven Monitored Channels for Digital Diagnostics (Five Basic Plus Two Auxiliary)**
- **Internal Calibration of Monitored Channels (Temp, $V_{CC2/3}$, Bias Current, Transmitted, and Received Power)**
- **Programmable Quick-Trip Logic for Turning Off Laser for Eye Safety**
- **Access to Monitoring and ID Information**
- **Programmable Alarm and Warning Thresholds**
- **Operates from 3.3V or 5V Supply**
- **25-Ball CSBGA, 5mm x 5mm Package**
- **Internal or External Temperature Sensor**
- **-40°C to +100°C Operating Temperature Range**
- **One 8-Bit Buffered DAC**

Pin Configuration



CSBGA (5mm x 5mm)

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
DS1862AB+	-40°C to +100°C	25 CSBGA
DS1862AB+T&R	-40°C to +100°C	25 CSBGA

+Denotes a lead-free/RoHS-compliant package.
T&R = Tape and reel.

Typical Operating Circuit appears at end of data sheet.

XFP Laser Control and Digital Diagnostic IC

ABSOLUTE MAXIMUM RATINGS

Voltage Range on Any Open-Drain Pin Relative to Ground.....-0.5V to +6.0V
Voltage Range on MOD-DESEL, SDA, SCL, FETG, THRSET, TX-D, AUX1MON, AUX2MON, IBIASMON, RSSI, BIASSET, MODSET, EN1, EN2.....-0.5V to (V_{CC3} + 0.5V)*
Voltage Range on SC-RX-LOS, SC-RX-LOL, RX-LOS, SC-TX-LOS, MOD-NR, EN1, EN2.....-0.5V to (V_{CC2} + 0.5V)*
Operating Temperature Range .....-40°C to +100°C
EEPROM Programming Temperature Range .....0°C to +70°C
Storage Temperature Range .....-55°C to +125°C
Soldering Temperature.....Refer to the IPC JEDEC J-STD-020 Specification.

**Not to exceed +6.0V.*

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

(V_{CC3} = +2.9V to +5.5V, T_A = -40°C to +100°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Main Supply Voltage	V_{CC3}	(Note 1)	+2.9		+5.5	V
Secondary Supply Voltage	V_{CC2}	V_{CC2} not to exceed V_{CC3} (Note 2)	+1.6		+3.6	V
High-Level Input Voltage (SDA, SCL)	V_{IH}	I_{IH} (max) = 10µA	0.7 x V_{CC3}		V_{CC3} + 0.5	V
Low-Level Input Voltage (SDA, SCL)	V_{IL}	I_{IL} (max) = -10µA	GND - 0.3		0.3 x V_{CC3}	V
High-Level Input Voltage (TX-D, MOD-DESEL, P-DOWN/RST) (Note 3)	V_{IH}	I_{IH} (max) = 10µA	2		V_{CC3} + 0.3	V
Low-Level Input Voltage (TX-D, MOD-DESEL, P-DOWN/RST) (Note 3)	V_{IL}	I_{IL} (max) = -10µA	-0.3		+0.8	V

DC ELECTRICAL CHARACTERISTICS

(V_{CC3} = +2.9V to +5.5V, V_{CC2} = +1.6V to +3.6V, T_A = -40°C to +100°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current	I_{CC3}	P-DOWN/RST = 1		3	5	mA
High-Level Output Voltage (FETG)	V_{OH}	I_{OH} (max) = -2mA	V_{CC3} - 0.5			V
Low-Level Output Voltage (MOD-NR, $\overline{\text{INTERRUPT}}$, SDA, FETG)	V_{OL}	I_{OL} (max) = 3mA	0		0.4	V
Resistor (Pullup)	R_{PU}		9	12	15	kΩ
I/O Capacitance	$C_{I/O}$	(Note 4)			10	pF
Leakage Current	I_L		-10		+10	µA
Leakage Current (SCL, SDA)	I_L		-10		+10	µA
Digital Power-On Reset	POD		1.0		2.2	V
Analog Power-On Reset	POA		2.0		2.6	V

DC ELECTRICAL CHARACTERISTICS—INTERFACE SIGNALS TO SIGNAL CONDITIONERS

(V_{CC2} = +1.6V to +3.6V, V_{CC3} = +2.9V to +5.5V, T_A = -40°C to +100°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
High-Level Input Voltage (SC-RX-LOS, SC-RX-LOL, SC-TX-LOS)	V_{IH}	I_{IH} (max) = 100µA	0.7 x V_{CC2}		V_{CC2} + 0.1	V
Low-Level Input Voltage (SC-RX-LOS, SC-RX-LOL, SC-TX-LOS)	V_{IL}	I_{IL} (max) = -100µA	0		0.3 x V_{CC2}	V
High-Level Output Voltage (EN1, EN2)	V_{OH}	I_{OH} (max) = -0.7mA	V_{CC2} - 0.2			V
	V_{OH2}	V_{CC2} = 2.5V to 3.6V, I_{OH} (max) = -2mA	V_{CC2} - 0.4			
	V_{OH3}	V_{CC2} = 1.6V, I_{OH} (max) = -0.7mA	V_{CC2} - 0.2			
Low-Level Output Voltage (EN1, EN2, RX-LOS)	V_{OL}	I_{OL} (max) = 0.7mA			0.20	V
	V_{OL2}	V_{CC2} = 2.5V to 3.6V, I_{OL} (max) = 2mA			0.40	
Leakage Current (SC-RX-LOS, SC-RX-LOL, SC-TX-LOS, RX-LOS)	I_L		-10		+10	µA

I²C AC ELECTRICAL CHARACTERISTICS

(V_{CC3} = +2.9V to +5.5V, T_A = -40°C to +100°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SCL Clock Frequency	f_{SCL}		0		400	kHz
Clock Pulse-Width Low	t_{LOW}		1.3			µs
Clock Pulse-Width High	t_{HIGH}		0.6			µs
Bus Free Time Between STOP and START Conditions	t_{BUF}		1.3			µs
START Hold Time	$t_{HD:SDA}$		0.6			µs
START Setup Time	$t_{SU:SDA}$		0.6			µs
Data In Hold Time	$t_{HD:DAT}$		0		0.9	µs
Data In Setup Time	$t_{SU:DAT}$		100			ns
Rise Time of Both SDA and SCL Signals	t_R	(Note 5)	$20 + 0.1C_B$		300	ns
Fall Time of Both SDA and SCL Signals	t_F	(Note 5)	$20 + 0.1C_B$		300	ns
STOP Setup Time	$t_{SU:STO}$		0.6			µs
MOD-DESEL Setup Time	$t_{HOST\_SELECT\_SETUP}$		2			ms
MOD-DESEL Hold Time	$t_{HOST\_SELECT\_HOLD}$		10			µs
Aborted Sequence Bus Release	$t_{MOD-DESEL\_ABORT}$				2	ms
Capacitive Load for Each Bus	C_B	(Note 5)			400	pF
EEPROM Write Time	t_W	≤ 4-byte write (Note 6)			16	ms

ANALOG OUTPUT CHARACTERISTICS

(V_{CC3} = +2.9V to +5.5V, V_{CC2} = +1.6V to +3.6V, T_A = -40°C to +100°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
$I_{BIASSET}$	$I_{BIASSET}$		0.01		1.50	mA
$I_{BIASSET}$ (Off-State Current)	$I_{BIASSET}$	Shutdown		±10	±100	nA
I_{MODSET}	I_{MODSET}		0.01		1.20	mA
I_{MODSET} (Off-State Current)	I_{MODSET}	Shutdown		±10	±100	nA
Voltage on $I_{BIASSET}$ and I_{MODSET}	V_{MAX}	(Note 7)	0.7		3.0	V
V_{THRSET}	V_{THRSET}	I_{MAX} = 100µA	50		1000	mV
V_{THRSET} Drift		Across temperature (Note 8)	-5		+5	%
V_{THRSET} Capacitance Load	C_{THRSET}				1	nF
APC Calibration Accuracy		+25°C			25	µA
APC Temp Drift		0.200mA to 1.5mA	-5		+5	%
		50µA to 200µA			12	µA
I_{BMD} DNL		Sink, SRC_SINK_B = 0	-0.9		+0.9	LSB
		Source, SRC_SINK_B = 1	-0.9		+0.9	
I_{BMD} INL		Sink, SRC_SINK_B = 0	-4.0		+4.0	LSB
		Source, SRC_SINK_B = 1	-4.0		+4.0	
I_{BMD} Voltage Drift					1.2	%/V
I_{BMD} FS Accuracy					1.5	%

ANALOG OUTPUT CHARACTERISTICS (continued)

(V_{CC3} = +2.9V to +5.5V, V_{CC2} = +1.6V to +3.6V, T_A = -40°C to +100°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
I_{MODSET} Accuracy		+25°C, I_{MODSET} = 0.04mA to 1.2mA	-1.5		+1.5	%
I_{MODSET} DNL		75µA range	-0.9		+0.9	LSB
		150µA range	-0.9		+0.9	
		300µA range	-0.9		+0.9	
		600µA range	-0.9		+0.9	
		1200µA range	-0.9		+0.9	
I_{MODSET} INL		75µA range	-1.5		+1.5	LSB
		150µA range	-1.5		+1.5	
		300µA range	-1.0		+1.0	
		600µA range	-1.0		+1.0	
		1200µA range	-1.0		+1.0	
I_{MODSET} Temp Drift					5	%
I_{MODSET} Voltage Drift					1.2	%/V
I_{MODSET} FS Accuracy					1.5	%
APC Bandwidth		I_{MD} / I_{APC} = 1 (Note 4)	6	10	30	kHz

AC ELECTRICAL CHARACTERISTICS—XFP CONTROLLER

(V_{CC3} = +2.9V to +5.5V, V_{CC2} = +1.6V to +3.6V, T_A = -40°C to +100°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Time to Initialize	t_{INIT}	V_{CC3} within ±5% of nominal	30		200	ms
TX-D Assert Time	t_{OFF}	I_{BIAS} and I_{MOD} below 10% of nominal			5	µs
TX-D Deassert Time	t_{ON}	I_{BIAS} and I_{MOD} above 90% of nominal			1	ms
P-DOWN/RST Assert Time	t_{PDR-ON}	I_{BIAS} and I_{MOD} below 10% of nominal			100	µs
P-DOWN/RST Deassert Time	$t_{PDR-OFF}$	I_{BIAS} and I_{MOD} above 90% of nominal			200	ms
MOD-DESEL Deassert Time	$t_{MOD-DESEL}$	Time until proper response to I^2C communication			2	ms
$\overline{\text{INTERRUPT}}$ Assert Delay	t_{INIT_ON}	Time from fault to interrupt assertion			100	ms
$\overline{\text{INTERRUPT}}$ Deassert Delay	t_{INIT_OFF}	Time from read (clear flags) to interrupt deassertion			500	µs
MOD-NR Assert Delay	$t_{MOD-NR-ON}$	Time from fault to MOD-NR assertion			0.5	ms
MOD-NR Deassert Delay	$t_{MOD-NR-OFF}$	Time from read (clear flags) to MOD-NR deassertion			0.5	ms
RX-LOS Assert Time	t_{LOS-ON}	Time from SC-RX-LOS assertion to RX-LOS assertion			100	ns
RX-LOS Deassert Time	$t_{LOS-OFF}$	Time from SC-RX-LOS deassertion to RX-LOS deassertion			100	ns
P-DOWN/RST Reset Time	t_{RESET}	Time from P-DOWN/RST assertion to initial reset	10			µs
Shutdown Time	t_{FAULT}	Time from fault to $I_{BIASSET}$, I_{MODSET}, and I_{BMD} below 10%			30	µs

AC ELECTRICAL CHARACTERISTICS—SOFT* CONTROL AND STATUS

(V_{CC3} = +2.9V to +5.5V, V_{CC2} = +1.6V to +3.6V, T_A = -40°C to +100°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SOFT TX-D Assert Time	t_{OFF_SOFT}	I_{BIAS} and I_{MOD} below 10% of nominal			50	ms
SOFT TX-D Deassert Time	t_{ON_SOFT}	I_{BIAS} and I_{MOD} above 90% of nominal			50	ms
SOFT P-DOWN/RST Assert Time	t_{PDR-ON_SOFT}	I_{BIAS} and I_{MOD} below 10% of nominal			50	ms
SOFT P-DOWN/RST Deassert Time	$t_{PDR-OFF\_SOFT}$	I_{BIAS} and I_{MOD} above 90% of nominal			200	ms
Soft MOD-NR Assert Delay	$t_{MOD-NR-ON\_SOFT}$	Time from fault to MOD-NR assertion			50	ms
Soft MOD-NR Deassert Delay	$t_{MOD-NR-OFF\_SOFT}$	Time from read (clear flags) to MOD-NR deassertion			50	ms
Soft RX_LOS Assert Time	t_{LOS-ON_SOFT}	Time from SC-RX-LOS assertion to RX-LOS assertion			50	ms
Soft RX_LOS Deassert Time	$t_{LOS-OFF\_SOFT}$	Time from SC-RX-LOS deassertion to RX-LOS deassertion			50	ms
Analog Parameter Data Ready (DATA-NR)					500	ms

**All SOFT timing specifications are measured from the falling edge of STOP signal during I^2C communication.*

ANALOG INPUT CHARACTERISTICS

(V_{CC3} = +2.9V to +5.5V, T_A = -40°C to +100°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
I_{BMD} Configurable Source or Sink (+/-)				0.05		1.50	mA
I_{BMD} Voltage (I_{BMD} - 0µA)	V_{BMD}	Source mode	I_{BMD} range 0 to 1.5mA		2.0		V
		Sink mode			1.2		
I_{BMD} Input Resistance	R_{BMD}			400	550	700	Ω

A/D INPUT VOLTAGE MONITORING (IBIASMON, AUX2MON, AUX1MON, RSSI, BMD)

(V_{CC3} = +2.9V to +5.5V, T_A = -40°C to +100°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Resolution	ΔV_{MON}			610		µV
Supply Resolution	$\Delta V_{CC2/3}$			1.6		mV
Input/Supply Accuracy	A_{CC}	At factory setting		0.25	0.5	%FS
Update Rate	t_{FRAME1}	AUX1MON and AUX2MON disabled		48	52	ms
	t_{FRAME2}	All channels enabled		64	75	
Input/Supply Offset	V_{OS}	(Note 4)		0	5	LSB
Full-Scale Input (IBIASMON and RSSI)		At factory setting	2.4875	2.5	2.5125	V
Full-Scale Input (AUX1MON, AUX2MON, V_{CC2}, V_{CC3})		At factory setting (Note 9)	6.5208	6.5536	6.5864	V
BMD (Monitor) (TX-P)		FS setting		1.5		mA

FAST ALARMS AND V_{CC} FAULT CHARACTERISTICS

(V_{CC3} = +2.9V to +5.5V, V_{CC2} = +1.6V to +3.6V, T_A = -40°C to +100°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
HIGH BIAS and TX-P Threshold FS		(Note 10)	2.48	2.5	2.52	mA
$V_{CC2/3}$ Fault Asserted Falling Edge Delay		↓ $V_{CC2/3}$ (Note 11)			75	ms
QT Temperature Coefficient			-3		+3	%
QT Voltage Coefficient					0.5	%/V
QT FS Trim Accuracy (4.2V, +25°C)			2.480	2.500	2.520	mA
QT Accuracy (Trip) (INL)			-2	0	+2	LSB
QT Voltco					0.5	%/V
QT Tempco				1.5	3	%

NONVOLATILE MEMORY CHARACTERISTICS

(V_{CC3} = +2.9V to +5.5V, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Endurance (Write Cycle)		+70°C	50k			Cycles
Endurance (Write Cycle)		+25°C	200k			Cycles

Note 1: All voltages are referenced to ground. Current into the IC is positive, and current out of the IC is negative.

Note 2: Secondary power supply is used to support optional variable power-supply feature of the XFP module. If V_{CC2} is not used (i.e., signal conditioners using 3.3V supply), V_{CC2} should be connected to the V_{CC3}.

Note 3: Input signals (i.e., TX-D, MOD-DESEL, and P-DOWN/RST) have internal pullup resistors.

Note 4: Guaranteed by design. Simulated over process and 50µA < I_{BMD} < 1500µA.

Note 5: C_B—total capacitance of one bus line in picofarads.

Note 6: EEPROM write begins after a STOP condition occurs.

Note 7: This is the maximum and minimum voltage on the MODSET and BIASSET pins required to meet accuracy and drift specifications.

Note 8: For V_{THRSET}, offset may be as much as 10mV.

Note 9: This is the uncalibrated offset provided by the factory; offset adjustment is available on this channel.

Note 10: %FS refers to calibrated FS in case of internal calibration, and uncalibrated FS in the case of external calibration. Uncalibrated FS is set in the factory and specified in this data sheet as FS (factory). Calibrated FS is set by the user, allowing a change in any monitored channel scale.

Note 11: See the *Monitor Channels* section for more detail or V_{CC2} and V_{CC3} selection.

XFP Laser Control and Digital Diagnostic IC

Timing Diagrams

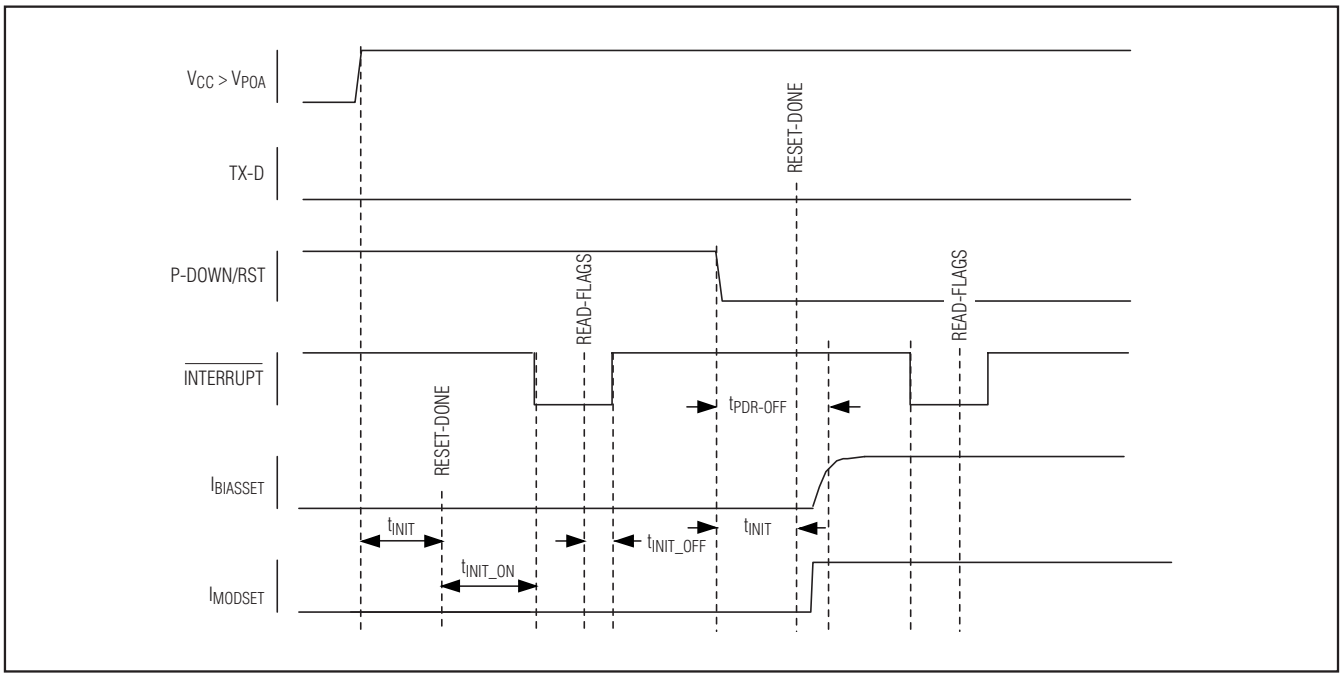


Figure 1. Power-On Initialization with P-DOWN/RST Asserted and TX-D/SOFT TX-D Not Asserted

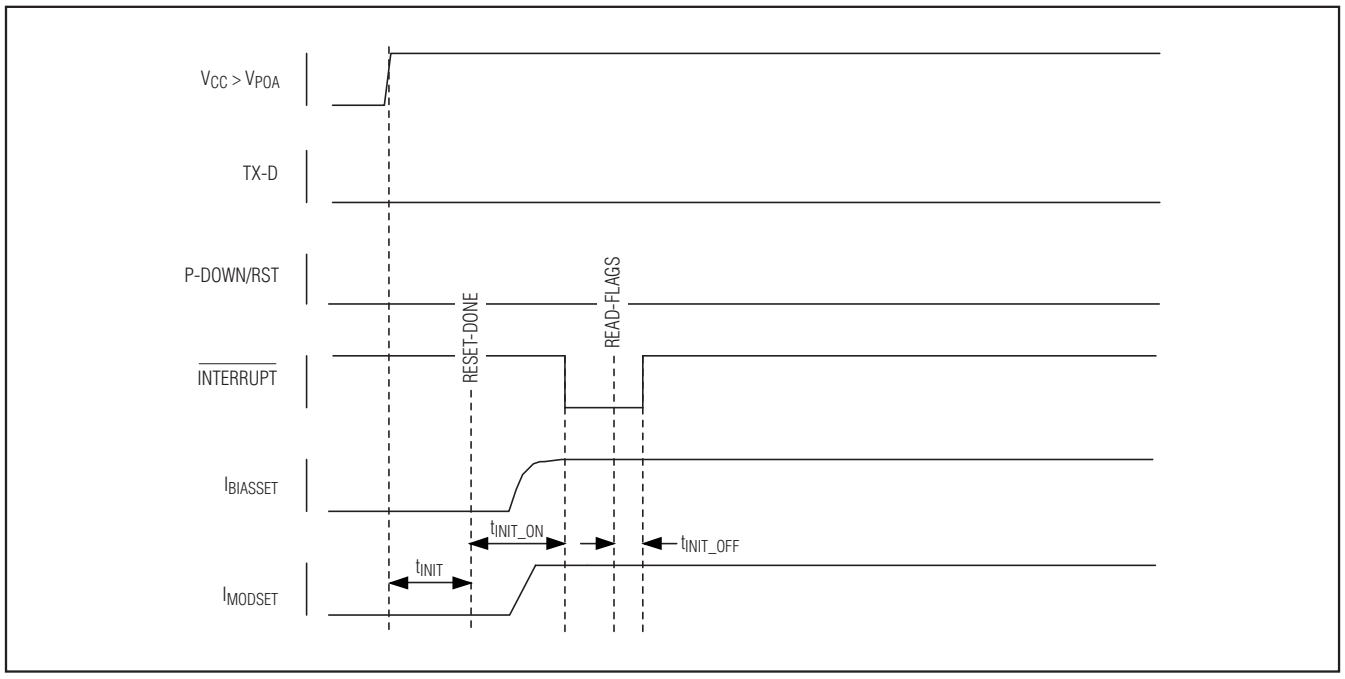


Figure 2. Power-On Initialization with P-DOWN/RST Not Asserted and TX-D/SOFT TX-D Not Asserted (Normal Operation)

Timing Diagrams (continued)

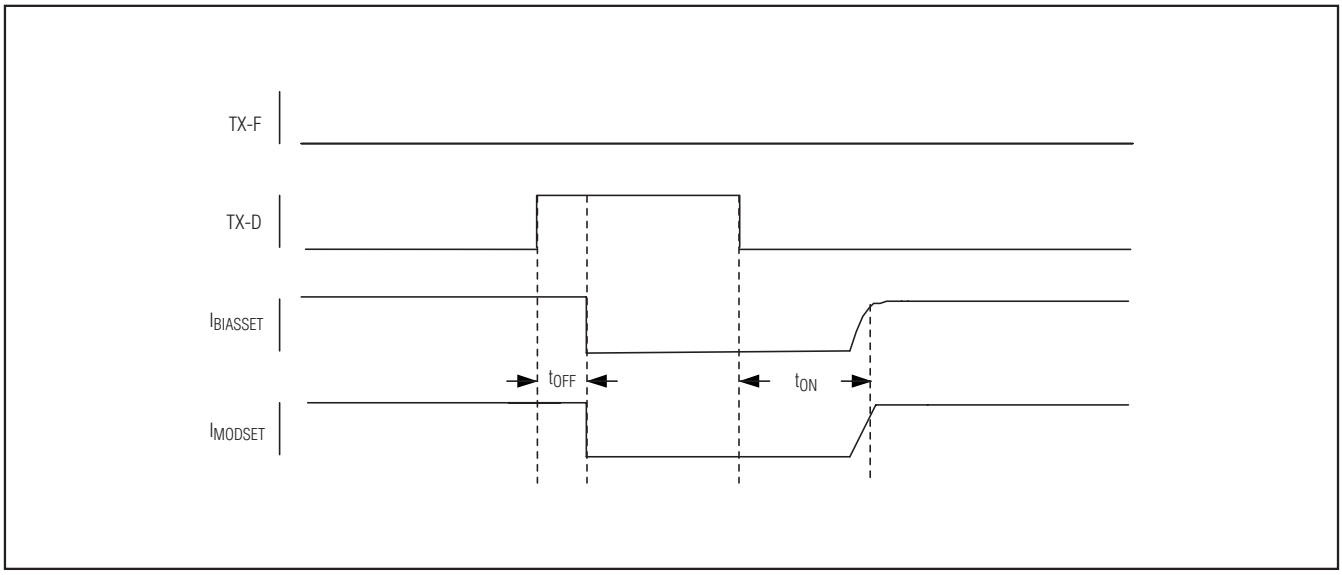


Figure 3. TX-D Timing During Normal Operation

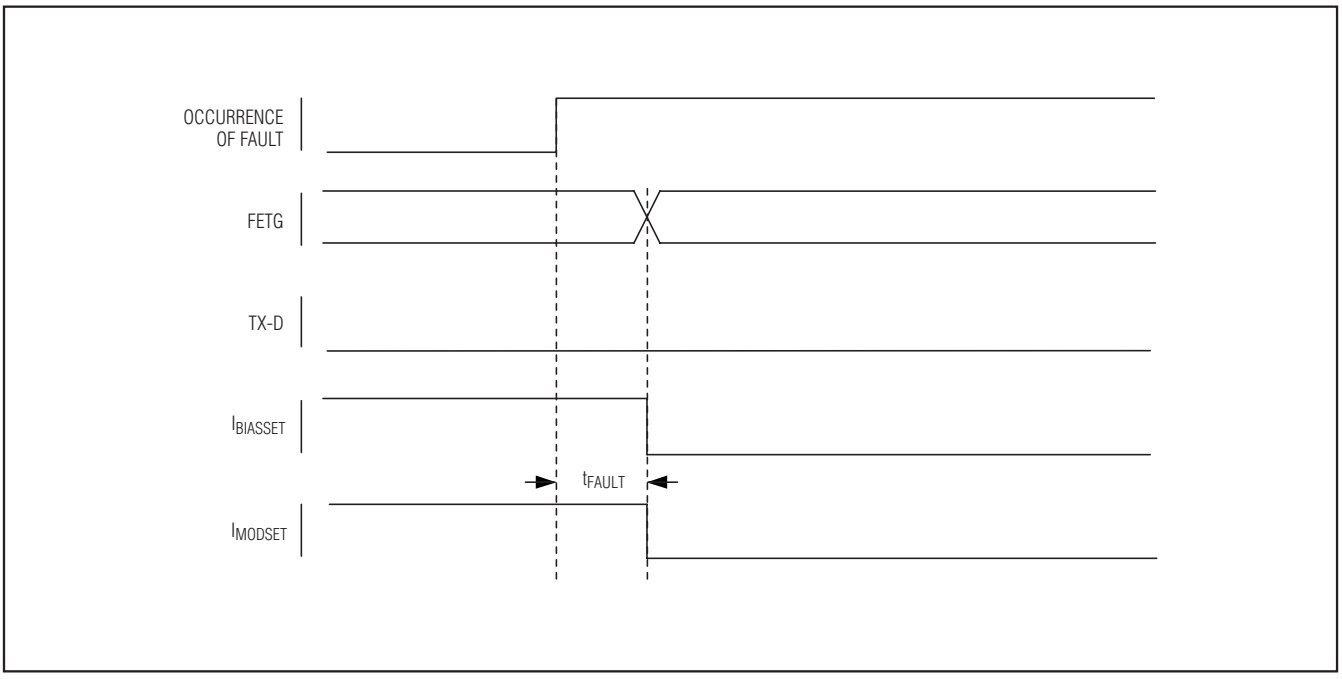


Figure 4. Detection of Safety Fault Condition

Timing Diagrams (continued)

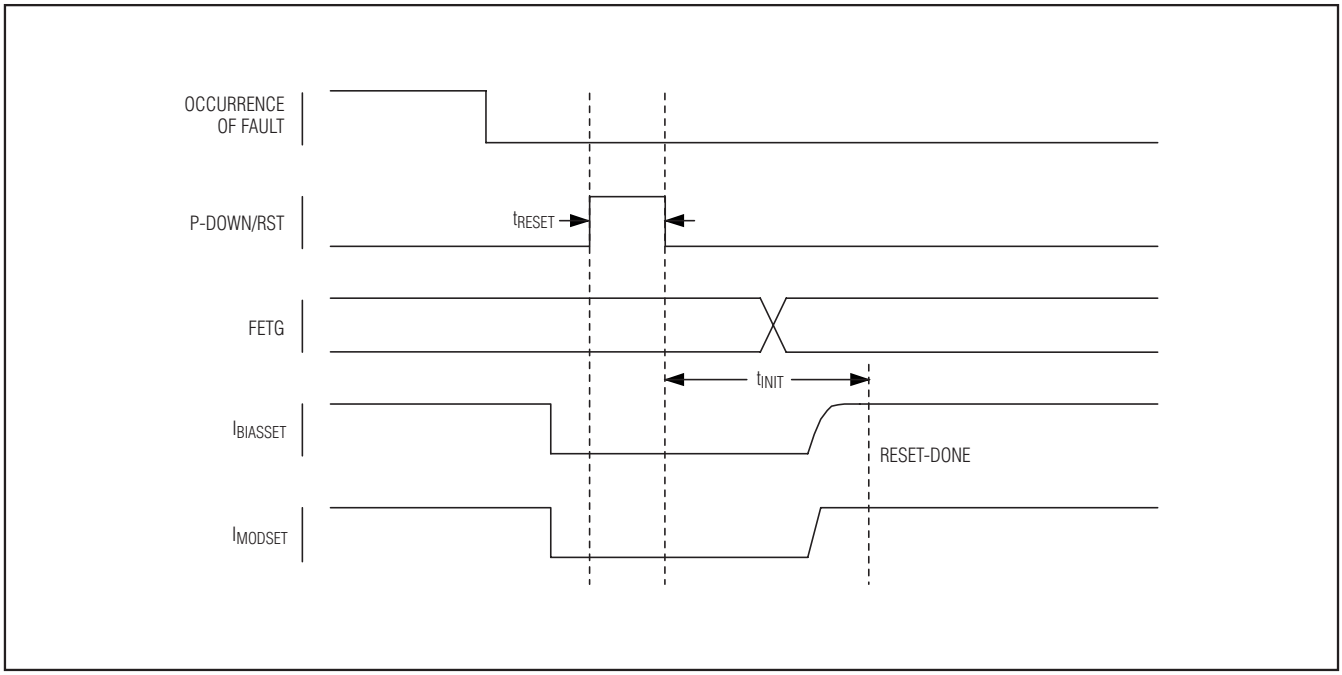


Figure 5. Successful Recovery from Transient Safety Fault Condition Using P-DOWN/RST

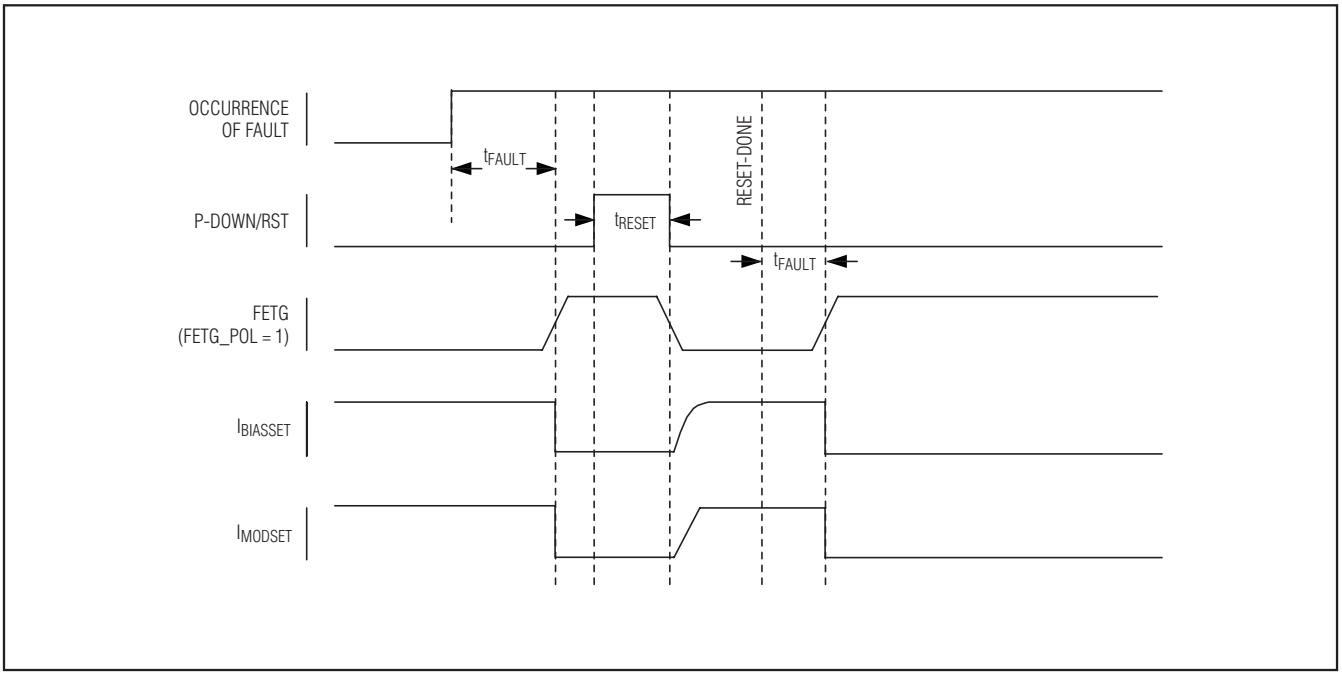


Figure 6. Unsuccessful Recovery from Transient Safety Fault Condition

Timing Diagrams (continued)

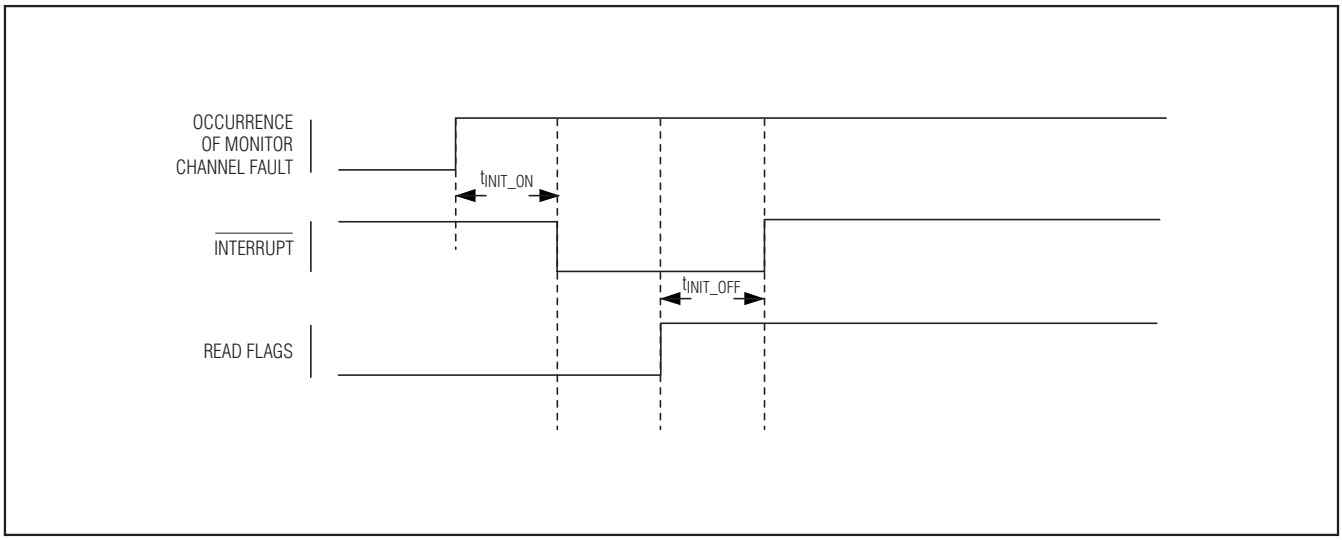


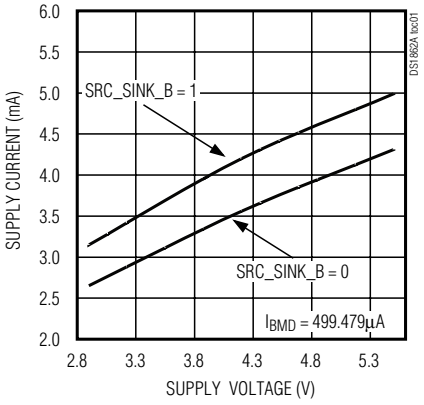
Figure 7. Monitor Channel Fault Timing

XFP Laser Control and Digital Diagnostic IC

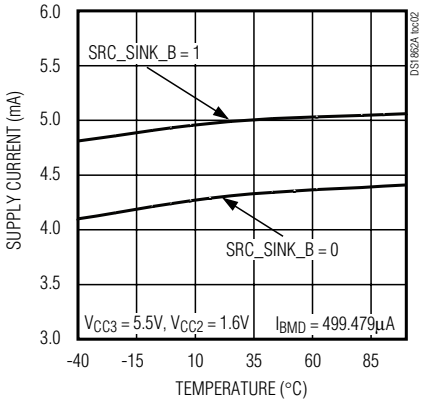
Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)

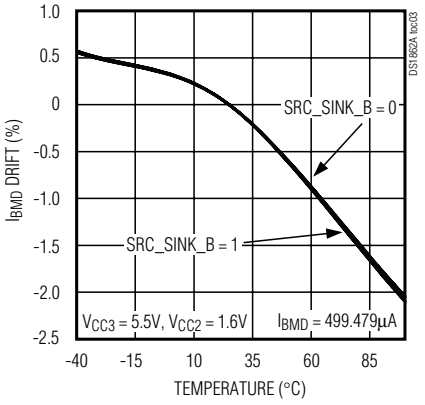
SUPPLY CURRENT vs. SUPPLY VOLTAGE



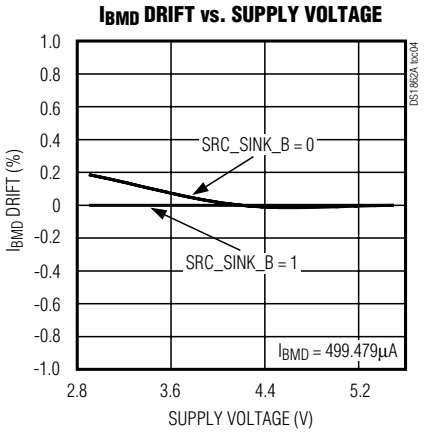
SUPPLY CURRENT vs. TEMPERATURE



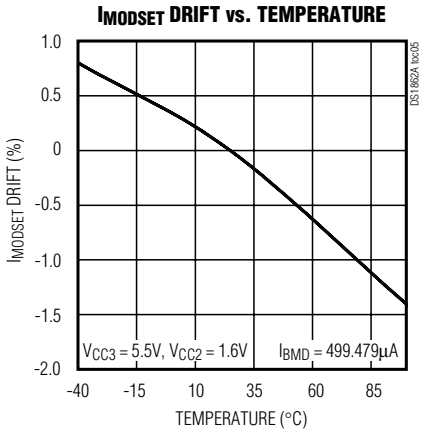
IBMD DRIFT vs. TEMPERATURE



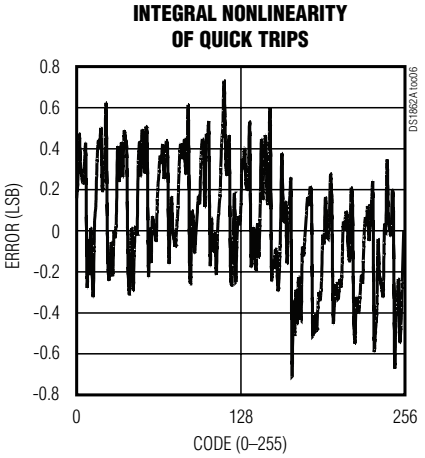
IBMD DRIFT vs. SUPPLY VOLTAGE



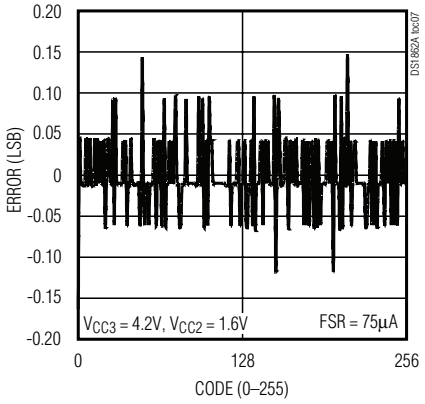
IMODSET DRIFT vs. TEMPERATURE



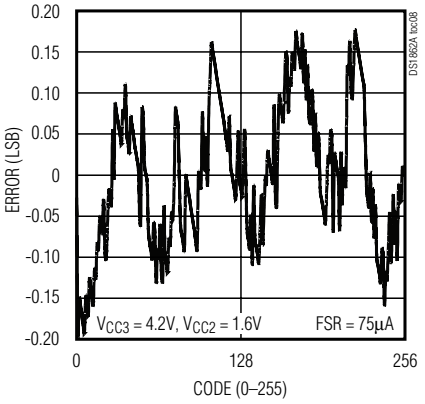
INTEGRAL NONLINEARITY OF QUICK TRIPS



DIFFERENTIAL NONLINEARITY OF IMODSET



INTEGRAL NONLINEARITY OF IMODSET

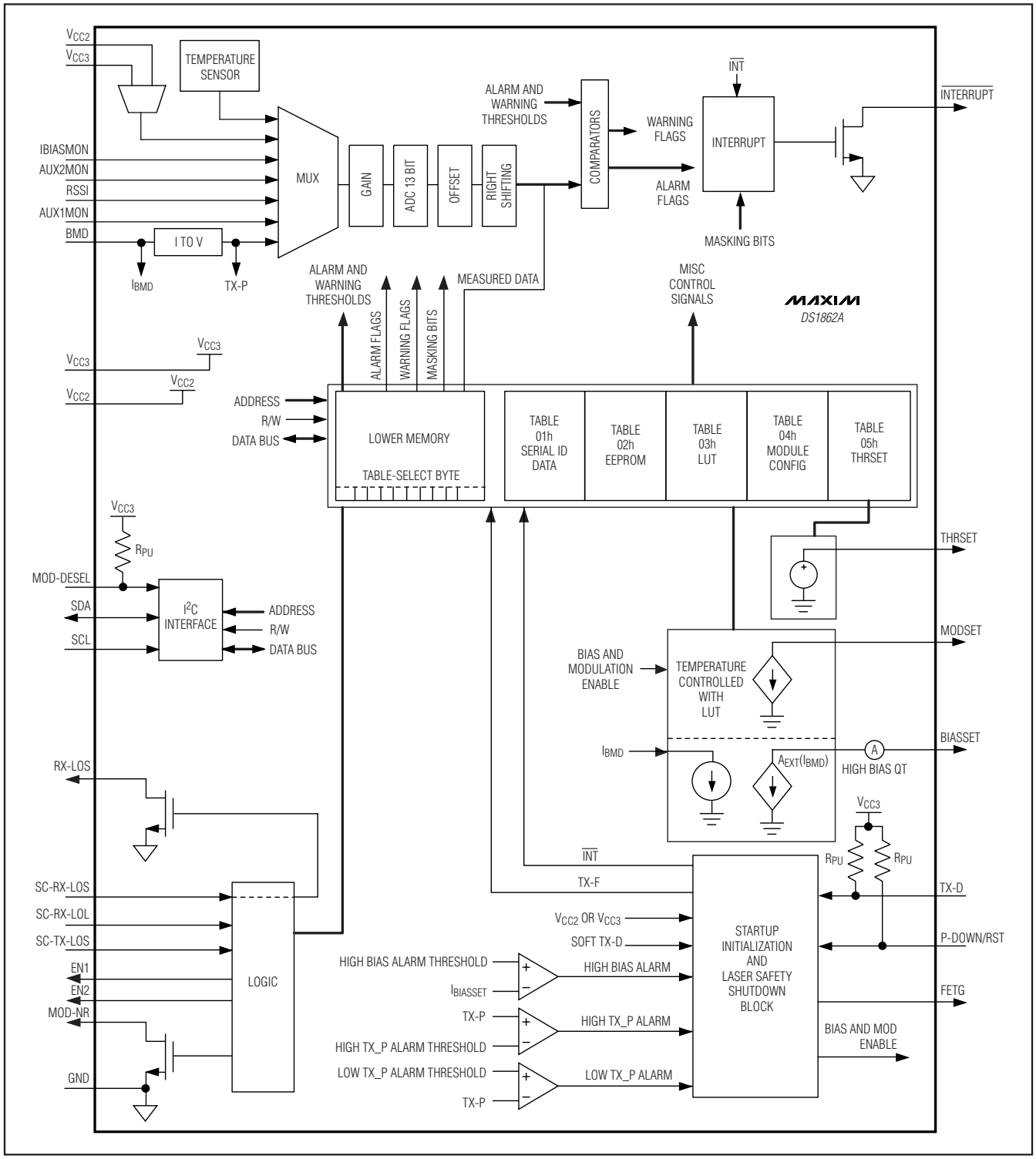


Pin Description

NAME	PIN	FUNCTION
P-DOWN/RST	A1	**Power-Down/Reset Input.** This multifunction pin is pulled high internally. See the *Power-Down/Reset Pin* section for additional information.
SC-RX-LOS	A2	**Signal Conditioner Receiver Loss-of-Signal Input.** This pin is an active-high input with LVCMOS/LVTTL voltage levels.
SC-RX-LOL	A3	**Signal Conditioner Receiver Loss-of-Lock Input.** This pin is an active-high input with LVCMOS/LVTTL voltage levels.
THRSET	A4	**Threshold Set Output.** This pin is a programmable voltage source that can be used for Rx signal conditioner.
V_{CC2}	A5	**1.8V Power-Supply Input**
RX-LOS	B1	**Receiver Loss of Signal.** This open-drain output indicates when there is insufficient optical power.
SCL	B2	**I^2C Serial-Clock Input**
FETG	B3	**FET Gate Output.** This pin can drive an external FET gate associated with safety fault disconnect.
RSSI	B4	**Received Power Signal Input**
MODSET	B5	**Modulation Current Output.** This pin is only capable of sinking current.
TX-D	C1	**Transmit Disable Input.** This pin has an internal pullup resistor.
SDA	C2	**I^2C Serial-Data Input/Output**
EN1	C3	**Enable 1 Output.** Functional control for signal conditioners.
EN2	C4	**Enable 2 Output.** Functional control for signal conditioners.
BIASSET	C5	**Bias Current Output.** This pin is only capable of sinking current.
$\overline{\text{INTERRUPT}}$	D1	**Interrupt.** This open-drain output pin indicates a possible operational fault or critical status condition to the host.
MOD-NR	D2	**Indicating Module Operational Fault.** Open-drain output. This pin indicates the status of the MOD-NR flag.
AUX1MON	D3	**Aux1 Monitor Input.** This pin can be used to measure any voltage quantity.
AUX2MON	D4	**Aux2 Monitor Input.** This pin can be used to measure any voltage quantity or external temperature
BMD	D5	**Monitor Diode Current Input.** This pin is capable of sourcing or sinking current.
GND	E1	**Ground**
MOD-DESEL	E2	**Module Deselect Input.** This pin must be pulled low to enable I^2C communication. This pin is pulled high internally.
IBIASMON	E3	**Bias Monitor Input.** This pin can be used to monitor the voltage across the laser.
SC-TX-LOS	E4	**Signal Conditioner Transmitter Loss of Signal.** This pin is an active-high input with LVCMOS/LVTTL voltage levels.
V_{CC3}	E5	**3.3V or 5V Power-Supply Input**

XFP Laser Control and Digital Diagnostic IC

Block Diagram



Detailed Description

The DS1862A's block diagram is described in detail within the following sections and memory map/memory description.

Automatic Power Control (APC)

The DS1862A's APC is accomplished by closed-loop adjustment of the bias current (BIASSET) until the feedback current (BMD) from a photodiode matches the value determined by the APC registers. The relationship between the APC register and I_{BMD} is given by:

$$I_{BMD} = 5.859\mu A \times APC_C<7:0> + (1.464\mu A \times APC_F<1:0>)$$

where $APC_C<7:0>$ is the 8-bit value in Table 04h, Byte 84h that controls the coarse BMD current, and $APC_F<1:0>$ is the 2-bit value that controls the fine BMD current.

The BMD pin appears as a voltage source in series with two resistors. The overall equivalent resistance of the BMD input pin can be closely approximated by the plot in Figure 8. The voltage that appears on the BMD pin, assuming no external current load, is 1.2V if BMD is in sink-current mode (SRC_SINK_B = 0) or 2.0V if BMD is set to source current (SRC_SINK_B = 1). This allows the photodiode to be referenced to either V_{CC3} or GND. When the control loop is at steady state, the BMD current setting matches the current that is measured by the I_{BMD} voltage across the internal resistance. During a transient period, the DS1862A adjusts the current drive on the BIASSET pin to bring the loop into steady state. The DS1862A is designed to support loop gains of 1/20 to 10.

On power-up, the BMD current ramps up to the previously saved current setting in EEPROM APC registers. While operating, the DS1862A monitors the BMD current. If it begins to deviate from the desired (set) I_{BMD} value, the current on the BIASSET pin is again adjusted to compensate.

Extinction Ratio Control Lookup Table (LUT)

The DS1862A uses a temperature indexed lookup table (LUT) to control the extinction ratio. The MODSET pin is capable of sinking current based on the 8-bit binary value that is controlling it. The DS1862A also features a user-configurable current range to increase extinction ratio resolution. Five current ranges, as described in Table 1, are available to control the current entering MODSET.

Table 1. Selectable Current Ranges for MODSET

LUT CURRENT RANGE TABLE 04h, BYTE 86h<2:0>	CURRENT RANGE (µA)
000	0 to 75
001	0 to 150
010	0 to 300
011	0 to 600
100	0 to 1200

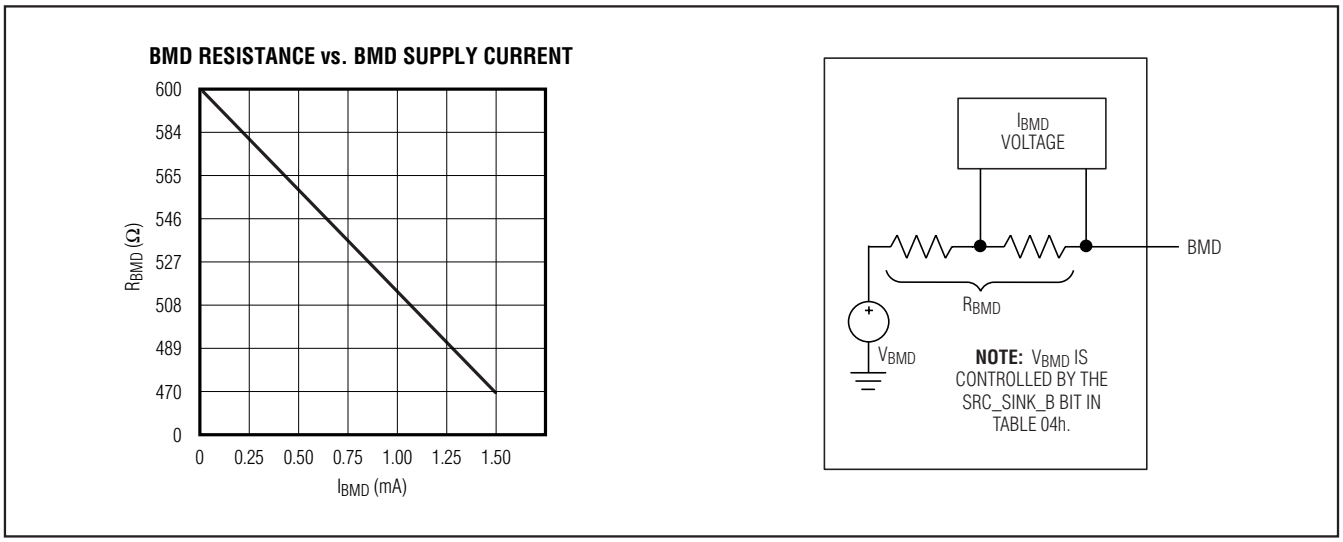


Figure 8. Approximate Model of the BMD Input

If the largest current range is selected, the maximum value of FFh (from LUT) corresponds to a 1200µA sink current. Regardless of the current range, the MODSET value always consists of 256 steps, including zero.

I_{MODSET} can be controlled automatically with the temperature-based lookup table, or by three other manual methods.

Automatic temperature addressed lookup is accomplished by an internal or external temperature sensor controlling an address pointer. This pointer indexes through 127 previously loaded 8-bit current values stored in the LUT. Each one of the 127 temperature slot locations corresponds to a 2°C increment over the -40°C to +102°C temperature range. Any temperature above or below these points causes the code in the first or last temperature slot to be indexed. Both the internal temperature sensor and an external sensor connected to AUX2MON are capable of providing a signal to control the extinction ratio automatically with an indexed LUT. Table 2 illustrates the relationship between the temperature and the memory locations in the LUT.

Table 2. Temperature Lookup Table

TEMPERATURE (°C)	CORRESPONDING LOOKUP TABLE ADDRESS
< -40	80h
-40	80h
-38	81h
-36	82h
…	…
+96	C4h
+98	C5h
+100	C6h
+102	C7h
> +102	C7h

Automatic and manual control of MODSET is controlled by two bits, TEN and AEN, that reside in Table 04h, Byte B2h. By default (from factory) TEN and AEN are both set, causing complete automatic temperature-based lookup. If TEN and/or AEN are altered, the DS1862A is set to one of the manual modes. Table 3 describes manual mode functionality.

Table 3. Truth Table for TEN and AEN Bits

TEN	AEN	DS1862A LUT FUNCTIONALITY
0	0	Manual mode that allows users to write a value directly to the LUT VALUE register (Table 04h, Byte B1h) to drive MODSET. While in this mode, the LUT INDEX POINTER register is not being updated, and no longer drives the LUT VALUE register.
0	1	Manual mode that allows users to write a value directly to the LUT VALUE register (Table 04h, Byte B1h) to drive MODSET. While in this mode, the LUT INDEX POINTER register is still being updated; however, it no longer drives the LUT VALUE register.
1	0	Manual mode that allows users to write a value to the LUT INDEX POINTER register (Table 04h, Byte B0), then the DS1862A updates the LUT VALUE register (Table 04h, Byte B1h) based on the user's index pointer.
1	1	Automatic mode (factory default). This mode automatically indexes the LUT based on temperature, placing the resulting LUT address in the LUT INDEX POINTER register (Table 04h, Byte B0h). Then the MODSET setting is transferred from that LUT address to the LUT VALUE register (Table 04h, Byte B1h). Lastly, the I_{MODSET} is set to the new MODSET code.

Monitor Channels

The DS1862A has seven monitored voltage signals that are polled in a round-robin multiplexed sequence and are updated with the frame rate, t_{FRAME}. All channels are read as 16-bit values, but have 13-bit resolution, and with the exception of temperature measurements, all channels are stored as unsigned values. The resulting 16-bit value for all monitored channels, except internal temperature, is calculated by internally averaging the analog-to-digital result eight times. The resulting internal temperature monitor channel is averaged 16 times. See the *Internal Calibration* section for a complete description of each channel's method(s) of internal calibration.

The AUX1MON, AUX2MON, and $V_{CC2/3}$ monitor channels are optional and can be disabled. This feature allows for shorter frame rate for the essential monitor channels. Channels that cannot be disabled are internal temperature, BMD, RSSI, and IBIASMON. A table of full-scale (FS) signal values (using factory internal calibration without right shifting) and the resulting FS code values for all seven channels is provided in Table 4.

Measuring Temperature—Internal or External

The DS1862A is capable of measuring temperature on three different monitor channels: internal temperature sensor, AUX1MON, and AUX2MON. Only the internal temperature and AUX2MON channels are capable of indexing the LUT to control the extinction ratio. To use an external temperature sensor on AUX2MON, the TEMP_INT/EXT bit in Table 04h, Byte 8Bh, must be set. While AUX2MON controls the extinction ratio, the internal temperature sensor does not stop running; despite extinction ratio control by AUX2MON, it is this internal temperature signal that continues to control the status of temperature flags. Also, when TEMP_INT/EXT = 1, the internal temperature clamps at -40°C and +103.9375°C, and when TEMP_INT/EXT = 0 it clamps at -120°C and +127.984°C. AUX2MON, however, does have its own flag to indicate an out-of-tolerance condition and assert the $\overline{\text{INTERRUPT}}$ pin.

Both AUX1MON and AUX2MON can be used to measure temperature as a function of voltage on their respective pins. They can be enabled by selecting either 0h or 4h from Table 5. Internal (or external) calibration may be required to transmute the input voltage to the desired two's-complement digital code, readable from the result registers in lower memory, Bytes 6Ah, 6Bh, 6Ch, 6Dh.

Measuring $V_{CC2/3}$

The DS1862A has the flexibility to internally measure either V_{CC2} or V_{CC3} to monitor supply voltage. V_{CC2} or V_{CC3} is user selectable by the $V_{CC2/3}$_SEL bit in Table 01h, Byte DCh. To remove $V_{CC2/3}$ from the round-robin monitor update scheme, despite having V_{CC2} or V_{CC3} selected to be monitored, the Reserve_EN bit in Table 04h, Byte 8Bh can be programmed to a 0. The analog power-on-reset flag, POA, indicates the status of V_{CC3} power supply. Even though POA seems to behave similarly to $V_{CC2/3}$ monitor channel, it is completely separate and has no connection.

RESERVE_EN	$V_{CC2/3}$_SEL	RESULT
0	0	$V_{CC2/3}$ result not enabled.
0	1	$V_{CC2/3}$ result not enabled.
1	0	V_{CC3} is being measured.
1	1	V_{CC2} is being measured.

Measuring APC and Laser Parameters—BMD, IBIASMON, RSSI

BMD and BIASSET are used to control and monitor the laser functionality. Regardless of the set BMD current in the APC register, the DS1862A measures BMD pin current and uses this value not only to adjust the current on the BIASSET pin, but also to monitor TX-P as well. The IBIASMON pin is used to input a voltage signal to the DS1862A that can be used to monitor the bias current through the laser. This monitor channel does not drive the HIGH BIAS quick-trip (QT) alarms for safety

Table 4. Monitor Channel FS and LSB Detail

SIGNAL	+FS SIGNAL	+FS (hex)	-FS SIGNAL	-FS (hex)	LSB
Temperature	127.984°C	7FF8	-120°C	8800	0.0625°C
$V_{CC2/3}$	6.5528V	FFF8	0V	0000	100µV
IBIASMON	2.4997V	FFF8	0V	0000	38.147µV
RSSI	2.4997V	FFF8	0V	0000	38.147µV
AUX1MON	6.5528V	FFF8	0V	0000	38.147µV
AUX2MON	6.5528V	FFF8	0V	0000	38.147µV
BMD (TX-P)	1.5mA	FFF8	0mA	0000	22.888nA

fault functionality, current on the BIASSET pin is monitored by the DS1862A to control the HIGH BIAS quick-trip alarm. Similar to TX-P, the RSSI pin is used to measure the received power, RX-P.

Measuring Voltage Quantities using AUX1MON and AUX2MON

AUX1MON and AUX2MON are auxiliary monitor inputs that may be used to measure additional parameters. AUX1/2MON feature a user-selectable register that determines the measured value's units (i.e., voltage, current, or temperature). In addition to indicating units, some of the 4-bit op codes, in Table 5, also place the part in special modes used for alarms and faults internally. Whichever units' scale is selected, the DS1862A is only capable of measuring a positive voltage quantity, therefore internal or external calibration may be required to get the binary value to match the measured quantity. A table of acceptable units and/or their corresponding user-programmable 4-bit op code is provided below.

Table 5. AUX1/2MON Functionality Selection (Unit Selection)

VALUE	DESCRIPTION OF AUX1/2MON INTENDED USE (UNITS OF MEASURE)
0000b	Auxiliary monitoring not implemented
0001b	APD bias voltage (16-bit value is voltage in units of 10mV)
0010b	Reserved
0011b	TEC current (mA) (16-bit value is current in units of 0.1mA)
0100b	Laser temperature (same encoding as module temperature)
0101b	Laser wavelength
0110b	+5V supply voltage (encoded as primary voltage monitor)
0111b	+3.3V supply voltage (encoded as primary voltage monitor)
1000b	+1.8V supply voltage (encoded as primary voltage monitor) (V_{CC2})
1001b	-5.2V supply voltage (encoded as primary voltage monitor)
1010b	+5V supply current (16-bit value is current in 0.1mA)
1101b	+3.3V supply current (16-bit value is current in 0.1mA)
1110b	+1.8V supply current (16-bit value is current in 0.1mA)
1111b	-5.2V supply current (16-bit value is current in 0.1mA)

Alarms and Warning Flags Based on Monitor Channels

All of the monitor channels feature alarm and warning flags that are asserted automatically as user-programmed thresholds are internally compared with monitor channel results. Flags may be set, which, if not masked, will generate an interrupt on the $\overline{\text{INTERRUPT}}$ pin or generate a safety fault. Whenever $V_{CC2/3}$, AUX2MON, AUX1MON, RSSI, and internal temperature go beyond their threshold trip points and the corresponding mask bit is 0, an interrupt is generated on the $\overline{\text{INTERRUPT}}$ pin and a corresponding warning or alarm flag is set. Similarly, a safety fault occurs whenever BMD or BIASSET go beyond threshold trip points. When this happens, the FETG pin immediately asserts and BIASSET and MODSET currents are shut down.

Monitor Channel Conversion Example

Table 6 provides an example of how a 16-bit ADC code corresponds to a real life measured voltage using the factory-set calibration on either RSSI or IBIASMON. By factory default, the LSB is set to 38.147µV.

Table 6. A/D Conversion Example

MSB (BIN)	LSB (BIN)	VOLTAGE (V)
11000000	00000000	1.875
10000000	10000000	1.255

To calculate V_{CC2}, V_{CC3}, AUX1MON, or AUX2MON, convert the unsigned 16-bit value to decimal and multiply by 100µV.

To calculate the temperature (internal), treat the two's-complement value binary number as an unsigned binary number, then convert it to decimal and divide by 256. If the result is grater than or equal to 128, subtract 256 from the result.

Temperature: high byte = -128°C to +127°C signed; low byte = 1/256°C.

Table 7. Temperature Bit Weights

S	2^6	2^5	2^4	2^3	2^2	2^1	2^0
2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	—	—	—

Table 8. Temperature Conversion Examples

MSB (BIN)	LSB (BIN)	TEMPERATURE (°C)
01000000	00000000	+64
01000000	00001000	+64.03215
01011111	00000000	+95
11110110	00000000	-10
11011000	00000000	-40

Internal Calibration

The DS1862A has two means for scaling an analog input to a digital result. The two devices alter the gain and offset of the signal to be calibrated. All of the inputs except internal temperature have unique registers for both the gain and the offset that can be found in Table 04h. See the table below for a complete description of internal calibration capabilities including right-shifting for all monitor channels.

Table 9. Internal Calibration Capabilities

SIGNAL	INTERNAL SCALING	INTERNAL OFFSET	RIGHT-SHIFTING
Temperature	—	x	—
$V_{CC2/3}$	x	x	—
IBIASMON	x	x	x
RSSI (RX-P)	x	x	x
AUX1MON	x	x	x
AUX2MON	x	x	x
BMD (TX-P)	x	x	x

To scale a specific input's gain and offset, the relationship between the analog input and the expected digital result must be known. The input that would produce a corresponding digital result of all zeroes is the null value (normally this input is GND). The input that would produce a corresponding digital result of all ones is the full-scale (FS) value minus one LSB. The FS value is also found by multiplying an all ones digital value by the weighted LSB. For example, a digital reading is 16 bits long, assume that the LSB is known to be 50µV, then the FS value would be 2^{16} x 50µV = 3.2768V.

A binary search can be used to find the appropriate gain value to achieve the desired FS of the converter. Once the gain value is determined, then it can be loaded into the appropriate channels' Gain register. This requires forcing two known voltages on to the monitor input pin. For best results, one of the forced voltages should be the NULL input and the other should be 90% of FS. Since the LSB of the least significant byte in the digital reading register is known, the expected digital results are also known for both the null and FS value inputs. Figure 9 describes the hysteresis built into the DS1862A's LUT functionality.

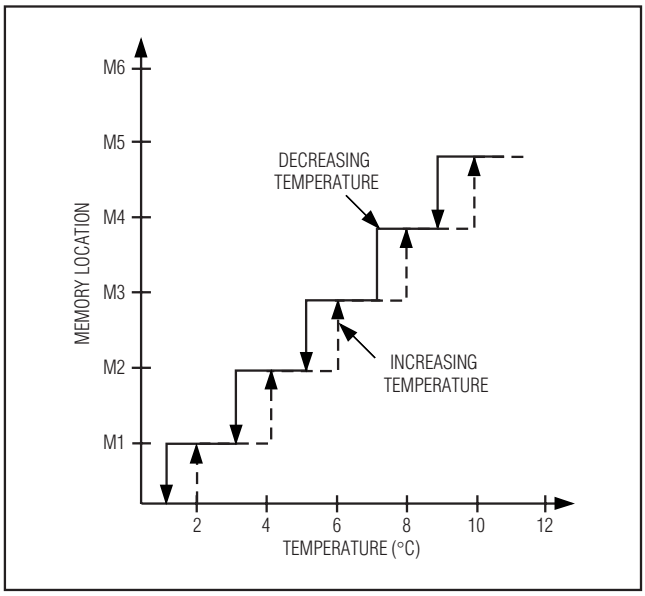


Figure 9. Lookup Table Hysteresis

With the exception of BMD, which can source or sink current, all monitored channels are high impedance and are only capable of directly measuring a voltage. If other measured quantities are desired, such as light, frequency, power, current, etc., they must be converted to a voltage. In this situation the user is not interested in voltage measurement on the monitored channel, but the measurement of the desired parameter. Only the relationship between the indirect measured quantity (light, frequency, power, current, etc.) to the expected digital result must be known.

An example of gain scaling using the recommended binary search procedure is provided with the following pseudo code.

To help will the computation, two integers need to be defined: count 1 and count 2. CNT1 = NULL / LSB and CNT2 = 90%FS / LSB. CLAMP is the largest result that can be accommodated.

```
/* Assume that the Null input is 0.5V. */
/* In addition, the requirement for LSB is 50µV. */
    FS = 65536 * 50e-6;          /* 3.2768 */
    CNT1 = 0.5 / 50e-6;          /* 10000 */
    CNT2 = 0.90*FS / 50e-6;      /* 58982 */
/* Thus the NULL input of 0.5V and the 90% of FS input
is 2.94912V. */
    set the trim-offset-register to zero;
    set Right-Shift register to zero (Typically zero.
    See the Right-Shifting section);
    gain_result = 0h;
    CLAMP = FFF8h/2^(Right_Shift_Register);
    For n = 15 down to 0
    begin
        gain_result = gain_result + 2^n;
        Force the 90% FS input (2.94912V);
        Meas2 = read the digital result from the part;
    If Meas2 >= CLAMP then
        gain_result = gain_result - 2^n;
    Else
        Force the NULL input (0.5V);
        Meas1 = read the digital result from the part;
        if (Meas2 - Meas1) > (CNT2 - CNT1) then
        gain_result = gain_result - 2^n;
    end;
    Set the gain register to gain_result;
```

The gain register is now set and the resolution of the conversion will best match the expected LSB. The next step is to calibrate the offset of the DS1862A. With the correct gain value written to the gain register, again force the NULL input to the monitor pin. Read the digital result from the part (Meas1). The offset value is equal to negative value of Meas1.

$$OFFSET\_REGISTER = \left[\frac{(-1)Meas1}{4}\right]$$

The calculated offset is now written to the DS1862A and the gain and offset-scaling procedure is complete.

Right-Shifting A/D Conversion Result (Scalable Dynamic Ranging)

Right-shifting is a digital method used to regain some of the lost ADC range of a calibrated system. If right-shifting is enabled, by simply loading a non-zero value into the appropriate Right-Shifting Register, then the DS1862A shifts the calibrated result just before it is stored into the monitor channels' register. If a system is calibrated so the maximum expected input results in a digital output value of less than 7FFFh (50% of FS), then it is a candidate for using the right-shifting method.

If the maximum desired digital output is less than 7FFFh, then the calibrated system is using less than 1/2 the ADC's range. Similarly, if the maximum desired digital output is less than 1FFFh, then the calibrated system is only using 1/8th the ADC's range. For example, if an applied maximum analog signal yields a maximum digital output less than 1FFCh, then only 1/8th of the ADC's range is used. Right-shifting improves the resolution of the measured signal as part of internal calibration. Without right-shifting, the 3 MS bits of the ADC will never be used. In this example, a value of 3 for the right-shifting maximizes the ADC range and a larger gain setting must be loaded to achieve optimal conversion. No resolution is lost since this is a 13-bit converter that is left justified. The value can be right-shifted 3 times without losing any resolution. The following table describes when the right-shifting method can be effectively used.

Table 10. Right-Shifting Selection

OUTPUT RANGE USED WITH ZERO RIGHT-SHIFTS	NUMBER OF RIGHT-SHIFTS NEEDED
0h .. FFFFh	0
0h .. 7FFFh	1
0h .. 3FFFh	2
0h .. 1FFFh	3
0h .. 0FFFh	4

Warning and Alarm Logic Based on AUX1/2MON, $V_{CC2/3}$, Temp, RX-P, and IBIASMON

The DS1862A is capable of generating an alarm and/or warning whenever an analog monitored channel goes out of a user-defined tolerance. Temperature, bias current (based on IBIASMON), receive power (based on RSSI), AUX1MON, AUX2MON, and $V_{CC2/3}$, are monitored channels that generate latched flags. See the figure below for more detail pertaining to AUX1MON and AUX2MON. Flags are latched into a high state the first time a monitored channel goes out of the defined operating window and for each monitored signal there is a Mask bit that can be set to prevent the corresponding alarm or warning flag from being set. Once a flag is set, it is cleared by simply reading its memory location.

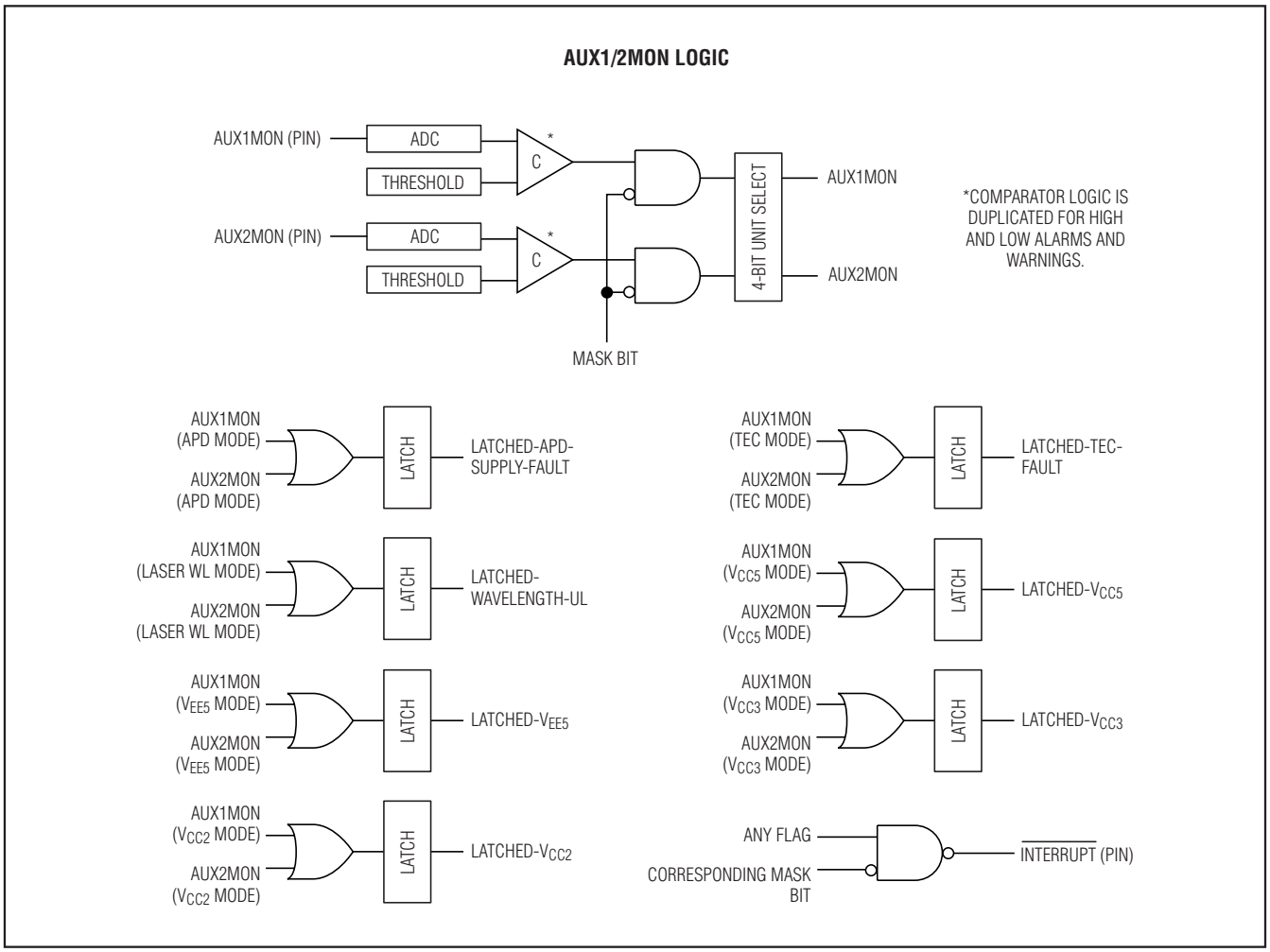


Figure 10. AUX1/2MON Monitor Logic

XFP Laser Control and Digital Diagnostic IC

Warning and Alarm Logic Based on Signal Conditioners

The DS1862A also has flags that are set by certain logical conditions on signal conditioner (SC) pins: SC-RX-LOL, SC-RX-LOS, SC-TX-LOS. Similarly, for each latched signal conditioner flag there are also mask bits that are capable of preventing the alarm or warning flag from causing an $\overline{\text{INTERRUPT}}$ pin to assert. Again, flags are cleared automatically whenever their memory address is read. See Figure 11 for more detail.

Quick-Trip Logic and FETG Shutdown Functionality

In addition to alarms and warnings, the DS1862A also has quick-trip (QT) functionality (sometimes referred to as fast alarms) that is capable of shutting down the LASER with the FETG pin in conjunction with shutting down I_{MODSET} and $I_{BIASSET}$. I_{BMD} and $I_{BIASSET}$ currents are measured and are compared with user-defined trip points to set the quick-trip flags: QT LOW TX-P, QT HIGH TX-P, and QT HIGH BIAS. These flags are also capable of being masked to prevent FETG from being asserted when an out-of-tolerance condition is detected. FETG is not asserted by setting the TX-D pin, SOFT TX-D, or P-DOWN/RST pin to a high state, however, I_{MODSET}, and $I_{BIASSET}$ will shut down. See Figure 12 for more detail.

The polarity of the FETG pin can also be reversed by setting the FETG_POL bit. Once a safety fault has occurred, the FETG pin and all of the attendant flags

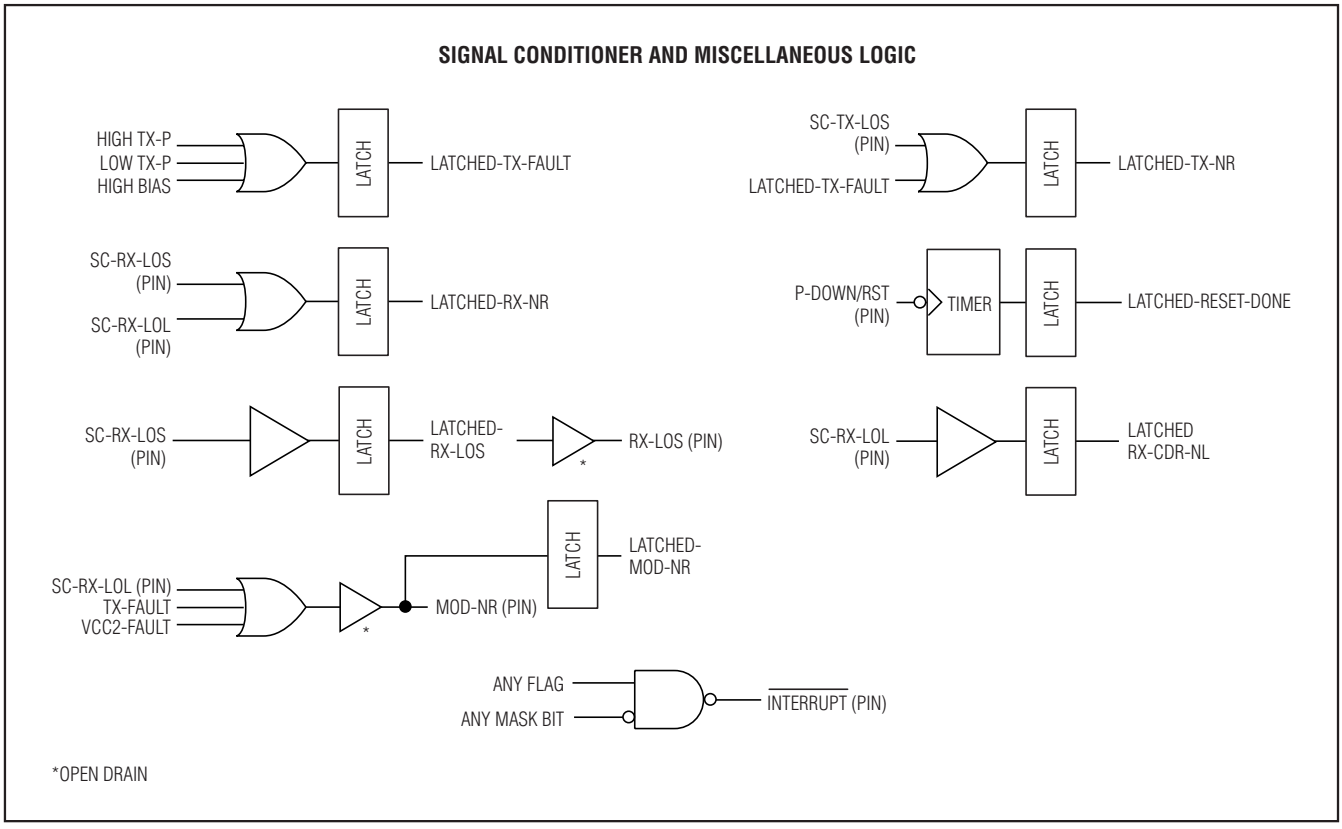


Figure 11. Signal Conditioner and Other Logic

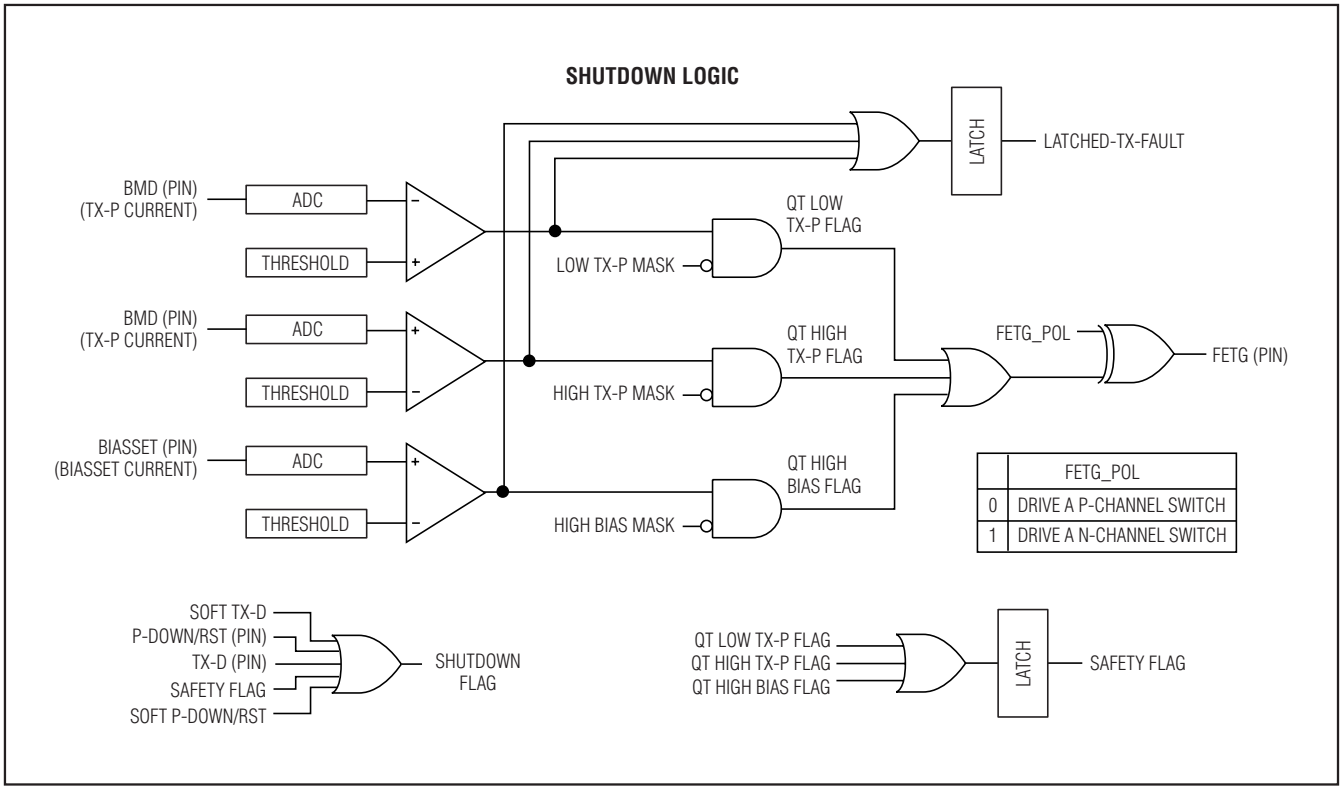


Figure 12. Safety Fault and Shutdown Logic

can only be reset by pulsing the P-DOWN/RST pin high for the reset time, t_{RESET}, or by toggling the SOFT P-DOWN/RST bit in Byte 6Eh, bit 3. See the *Power-Down/Reset Pin* section for more details.

Power-Down/Reset Pin

The P-DOWN/RST pin is a multifunction input pin that resets and/or powers down the DS1862A. Since the pin is internally pulled up, its normal state is released, which corresponds to power-down mode. If the P-DOWN/RST pin is released, or driven high, the DS1862A responds by shutting down the MODSET and BIASSET currents. Once the pin is pulled low, operation continues (if not inhibited by a safety fault). Besides powering down the DS1862A, a high-going pulse with minimum reset time, t_{RESET}, can be applied to the P-DOWN/RST pin. This is necessary to restart the DS1862A, especially if it is in a safety shutdown condition and needs to be restarted after the safety condition has been rectified. See the timing diagrams for proper pin timing.

Power-Down Functionality

During power-down mode $I_{BIASSET}$ and I_{MODSET} drop below 10µA, effectively shutting down the laser. FETG is not asserted and safety faults do not occur during this period. During power-down, I^2C communication is still active, but the signal conditioner pins EN1 and EN2 are noncontrollable and automatically change to the states: EN1 = 1 and EN2 = 0. Other internal flags/signals that are based on the signal conditioner inputs still reflect the status on the signal conditioner pins during power-down. For example, RX-LOS still reflects the status of SC-RX-LOS, and MOD-NR still reflects the logical states for the signal conditioner pins. Similarly, it is possible for FETG to be asserted, even though the BIASSET and MODSET currents are shut down. However, during power-down and a short period, $t_{PDR-OFF}$, during power-up, TX-P Low flag is ignored (internally automatically masked out) and does not contribute to FETG's logic.

During an asserted period of P-DOWN/RST (DS1862A in power-down), and V_{CC3} is cycled, the DS1862A remains in power-down mode upon power-up. While in power-down mode the $\overline{\text{INTERRUPT}}$ pin does not assert. Once V_{CC3} has returned, the reset done flag asserts after the interrupt assert delay, t_{INIT_ON}.

Reset Functionality

Besides powering down the DS1862A, the P-DOWN/RST pin also functions to reset the DS1862A. After a high-going pulse of time t_{RESET}, several events occur within the DS1862A. First, MODSET and BIASSET currents shut down and are then reinstated. Second, between the rising edge of the reset pulse and the assertion of the reset-done flag (t_{INIT}), the low TX-P flag is ignored and does not cause FETG to trip. After time t_{INIT}, the low TX-P flag becomes functional. Also, at this time, the reset-done flag is asserted, causing an interrupt to be generated. If there are no faults before t_{INIT}, then no interrupts are asserted on the $\overline{\text{INTERRUPT}}$ pin.

If V_{CC3} is powered up while P-DOWN/RST is high, then the reset-done flag must be cleared twice. The first time the reset-done flag is generated by V_{CC3} powering up, the second time reset-done is generated by a falling edge on P-DOWN/RST. If V_{CC3} is continuously powered while P-DOWN/RST is low then only one reset-done flag needs to be cleared. See the timing diagrams for graphical detail.

Memory Map

Memory Organization

The DS1862A features six separate memory tables that are internally organized into 4-word rows. The Lower Memory is addressed from 00h to 7Fh and contains alarm and warning thresholds, flags, masks, several control registers, password entry area (PE), and the table select byte. Table 01h primarily contains user EEPROM as well as several control bytes for various functions. Table 02h is strictly user EEPROM that is protected by a host password. Table 03h is strictly used for controlling the extinction ratio with an LUT. Table 04h is a multifunction space that contains internal calibration values for monitored channels, LUT index pointers, and miscellaneous control bytes. Table 05h is factory programmed and stores SCALE values for use with suggested external temperature sensors. Also, one byte in Table 05h controls the THRSET voltage source and is completely accessible without any password protection. See the *Detailed Register Description* section for a more complete detail of each byte's function, as well as Table 11 for read/write permissions for each byte. Many nonvolatile memory locations are actually SRAM-shadowed EEPROM, which are controlled by the SEEB bit in Table 04h, Byte B2h.

The DS1862A incorporates SRAM-shadowed EEPROM memory locations for key memory addresses that may be rewritten many times. By default the shadowed-EEPROM bit, SEEB, is not set and these locations act as ordinary EEPROM. By setting SEEB, these locations begin to function like SRAM cells, which allow an infinite number of write cycles without concern of wearing out the EEPROM. This also eliminates the requirement for the EEPROM write time, t_{WR}. Because changes made with SEEB enabled do not affect the EEPROM, these changes are not retained through power cycles. The power-up value is the last value written with SEEB disabled. This function can be used to limit the number of EEPROM writes during calibration or to change the monitor thresholds periodically during normal operation helping to reduce the number of times EEPROM is written. The following information describes which locations are shadowed-EEPROM.

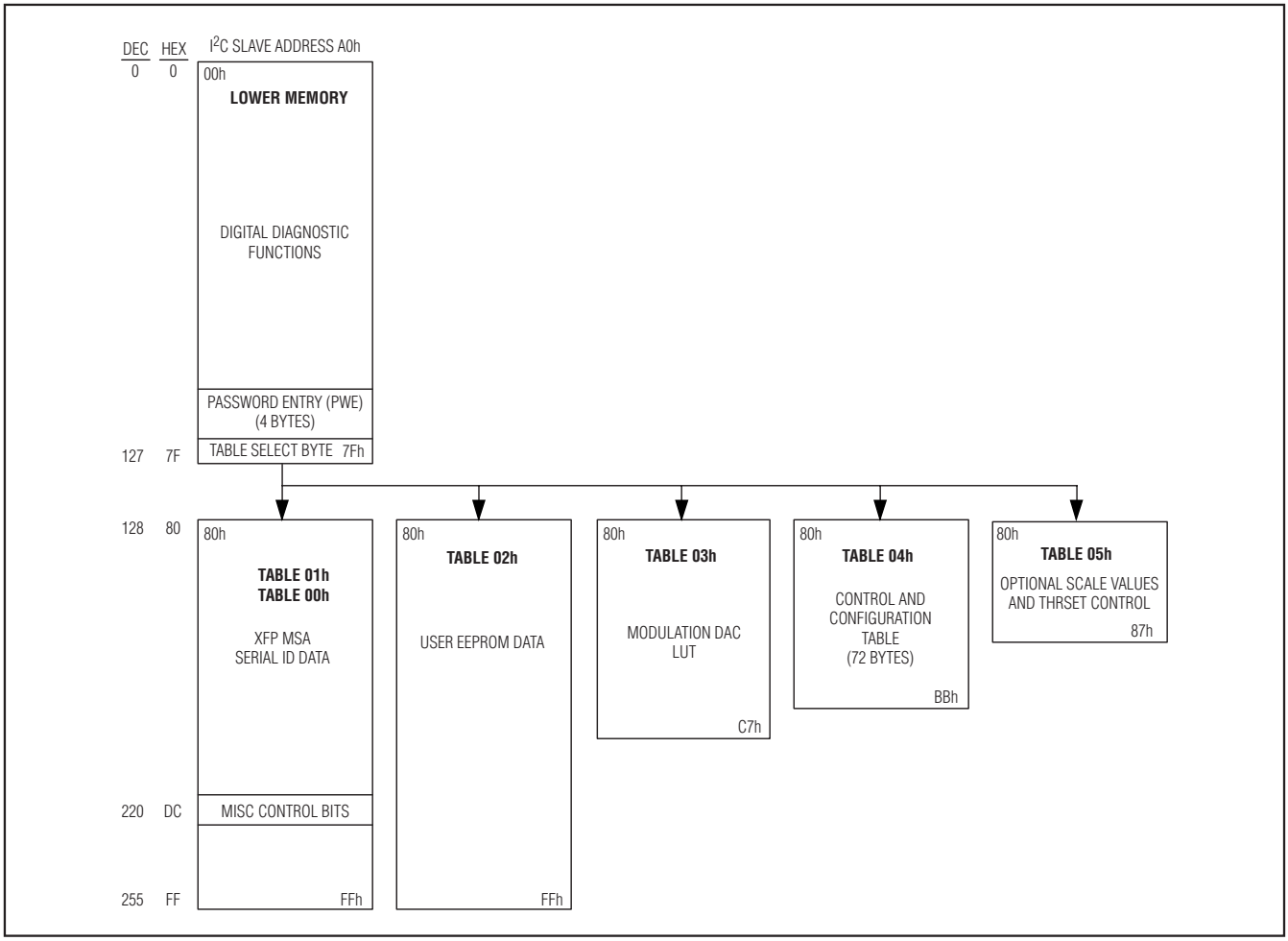


Figure 13. General View of DS1862A Memory Organization

Register Map

Table 11. Permission Table

PERMISSION	READ	WRITE
<0>	At least one byte in this row is different than the rest of the bytes, so look at each byte separately for permissions.	
<1>	ALL	ALL
<2>	ALL	MODULE
<3>	ALL	HOST
<4>	MODULE	MODULE
<5>	ALL	FACTORY
<6>	NEVER	HOST
<7>	NEVER	MODULE