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19-4883; Rev 2; 8/09

Burst-Mode PON Controller With Integrated Monitoring

General Description

The DS1863 controls and monitors all the burst-mode transmitter and video receiver biasing functions for a passive optical network (PON) transceiver. It has an APC loop with tracking-error compensation that provides the reference for the laser driver's bias current and a temperature-indexed lookup table (LUT) that controls the modulation current. It continually monitors for high output current, high bias current, and low and high transmit power with its internal fast comparators to ensure that laser shutdown for eye safety requirements are met without adding external components. Five ADC channels monitor V_{CC}, internal temperature, and three external monitor inputs (MON1, MON2, MON3) that can be used to meet transmitter and receive monitoring requirements.

Applications

BPON, GPON, and GEPON Burst-Mode Transmitters

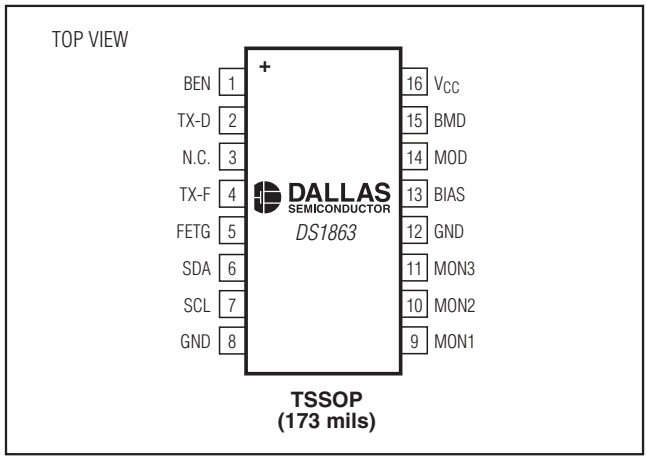
Laser Control and Monitoring

Broadband Local Access

Features

- **Meets BPON, GPON, and GEPON Timing Requirements for Burst-Mode Transceivers**
- **Bias Current Control Provided by APC Loop with Tracking Error Compensation**
- **Modulation Current Is Controlled by a Temperature-Indexed Lookup Table**
- **Supports 0dB, -3dB, -6dB Power Leveling Settings with No Additional Calibration**
- **Internal Direct-to-Digital Temperature Sensor**
- **Five Analog Monitor Channels: Temperature, V_{CC}, MON1, MON2, and MON3**
- **Comprehensive Fault Management System with Maskable Laser Shutdown Capability**
- **Two-Level Password Access to Protect Calibration Data**
- **120 Bytes of Password 1 (PW1) Protected Nonvolatile Memory**
- **128 Bytes of Password 2 (PW2) Protected Nonvolatile Memory**
- **I^2C-Compatible Interface for Calibration and Monitoring**
- **Operating Voltage: 2.85V to 3.9V**
- **Operating Temperature: -40°C to +95°C**
- **16-Pin, Lead-Free TSSOP Package**

Pin Configuration



TSSOP (173 mils)

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
DS1863E+	-40°C to +95°C	16 TSSOP
DS1863E+T&R	-40°C to +95°C	16 TSSOP

+Denotes a lead(Pb)-free/RoHS-compliant package.
T&R = Tape and reel.

Burst-Mode PON Controller With Integrated Monitoring

ABSOLUTE MAXIMUM RATINGS

Voltage on V_{CC}, SDA and SCL Pin Relative to Ground .....-0.5V to 6V
Voltage on BEN, TX-D, TX-F, MON1–MON3, BMD Relative to Ground .....-0.5V to V_{CC} + 0.5V (subject to not exceeding +6V)

Operating Temperature Range .....-40°C to +95°C
Programming Temperature Range .....0°C to +70°C
Storage Temperature Range .....-55°C to +125°C
Soldering Temperature .....See J-STD-020 specification

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

(T_A = -40°C to +95°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	V_{CC}	(Note 1)	+2.85		3.9	V
High-Level Input Voltage (SDA, SCL, BEN)	$V_{IH:1}$		0.7 x V_{CC}		V_{CC} + 0.3	V
Low-Level Input Voltage (SDA, SCL, BEN)	$V_{IL:1}$		-0.3		0.3 x V_{CC}	V
High-Level Input Voltage (TX-D)	$V_{IH:2}$		2.0		V_{CC} + 0.3	V
Low-Level Input Voltage (TX-D)	$V_{IL:2}$		-0.3		0.8	V

ELECTRICAL CHARACTERISTICS

(V_{CC}= +2.85V to +3.9V, T_A = -40°C to +95°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current	I_{CC}	(Notes 1, 2)		5	7	mA
Output Leakage (SDA, TX-F)	I_{LO}				1	µA
Low-Level Output Voltage (SDA, TX-F, FETG)	V_{OL}	I_{OL} = 4mA			0.4	V
		I_{OL} = 6mA			0.6	
High-Level Output Voltage (FETG)	V_{OH}	I_{OH} = 4mA (Note 2)	V_{CC} – 0.4			V
FETG Before Recall		(Note 3)		10	100	nA
Input Leakage Current (SCL, BEN, TX-D)	$I_{LI:1}$				1	µA
Digital Power-On Reset	POD		1.0		2.2	V
Analog Power-On Reset	POA		2.1		2.75	V

ANALOG INPUT CHARACTERISTICS (BMD)

(V_{CC} = +2.85V to +3.9V, T_A = -40°C to +95°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
BMD Full-Scale Voltage Range	V_{APC}	(Note 4)		2.5		V
Resolution		(Note 4)		8		bits
V_{APC} Error		T_A = +25°C (Note 5)	-1.75		+1.75	%FS
V_{APC} Integral Nonlinearity			-1		+1	LSB
V_{APC} Differential Nonlinearity			-1		+1	LSB
V_{APC} Temp Drift			-2.5		+2.5	%FS
Input Resistance			35	50.0	65	kΩ

ANALOG OUTPUT CHARACTERISTICS

(V_{CC}= +2.85V to +3.9V, T_A = -40°C to +95°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
BIAS Current	I_{BIAS}	(Note 1)		1.2		mA
I_{BIAS} Shutdown Current	$I_{BIAS:OFF}$			10	100	nA
Voltage at I_{BIAS}			0.7	1.2	1.4	V
MOD Full-Scale Voltage	V_{MOD}	(Note 6)		1.25		V
MOD Output Impedance		(Note 7)		3.14		kΩ
V_{MOD} Error		T_A = +25°C (Note 8)	-1.25		+1.25	%FS
V_{MOD} Integral Nonlinearity			-1		+1	LSB
V_{MOD} Differential Nonlinearity			-1		+1	LSB
V_{MOD} Temperature Drift			-2		+2	%FS

CONTROL LOOP AND QUICK-TRIP TIMING CHARACTERISTICS

(V_{CC}= +2.85V to +3.9V, T_A = -40°C to +95°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
First BMD Sample Following BEN	t_{FIRST}	(Note 9)				
Remaining Updates During BEN	t_{REP}	(Note 9)				
BEN High Time	$t_{BEN:HIGH}$		420			ns
BEN Low Time	$t_{BEN:LOW}$		96			ns
BIAS and MOD Turn-Off Delay	t_{OFF}				5	µs
BIAS and MOD Turn-On Delay	t_{ON}				5	µs
FETG Turn-On Delay	$t_{FETG:ON}$				5	µs
FETG Turn-Off Delay	$t_{FETG:OFF}$				5	µs
Binary Search Time	t_{SEARCH}	(Note 10)	5		13	BIAS Samples
ADC Round-Robin Time	t_{RR}				65	ms

ANALOG VOLTAGE MONITORING

(V_{CC} = +2.85V to +3.9V, T_A = -40°C to +95°C, unless otherwise noted.)

PARAMETER		SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ADC Resolution					13		Bits
Input/Supply Accuracy (MON1, MON2, MON3, V_{CC})		ACC	At factory setting		0.25	0.5	%FS
Update Rate for Temperature, MON1, MON2, MON3, V_{CC}		$t_{FRAME:1}$			52	70	ms
Input/Supply Offset (MON1, MON2, MON3, V_{CC})		V_{OS}	(Note 11)		0	5	LSB
Factory Setting	MON1, MON2, MON3				2.5		V
	V_{CC}		Full scales are user programmable		6.5536		

I²C AC ELECTRICAL CHARACTERISTICS

(V_{CC} = +2.85V to +3.9V, T_A = -40°C to +95°C, unless otherwise noted, see Figure 9.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SCL Clock Frequency	f_{SCL}	(Note 12)	0		400	kHz
Clock Pulse-Width Low	t_{LOW}		1.3			µs
Clock Pulse-Width High	t_{HIGH}		0.6			µs
Bus Free Time Between STOP and START Condition	t_{BUF}		1.3			µs
START Hold Time	$t_{HD:STA}$		0.6			µs
START Setup Time	$t_{SU:STA}$		0.6			µs
Data-In Hold Time	$t_{HD:DAT}$		0		0.9	µs
Data-In Setup Time	$t_{SU:DAT}$		100			ns
Rise Time of Both SDA and SCL Signals	t_R	(Note 13)	$20 + 0.1C_B$		300	ns
Fall Time of Both SDA and SCL Signals	t_F	(Note 13)	$20 + 0.1C_B$		300	ns
STOP Setup Time	$t_{SU:STO}$		0.6			µs
Capacitive Load for Each Bus Line	C_B	(Note 13)			400	pF
EEPROM Write Time	t_W	(Note 14)			20	ms

NONVOLATILE MEMORY CHARACTERISTICS

(V_{CC} = +2.85V to +3.9V, unless otherwise noted.)

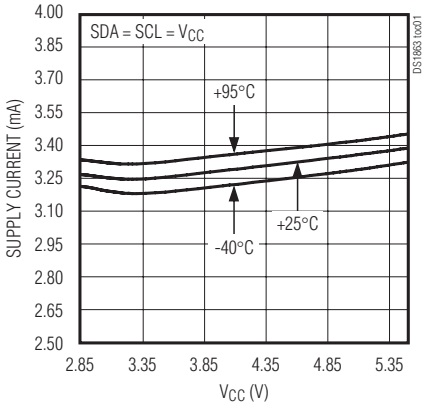
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
EEPROM Write Cycles		+70°C	50,000			

Note 1: All voltages are referenced to ground. Currents into the IC are positive and out of the IC are negative.
Note 2: Digital Inputs are at rail. FETG is disconnected SDA = SCL = 1.
Note 3: See the *Safety Shutdown (FETG) Output* section for details.
Note 4: Eight ranges allow the full-scale range to change from 625mV to 2.5V.
Note 5: This specification applies to the expected full-scale value for the selected range. See the Comp Ranging byte for available full-scale ranges.
Note 6: Eight ranges allow the full-scale range to change from 312.5mV to 1.25V.
Note 7: The output impedance of the DS1863 is proportional to its scale setting. For instance, if using the 1/2 scale, the output impedance would be 1.5kΩ.
Note 8: This specification applies to the expected full-scale value for the selected range. See the Mod Ranging byte for available full-scale ranges.
Note 9: See the *APC/Quick-Trip Sample Timing* section for details.
Note 10: Assuming an appropriate initial step is programmed that would cause the power to exceed the APC set point within 4 steps, the bias current will be within 1% within the time specified by the binary search time.
Note 11: Guaranteed by design.
Note 12: I²C interface timing shown is for fast-mode (400kHz) operation. This device is also backward-compatible with I²C standard-mode timing.
Note 13: C_B—total capacitance of one bus line in picofarads.
Note 14: EEPROM write begins after a STOP condition occurs.

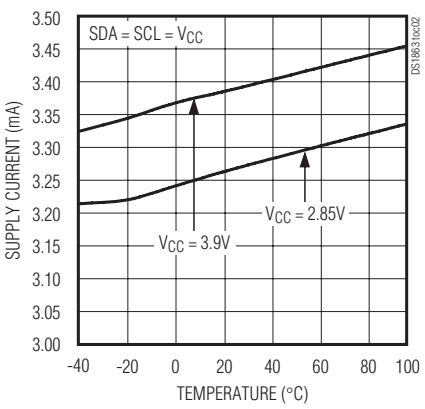
Typical Operating Characteristics

(V_{CC} = 3.3V, T_A = +25°C, unless otherwise noted.)

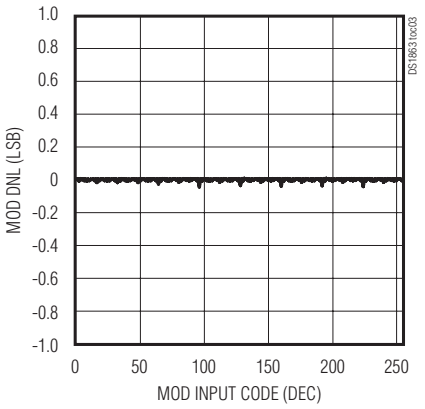
SUPPLY CURRENT vs. SUPPLY VOLTAGE



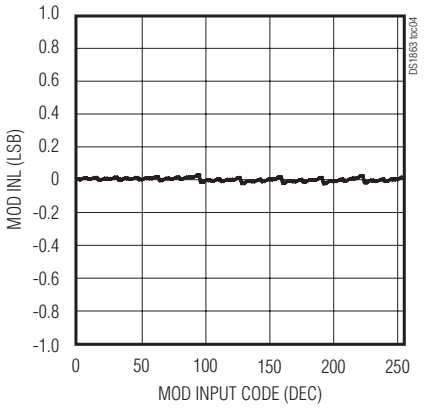
SUPPLY CURRENT vs. TEMPERATURE



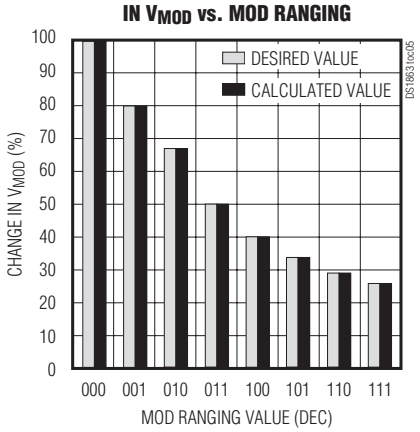
MOD DNL



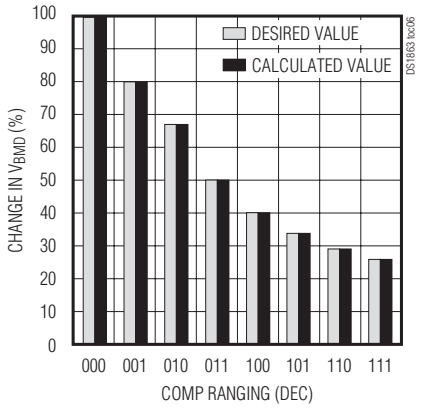
MOD INL



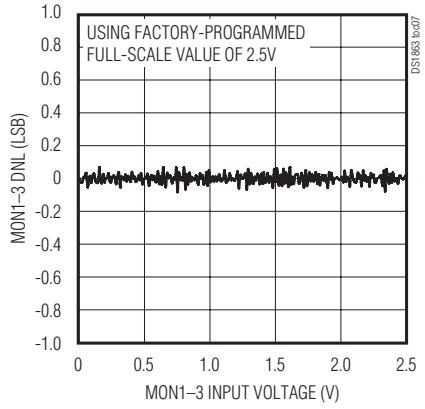
CALCULATED AND DESIRED % CHANGE IN V_{MOD} vs. MOD RANGING



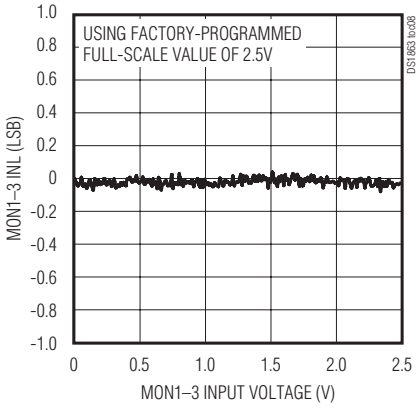
DESIRED AND CALCULATED CHANGE IN V_{BMD} vs. COMP RANGING



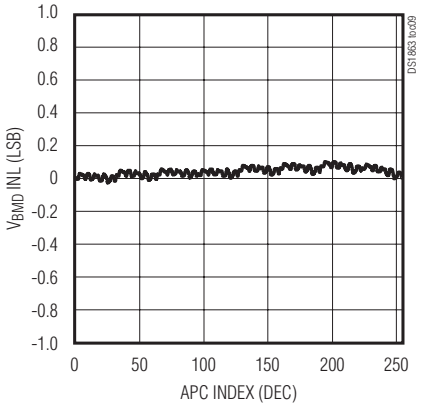
MON1–3 DNL



MON1–3 INL



V_{BMD} INL vs. APC INDEX

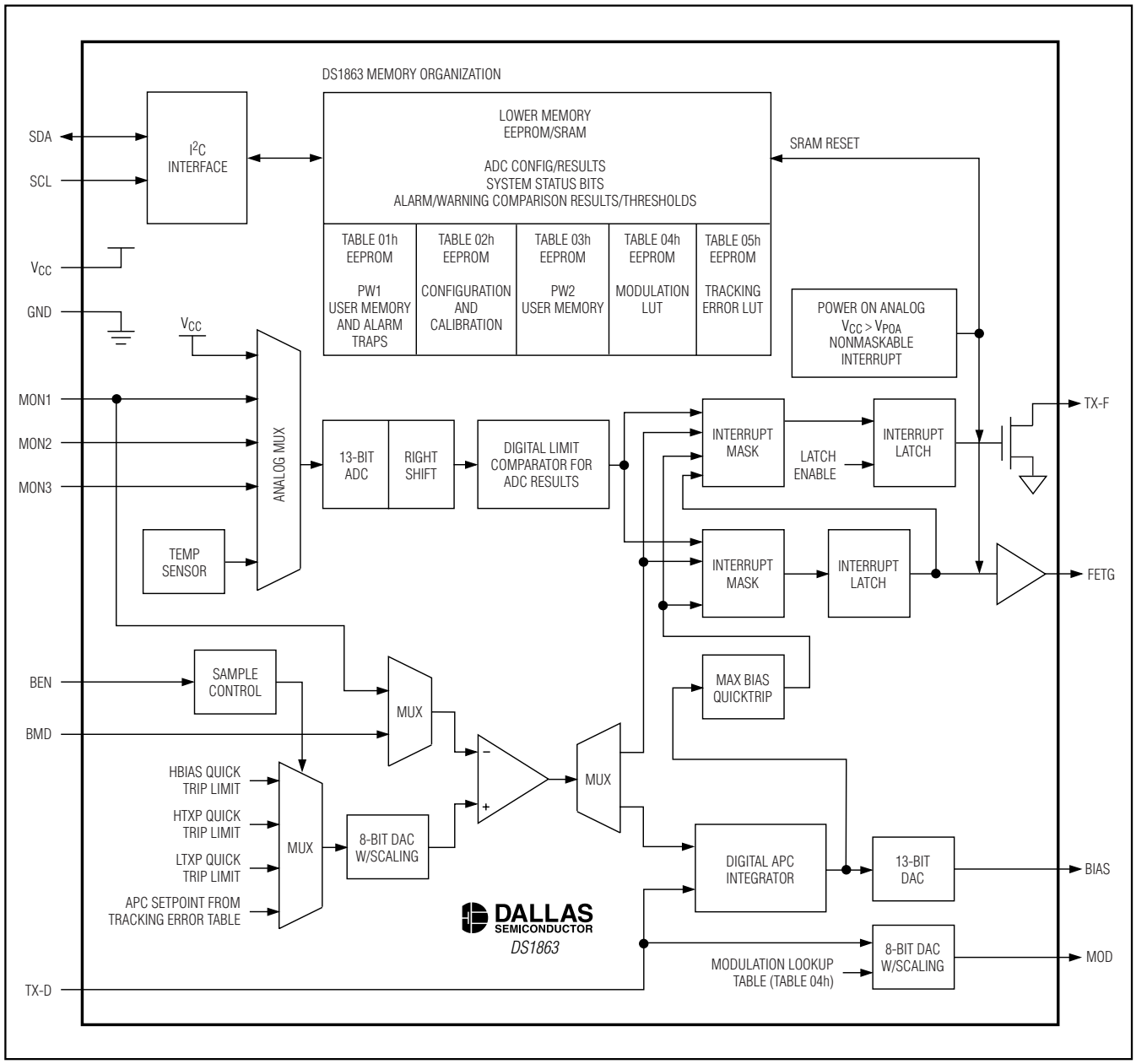


Burst-Mode PON Controller With Integrated Monitoring

Pin Description

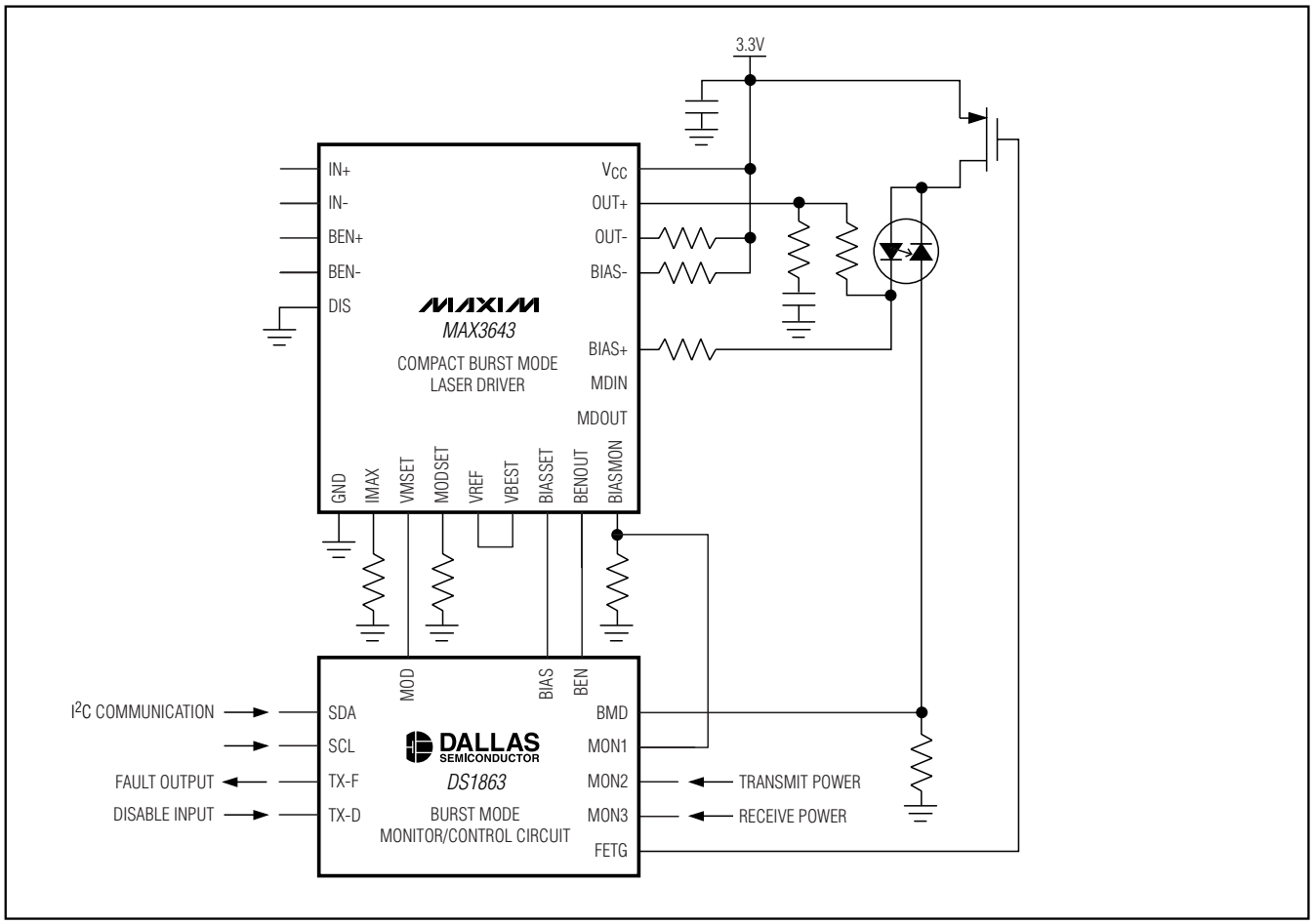
PIN	NAME	DESCRIPTION
1	BEN	Burst Enable Input. Triggers the sampling of the APC and Quick-trip monitors.
2	TX-D	Transmit Disable Input. Disables BIAS and MOD outputs.
3	N.C.	No Connection
4	TX-F	Transmit Fault Output. Open-drain.
5	FETG	Output to FET Gate. Signals an external N or P Channel MOSFET to enable/disable the laser's current.
6	SDA	I^2C Serial Data I/O
7	SCL	I^2C Serial Clock Input
8	GND	Ground
9	MON1	External Analog Inputs. The voltage at these pins is digitized by the internal analog-to-digital converter and can be read through the I^2C interface. Alarm and warning values can be assigned to interrupt the processor based on the ADC result.
10	MON2	
11	MON3	
12	GND	Ground
13	BIAS	Bias Current Output. This current DAC generates the bias current reference for the MAX3643.
14	MOD	Modulation Output Voltage. This 8-bit voltage output has 8 full-scale ranges from 1.25V to 0.3125V. This pin is connected to the MAX3643's VMSET input to control the modulation current.
15	BMD	Monitor Diode Input (Feedback Voltage, Transmit Power Monitor)
16	V_{CC}	Power Supply Input

Block Diagram



Burst-Mode PON Controller With Integrated Monitoring

Typical Operating Circuit



Detailed Description

The DS1863 integrates the control and monitoring functionality required to implement a PON system using Maxim's MAX3643 compact burst mode laser driver. The compact laser driver solution offers a considerable cost benefit by integrating control and monitoring features in low power CMOS process, while leaving only the high speed portions to the laser driver IC.

APC Control

BIAS current is controlled by an Average Power Control (APC) loop. The APC loop uses digital techniques to overcome the difficulties associated with controlling burst mode systems.

The APC loop's feedback is the monitor diode (BMD) current, which is converted to a voltage using an external resistor. The feedback voltage is compared to an 8-bit scaleable voltage reference, which determines the APC set point of the system. Scaling of the reference voltage along with the modulation output can be utilized to implement GPON power leveling.

The DS1863 has a Lookup Table to allow the APC set point to change as a function of temperature to compensate for Tracking Error (TE). The TE LUT (Table 05h), has 36 entries that determine the APC setting in 4°C windows between -40°C to +100°C.

Ranging of the APC DAC is possible by programming a single byte in Table 02h.

Modulation Control

The MOD voltage is controlled using an internal temperature indexed Lookup Table.

The MOD output is an 8-bit scaleable voltage output that interfaces with the MAX3643's VMSET input. An external resistor to ground from the MAX3643's MODSET pin sets the maximum current the voltage at VMSET input can produce for a given output range. This resistor value should be chosen to produce the maximum modulation current the laser type requires over temperature. The modulation LUT can be programmed in 2°C increments over the -40°C to +102°C range to provide temperature compensation for the laser's modulation. The modulation DAC's scaling can be used (with APC scaling) to implement GPON power leveling with a single LUT that works for all three power levels.

Ranging of the MOD DAC is possible by programming a single byte in Table 02h.

BIAS and MOD Output During Initial Power-Up

On power-up the modulation and bias outputs will remain off until V_{CC} is above V_{POA}, a temperature conversion has been completed, and if the V_{CC} LO ADC alarm is enabled, then a V_{CC} conversion above the customer defined V_{CC} low alarm level has cleared the V_{CC} low alarm. Once all of these conditions are satisfied, the MOD output will be enabled with the value determined by the temperature conversion and the modulation LUT.

When the MOD output is enabled and BEN is high, the I_{BIAS} DAC output will be turned on to a value equal to I_{STEP} (see above). The start-up algorithm checks if this bias current causes a feedback voltage above the APC set-point, and if it does not it continues increasing the I_{BIAS} by I_{STEP} until the APC set-point is exceeded. When the APC set point is exceeded, the device will begin a binary search to quickly reach the bias current corresponding to the proper power level. After the binary search is completed the APC integrator is enabled, and single LSB steps are taken to tightly control the average power.

All quick-trip and ADC alarm flags are masked until the binary search is completed. However, the BIAS MAX alarm is monitored during this time to prevent the bias output from exceeding MAX IBIAS. During the bias current initialization, the bias current is not allowed to exceed MAX IBIAS. If this occurs during the I_{STEP} sequence then the binary search routine is enabled. If MAX IBIAS is exceeded during the binary search, then the next smaller step is activated. I_{STEP} or binary increments that would cause I_{BIAS} to exceed MAX IBIAS are not taken. Many of the alarm sources are likely to trip

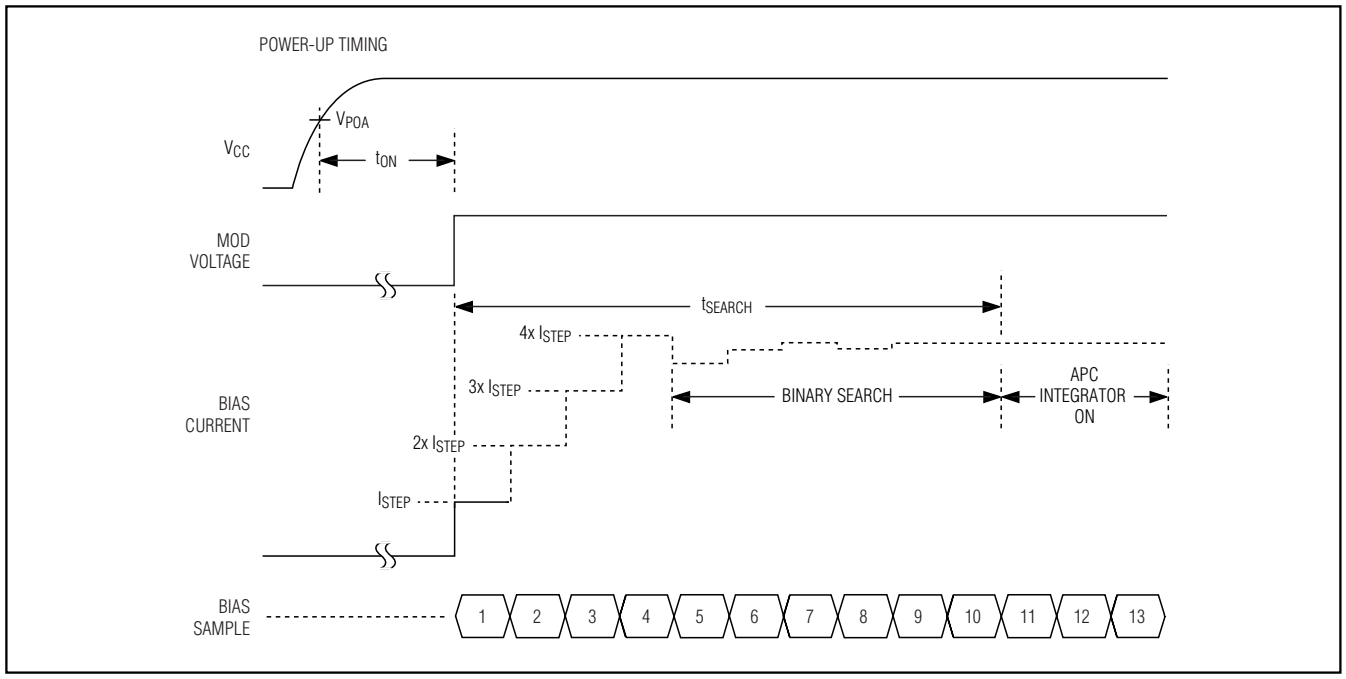


Figure 1. DS1863 Power-Up.

Burst-Mode PON Controller With Integrated Monitoring

during start-up. Masking the alarms until the completion of the binary search prevents false alarms.

I_{STEP} is programmed by the customer using the Start-up Step register. This value should be programmed to the maximum safe current increase that is allowable during start-up. If this value is programmed too low, the DS1863 will still operate, but it could take significantly longer for the algorithm to converge and hence to control the average power.

If a fault is detected, and TX-D is toggled to re-enable the outputs, the DS1863 will power up following a similar sequence to an initial power up. The only difference is that the DS1863 already has determined the present temperature, so the t_{INIT} time is not required for the DS1863 to recall the APC and MOD set points from EEPROM.

BIAS and MOD Output as a Function of Transmit Disable (TX-D)

If TX-D is asserted (logic 1) during operation, the outputs will immediately turn off (t_{OFF}). When TX-D is deasserted (logic 0), the DS1863 will turn on the MOD output with the value associated with the present temperature, and initialize the I_{BIAS} using the same search algorithm as done at start-up. Soft TX-D (Lower Memory, Register 6Eh) when asserted would allow a software control identical to the TX-D pin.

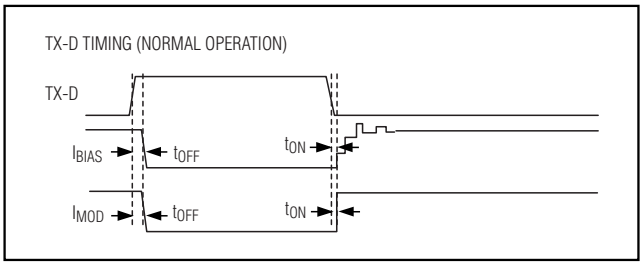


Figure 2. TX-D Timing (Output Disabled During Normal Operating Conditions).

APC/Quick-Trip Shared Comparator Timing

The DS1863's input comparator is shared between the APC control loop and the three quick-trip alarms (HTXP, LTXP and HBIAS). The comparator polls the alarms in a round-robin multiplexed sequence. Six of every eight of the comparator readings will be used for APC Loop bias current control. The other two updates will be used to check the HTXP/LTXP (Monitor Diode voltage) and the HBIAS (MON1) signals against the internal APC and BIAS reference. The HTXP/LTXP comparison will check HTXP if the last bias-update comparison was above the APC set-point, and LTXP if the last bias update comparison was below the APC set-point.

The DS1863 has a programmable comparator sample time based on an internally generated clock to facilitate a wide variety of external filtering options suitable for burst mode transmitter data rates between 155Mbits/s and 1250Mbits/s. The rising edge of burst enable (BEN) triggers the sample to occur, and the Sample Rate register determines the delay. The internal clock is asynchronous to BEN, causing a 100ns uncertainty as to when the first sample will occur following BEN. After the first sample occurs, subsequent samples will occur on a regular interval. The following sample rate options are available.

SR_3–SR_0	MINIMUM TIME FROM BEN TO FIRST SAMPLE (t_{FIRST}) ±50ns	REPEATED SAMPLE PERIOD FOLLOWING FIRST SAMPLE (t_{REP})
0000b	350ns	800ns
0001b	550ns	1200ns
0010b	750ns	1600ns
0011b	950ns	2000ns
0100b	1350ns	2800ns
0101b	1550ns	3200ns
0110b	1750ns	3600ns
0111b	2150ns	4400ns
1000b	2950ns	6000ns
1001b*	3150ns	6400ns

**All codes greater than 1001b (1010b–111b) use the maximum sample time of code 1001b.*

Comparisons of the HTXP, LTXP, and HBIAS quick-trip alarms will not occur during the burst enable low time. Any quick-trip alarm that is detected will by default remain active until a subsequent comparator sample shows the condition no longer exists.

A second bias current monitor compares the DS1863's bias current DAC's code to a digital value stored in the MAX IBIAS register. This comparison is made every bias current update to ensure that a high bias current will be quickly detected.

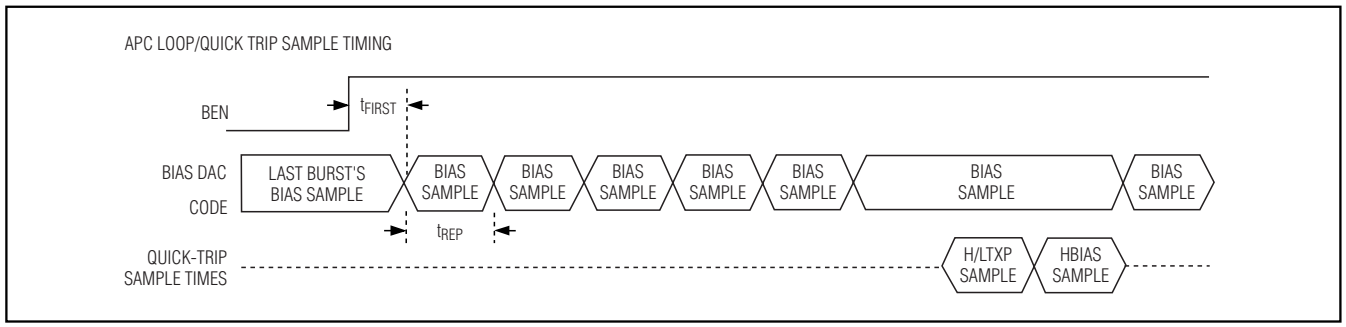


Figure 3. APC/Quick-Trip Alarm Sample Timing.

Monitors And Fault Detection

Monitors

Monitoring functions on the DS1863 include four quick-trip comparators and five ADC channels

This monitoring combined with the interrupt masks determines when/if the DS1863 shuts down its outputs and triggers the TX-F and FETG outputs. All of the monitoring levels and interrupt masks are user programmable with the exception of POA, which trips at a fixed range and is non-maskable for safety reasons.

Four Quick-Trip Monitors And Alarms

Four quick-trip monitors are provided to detect potential laser safety issues. These monitor

1) High Bias Current (HBIAS)
2) Low Transmit Power (LTXP)
3) High Transmit Power (HTXP)
4) Max Output Current (MAX IBIAS)

The high and low transmit power quick-trip registers (HTXP and LTXP) set the thresholds used to compare against the BMD voltage to determine if the transmit power is within specification. The HBIAS quick-trip compares the MON1 input (generally from the MAX3643 bias monitor output) against its threshold setting to determine if the present bias current is above specification. The Max Bias quick-trip is a digital comparison that determines if the Bias Output code indicates the bias current is above specification. The bias current will not be allowed to exceed the value set in this register. When the DS1863 detects the bias is at the limit it will set the BIAS MAX status bit and hold the bias current at the MAX IBIAS level. The quick-trips are routed to the TX-F and FETG outputs via interrupt masks to allow combinations of these alarms to be used to trigger these outputs. Any time FETG is triggered the DS1863 will also disable its outputs. All the quick-trip alarm levels and masks are programmable through the I^2C interface.

Five ADC Monitors And Alarms

The ADC monitors five channels that measure temperature (internal temp sensor), V_{CC}, MON1, MON2, and MON3 using an analog multiplexer to measure them round robin with a single ADC. Each channel has a customer programmable full scale range and offset value that will be factory programmed to default value (see below). Additionally, MON1, MON2, and MON3 have the ability to right shift results by up to 7 bits before the results are compared to alarm thresholds or read over the I^2C bus. This allows customers with specified ADC ranges to calibrate the ADC full scale to a factor of $1/2^n$ of their specified range to measure small signals. The DS1863 can then right shift the results by n bits to maintain the bit weight of their specification.

ADC Default Monitor Full Scale Ranges

SIGNAL (UNITS)	+ FS SIGNAL	+ FS HEX	- FS SIGNAL	- FS HEX
Temperature (°C)	127.996	7FFF	-128	8000
V_{CC} (V)	6.5528	FFF8	0V	0000
MON1, MON2, MON3 (V)	2.4997	FFF8	0V	0000

The ADC results (after right shifting, if used) are compared to high alarm thresholds (to check if the results exceeded this threshold), the low alarm thresholds (to check if the ADC results are below this threshold) and the warning threshold after each conversion (20 comparisons total), and the corresponding alarms are set which can be used to trigger the TX-F or FETG outputs. These ADC thresholds are user programmable via the I^2C interface, as are the masking registers that can be

used to prevent the alarms from triggering the TX-F and FETG outputs. See below for more detail on the TX-F and FETG outputs.

ADC Timing

There are five analog channels that are digitized in a round robin fashion in the order shown in Figure 4. The total time required to convert all five channels is t_{RR} (see electrical specifications for details).

Right Shifting A/D Conversion Result

If the weighting of the ADC digital reading must conform to a Predetermined Full-Scale (PFS) value defined by a specification, then right shifting can be used to adjust the PFS analog measurement range while maintaining the weighting of the ADC results. The DS1863's range is wide enough to cover all requirements; when maximum input value is far short of the FS value, right shifting can be used to obtain greater accuracy. For instance, the maximum voltage might be 1/8 of the specified PFS value, so only 1/8 of the converter's range is effective over this range. An alternative is to calibrate the ADC's full scale range to 1/8 the readable PFS value and use a right-shift value of 3. With this implementation, the resolution of the measurement has increased by a factor of 8, and because the result is digitally divided by 8 by right shifting, the bit weight of the measurement still meets the standard.

The right shift operation on the A/D converter results is carried out based on the contents of Right Shift Control Registers (Table 02h Registers 8Eh to 8Fh) in EEPROM. Three analog channels: MON1 to MON3 each have 3 bits allocated to set the number of right shifts. Up to 7 right shift operations are allowed and will be executed as a part of every conversion before the results are compared to the high and low alarm levels, or loaded into their corresponding measurement registers 62h to 69h. This is true during the setup of internal calibration as well as during subsequent data conversions.

Transmit Fault (TX-F) Output

The TX-F output has masking registers for the five ADC alarms and the four QT alarms to select which comparisons cause it to assert. In addition, the FETG alarm is selectable via the TX-F mask to cause TX-F to assert. All alarms, with the exception of FETG, will only cause TX-F to remain active while the alarm condition persists. However, the TX-F latch bit can enable the TX-F output to remain active until it is cleared by the TX-F reset bit, TX-D, soft TX-D, or by power cycling the part. If the FETG output is configured to trigger TX-F, then it is indicating that the DS1863 is in shutdown, and will require TX-D, soft TX-D, or cycling power to reset. The ADC and Quick-trip alarms (with the exception of BIAS MAX) are ignored for the first 8-10 bias current updates during power up. Only enabled alarms will activate TX-F.

The following table shows TX-F as a function of TX-D and the alarm sources.

TX-F as a Function of TX-D and Alarm Sources

$V_{CC} > V_{POA}$	TX-D	NON-MASKED TX-F ALARM	TX-F
No	X	X	1
Yes	0	0	0
Yes	0	1	1
Yes	1	X	0

Safety Shutdown (FETG) Output

The FETG output has masking registers (separate from TX-F) for the five ADC alarms and the four QT alarms to select which comparisons cause it to assert. Unlike TX-F,

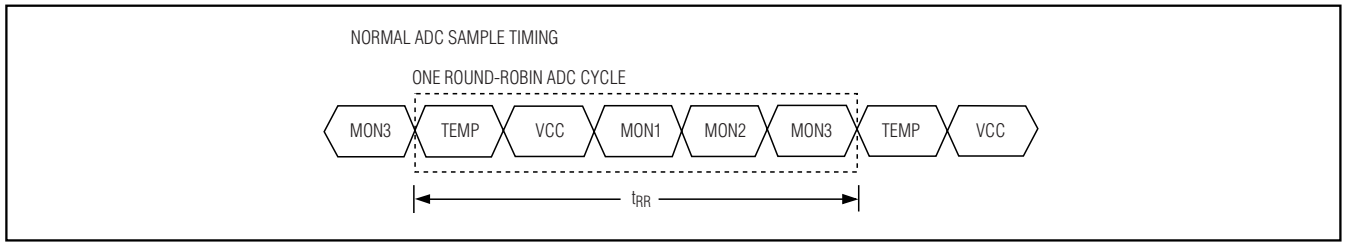


Figure 4. ADC Round-Robin Timing.

If V_{CC} low alarm is set for either the TX-F or FETG output, the Round Robin timing will cycle between only TEMP and V_{CC}.

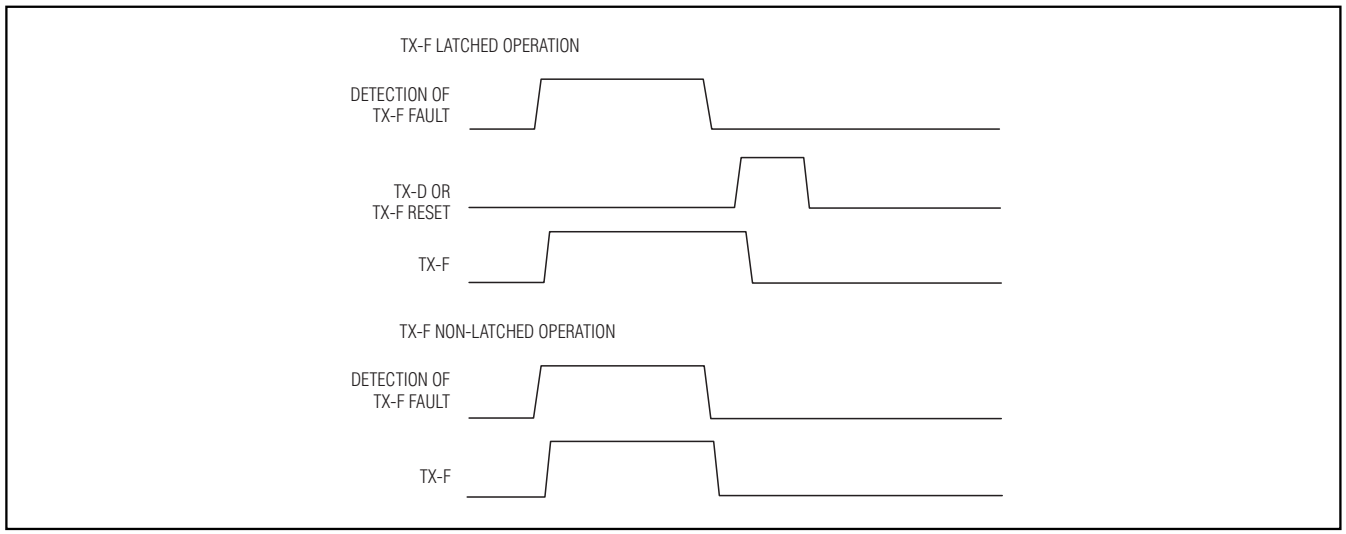


Figure 5. DS1863 TX-F Timing.

FETG output is always latched in case it is triggered by an unmasked alarm condition. Its output polarity is programmable to allow an external N or P MOSFET to open during alarms to shut off the laser diode current. If the FETG output triggers indicating the DS1863 is in shutdown, then it requires TX-D, soft TX-D, or cycling power to be reset. Under all conditions when the analog outputs are re-initialized after being disabled, all the alarms with the exception of the V_{CC} low ADC alarm will be cleared. The V_{CC} low alarm must remain active to prevent the output from attempting to operate when inadequate V_{CC} exists to operate the laser driver. Once adequate V_{CC} is present to clear the V_{CC} low alarm, the outputs will be enabled following the same sequence as power up.

As mentioned before the FETG is an output used to disable the laser current via a series N or P MOSFET. This requires that the FETG output is capable of sinking or sourcing current. Because the DS1863 will not know if it should sink or source current before V_{CC} exceeds V_{POA}, which triggers the EE recall, this output will be high impedance when V_{CC} is below V_{POA}. (see "Low Voltage Operation" section for details and diagram). The application circuit must use a pull-up or pull-down resistor on this pin that pulls FETG to the alarm/shutdown state (high for a PMOS, low for a NMOS). Once V_{CC} is above V_{POA}, the DS1863 will pull the FETG output to the state determined by the FETG DIR bit (Table 02h, Register 89h). FETG DIR will be 0 if an NMOS is used and 1 if a PMOS is used.

FETG and MOD and BIAS Outputs as a Function of TX-D and Alarm Sources

$V_{CC} > V_{POA}$	TX-D	NON-MASKED FETG ALARM	FETG	MOD AND BIAS OUTPUTS
Yes	0	0	FETG DIR	Enabled
Yes	0	1	FETG DIR	Disabled
Yes	1	X	FETG DIR	Disabled

Determining Alarm Causes Using The I²C Interface

To determine the cause of the TX-F or FETG alarm, the system processor can read the DS1863's Alarm Trap Bytes (ATB) through the I^2C interface (in Table 01h). The ATB have a bit for each alarm. Any time an alarm occurs, regardless of the mask bit's state, the DS1863 sets the corresponding bit in the ATB. Active ATB bits will remain set until written to zeros via the I^2C interface. On power up the ATB will be zeros until alarms dictate otherwise.

Die Identification

DS1863 will have an ID hard coded to its die. Two registers (Table 02h bytes 86h–87h) are assigned for this feature. Byte 86h will read 63h to identify the part as the DS1863, byte 87h will read to A1h (for A1 die revision).

Low-Voltage Operation

The DS1863 contains two Power-On Reset (POR) levels. The lower level is a Digital POR (V_{POD}) and the

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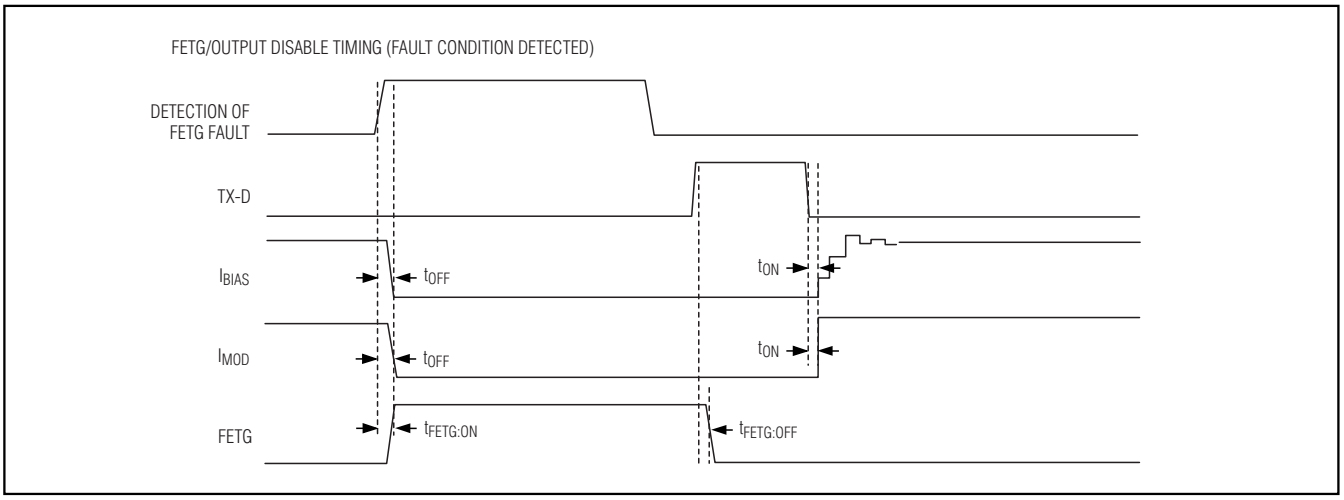

Figure 6. FETG/Modulation and Bias Timing (Fault Condition Detected).

higher level is an Analog POR (V_{POA}). At start up, before the supply voltage rises above V_{POA}, the outputs are disabled (FETG and BIAS outputs are high impedance, MOD is low), all SRAM outputs are low (including Shadowed EEPROM), and all analog circuitry is disabled. When V_{CC} reaches V_{POA}, the SEE is recalled, and the analog circuitry is enabled. While V_{CC} remains above V_{POA}, the device is in its normal operating state, and it responds based on its nonvolatile configuration. If during operation V_{CC} falls below V_{POA}, but is still above V_{POD}, then the SRAM will retain the SEE settings from the first SEE recall, but the device analog will be shut down and the outputs disabled. FETG will be driven to its alarm state defined by the FETG DIR bit (Table 02h, Register 89h). If the supply voltage recovers back above V_{POA}, then the device will immediately resume normal functioning. If the supply voltage falls below V_{POD}, then the device SRAM will be placed in its default state and another SEE recall will be required to reload the nonvolatile settings. The EEPROM recall will occur the next time V_{CC} next exceeds V_{POA}. Figure 7 shows the sequence of events as the voltage varies.

Any time V_{CC} is above V_{POD}, the I^2C interface can be used to determine if V_{CC} is below the V_{POA} level. This is accomplished by checking the RDYB bit in the Status (6Eh) byte. RDYB is set when V_{CC} is below V_{POA}; when V_{CC} rises above V_{POA} RDYB is timed (within 500µs) to go to 0, at which point the part is fully functional.

For all Device Addresses sourced from EEPROM (Byte 8Ch, Table 01h in memory) the default Device Address is A2h until V_{CC} exceeds V_{POA} allowing the device address to be recalled from the EEPROM.

Power-On Analog (POA)

POA holds the DS1863 in reset until V_{CC} is at a suitable level ($V_{CC} > V_{POA}$) for the part to accurately measure with its ADC and compare analog signals with its quick-trip monitors. Because V_{CC} cannot be measured by the ADC when V_{CC} is less than V_{POA}, POA also asserts the V_{CC} low alarm, which must be cleared by a V_{CC} ADC conversion that is greater than the customer programmable V_{CC} low ADC limit. This prevents the TX-F and FETG outputs from glitching during a slow power up. The TX-F and FETG output will not latch until there is a conversion above V_{CC} low limit.

The POA alarm is non-maskable. The TX-F, and FETG outputs shuts off any time V_{CC} is below V_{POA}. See *Low Voltage Operation* section for more information.

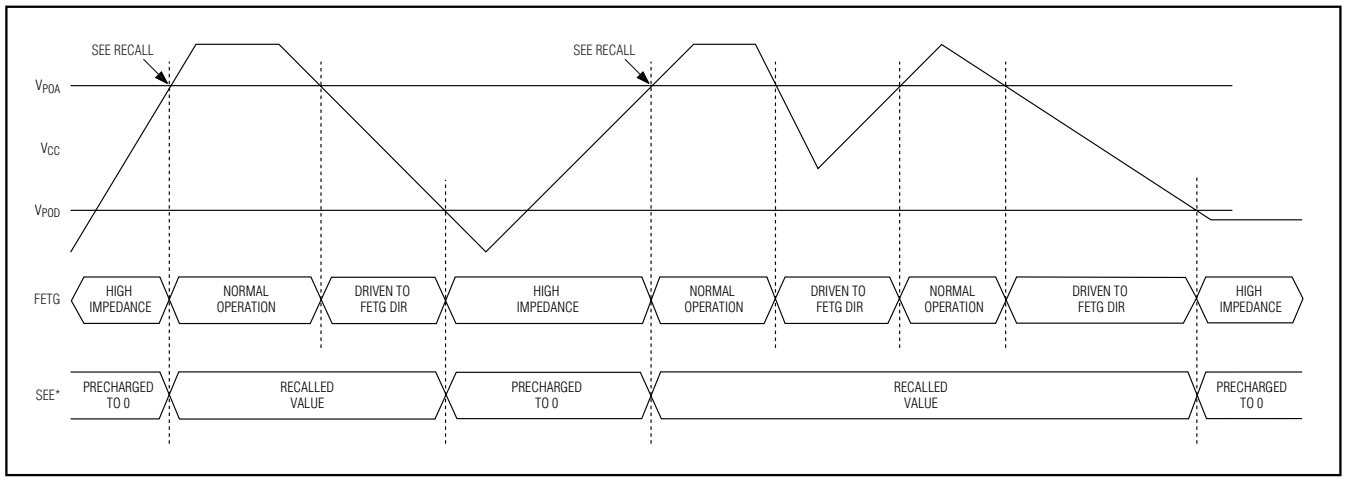

Figure 7. DS1863 Digital and Analog Power-On Reset.

DS1863 Memory Map

Memory Organization

The DS1863 features six memory banks that include the following.

The **Lower Memory** is addressed from 00h to 7Fh and contains alarm and warning thresholds, flags, masks, several control registers, password entry area (PWE), and the Table Select byte. The Table Select Byte determines which Table (01h–05h) will be mapped into the upper memory locations.

Table 01h primarily contains user EEPROM (with PW1 level access) as well as some Alarm and Warning status bytes.

Table 02h is a multifunction space that contains Configuration registers, scaling and offset values, Passwords, interrupt registers as well as other miscellaneous control bytes.

Table 03h is strictly user EEPROM that is protected by a PW2 level password.

Table 04h contains a temperature indexed Look up Table (LUT) for control of the modulation voltage. The modulation LUT can be programmed in 2°C increments over the -40°C to +102°C range. Access to this register is protected by a PW2 level password.

Table 05h contains another LUT which allows the APC set point to change as a function of temperature to compensate for Tracking Error (TE). This TE LUT, has 36 entries that determine the APC setting in 4°C windows between -40°C to 100°C. Access to this register is protected by a PW2 level password.

Complete detail of each byte's function, as well as Read/Write permissions for each Byte for each table is provided in the *Register Descriptions* sections.

Shadowed EEPROM

Many nonvolatile (NV) memory locations (listed within the *Detailed Register Description* section) are actually Shadowed-EEPROM which are controlled by the SEEB bit in Table 02h, Byte 80h.

The DS1863 incorporates Shadowed EEPROM memory locations for key memory addresses that may be rewritten many times. By default the Shadowed EEPROM Bit, SEEB, is not set and these locations act as ordinary EEPROM. By setting SEEB these locations function like SRAM cells, which allow an infinite number of write cycles without concern of wearing out the EEPROM. This also eliminates the requirement for the EEPROM write time, t_{WR}. Because changes made with SEEB enabled do not affect the EEPROM, these changes are not retained through power cycles. The power-up value is the last value written with SEEB disabled. This function can be used to limit the number of EEPROM writes during calibration or to change the monitor thresholds periodically during normal operation helping to reduce the number of times EEPROM is written. The Memory Map description indicates which locations are shadowed-EEPROM.

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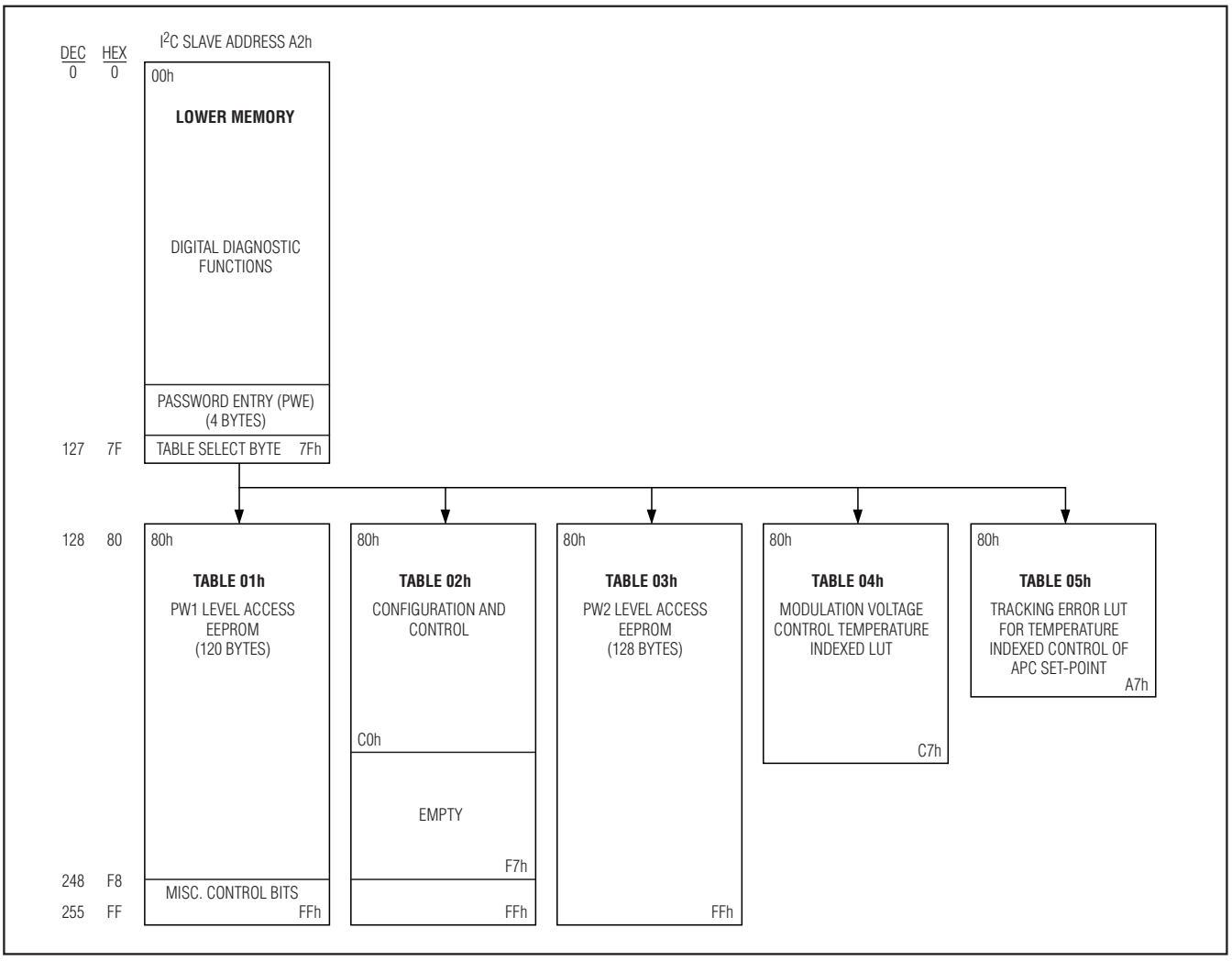

Figure 8. DS1863 Memory Map.

I²C Definitions

Master Device: The master device controls the slave devices on the bus. The master device generates SCL clock pulses, START and STOP conditions.

Slave Devices: Slave devices send and receive data at the master's request.

Bus Idle or Not Busy: Time between STOP and START conditions when both SDA and SCL are inactive and in their logic-high states. When the bus is idle it often initiates a low-power mode for slave devices.

START Condition: A START condition is generated by the master to initiate a new data transfer with a slave. Transitioning SDA from high to low while SCL remains high generates a START condition. See the timing diagram for applicable timing.

STOP Condition: A STOP condition is generated by the master to end a data transfer with a slave. Transitioning SDA from low to high while SCL remains high generates a STOP condition. See the timing diagram for applicable timing.

Repeated START Condition: The master can use a repeated START condition at the end of one data transfer to indicate that it will immediately initiate a new data transfer following the current one. Repeated STARTS are commonly used during read operations to identify a

specific memory address to begin a data transfer. A repeated START condition is issued identically to a normal START condition. See the timing diagram for applicable timing.

Bit Write: Transitions of SDA must occur during the low state of SCL. The data on SDA must remain valid and unchanged during the entire high pulse of SCL plus the setup and hold-time requirements (Figure 9). Data is shifted into the device during the rising edge of the SCL.

Bit Read: At the end of a write operation, the master must release the SDA bus line for the proper amount of setup time before the next rising edge of SCL during a bit read. The device shifts out each bit of data on SDA at the falling edge of the previous SCL pulse and the data bit is valid at the rising edge of the current SCL pulse. Remember that the master generates all SCL clock pulses including when it is reading bits from the slave.

Acknowledgement (ACK and NACK): An Acknowledgement (ACK) or Not Acknowledge (NACK) is always the 9th bit transmitted during a byte transfer. The device receiving data (the master during a read or the slave during a write operation) performs an ACK by transmitting a zero during the 9th bit. A device performs a NACK by transmitting a one during the 9th bit. Timing for the ACK and NACK is identical to all other bit writes. An ACK is the acknowledgment that the device is properly receiving data. A NACK is used to terminate a read sequence or as an indication that the device is not receiving data.

Byte Write: A byte write consists of 8 bits of information transferred from the master to the slave (most significant bit first) plus a 1-bit acknowledgement from the slave to the master. The 8 bits transmitted by the master are done according to the bit write definition and the acknowledgement is read using the bit read definition.

Byte Read: A byte read is an 8-bit information transfer from the slave to the master plus a 1-bit ACK or NACK from the master to the slave. The 8 bits of information that are transferred (most significant bit first) from the slave to the master are read by the master using the bit read definition, and the master transmits an ACK using the bit write definition to receive additional data bytes. The master must NACK the last byte read to terminate communication so the slave will return control of SDA to the master.

Slave Address Byte: Each slave on the I^2C bus responds to a slave addressing byte (Figure 10) sent immediately following a START condition. The slave address byte contains the slave address in the most significant 7 bits and the R/$\overline{W}$ bit in the least significant bit.

The DS1863's slave address can be configured to any value between 00h to FEh using the Device Address Byte (Table 02h, Register 8Ch). The user also has to set the ASEL bit (Table 02h, Register 89h) for this address to be active. The default address is A2h (see Figure 10). By writing the correct slave address with R/$\overline{W}$ = 0, the master indicates it will write data to the slave. If R/$\overline{W}$ = 1, the master will read data from the slave. If an incorrect slave address is written, the DS1863 will assume the master is communicating with another I^2C device and ignore the communications until the next START condition is sent.

Memory Address: During an I^2C write operation, the master must transmit a memory address to identify the memory location where the slave is to store the data. The memory address is always the second byte transmitted during a write operation following the slave address byte.

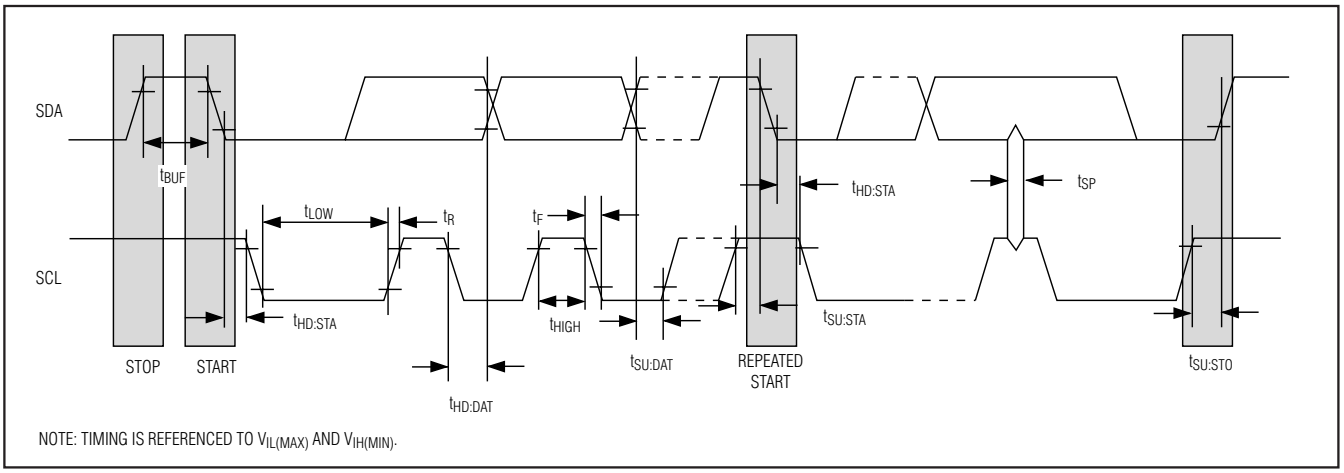

Figure 9. I^2C Timing Diagram.

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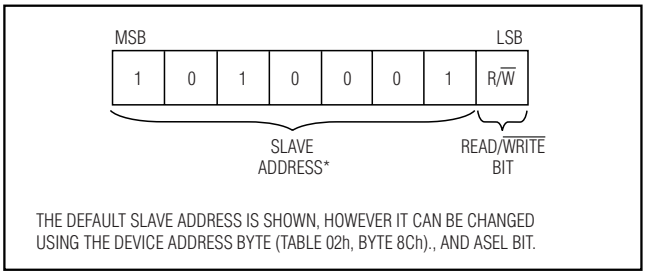

Figure 10. DS1863 Slave Address Byte (Default)

I²C Communication

Writing a Single Byte to a Slave: The master must generate a START condition, write the slave address byte (R/$\overline{W}$ = 0), write the byte of data, and generate a STOP condition. The master must read the slave's acknowledgement during all byte write operations.

Writing Multiple Bytes to a Slave: To write multiple bytes to a slave, the master generates a start condition, writes the slave address byte (R/$\overline{W}$ = 0), writes the memory address, writes up to 8 data bytes, and generates a stop condition. The DS1863 writes 1 to 8 bytes (1 page or row) with a single write transaction. This is internally controlled by an address counter that allows data to be written to consecutive addresses without transmitting a memory address before each data byte is sent. The address counter limits the write to one 8-byte page (one row of the memory map). Attempts to write to additional pages of memory without sending a stop condition between pages results in the address counter wrapping around to the beginning of the present row.

Example: A 3-byte write starts at address 06h and writes three data bytes (11h, 22h, and 33h) to three "consecutive" addresses. The result is that addresses 06h and 07h would contain 11h and 22h, respectively, and the third data byte, 33h, would be written to address 00h.

To prevent address wrapping from occurring, the master must send a stop condition at the end of the page, then wait for the bus-free or EEPROM-write time to elapse. Then the master can generate a new start condition, and write the slave address byte (R/$\overline{W}$ = 0) and the first memory address of the next memory row before continuing to write data.

Acknowledge Polling: Any time an EEPROM location is written, the DS1863 requires the EEPROM write time (t_W) after the STOP condition to write the contents of the byte of data to EEPROM. During the EEPROM write time, the device will not acknowledge its slave address because it is busy. It is possible to take advantage of that phenomenon by repeatedly addressing the DS1863, which allows the next page to be written as soon as the DS1863 is ready to receive the data. The alternative to acknowledge polling is to wait for a maximum period of t_W to elapse before attempting to write again to the device.

EEPROM Write Cycles: When EEPROM writes occur to the memory, the DS1863 will write to all three EEPROM memory locations, even if only a single byte was modified. Because all three bytes are written, the bytes that were not modified during the write transaction are still subject to a write cycle. This can result in all three bytes being worn out over time by writing a single byte repeatedly. The DS1863's EEPROM write cycles are specified in the *NV Memory Characteristics* table. The specification shown is at the worst-case temperature. If zero-crossing detection is enabled, EEPROM write cycles cannot begin until after the zero-crossing detection is complete.

Reading a Single Byte from a Slave: To read a single byte from the slave, the master generates a START condition, writes the slave address byte with R/$\overline{W}$ = 1, reads the data byte with a NACK to indicate the end of the transfer, and generates a STOP condition. When a single byte is read, it will always be the Potentiometer 0 value.

Reading Multiple Bytes from a Slave: The read operation can be used to read multiple bytes with a single transfer. When reading bytes from the slave, the master simply ACKs the data byte if it desires to read another byte before terminating the transaction. After the master reads the last byte, it NACKs to indicate the end of the transfer and generates a STOP condition. The first byte read will be the Potentiometer 0 Wiper Setting. The next byte will be the Potentiometer 1 Wiper Setting. The third byte is the Configuration Register byte. If an ACK is issued by the master following the Configuration Register byte, then the DS1863 will send the Potentiometer 0 Wiper Setting again. This round robin reading will occur as long as each byte read is followed by an ACK from the master.

Lower Memory Register Map

This register map shows each byte/word in terms of the row it is on in the memory. The first byte in the row is located in memory at the row address (hexadecimal) in the left most column. Each subsequent byte on the row is one/ two memory locations beyond the previous byte/word's address. A total of eight bytes are present on each row. For more information about each of these bytes see the corresponding register description.

LOWER MEMORY									
ROW (HEX)	ROW NAME	WORD 0		WORD 1		WORD 2		WORD 3	
		BYTE 0/8	BYTE 1/9	BYTE 2/A	BYTE 3/B	BYTE 4/C	BYTE 5/D	BYTE 6/E	BYTE 7/F
00	<1>THRESHOLD$_0$	TEMP ALARM HI		TEMP ALARM LO		TEMP WARN HI		TEMP WARN LO	
08	<1>THRESHOLD$_1$	V_{CC} ALARM HI		V_{CC} ALARM LO		V_{CC} WARN HI		V_{CC} WARN LO	
10	<1>THRESHOLD$_2$	MON1 ALARM HI		MON1 ALARM LO		MON1 WARN HI		MON1 WARN LO	
18	<1>THRESHOLD$_3$	MON2 ALARM HI		MON2 ALARM LO		MON2 WARN HI		MON2 WARN LO	
20	<1>THRESHOLD$_4$	MON3 ALARM HI		MON3 ALARM LO		MON3 WARN HI		MON3 WARN LO	
28	<1>SHADOWED EE	SEE	SEE	SEE	SEE	SEE	SEE	SEE	SEE
30	<1>PW2 EE	EE	EE	EE	EE	EE	EE	EE	EE
38	<1>PW2 EE	EE	EE	EE	EE	EE	EE	EE	EE
40	<1>PW2 EE	EE	EE	EE	EE	EE	EE	EE	EE
48	<1>PW2 EE	EE	EE	EE	EE	EE	EE	EE	EE
50	<1>PW2 EE	EE	EE	EE	EE	EE	EE	EE	EE
58	<1>PW2 EE	EE	EE	EE	EE	EE	EE	EE	EE
60	<2>ADC VALUES$_0$	TEMP VALUE		V_{CC} VALUE		MON1 VALUE		MON2 VALUE	
68	<0> ADC VALUES$_1$	<2>MON3 VALUE		<2>RESERVED		<2>RESERVED		<0>STATUS	<3>UPDATE
70	<2>ALARM/WARN	ALARM$_3$	ALARM$_2$	ALARM$_1$	ALARM$_0$	WARN$_3$	WARN$_2$	RESERVED	
78	<0>TABLE SELECT	<6>RESERVED	<6>RESERVED	<6>RESERVED	<6>PWE MSB		<6>PWE LSB		<5>TBL SEL

Access Code	<0>	<1>	<2>	<3>	<4>	<5>	<6>	<7>	<8>	<9>	<10>	<11>
Read Access	See each bit/byte separately	All	All	All	PW2	All	N/A	PW1	PW2	N/A	PW2	All
Write Access		PW2	N/A	All and DS1863 Hardware	PW2 + mode bit	All	All	PW1	PW2	PW2	N/A	PW1

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Table 01h. Register Map

TABLE 01h (PW1)									
ROW (HEX)	ROW NAME	WORD 0		WORD 1		WORD 2		WORD 3	
		BYTE 0/8	BYTE 1/9	BYTE 2/A	BYTE 3/B	BYTE 4/C	BYTE 5/D	BYTE 6/E	BYTE 7/F
80	<7>PW1 EE	EE	EE	EE	EE	EE	EE	EE	EE
88	<7>PW1 EE	EE	EE	EE	EE	EE	EE	EE	EE
90	<7>PW1 EE	EE	EE	EE	EE	EE	EE	EE	EE
98	<7>PW1 EE	EE	EE	EE	EE	EE	EE	EE	EE
A0	<7>PW1 EE	EE	EE	EE	EE	EE	EE	EE	EE
A8	<7>PW1 EE	EE	EE	EE	EE	EE	EE	EE	EE
B0	<7>PW1 EE	EE	EE	EE	EE	EE	EE	EE	EE
B8	<7>PW1 EE	EE	EE	EE	EE	EE	EE	EE	EE
C0	<7>PW1 EE	EE	EE	EE	EE	EE	EE	EE	EE
C8	<7>PW1 EE	EE	EE	EE	EE	EE	EE	EE	EE
D0	<7>PW1 EE	EE	EE	EE	EE	EE	EE	EE	EE
D8	<7>PW1 EE	EE	EE	EE	EE	EE	EE	EE	EE
E0	<7>PW1 EE	EE	EE	EE	EE	EE	EE	EE	EE
E8	<7>PW1 EE	EE	EE	EE	EE	EE	EE	EE	EE
F0	<7>PW1 EE	EE	EE	EE	EE	EE	EE	EE	EE
F8	<11>ALARM TRAP	$ALARM_3$	$ALARM_2$	$ALARM_1$	$ALARM_0$	$WARN_3$	$WARN_2$	RESERVED	

Access Code	<0>	<1>	<2>	<3>	<4>	<5>	<6>	<7>	<8>	<9>	<10>	<11>
Read Access	See each bit/byte separately	All	All	All	PW2	All	N/A	PW1	PW2	N/A	PW2	All
Write Access		PW2	N/A	All and DS1863 Hardware	PW2 + mode bit	All	All	PW1	PW2	PW2	N/A	PW1

Table 02h. Register Map

TABLE 02h (PW2)									
ROW (HEX)	ROW NAME	WORD 0		WORD 1		WORD 2		WORD 3	
		BYTE 0/8	BYTE 1/9	BYTE 2/A	BYTE 3/B	BYTE 4/C	BYTE 5/D	BYTE 6/E	BYTE 7/F
80	<0>$CONFIG_0$	<8>MODE	<4>TINDEX	<4>MOD DAC	<4>APC DAC	<4>$BIAS\ DAC_2$	<4>$BIAS\ DAC_2$	<10>DEVICE ID	<10>DEVICE VER
88	<8>$CONFIG_1$	UPDATE RATE	CONFIG	START-UP STEP	MOD RANGING	DEVICE ADDRESS	COMP RANGING	$RSHIFT_1$	$RSHIFT_0$
90	<8>$SCALE_0$	RESERVED		V_{CC} SCALE		MON1 SCALE		MON2 SCALE	
98	<8>$SCALE_1$	MON3 SCALE		RESERVED		RESERVED		RESERVED	
A0	<8>$OFFSET_0$	RESERVED		V_{CC} OFFSET		MON1 OFFSET		MON2 OFFSET	
A8	<8>$OFFSET_1$	MON3 OFFSET		RESERVED		RESERVED		INTERNAL TEMP OFFSET*	
B0	<9>PWD VALUE	PW1 MSB		PW1 LSB		PW2 MSB		PW2 LSB	
B8	<8>INTERRUPT	FETG EN_1	FETG EN_0	TX-F EN_1	TX-F EN_0	HTXP	LTXP	HBIAS	MAX IBIAS
C0-F7	EMPTY	EMPTY	EMPTY	EMPTY	EMPTY	EMPTY	EMPTY	EMPTY	EMPTY
F8	<4>MAN IBIAS	MAN $IBIAS_0$	MAN $IBIAS_1$	MAN_CNTL	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED

**The Final Result must be XOR'ed with BB40h before writing to this register.*

Access Code	<0>	<1>	<2>	<3>	<4>	<5>	<6>	<7>	<8>	<9>	<10>	<11>
Read Access	See each bit/byte separately	All	All	All	PW2	All	N/A	PW1	PW2	N/A	PW2	All
Write Access		PW2	N/A	All and DS1863 Hardware	PW2 + mode bit	All	All	PW1	PW2	PW2	N/A	PW1

Table 03h. Register Map

TABLE 03h (PW2)									
ROW (HEX)	ROW NAME	WORD 0		WORD 1		WORD 2		WORD 3	
		BYTE 0/8	BYTE 1/9	BYTE 2/A	BYTE 3/B	BYTE 4/C	BYTE 5/D	BYTE 6/E	BYTE 7/F
80	<8>PW2 EE	EE	EE	EE	EE	EE	EE	EE	EE
88	<8>PW2 EE	EE	EE	EE	EE	EE	EE	EE	EE
90	<8>PW2 EE	EE	EE	EE	EE	EE	EE	EE	EE
98	<8>PW2 EE	EE	EE	EE	EE	EE	EE	EE	EE
A0	<8>PW2 EE	EE	EE	EE	EE	EE	EE	EE	EE
A8	<8>PW2 EE	EE	EE	EE	EE	EE	EE	EE	EE
B0	<8>PW2 EE	EE	EE	EE	EE	EE	EE	EE	EE
B8	<8>PW2 EE	EE	EE	EE	EE	EE	EE	EE	EE
C0	<8>PW2 EE	EE	EE	EE	EE	EE	EE	EE	EE
C8	<8>PW2 EE	EE	EE	EE	EE	EE	EE	EE	EE
D0	<8>PW2 EE	EE	EE	EE	EE	EE	EE	EE	EE
D8	<8>PW2 EE	EE	EE	EE	EE	EE	EE	EE	EE
E0	<8>PW2 EE	EE	EE	EE	EE	EE	EE	EE	EE
E8	<8>PW2 EE	EE	EE	EE	EE	EE	EE	EE	EE
F0	<8>PW2 EE	EE	EE	EE	EE	EE	EE	EE	EE
F8	<8>PW2 EE	EE	EE	EE	EE	EE	EE	EE	EE

Access Code	<0>	<1>	<2>	<3>	<4>	<5>	<6>	<7>	<8>	<9>	<10>	<11>
Read Access	See each bit/byte separately	All	All	All	PW2	All	N/A	PW1	PW2	N/A	PW2	All
Write Access		PW2	N/A	All and DS1863 Hardware	PW2 + mode bit	All	All	PW1	PW2	PW2	N/A	PW1

Table 04h. Register Map

TABLE 04h (LUT FOR MOD)									
ROW (HEX)	ROW NAME	WORD 0		WORD 1		WORD 2		WORD 3	
		BYTE 0/8	BYTE 1/9	BYTE 2/A	BYTE 3/B	BYTE 4/C	BYTE 5/D	BYTE 6/E	BYTE 7/F
80	<8>LUT4	MOD	MOD	MOD	MOD	MOD	MOD	MOD	MOD
88	<8>LUT4	MOD	MOD	MOD	MOD	MOD	MOD	MOD	MOD
90	<8>LUT4	MOD	MOD	MOD	MOD	MOD	MOD	MOD	MOD
98	<8>LUT4	MOD	MOD	MOD	MOD	MOD	MOD	MOD	MOD
A0	<8>LUT4	MOD	MOD	MOD	MOD	MOD	MOD	MOD	MOD
A8	<8>LUT4	MOD	MOD	MOD	MOD	MOD	MOD	MOD	MOD
B0	<8>LUT4	MOD	MOD	MOD	MOD	MOD	MOD	MOD	MOD
B8	<8>LUT4	MOD	MOD	MOD	MOD	MOD	MOD	MOD	MOD
C0	<8>LUT4	MOD	MOD	MOD	MOD	MOD	MOD	MOD	MOD

Table 05h. Register Map

TABLE 05h (LUT FOR APC)									
ROW (HEX)	ROW NAME	WORD 0		WORD 1		WORD 2		WORD 3	
		BYTE 0/8	BYTE 1/9	BYTE 2/A	BYTE 3/B	BYTE 4/C	BYTE 5/D	BYTE 6/E	BYTE 7/F
80	<8>LUT5	APC REF	APC REF	APC REF	APC REF	APC REF	APC REF	APC REF	APC REF
88	<8>LUT5	APC REF	APC REF	APC REF	APC REF	APC REF	APC REF	APC REF	APC REF
90	<8>LUT5	APC REF	APC REF	APC REF	APC REF	APC REF	APC REF	APC REF	APC REF
98	<8>LUT5	APC REF	APC REF	APC REF	APC REF	APC REF	APC REF	APC REF	APC REF
A0	<8>LUT5	APC REF	APC REF	APC REF	APC REF	RESERVED	RESERVED	RESERVED	RESERVED

Access Code	<0>	<1>	<2>	<3>	<4>	<5>	<6>	<7>	<8>	<9>	<10>	<11>
Read Access	See each bit/byte separately	All	All	All	PW2	All	N/A	PW1	PW2	N/A	PW2	All
Write Access		PW2	N/A	All and DS1863 Hardware	PW2 + mode bit	All	All	PW1	PW2	PW2	N/A	PW1

Lower Memory Registers Description

Lower Memory Register 00h to 01h: Temp Alarm Hi

FACTORY DEFAULT: 7FFFh
READ ACCESS All
WRITE ACCESS PW2
MEMORY TYPE: Nonvolatile (SEE)

00h	S	2^6	2^5	2^4	2^3	2^2	2^1	2^0
01h	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}
	bit7							bit0

Temperature measurements above this 2's complement threshold will set its corresponding alarm bit. Measurements equal to or below this threshold will clear its alarm bit.

Lower Memory Register 02h to 03h: Temp Alarm Lo

FACTORY DEFAULT: 8000h
READ ACCESS All
WRITE ACCESS PW2
MEMORY TYPE: Nonvolatile (SEE)

02h	S	2^6	2^5	2^4	2^3	2^2	2^1	2^0
03h	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}
	bit7							bit0

Temperature measurements above this 2's complement threshold will set its corresponding alarm bit. Measurements equal to or below this threshold will clear its alarm bit.

Lower Memory Register 04h to 05h: Temp Warn Hi

FACTORY DEFAULT: 7FFFh
READ ACCESS All
WRITE ACCESS PW2
MEMORY TYPE: Nonvolatile (SEE)

04h	S	2^6	2^5	2^4	2^3	2^2	2^1	2^0
05h	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}
	bit7							bit0

Temperature measurements above this 2's complement threshold will set its corresponding warning bit. Measurements equal to or below this threshold will clear its warning bit.

Lower Memory Register 06h to 07h: Temp Warn Lo

FACTORY DEFAULT: 8000h
READ ACCESS All
WRITE ACCESS PW2
MEMORY TYPE: Nonvolatile (SEE)

06h	S	2^6	2^5	2^4	2^3	2^2	2^1	2^0
07h	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}
	bit7							bit0

Temperature measurements below this 2's complement threshold will set its corresponding warning bit. Measurements above this threshold will clear its warning bit.

Lower Memory Register 08h to 09h: V_{CC} Alarm Hi

FACTORY DEFAULT: FFFFh
READ ACCESS All
WRITE ACCESS PW2
MEMORY TYPE: Nonvolatile (SEE)

08h	2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^9	2^8
09h	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
	bit7							bit0

Voltage measurements of the V_{CC} input above this unsigned threshold will set its corresponding alarm bit. Measurements below this threshold will clear its alarm bit.

Lower Memory Register 0Ah to 0Bh: V_{CC} Alarm Lo

FACTORY DEFAULT: 0000h
READ ACCESS All
WRITE ACCESS PW2
MEMORY TYPE: Nonvolatile (SEE)

0Ah	2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^9	2^8
0Bh	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
	bit7							bit0

Voltage measurements of the V_{CC} below above this unsigned threshold will set its corresponding alarm bit. Measurements above this threshold will clear its alarm bit.