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Rev 0; 4/06

SFP Laser Controller and Diagnostic IC

General Description

The DS1864 is an SFF-8472 multisource agreement (MSA)-compliant laser controller/monitor that is ideal for SFP optical-transceiver module designs. It controls laser driver bias and modulation currents through a pair of temperature-controlled current-sink DACs. System diagnostics are provided by monitoring three analog inputs, V_{CC}, and temperature through the internal temperature sensor. The device also contains all EEPROM required by the SFF-8472 MSA, including all A0h and A2h EEPROM. The DS1864's memory map can be configured to be compatible with both the DS1852/DS1856 and the DS1859 memory maps. Additionally, memory is secured with customer-configurable two-level password protection.

Eye-safety features are integrated by three fast-trip comparators that monitor transmit-power high, transmit-power low, and bias current. The fast-trip comparators drive a FET driver output to disable the laser in the case of eye safety violation.

With its integrated laser driver control, system diagnostics, eye-safety features, and internal temperature sensor, the DS1864 provides an ideal solution for SFP optical transceiver modules by improving system performance, reducing board space, and simplifying design.

Applications

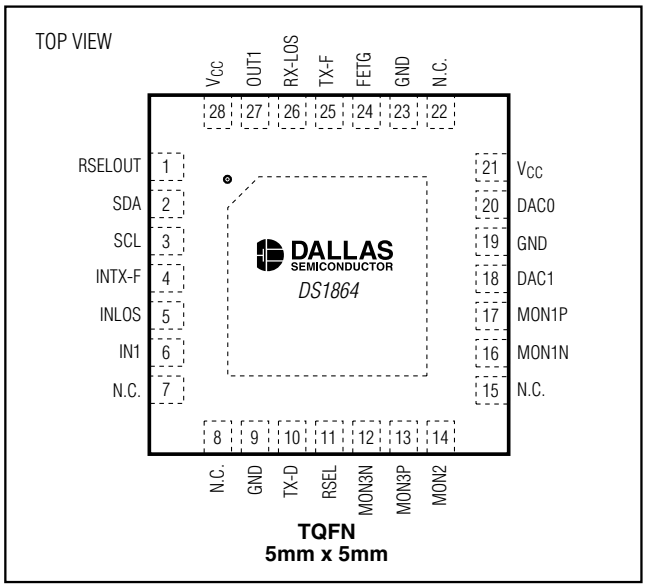
SFP Optical Transceiver Modules

Laser Control and Monitoring

Features

- **SFF-8472 MSA Compatible**
- **Five Monitored Channels (Temperature, V_{CC}, MON1, MON2, MON3)**
  - **Three External Analog Inputs (MON1, MON2, MON3) Support Internal and External Calibration**
  - **Enhanced RSSI Monitoring (26dB Range, 0.5dB Accuracy)**
  - **Scalable Dynamic Range for External Analog Inputs**
  - **Internal Direct-to-Digital Temperature Sensor**
  - **Alarm and Warning Flags for All Monitored Channels**
- **Two Linear 8-Bit Current-Sink DACs**
  - **Two User-Selectable Full-Scale Ranges (0.5mA or 1.5mA)**
  - **Values Changeable Every 2°C**
- **Three Fast-Trip Comparators (Tx Power High, Tx Power Low, and Bias Current) for Eye Safety**
- **Flexible, Two Level Password Scheme Provides Three Levels of Security**
- **Provides All Optional and Required SFF-8472 MSA EEPROM (Both A0h and A2h Memory)**
- **I^2C-Compatible Serial Interface**
- **Operates from a 3.3V or 5V Supply**
- **-40°C to +95°C Operating Temperature Range**
- **28-Pin TQFN Package (5mm x 5mm)**

Pin Configuration



TQFN
5mm x 5mm

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
DS1864T	-40°C to +95°C	28 TQFN (5mm x 5mm)
DS1864T+	-40°C to +95°C	28 TQFN (5mm x 5mm)

+Denotes lead-free only package.

Typical Operating Circuit appears at end of data sheet.

SFP Laser Controller and Diagnostic IC

ABSOLUTE MAXIMUM RATINGS

Voltage Range on V_{CC} Relative to Ground .....-0.5V to +6.0V
Voltage Range on Inputs Relative to Ground* .....-0.5V to (V_{CC} + 0.5V)
Voltage Range on DAC Pins Relative to Ground* .....-0.5V to (V_{CC} + 0.5V)
Current into DAC Pins 5mA
Operating Temperature Range .....-40°C to +95°C
Programming Temperature Range .....0°C to +70°C
Storage Temperature Range .....-55°C to +125°C
Soldering Temperature .....See IPC/J-STD-020 Specification

**Not to exceed 6.0V.*

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

(T_A = -40°C to +95°C)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	V_{CC}	(Note 1)	2.97		5.50	V
Input Logic 0 (SDA, SCL)	V_{IL}	I_{IL}(max) = -10µA	-0.3		+0.3 x V_{CC}	V
Input Logic 1 (SDA, SCL)	V_{IH}	I_{IH}(max) = 10µA	0.7 x V_{CC}		V_{CC} + 0.3	V
Input Logic Levels (TX-D, INLOS, RSEL, IN1)	V_{IL}	Input Logic 0	-0.3		0.9	V
	V_{IH}	Input Logic 1	1.5		V_{CC} + 0.3	

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 2.97V to 5.5V, T_A = -40°C to +95°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current	I_{CC}	(Notes 2 and 3)		3	5	mA
Input Leakage (SDA, SCL)	I_{IL}		-1		+1	µA
Low-Level Output Voltage (SDA)	V_{OL1}	3mA sink current			0.4	V
	V_{OL2}	6mA sink current			0.6	
I/O Capacitance	$C_{I/O}$	For SDA/SCL			10	pF
TX-D Pullup Resistor	R_{PU}	T_A = +25°C	14	20	24	kΩ
Digital Power-On Reset	V_{POD}		1.0		2.2	V
Analog Power-On Reset	V_{POA}		2.00		2.97	V
High-Level Output Voltage (FETG)	V_{OH}	4mA source current	V_{CC} - 0.4		V_{CC} + 0.3	V
Low-Level Output Voltage (TX-F, LOS Voltage, FETG)	V_{OL}	4mA sink current	0.0		0.4	V
Input Current Each I/O Pin		0.4 < $V_{I/O}$ < 0.9V_{CC}	-10		+10	µA

ANALOG OUTPUT CHARACTERISTICS

(V_{CC} = 2.97V to 5.5V, T_A = -40°C to +95°C.)

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNITS
I_{DAC0} and I_{DAC1}	Range 1	Position FFh (Note 6)		0.5		mA
	Range 2			1.5		mA
I_{DAC0} and I_{DAC1} (Off State Current)		Shutdown or Position 00h		10	100	nA
Voltage at I_{DAC0} and I_{DAC1}			0.7		V_{CC}	V
I_{DAC0} and I_{DAC1} Accuracy (Note 6)	Range 1	I_{DAC} < 50µA			±10	µA
		I_{DAC} > 50µA			±4	%
	Range 2	I_{DAC} < 50µA			±10	µA
		I_{DAC} > 50µA			±4	%
Resolution				0.4		%FS

ANALOG VOLTAGE MONITORING CHARACTERISTICS

(V_{CC} = 2.97V to 5.5V, T_A = -40°C to +95°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Full-Scale Monitor Input		At factory setting (Note 4)	2.4875	2.5000	2.5125	V
Full-Scale V_{CC} Monitor		At factory setting (Note 5)	6.5208	6.5536	6.5864	V
Monitor Resolution (V_{CC}, IBI, TXP, RIN)				0.024		%FS
MON1P to MON1N FS		MON1 (Note 7)	0		2.5	V
MON1P, MON1N Common-Mode Voltage			0		V_{CC}	V
MON1P (Single-Ended)		(Notes 7 and 8)			2.5	V
MON1 FS (Factory)		(Note 7)		2.5		V
MON2 FS (Factory)		(Note 7)		2.5		V
MON3 FS (Factory)		V_{MON3} = 2.5V (Note 7)		2.5		V
Supply Accuracy	V_{CCacc}	(Note 7)			0.5	%FS
MON1 Accuracy	$MON1_{acc}$	(Note 7)			0.5	%FS
MON2 Accuracy	$MON2_{acc}$	(Note 7)			0.5	%FS
MON3 Accuracy	$MON3_{acc}$	(Notes 7 and 9)			0.5	%FS
Monitoring Update Rate	t_{frame}	Dual range disabled		21.5	26.0	ms
		Dual range enabled		57	70	
Fast-Trip Comparator Accuracy	FC_{acc}				±4	%FS

DIGITAL THERMOMETER CHARACTERISTICS

(V_{CC} = 2.97V to 5.5V, T_A = -40°C to +95°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Thermometer Error	T_{ERR}	-40°C to +95°C (Notes 10, 17)	-3		+3	°C
Update Rate	t_{frame}	Dual range disabled		57	70	ms
		Dual range enabled		67	80	

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 2.97V to 5.5V, T_A = -40°C to +95°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SHUTDOWN AND FAULTS (SEE FAULT AND SHUTDOWN TIMING DIAGRAMS FIGURES 1 TO 10), FOR FAST ALARMS AND SFP MANAGEMENT						
TX-D (to DACs Off-State Currents)	t_{OFF} Figure 4	From ↑ TX-D (Notes 11, 17)			5	µs
Recovery from Normal Disable (to DACs Set Values)	t_{ON} Figure 4	From ↓ TX-D (Notes 12, 17)			0.8	ms
Recovery After Power-Up (to DACs Set Values)	t_{INIT_DACs} Figure 9	From ↑ V_{CC} = 2.97V (Notes 11, 17)			100	ms
Shutdown Response Time (to DACs Off-State Current)	t_{FAULT} Figure 5	I_{BMD} > TripHi or I_{BIAS} > Trip I_{BMD} < TripLo (Notes 11, 17)			50	µs
Recovery from Safety Fault Shutdown (to DACs Set Values)	t_{INITSF} Figures 6 and 10	From ↓ TX-D (Notes 11, 17)			50	ms
Fault Reset Time (to TX-F = 0)	t_{INITR1} Figure 2	From ↓ TX-D	100		200	ms
Fault Reset Time (to TX-F = 0)	t_{INITR2} Figures 1, 2, 3, and 6	From ↑ V_{CC} = 2.97V	100		200	ms
Fault Assert Time (to TX-F = 1)	t_{FAULT} Figure 5	I_{BMD} > TripHi or I_{BIAS} > Trip I_{BMD} < TripLo (Note 11)			50	µs
LOS Assert Time	t_{LOSS_ON} Figure 8	RSSI < Trip (Note 12)			50	µs
LOS Deassert Time	t_{LOSS_OFF} Figure 8	RSSI > Trip (Note 12)			50	µs

AC ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = 2.97V to 5.5V, T_A = -40°C to +95°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
TIMING FOR SOFT CONTROL AND STATUS FUNCTIONS						
TX-D Assert Time	t_{OFF}	Time from TX-D set until DACs fall below 10% of nominal (Notes 13, 17)			10	ms
TX-D Deassert time	t_{ON}	Time from TX-D cleared until DACs rise above 90% of nominal (Notes 13, 17)			50	ms
Time to Initialize, Including Reset of TX-F	t_{INIT}	Time from power-on or negation of TX-F using TX-D; serial communication possible			200	ms
TX-F Assert Time	t_{FAULT}	Time from fault to TX-F set (Note 17)			50	ms
RX-LOS Assert Time	t_{LOS_ON}	Time from occurrence of loss of signal to RX-LOS set			50	ms
RX-LOS Deassert Time	t_{LOS_OFF}	Time from occurrence of presence of signal to RX-LOS cleared			50	ms
Rate-Select Change Time	t_{RATE_SEL}	Time from change of state of rate-select bit to rate-select output (RSELOUT) pin change			50	ms

I²C AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 2.97V to 5.5V; T_A = -40°C to +95°C, timing referenced to $V_{IL(MAX)}$ and $V_{IH(MIN)}$.) (See Figure 19)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SCL Clock Frequency	f_{SCL}	(Note 14)	0		400	kHz
Bus Free Time Between Stop and Start Conditions	t_{BUF}		1.3			µs
Hold Time (Repeated) Start Condition	$t_{HD:STA}$		0.6			µs
Low Period of SCL	t_{LOW}		1.3			µs
High Period of SCL	t_{HIGH}		0.6			µs
Data Hold Time	$t_{HD:DAT}$		0		0.9	µs
Data Setup Time	$t_{SU:DAT}$		100			ns
Start Setup Time	$t_{SU:STA}$		0.6			µs
SDA and SCL Rise Time	t_R	(Note 15)	$20 + 0.1C_B$		300	ns
SDA and SCL Fall Time	t_F	(Note 15)	$20 + 0.1C_B$		300	ns
Stop Setup Time	$t_{SU:STO}$		0.6			µs
SDA and SCL Capacitive Loading	C_B	(Note 15)			400	pF
EEPROM Write Time	t_W	(Note 16)		10	20	ms

NONVOLATILE MEMORY CHARACTERISTICS

(V_{CC} = 2.97V to 5.5V, T_A = -40°C to +95°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
EEPROM Writes		+70°C (Note 17)	50,000			Writes

Note 1: All voltages are referenced to ground. Currents into the IC are positive, and currents out of the IC are negative.

Note 2: Supply current is measured with all logic inputs at their inactive state (SDA = SCL = V_{CC}) and driven to well-defined logic levels. All outputs are disconnected.

Note 3: DAC0/DAC1 positions programmed to FFh and with outputs floating.

Note 4: Full-scale is user programmable. The maximum voltage that the MON inputs read is approximately full-scale, even if the voltage on the inputs is greater than full-scale.

Note 5: This voltage defines the maximum range of the analog-to-digital (ADC) converter voltage, not the maximum V_{CC} voltage.

Note 6: Accuracy specification includes supply and temperature variations. Measured at 1.2V.

Note 7: %FS refers to calibrated full scale in the case of internal calibration, and uncalibrated full scale in the case of external calibration. Uncalibrated full scale is set at the factory and is specified in this data sheet as V_{CC} FS (Factory), MON1 FS (Factory), MON2 FS (Factory), and MON3 FS (Factory). Calibrated full scale is set by the user, allowing him to change any of these scales for his instrumentation.

Note 8: When used single-ended, MON1N must be connected to GND.

Note 9: 0.5%FS with 0.5dB (~11%) accuracy results in 16.4dB range. Assuming some overlap of the ranges, this scheme should cover the required 26dB range.

Note 10: See Figure 14 for thermometer error.

Note 11: When the DACs are re-enabled, they ramp up to their final values. The ramp up starts from 0 and should not exceed its final value at any point during its initial transient.

Note 12: This spec is the time it takes, from RSSI voltage below the RSSI voltage trip threshold, to LOS asserted high.

Note 13: Measured from the falling clock edge after the stop bit of the write transaction.

Note 14: I^2C interface timing shown for is for fast-mode (400kHz) operation. This device is also backward-compatible with I^2C standard-mode timing.

Note 15: C_B—total capacitance of one bus line in picofarads.

Note 16: EEPROM write begins after a stop condition occurs.

Note 17: This parameter is guaranteed by design.

Timing Diagrams

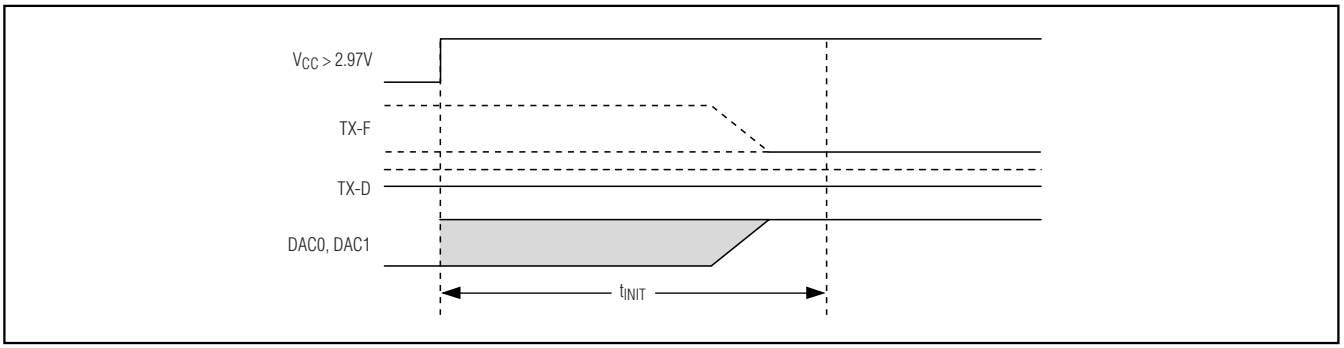


Figure 1. Power-On Initialization with TX-D Low

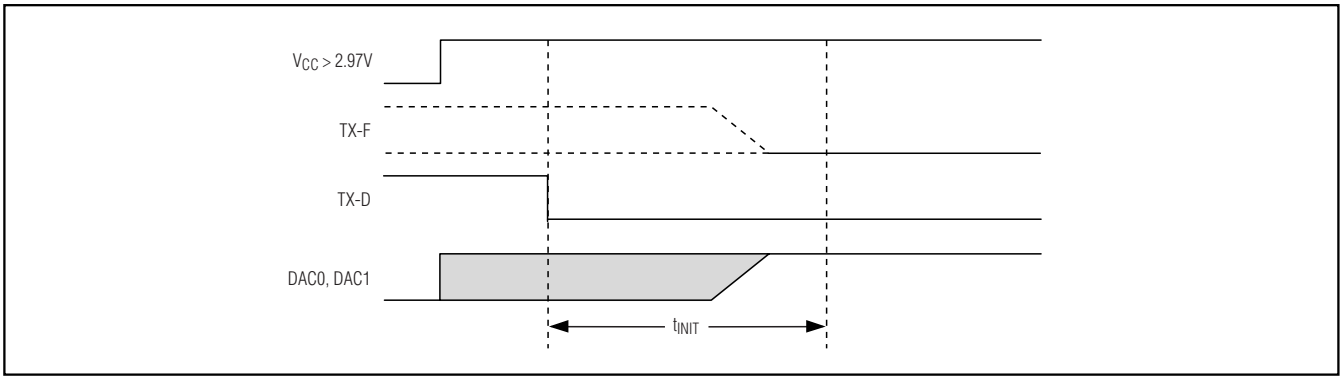


Figure 2. Power-On Initialization with TX-D Asserted

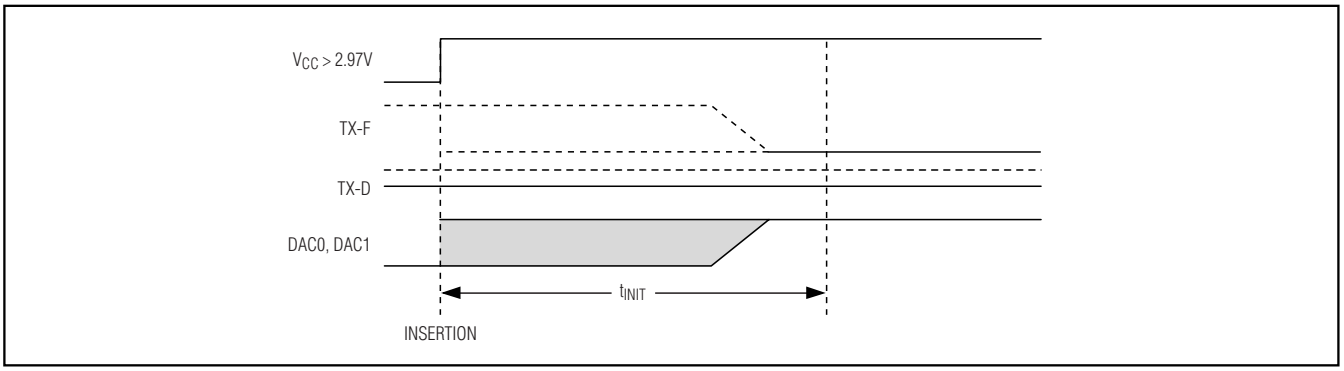


Figure 3. Example of Initialization with TX-D Low (Hot-Plug)

Timing Diagrams (continued)

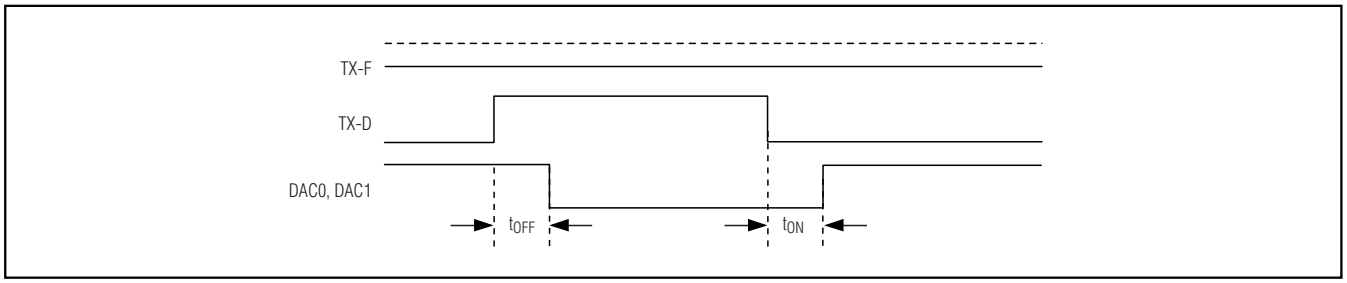


Figure 4. TX-D Timing During Normal Operation

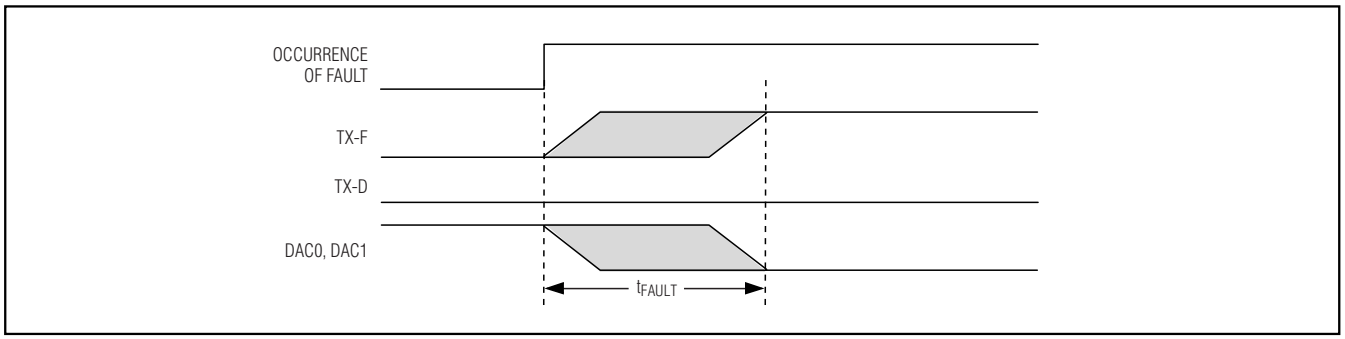


Figure 5. Detection of Transmitter Safety Fault Operation

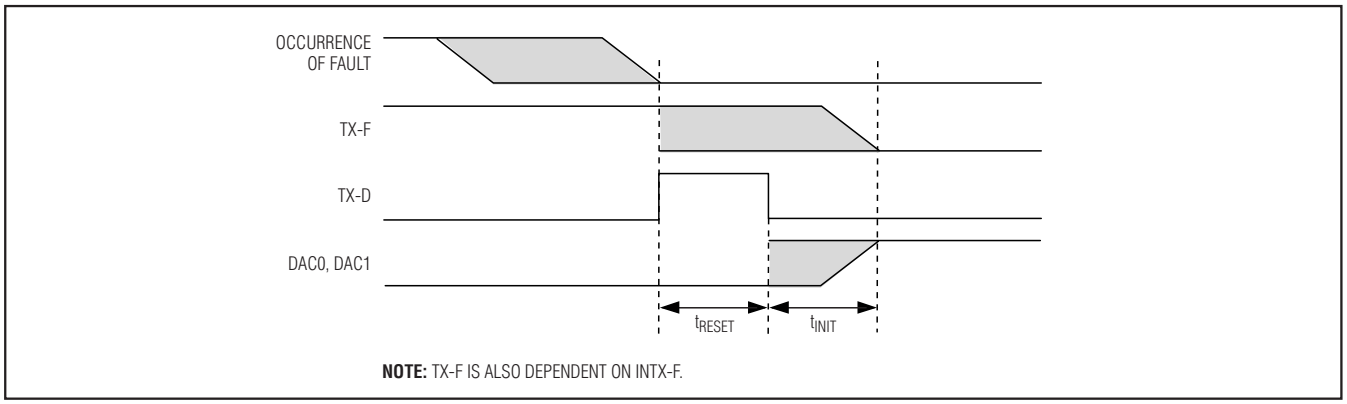


Figure 6. Successful Recovery from Transient Safety Fault Condition

Timing Diagrams (continued)

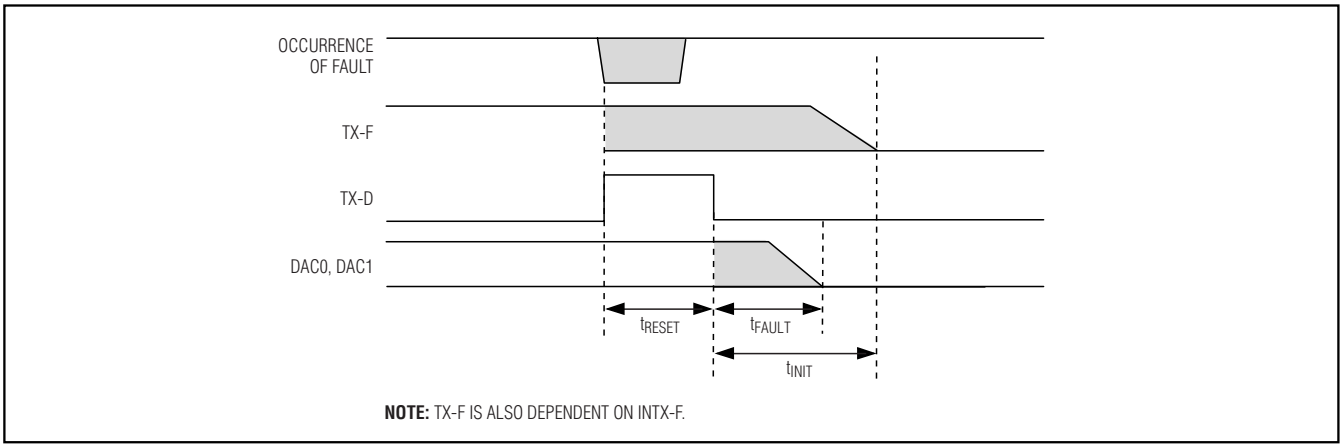


Figure 7. Unsuccessful Recovery from a Transient Safety Fault Condition

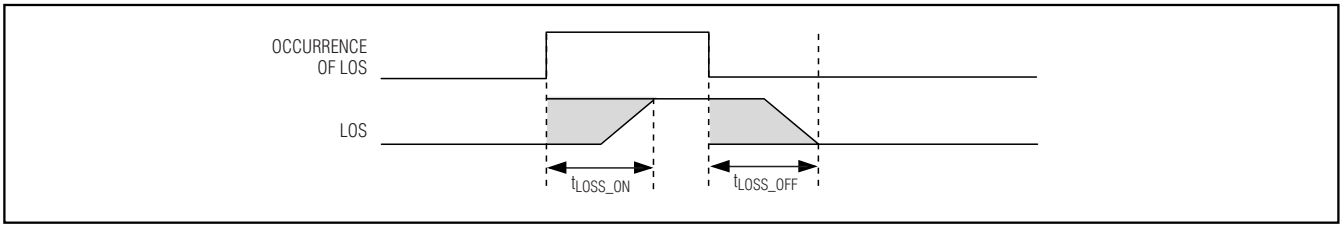


Figure 8. Timing of LOS Detection

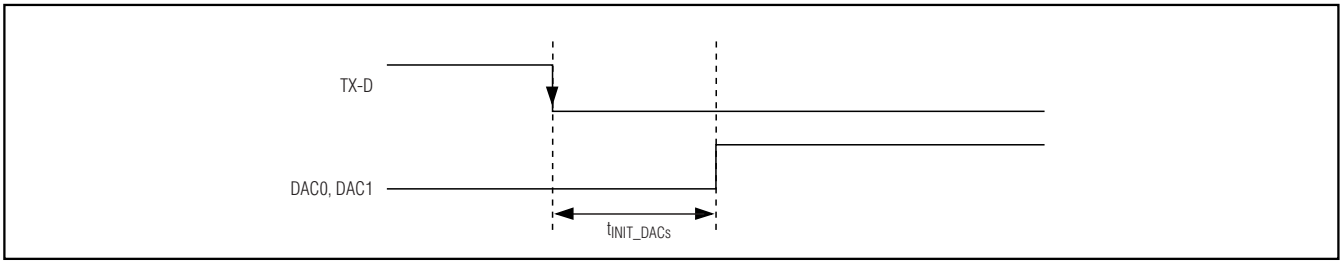


Figure 9. Output Enable/Power-Up

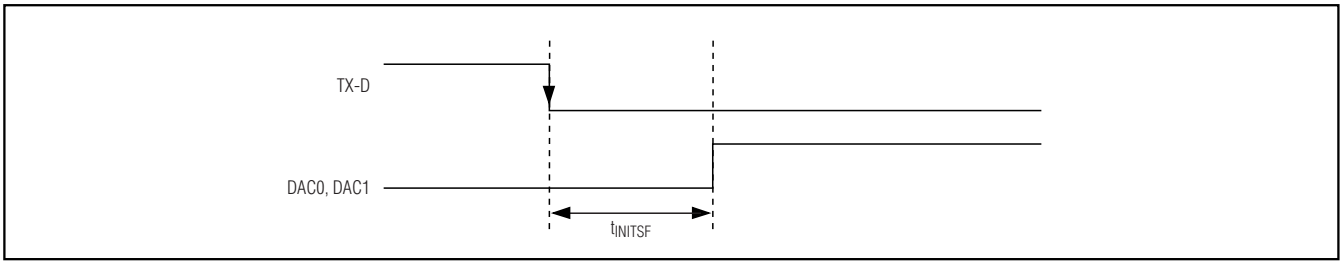


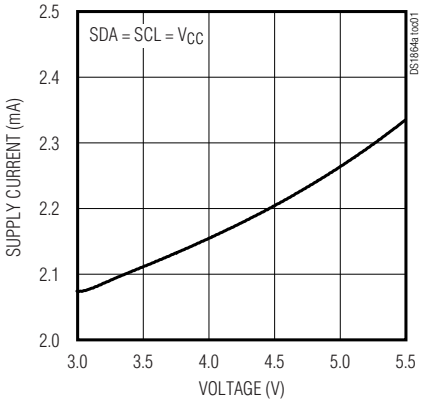
Figure 10. Output Enable/Recovery from Safety Fault Shutdown

SFP Laser Controller and Diagnostic IC

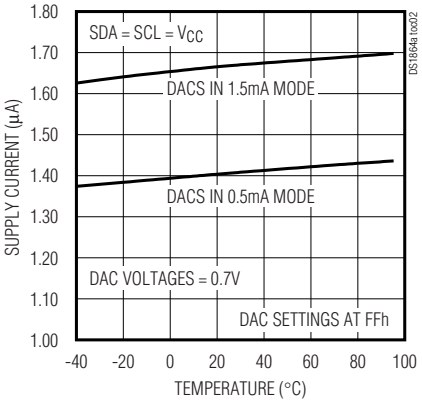
Typical Operating Characteristics

(V_{CC} = +3.3V, T_A = 25°C, unless otherwise noted.)

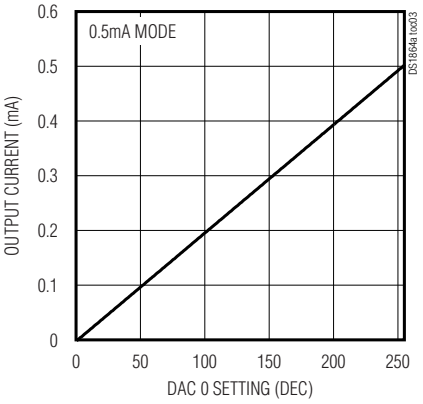
SUPPLY CURRENT vs. VOLTAGE



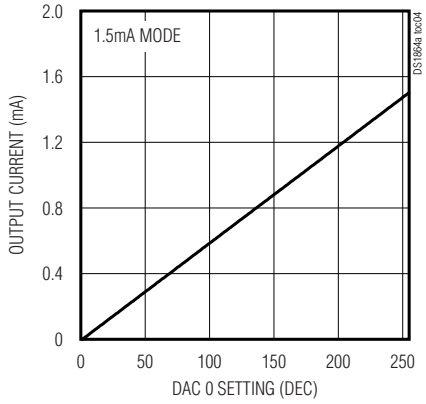
SUPPLY CURRENT vs. TEMPERATURE



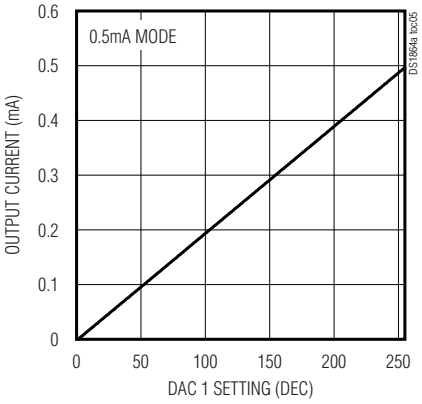
OUTPUT CURRENT vs. DAC 0 SETTING



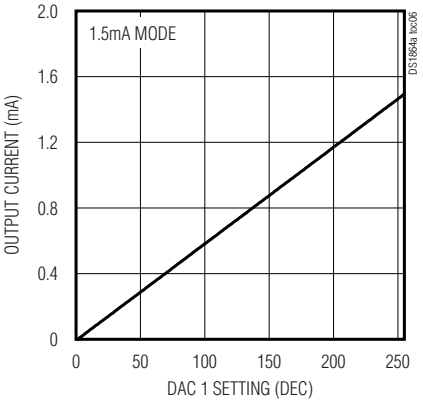
OUTPUT CURRENT vs. DAC 0 SETTING



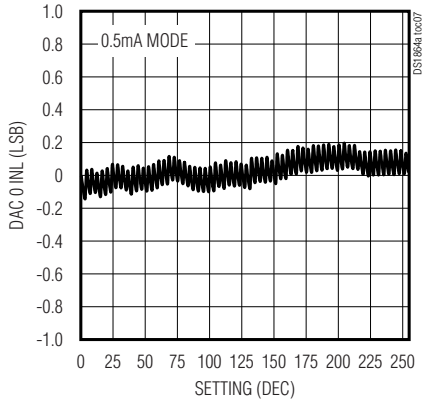
OUTPUT CURRENT vs. DAC 1 SETTING



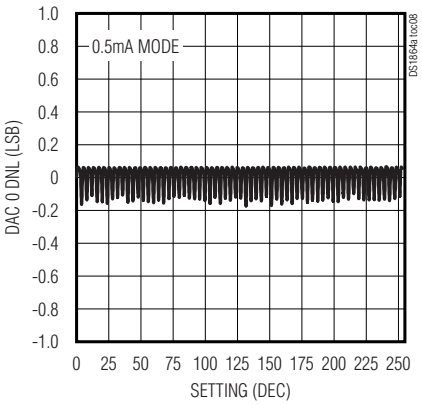
OUTPUT CURRENT vs. DAC 1 SETTING



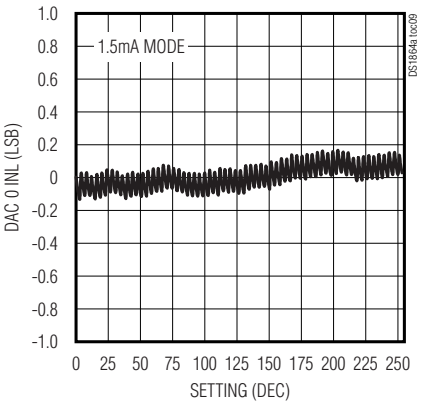
DAC 0 INL (LSB)



DAC 0 DNL (LSB)



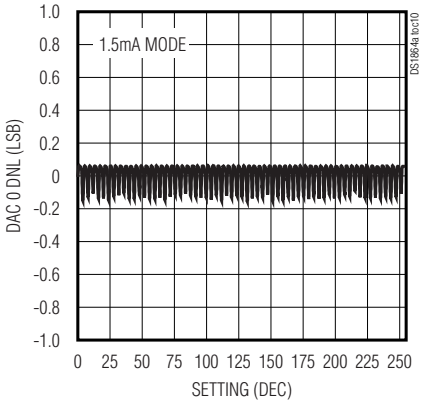
DAC 0 INL (LSB)



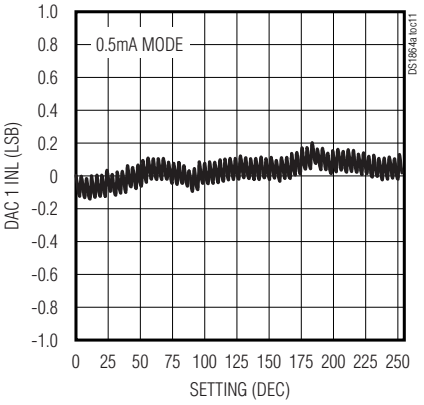
Typical Operating Characteristics (continued)

(V_{CC} = +3.3V, T_A = 25°C, unless otherwise noted.)

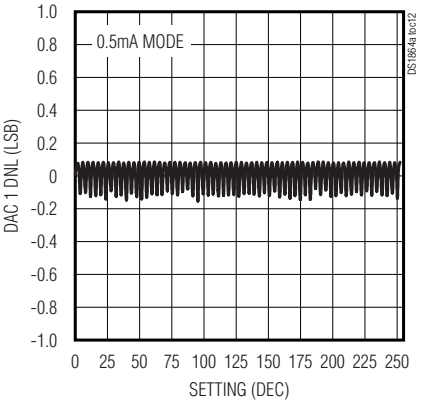
DAC 0 DNL (LSB)



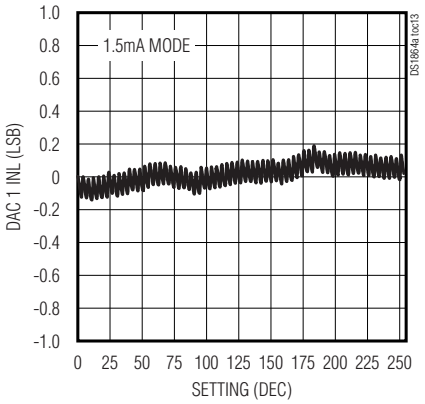
DAC 1 INL (LSB)



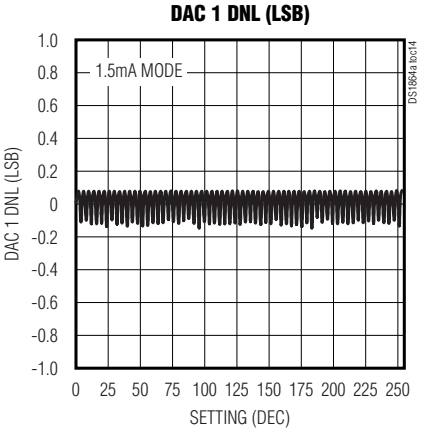
DAC 1 DNL (LSB)



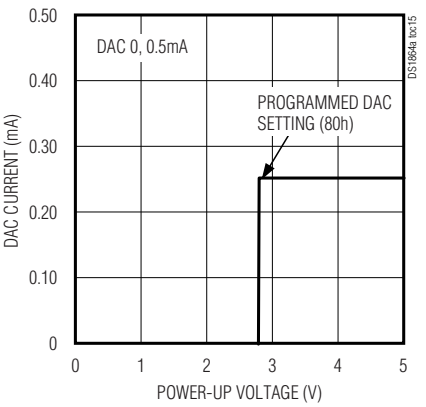
DAC 1 INL (LSB)



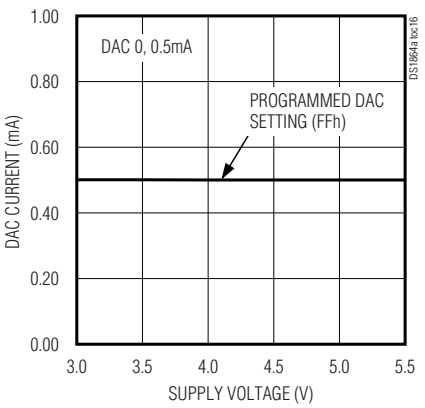
DAC 1 DNL (LSB)



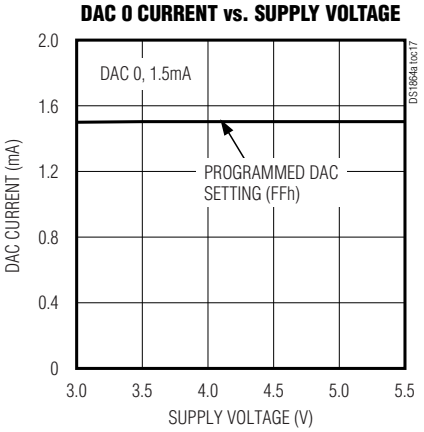
DAC SETTING vs. POWER-UP VOLTAGE



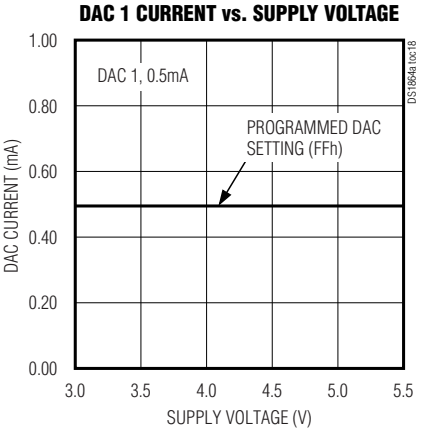
DAC 0 CURRENT vs. SUPPLY VOLTAGE



DAC 0 CURRENT vs. SUPPLY VOLTAGE



DAC 1 CURRENT vs. SUPPLY VOLTAGE

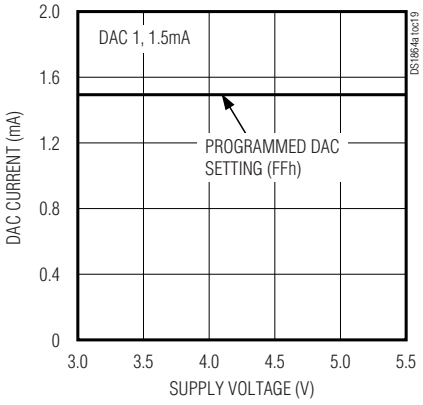


SFP Laser Controller and Diagnostic IC

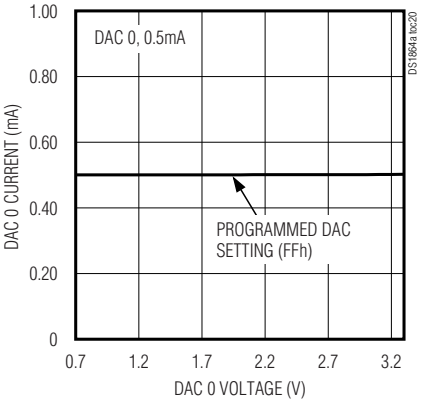
Typical Operating Characteristics (continued)

(V_{CC} = +3.3V, T_A = 25°C, unless otherwise noted.)

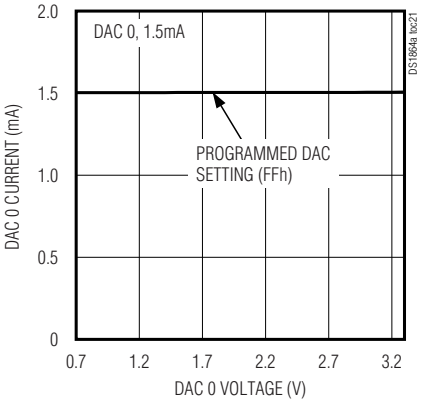
DAC 1 CURRENT vs. SUPPLY VOLTAGE



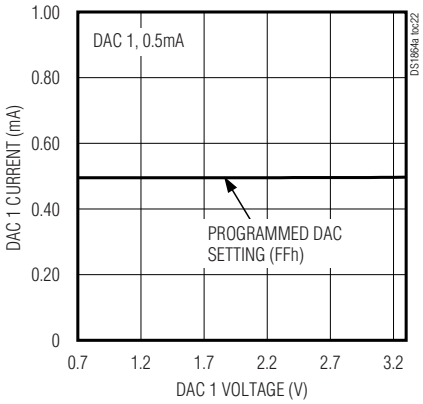
DAC 0 CURRENT vs. FUNCTION OF THE VOLTAGE ON THE DAC



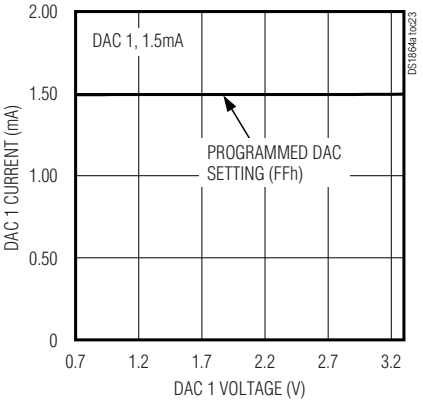
DAC 0 CURRENT vs. FUNCTION OF THE VOLTAGE ON THE DAC



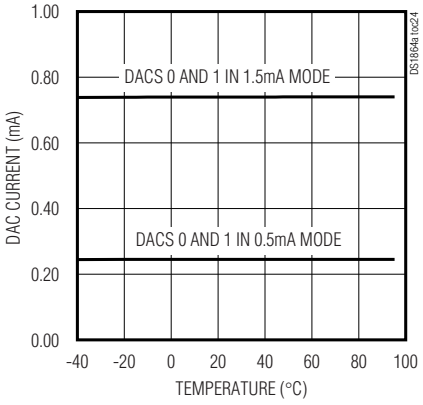
DAC 1 CURRENT vs. FUNCTION OF THE VOLTAGE ON THE DAC



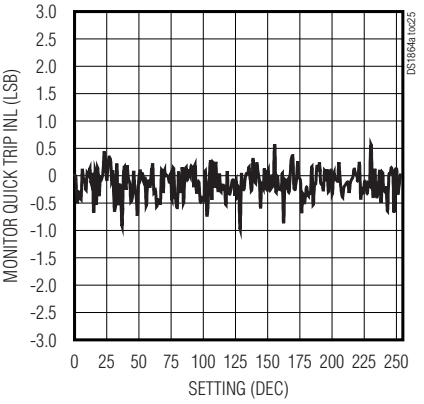
DAC 1 CURRENT vs. FUNCTION OF THE VOLTAGE ON THE DAC



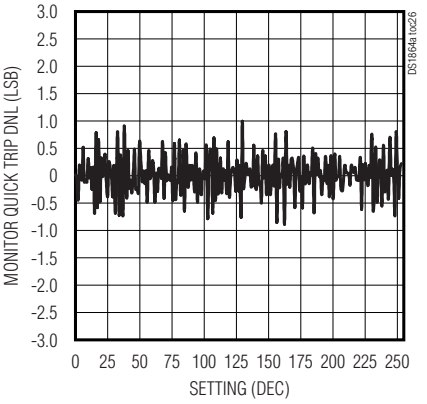
DAC CURRENT AT SETTING 7Fh vs. TEMPERATURE



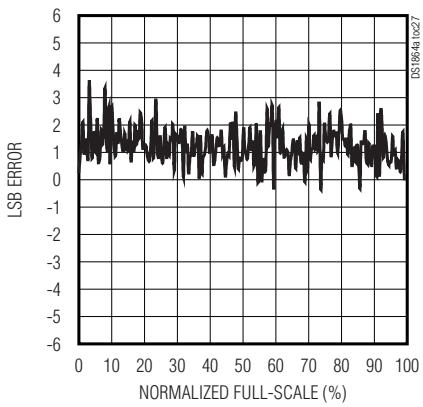
MONITOR FAST-TRIP INL (LSB)



MONITOR FAST-TRIP DNL (LSB)



LSB ERROR vs. FULL-SCALE INPUT



Pin Description

PIN	PIN NAME	DESCRIPTION
1	RSELOUT	Open-Drain Rate-Select Output
2	SDA	I^2C Serial Data Input/Output
3	SCL	I^2C Serial Clock Input
4	INTX-F	TX-F Input from External Device
5	INLOS	Loss of Signal Input from External Device
6	IN1	Digital Input
7	N.C.	No Connection
8	N.C.	No Connection
9	GND	Ground. All GND pins must be connected.
10	TX-D	Transmit Disable Input. Places DAC0 and DAC1 in high-impedance state.
11	RSEL	Rate Select Logic Input
12	MON3N	Voltage Monitor Input, Low Side. Used typically for RSSI.
13	MON3P	Voltage Monitor Input, High Side. Used typically for RSSI.
14	MON2	Voltage Monitor Input. Used typically for Transmit Power (TXP).
15	N.C.	No Connection
16	MON1N	Voltage Monitor Input, Low Side. Used typically for Bias Sense Current (IBIAS).
17	MON1P	Voltage Monitor Input, High Side. Used typically for Bias Sense Current (IBIAS).
18	DAC1	Lookup Table-Controlled Current Sink
19	GND	Ground. All GND pins must be connected.
20	DAC0	Lookup Table-Controlled Current Sink
21	V_{CC}	Power Supply. All V_{CC} pins must be connected.
22	N.C.	No Connection
23	GND	Ground. All GND pins must be connected.
24	FETG	Logic Output Driving External FET
25	TX-F	Open-Drain Fault Output
26	RX-LOS	Open-Drain Loss of Signal Output
27	OUT1	Open-Drain Digital Output
28	V_{CC}	Power Supply. All V_{CC} pins must be connected.

SFP Laser Controller and Diagnostic IC

Functional Diagrams

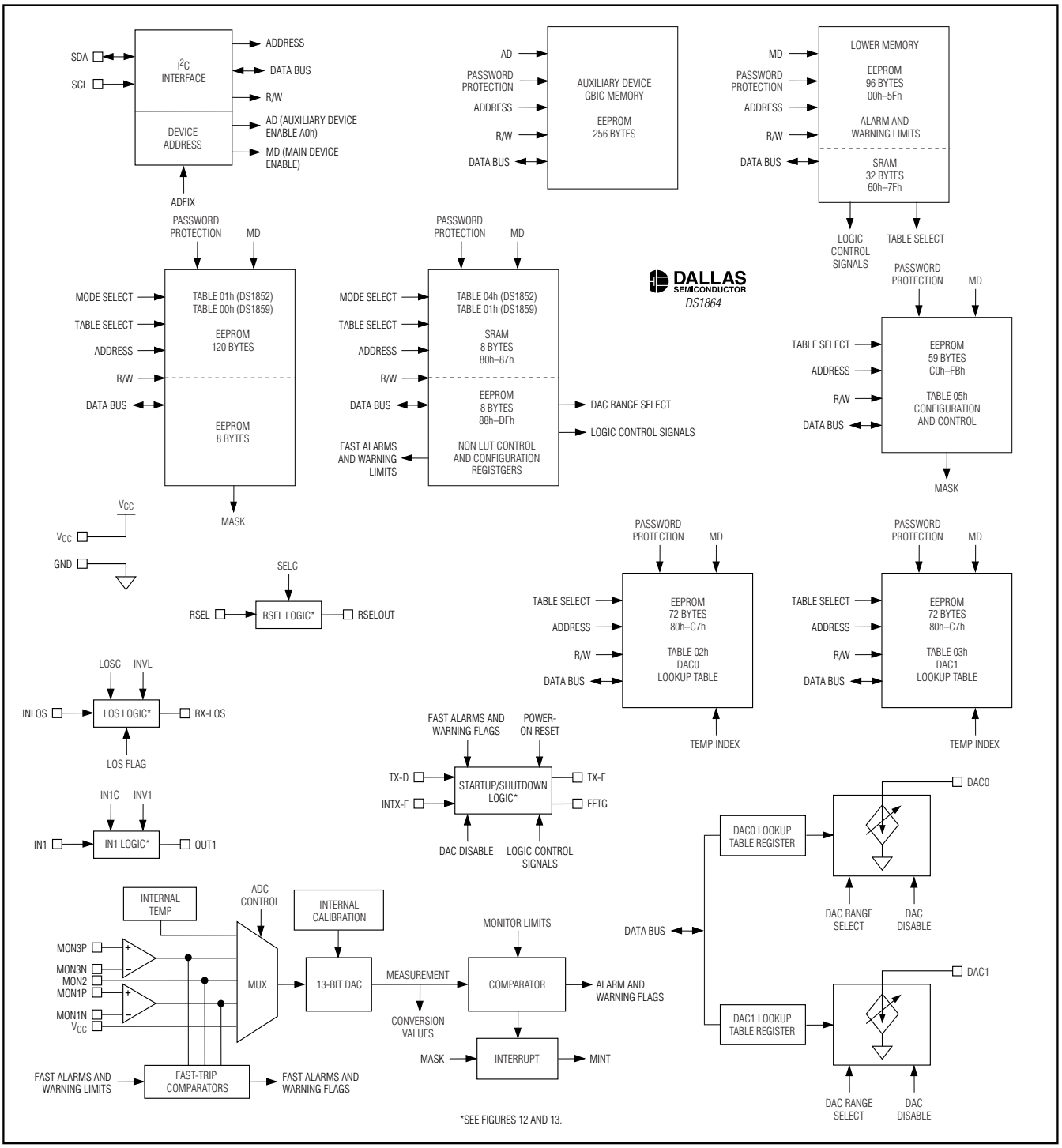


Figure 11. Block Diagram, Main

Functional Diagrams (continued)

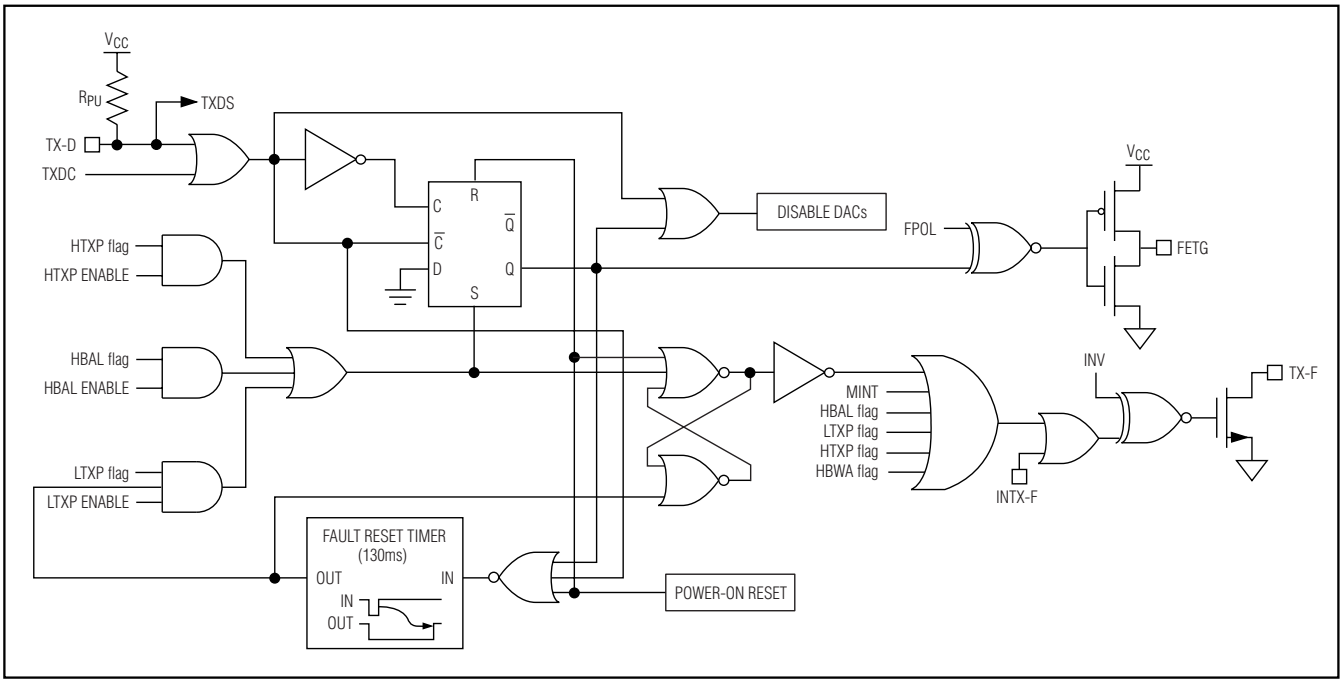


Figure 12. Block Diagram, Shutdown

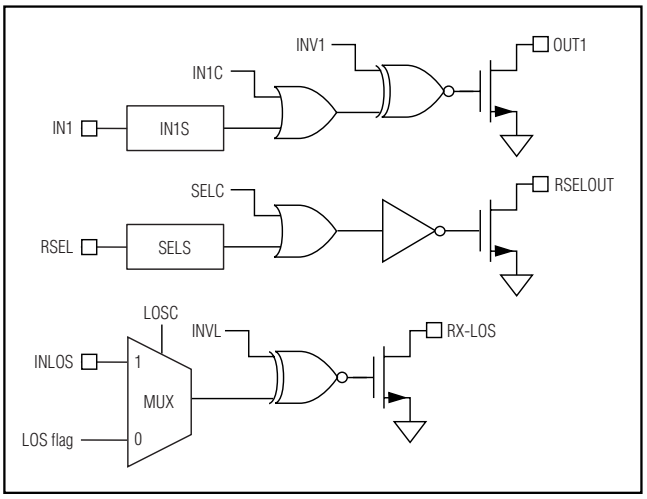


Figure 13. Block Diagram, Outputs

SFP Laser Controller and Diagnostic IC

Detailed Description

The DS1864 manages all system monitoring functions in a fiber-optic data transceiver module in accordance with SFF-8472 MSA. The IC communicates with a host system through a I^2C bus, and can be programmed with a unique I^2C address.

The IC offers temperature-controlled lookup tables for its two current-sink DACs. Monitoring and calibration functions for supply voltage, temperature and three analog signals are available, as well as programmable alarm and warning flags for these signals which can be used to trigger interrupts based on user-specified limits.

The IC also possesses laser shutdown (eye safety) features such as programmable fast-trip alarms and interrupts, in addition to signals such as FETG for laser safety disconnect.

The memory is protected by a customizable two-layer password scheme. Furthermore, the memory layout can be configured to be compatible with the DS1852/DS1856 or the DS1859.

An overview of the DS1864's functions is shown in the block diagram in Figure 11. Additional DS1864 functions are shown in Figures 12 and 13.

Control Features

The DS1864 contains two current-sink DACs, DAC0 and DAC1. Normally, each DAC is controlled by a temperature-indexed lookup table (LUT), which can change the DAC settings based on the temperature measured by the internal temperature sensor. However, each DAC can also be manually programmed by the user.

DAC0 and DAC1

The current-sink DACs are linear and have two user-selectable ranges, 1.5mA and 0.5mA. The range is selected by the DAC0R and DAC1R bits located in address 88h in Table 04h (Table 01h in DS1859 configuration). The 1.5mA range is selected when the corresponding bit is set to a 1, and the 0.5mA range is selected when the corresponding bit is set to a 0. The temperature-indexed LUT for each DAC determines the value to be loaded in to the DAC0 and DAC1 registers (bytes 82h and 83h respectively in Table 04h (Table 01h in DS1859 configuration)). The DACs can be disabled (placed in a high-impedance mode) by pulling the TX-D pin high. The TXDC control bit (Lower Memory Register, byte 6Eh, bit 6) can also be used to disable the DAC outputs by placing them in a high-impedance state.

To determine the DAC position to produce a desired current, the following equation can be used:

$$\text{DESIRED POSITION} = \left(\frac{\text{DESIRED CURRENT}}{\text{FULL SCALE CURRENT}} \right) \times 255$$

Update bits are provided to indicate when an A/D conversion has completed for each monitored value. These bits are located in Lower Memory, byte 77h.

DAC Lookup Table (LUT) Operation

The current-sink DAC settings are determined by temperature-controlled Lookup Tables (LUTs). The LUTs are located in Table 02h for DAC0 and Table 03h for DAC1. The lookup tables are 72 bytes each and allow the biasing to be adjusted every 2°C between -40°C and +102°C. Temperatures less than -40°C or greater than +102°C use the -40°C or +102°C values, respectively. The values programmed into the LUTs are 8-bit unsigned values that represent the desired DAC setting for each 2°C temperature window. The LUTs have 1°C hysteresis (see Figure 14) to prevent the DAC's setting from chattering in the event the temperature remains near a LUT switching point. Table 1 shows which register corresponds to which temperature in the LUTs. Figure 14 shows how the LUT chooses which memory location to use for the DACs depending on the temperature read from the internal temperature sensor.

The Temperature Index Byte (address 81h, Table 04h (Table 01h in DS1859 configuration)) is automatically calculated following each temperature conversion and points to the corresponding location in the LUTs for the

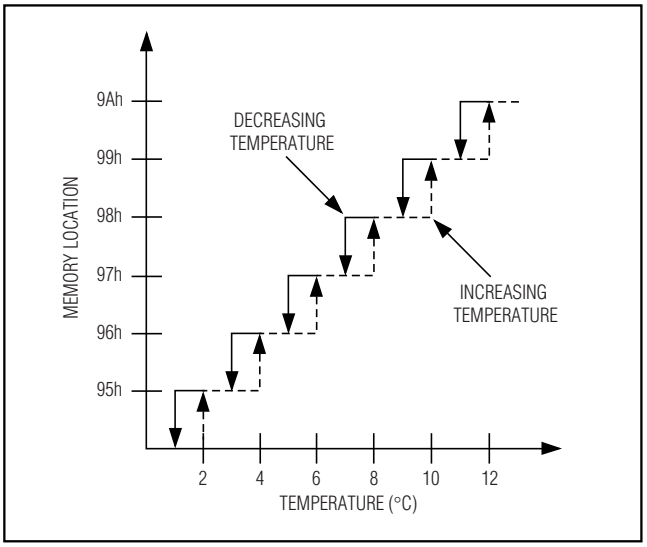


Figure 14. LUT Hysteresis

Table 1. LUT Addresses For Corresponding Temperature Values

ADDRESS (hex)	CORRESPONDING TEMPERATURE (°C)
80	≤ -40°C
81	-38°C
82	-36°C
—	—
C6	+100°C
C7	≥ +102°C

current temperature. The DAC value referenced in the LUT is then loaded into address 82h of Table 04h (Table 01h in DS1859 configuration) for DAC0 and into address 83h of Table 04h (Table 01h in DS1859 configuration) for DAC1.

DAC Manual Mode

During normal operation, the DAC setting is automatically modified once per conversion cycle based on the ADC results. However, if the TEN bit (bit 1, address 80h, Table 04h (Table 01h in DS1859 configuration)) is set to 0, the DACs are placed in a manual mode and temperature indexing is disabled. Once in manual mode, the user programs the current-sink DACs by writing the desired positions to addresses 82h and 83h in Table 04h (Table 01h in DS1859 configuration) to control DAC0 and DAC1, respectively.

RSEL Operation

The rate select pin (RSEL) along with the SELC rate select bit (Lower Memory Register, byte 6Eh, bit 3) determine the state of the RSELOUT pin, which is intended to be used to control receiver multirate performance. The RSEL pin state is OR'ed with the state of the SELC bit to determine the RSELOUT pin state. Bit SELS (Lower Memory Register, byte 6Eh, bit 4) indicates the state of the RSEL pin. See Figure 13 for more details.

Monitoring Features

The DS1864 incorporates five basic monitor channels, which include temperature, supply voltage (V_{CC}), and three external channels (MON1, MON2, and MON3). These analog signals are sampled and converted into digital measurements and compared to threshold limits to determine alarm and warning signals and fault states. These five signals can be calibrated externally, using reserved registers for calibration values, or internally, using built-in gain, offset, and right-shifting functions.

Digital Diagnostics

In optical transceiver applications, the external monitor channels are typically used for Bias Current (IBI) through pins MON1P and MON1N, Transmitted Power (TXP) through a MON2 pin, and Received Power (RIN) through pins MON3P and MON3N. While MON2 is a single-ended monitor, MON1 and 3 have the option of being used as differential or single-ended monitors. To use these channels single-ended, connect the 'N' side to ground. A 13-bit ADC samples and digitizes the five analog signals and the results are stored in registers 60h through 69h in the Lower Memory. The representative digital values are 13-bits wide (left justified), and are stored in successive register pairs. The temperature value is stored in a 2's complement format, while V_{CC} and the three analog inputs are stored in an unsigned format. The digital values are updated every t_{FRAME}. From these measurements, alarms and warnings are generated after a digital comparison with high and low set limits. A maskable interrupt, MINT, asserted through TX-Fault, can be enabled based on any combination of alarms and warnings.

Alarm and Warning Flags

Alarm and warning flags are generated by comparing the digitally converted values of the measured temperature, supply voltage, and three MON inputs with user-programmed upper and lower limits. These limits are stored in EEPROM locations 00h through 27h in the Lower Memory. The two types of flags, alarm and warning, are also stored in the Lower Memory. Addresses 70h and 71h contain the alarm flags, while addresses 74h and 75h contain the warning flags. The *Alarms and Warnings* section under *Fault Management* describe how to program the alarm and warning thresholds, and how to use them to generate interrupts.

Calibration Overview

Calibration is provided internally or externally. External calibration makes use of a range of registers, reserved for this purpose according to SFF-8472 standard. This range is 38h to 5F in the Lower Memory Registers. The calibration constants are loaded in the registers during system test. In external calibration mode, a host processor retrieves the constants and computes the calibrated data.

The DS1864 features internal calibration for the five analog channels. Internal calibration makes use of two registers for four of the five monitored analog channels: V_{CC}, MON1 (Bias Current (IBI)), MON2 (Transmitted Power (TXP)) and MON3 (Received Power (RIN)). One register is for offset calibration, the other for gain calibration. Both registers are loaded during system test. Only the offset scaling register is used for temperature.

Internal calibration applies to measured values acquired by the ADC, and does not apply to the fast alarms. If internal calibration is desired, each analog channel requires that registers 8Eh through AFh in Table 04h (Table 01h in DS1859 configuration) are loaded with the appropriate values to calibrate for gain and offset. Every gain and offset register is 2-bytes wide. Both gain and offset calibration are independently capable of converting input variables into a digital output range spanning 0000h to FFFFh.

The last adjustment is made by using right-shifting. Right-shifting registers are located in registers A2h through ABh and AEh to AFh, and store a 3-bit value used to shift each MON value from 0 to 7 spaces to the right. The effect of this is to make better use of the ADC range and increase the accuracy of the readings. Right-shifting is the last function performed on the MON signal before the digital value is sent to the MON register.

Temperature Monitor Operation

The internal temperature monitor values are stored in 16-bit 2's complement format, and located in memory addresses 60h and 61h of the Lower Memory. The temperature conversions are updated every t_{FRAME}, and do not occur during an active read or write to memory. The factory default calibration values for the temperature monitor are shown in Table 2.

Table 2. Internal Temperature Monitor Factory Default Calibration

SIGNAL	+FS SIGNAL	+FS (hex)	-FS SIGNAL	-FS (hex)
Temperature	+127.96875°C	7FF8	-128.00°C	8000

To convert the 2s complement register value to the temperature it represents, first convert the 2-byte hexadecimal value to a decimal value as if it is an unsigned value, then divide the result by 256. Finally, subtract 256 if the result of the division is greater than or equal to +128. Example converted values are shown in Table 3 below.

Table 3. Temperature Conversion Values

MSB (bin)	LSB (bin)	TEMPERATURE (°C)
01000000	00000000	64
01000000	00001111	64.059
01011111	00000000	95
11110110	00000000	-10
11011000	00000000	-40

The offset of the temperature sensor can be adjusted using the internal calibration registers to account for differences between the ambient temperature at the location of the DS1864 and the temperature of the device it is biasing. When offsets are applied to the temperature measurement, the value converted is offset by a fixed value from the DS1864's ambient temperature. For more information, see the following *Temperature Monitor Offset Calibration* section.

Temperature Monitor Offset Calibration

The DS1864's temperature sensor comes precalibrated and requires no further adjustment by the customer for proper operation. However, it is possible to characterize a system and add a fixed offset to the DS1864's temperature reading so it is representative of another location's temperature. This is not required for biasing because the temperature offset can be accounted for by adjusting the data's location in the LUTs, but this feature is available for customers that see application benefits.

To change the temperature sensor's offset: write the temperature offset register to 0000h, measure the source reference temperature (T_{REF}, °C), and read the temperature from the DS1864 (T_{DS1864}, °C). Then, the following formula can be used to calculate the value for the temperature offset register.

$$\text{TEMP OFFSET} = \left(64 \times (-275 + T_{REF} - T_{DS1864})\right) \text{XOR}_{\text{BITWISE}}\ \text{BB40h}$$

Once the value is calculated, write it to the temperature offset register.

Voltage Monitor Operation

In addition to monitoring temperature, the DS1864 monitors V_{CC} and the three MON inputs in a round-robin fashion using its 13-bit A/D converter. The converted values are stored in memory addresses 62h to 69h as 16-bit unsigned numbers with the ADC results left justified in the register. The round-robin update time is specified by t_{FRAME} in the analog voltage monitoring characteristics.

The default factory-calibrated values for the voltage monitors are shown in Table 4.

By using the internal gain and offset calibration registers the +FS and -FS signal values shown in Table 4 can be modified to meet customer needs. For more information on calibration, see the following *Voltage Monitor Calibration* section.

Note: ±FS voltages shown in Table 4 were calculated assuming factory-programmed gain and offset values in addition to right shifting set to 0.

Table 4. Voltage Monitor Factory Default Calibration

SIGNAL	+FS (V)	+FS (hex)	-FS (V)	-FS (hex)
V_{CC}	6.5528V	FFF8	0V	0000
MON1	2.4997V	FFF8	0V	0000
MON2	2.4997V	FFF8	0V	0000
MON3	2.4997V	FFF8	0V	0000

To calculate the voltage measured from the register value, first calculate the LSB weight of the 16-bit register. The LSB weight is equal to the full-scale voltage span divided 65528. Next, convert the hexadecimal register value to decimal and multiply it times the LSB weight.

Example: Using the factory default V_{CC} trim, what voltage is measured if the V_{CC} register value is C340h? The LSB for V_{CC} is equal to (6.5528V - 0V) / 65528 = 100.00µV. C340h is equal to 49984 decimal, which yields a supply voltage equal to 49984 x 100.00µV = 4.9984V. Table 5 shows more conversion examples based on the factory trimmed A/D settings.

The factory-programmed LSB for V_{CC} is 100µV. The factory-programmed LSB weight for the MON channels is 38.147µV.

Table 5. Voltage Monitor Conversion Examples

SIGNAL	LSB WEIGHT µV)	REGISTER VALUE (HEX)	INPUT VOLTAGE (V)
V_{CC}	100.00	8080	3.2896
V_{CC}	100.00	C0F0	4.9392
MON1	38.147	AA00	1.6601
MON2	38.147	1880	0.2392
MON3	38.147	9CF0	1.5326

Voltage Monitor Calibration (Gain, Offset, and Right Shifting)

The DS1864 has the ability to scale each analog voltage's gain and offset to produce the desired digital result. Each of the inputs (V_{CC}, MON1, MON2, MON3) has specific registers for the gain, offset, and right shifting (in memory Table 04h (Table 01h in DS1859 configuration)) allowing them to be individually calibrated.

To scale the gain and offset of the converter for a specific input, one must first know the relationship between the analog input and the expected digital result. The input that would produce a digital result of all zeros is the null value (normally this input is GND). The input that would produce a digital result of all ones (FFF8h) is the full-scale (FS) value. The expected FS value is also found by multiplying FFF8h by the LSB weight.

The right-shifting operation on the A/D converter output is carried out based on the contents of Registers Right Shift1 and Right Shift2 in EEPROM. Each of the three analog channels (MON1 (Bias Current (IBI)), MON2 (Transmitted Power (TXP)), and MON3 (Received Power (RIN)) is allocated 3 bits to set the number of right shifts. Up to 7 right-shift operations are allowed and will be executed as a part of every conversion before the result is loaded in the corresponding measurement registers 62h to 69h. This is true during the setup of internal calibration as well as during subsequent data conversions.

Example: Since the FS digital reading is 65528 (FFF8h) LSBs, if the LSB's weight is 50µV, then the FS value is 65528 x 50µV = 3.2764V.

A binary search is used to calibrate the gain of the converter. This requires forcing two known voltages on the input pin. It is preferred that one of the forced voltages is the null input and the other is 90% of FS. Since the LSB of the least significant bit in the digital reading register is known, the expected digital results can be calculated for both the null input and the 90% of full-scale value.

An explanation of the binary search used to scale the gain is best served with the following example pseudo-code:

```
/* Assume that the null input is 0.5V */
/* Assume that the requirement for the LSB is 50µV */
        FS = 65528 * 50e-6;             /*3.2764V */
        CNT1 = 0.5 / 50e-6;             /* 1000 */
        CNT2 = 0.9 X FS / 50e-6;        /* 58968 */

/* So the null input is 0.5V and 90% of FS is 2.94876V */

        Set the input's offset register to zero
        gain_result = 0h;       /* Working register for gain calculation */
        CLAMP = FFF0h;          /* This is the max A/D value*/

        For n = 15 down to 0
        begin
                gain_result = gain_result + 2^n;
                Write gain_result to the input's gain register;
                Force the 90% FS input (2.94876V);
                Meas2       = A/D result from DS1864;
                If Meas2 >= CLAMP
                Then
                        gain_result = gain_result - 2^n;
                Else
                        Force the null input (0.5V)
                        Meas1 = A/D result from DS1864
                        If [(Meas2-Meas1)>(CNT2-CNT1)]
                        Then
                                gain_result = gain_result - 2^n;
        end;
        Write gain_result to the input's gain register;
```

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The gain register is now set and the resolution of the conversion will match the expected LSB. Customers requiring nonzero null values (e.g., 0.5V as the example shows) must next calibrate the input's offset. If the desired null value is 0V, leave the offset register programmed to 0000h and skip this step.

To calibrate the offset register, program the gain register with the gain_result value determined above. Next, force the null input voltage (0.5V for the example) and read the digital result from the part (Meas1). The offset value can be calculated using the following formula:

$$\text{OFFSET} = -1 \times \left(\frac{\text{Meas1}}{4}\right)$$

This value is then programmed into the corresponding offset register.

Enhanced RSSI Monitoring (Dual-Range Functionality)

The DS1864 offers a brand new feature to improve the accuracy and range of MON3, which is most commonly used for monitoring RSSI. Predecessors of the DS1864, namely the DS1859 and the DS1856, feature programmable gain, offset, and right shifting (Scalable Dynamic Ranging) on each of the MON channels. These three elements are extremely beneficial when monitoring low-amplitude signals such as RSSI. The accuracy of the RSSI measurements is increased at the small cost of reduced range (of input signal swing). The DS1864 eliminates this tradeoff by offering "dual-range" calibration on the MON3 channel. This feature enables right shifting (along with its gain and offset settings) when the input signal is below a set threshold (within the range that benefits using right shifting) and then automatically disables right shifting (recalling different gain and offset settings) when the input signal exceeds the threshold. Also, to prevent "chattering," hysteresis prevents excessive switching between modes in addition to ensuring that continuity is maintained. Dual-range operation is enabled by default (factory programmed in EEPROM). However, it can easily be disabled by the RSSIF and RSSIC bits, which are described later in this section. When dual-range operation is disabled, MON3 operates identically to the other MON channels, although featuring a differential input.

Dual-range functionality consists of two modes of operation: fine mode and course mode. Each mode is calibrated for a unique transfer function, hence the term "dual range." Table 7 highlights the registers related to MON3. Fine mode is equivalent to the other MON channels and is similar to the DS1859 and DS1856. Fine mode is calibrated using the gain, offset, and right shifting registers at locations shown in Table 7 and is ideal for relatively small analog input voltages. Course mode is automatically switched to when the input exceeds the threshold (to be discussed in a subsequent paragraph). Course mode is calibrated using different gain and offset registers, but lacks right shifting (since course mode is only used on large input signals). The gain and offset registers for course mode are also shown in Table 7. Additional information for each of the registers can be found in the memory map.

Dual-range operation is transparent to the end user. The results of MON3 analog-to-digital conversions are still stored/reported in the same memory locations (68 to 69h, Lower Memory) regardless of whether the conversion was performed in fine mode or course mode. The only way to tell which mode generated the digital result is by reading the RSSIS bit.

When the DS1864 is powered up, analog-to-digital conversions begin in a round-robin fashion. Every MON3 timeslice begins with a fine mode analog to digital conversion (using fine mode's gain, offset, and right-shifting settings). See the flowchart in Figure 15. Then, depending on whether the last MON3 timeslice resulted in a course mode conversion and also depending on the value of the current fine conversion, decisions are made whether to use the current fine mode conversion result or to make an additional conversion (within the same MON3 timeslice), using course mode (using course mode's gain and offset settings—and remember, no right shifting) and reporting the course mode result. The flowchart also illustrates how hysteresis is implemented. The fine mode conversion is compared to one of two thresholds. The actual threshold values are a function of the number of right shifts being used. Table 6 shows the threshold values for each possible number of right shifts.

The RSSIF and RSSIC bits are used to force fine mode or course mode conversions, or to disable the dual-range functionality. Dual-range functionality is enabled by default (both RSSIC and RSSIF are factory programmed to "0" in EEPROM). It can be disabled by setting RSSIC to 0 and RSSIF to 1. These bits are also useful when calibrating MON3. For additional information, see the *Memory Map*.

Fault Management

The DS1864 provides a variety of system alerts to help automate laser control. These alerts are in the form of fast-trip comparators, fast-trip alarm and warning thresholds, diagnostic alarm and warning thresholds, and configurable laser eye safety and shutdown logic. Fast-trip comparator values are measured against fast-trip thresholds to set alarms and to enable fault and

Table 6. MON3 Hysteresis Threshold Values

# OF RIGHT SHIFTS	FINE MODE MAX (HEX)	COURSE MODE MIN* (HEX)
0	FFF8	F000
1	7FFC	7800
2	3FFE	3C00
3	1FFF	1E00
4	0FFF	0F00
5	07FF	0780
6	03FF	03C0
7	01FF	01E0

**This is the minimum reported course mode conversion.*

Table 7. MON3 Configuration Registers

	FINE MODE	COURSE
GAIN REGISTER	98 to 99h, Table 04h*	9A to 9Bh, Table 04h*
OFFSET REGISTER	A8 to A9h, Table 04h*	AA to ABh, Table 04h*
RIGHT SHIFT REGISTER	8Fh, Table 04h*	N/A
RSSIC AND RSSIF BITS	8Ah, Table 04h*	
RSSIS BIT	77h, Lower Memory	
MON3 MEASUREMENT	68 to 69h, Lower Memory	

**Table 04h in DS1852 configuration or Table 01h in DS1859 configuration.*

shutdown signals. Alarm and warning thresholds keep the system functioning within user-programmed parameters. All alarm and warning flags are active high. Fast-trip alarms and warnings can be configured to overwrite the diagnostic flags for the same function. Laser safety features are also implemented to accept and send alarm signals to control laser activity.

Fast-Trips

The three monitor channels (MON1, MON2, and MON3) have associated fast channels. A sequencer with fast-trip comparators monitors the three voltage channels: MON1 (Bias Current (IBI)), MON2 (Transmitted Power (TXP)), and MON3 (Received Power (RIN)). These signals are the same raw (uncalibrated) signals used for the diagnostic circuits. Five fast-trip flags (alarms and warnings) are generated: high-bias alarm (HBAL), high-bias warning (HBWA), high transmitted power (HTXP), low transmitted power (LTXP), and loss of received signal (LOS), see Figure 12. These flags are located in Lower Memory, byte 73h. These flags are latched temporarily by design as required by the sequencer. In order to disable a comparator, set its threshold to 00h for low flags and FFh for high flags. The FT_enable bit (bit 3, byte 80h, Table 04h (Table 01h in DS1859 configuration)) determines if fast-trip alarms are enabled or disabled.

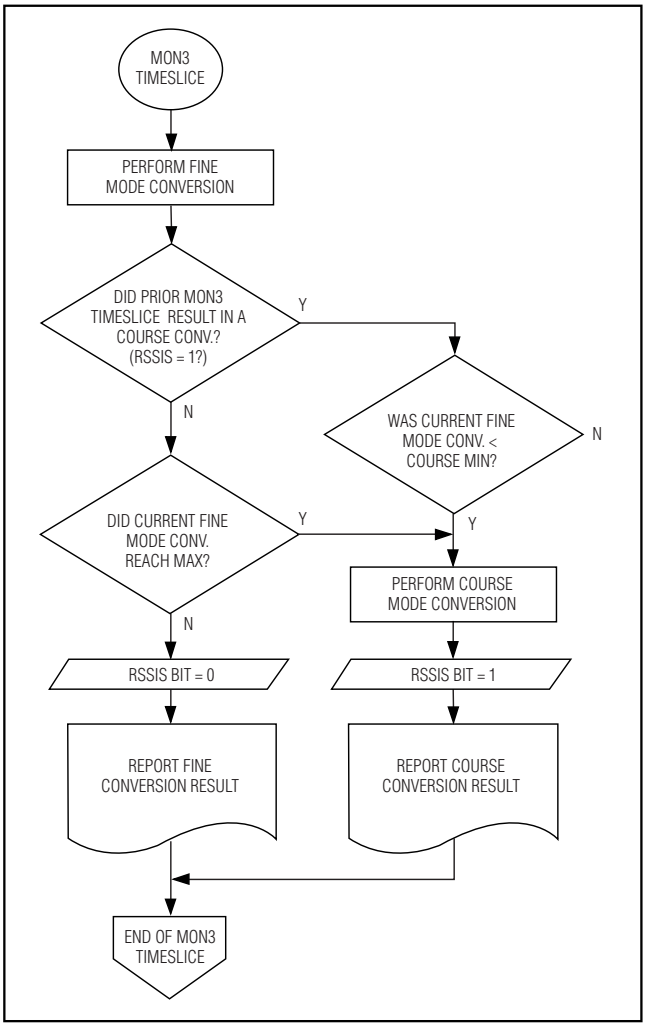

Figure 15. Dual-Range Functionality Flowchart

The thresholds for HBAL and HBWA can be programmed to be temperature compensated. Registers B0h to B7h for HBAL and B8h to BFh for HBWA of Table 04h (Table 01h in DS1859 configuration) are where the temperature-compensated alarm and warning thresholds are stored. Register DBh of Table 04h (Table 01h in DS1859 configuration) is the location of the HTXP programmable threshold. Register DCh of

Table 04h (Table 01h in DS1859 configuration) is the location of the LTXP programmable threshold. Register DDh of Table 04h (Table 01h in DS1859 configuration) is the location of the LOS programmable threshold.

Alarms and Warnings

There are ten comparators for alarms and ten comparators for warnings for the five analog channels: V_{CC}, Temperature, MON1, MON2, and MON3. These comparators have high and low threshold limits, which are used to determine when alarm and warning flags are triggered. A high alarm flag occurs when a comparator determines if the monitored analog value is above a programmable threshold. A low alarm flag occurs when a comparator determines if the monitored analog value is below a programmable threshold. The same applies for high and low warning flags, though warning flags are typically set to trip prior to the alarm flags. The programmable thresholds have a 2-byte set point in the same format as the ADC values stored in Lower Memory bytes 60h through 69h. The programmable high and low thresholds for both alarms and warnings are located in Lower Memory bytes 00h through 27h. The status bits for the alarm flags are located in Lower Memory bytes 70h and 71h. The status bits for the warning flags are located in Lower Memory bytes 74h and 75h. A high alarm or warning flag is set to a 1 when the corresponding digital value exceeds the user programmed high threshold. A low alarm or warning flag is set to a 1 when the corresponding digital value goes below the user-programmed low threshold. Comparisons of all measured values with high and low alarm and warning limits are done automatically.

The MASK bits control which flags can assert the maskable interrupt bit, MINT (bit 0, address 71h of the Lower Memory). The MASK bits are located in Table 01h, bytes F8h through FBh, or Table 05h, bytes F8h through FBh, depending on the state of the MASK bit (Table 04h (Table 01h in DS1859 configuration), byte DAh, bit 0). If the MASK bit is 0, then the values in addresses F8h through FBh in Table 05h will determine which flags will assert MINT. If the MASK bit is 1, then the values in addresses F8h through FBh in Table 01h (Table 00h in DS1859 configuration) will determine which flags will assert MINT.

TX-F, INTX-F, and TX-D

The TX-F pin is used to indicate a DAC shutdown and/or laser fault. See the logic diagram in Figure 12. The TXDC control bit (bit 6, byte 6Eh of the Lower Memory) is a software-controllable shutdown feature. It not only triggers TX-F to go active when set to a 1, but will also disable the DACs, shutting down the laser. The TX-D pin acts like a hardware version of the TXDC bit, triggering the TX-F pin and disabling the DACs when set high. The MINT interrupt bit discussed earlier also can trigger the TX-F pin if configured to enable when one of its alarm or warning flags goes high. Four fast-trip flags also can trigger TX-F to go active. The INTX-F pin, used for triggering from an externally generated transmit fault signal, can also be used to trigger the TX-F pin. The INV bit (bit 2, byte 89h, Table 04h (Table 01h in DS1859 configuration)) is used to invert the polarity of the TX-F pin. TXF bit (bit 2, byte 6Eh, Lower Memory) is a status bit that indicates the state of the output pin TX-F. The TX-F pin is not latched, except in the case of a shutdown fault. The status of TX-F will reset to inactive upon removal of the causes of the alarms, or upon resetting of the shutdown fault. The TX-F pin is open drain.

RX-LOS and INLOS

The RX-LOS pin is used to indicate a loss of received signal on the MON3 (Received Power) input. RX-LOS can be triggered by either the external signal, INLOS, or the internal alarm, LOS flag. INLOS is an input pin that can be used to indicate a loss of signal generated from an external source. LOS flag (bit 2, byte 73h of Lower Memory) can also be used to indicate a loss of signal. LOS flag is active high when the value of MON3 goes below its threshold, set by programming byte DDh of Table 04h (Table 01h in DS1859 configuration) to the desired limit. To configure which signal triggers RX-LOS, the LOSC bit (bit 6, byte 89h, Table 04h (Table 01h in DS1859 configuration)) is used. If LOSC = 1, INLOS is used to trigger the RX-LOS indicator. If LOSC = 0, then the LOSC flag is used. The final control bit for this logic is the INVL bit. The INVL bit (bit 0, byte 89h, Table 04h (Table 01h in DS1859 configuration)) is used to invert the polarity of the RX-LOS pin. The RX-LOS pin is open drain. See Figure 13 for details.

FETG Laser Safety Features

An auxiliary shutdown signal FETG can be asserted during a safety fault to disconnect the laser from its supply as a laser safety disconnect. The polarity of this signal is determined by the FPOL bit (bit 7, byte DAh in Table 04h (Table 01h in DS1859 configuration)). If FPOL is 1, then FETG is high in a shutdown condition. If FPOL is 0, then FETG is low in a shutdown condition.

A safety fault is a latched event that is generated from the fast-trip flags (LTXP, HBAL, and HTXP). These flags can be independently configured to initiate a safety fault using the enable bits (bits 4, 5, and 6 in byte DAh of Table 04h (Table 01h in DS1859 configuration)). A 1 for these bits enables that specific flag to generate a safety fault, while a 0 masks the flag. When a safety fault is generated, the DACs are disabled (forced to a high-impedance state), FETG is disabled (driven low),

and TX-F is set active. A falling edge of transmit disable (the logic OR of TX-D/TXDC) will initiate a safety fault recovery. At this point, the FETG output and the DACs are enabled. The TX-F output will not be disabled until a t_{INITR1} time later. LTXP is masked during this time period to allow for system recovery. HBAL and HTXP flags are not masked and will generate another safety fault if their appropriate limit is exceeded. A safety fault is not generated on standard shutdowns (the logic OR of TX-D/TXDC).

Power-Up and Low-Voltage Operation

During power-up, the device is inactive until V_{CC} exceeds the analog power-on-reset (V_{POA}), at which time the device becomes fully functional. Once V_{CC} exceeds V_{POA}, the RDYB bit (address byte 6Eh, bit 0) is timed to go from a 1 to a 0 and indicates when A/D conversions begin. If V_{CC} ever dips below V_{POA}, the RDYB bit reads as a 1 again. Once a device exceeds V_{POA} and the EEPROM is recalled, the values remain active (recalled) until V_{CC} falls below V_{POD}.

As the device powers up, the V_{CC} low alarm flag defaults to a 1 until the first V_{CC} A/D conversion occurs and sets or clears the flag accordingly.

Memory Organization

The DS1864 memory map is divided into seven sections that include Auxiliary Memory, Lower Memory, and five Upper Memory tables. The Upper Memory tables are addressed by setting the Table Select Byte (7Fh in the Lower Memory) to the desired table number and accessing the upper memory locations (80h to FFh). The Lower Memory and Auxiliary Device can be addressed at any time regardless of the state of the Table Select Byte. The Lower Memory and Table 04h (Table 01h in DS1859 configuration) are used to configure the DS1864 and read the status of the monitors. Memory Tables 02h and 03h contain the temperature indexed DAC Lookup Tables. Memory Tables 05h and 01h (Table 00h in DS1859 configuration) contain masks for alarm and warning flags. Table 01h (Table 00h in DS1859 configuration) also contains password settings. The Mode bit (bit 3, byte 89h in Table 04h (Table 01h in DS1859 configuration)) selects between DS1852/DS1856-compatible memory configuration or the DS1859-compatible memory configuration. See Figures 16 and 17 for more information.

Die Identification

DS1864 has an ID hard coded in its die. Three registers (Table 05h, bytes C0h to C2h) are assigned for this feature. Two registers are for the device ID, and a third register is for the version number. ID registers are hard-wired at the time of manufacture and are globally readable through the I^2C interface.

Memory Map Configurations

The default DS1864 memory configuration is compatible with the DS1852 memory map. The Mode bit (bit 3, register 89h of Table 04h (Table 01h in DS1859 configuration)) can be selected to make the DS1864 memory map compatible with the DS1859 memory map. Figure 16 shows the DS1852/DS1856 compatible configuration (default), and Figure 17 shows the DS1859-compatible configuration.

When the DS1864 is in the DS1852-compatible configuration, user memory is in Table 01h. In contrast, when the DS1864 is in the DS1859-compatible configuration (having set Mode to 1), user memory is in Table 00h. In addition, Table 04h in the DS1852 configuration will be reassigned as Table 01h in the DS1859 configuration.

Memory Protection and Passwords

The memory of the DS1864 is protected by two passwords, PW1 (user password) and a PW2 (vendor password). The password entry location for both passwords is in 7Bh-7Eh of Lower Memory and resides in SRAM. The PW2 password setting locations are in Table 04h (Table 01h in DS1859 configuration), registers C1h to C6h. The PW1 password settings are in Table 05h, registers D1h to D6h. Password setting and password entry bytes are write only (read as 0s).

Furthermore, the Auxiliary Memory and Main Device Memory are divided into eight blocks; see Table 9. The read and write protection for each block is activated by an enable bit. Two sets of enable bytes are used for both PW1 and PW2 level access, one byte to allow read access to the memory blocks and one byte for write access to the memory blocks. The two PW2 password enable bytes are located in Table 04h (Table 01h in DS1859 configuration), registers C1h and C2h. The PW1 password enable bytes are located in Table 05h, registers D1h and D2h. Table 8 shows how the password enable bytes can be configured to protect the memory blocks. Table 9 shows the bit assignments for each of the eight blocks of DS1864 memory. See the registers mentioned above in the *Memory Map* section for more details.

Note that regardless of read/write permissions for a given table, password settings and password entry are unconditionally read protected. They are write protected if the proper write enable bit is set to 1. Bytes 78h to 7Fh in Lower Memory are unprotected.

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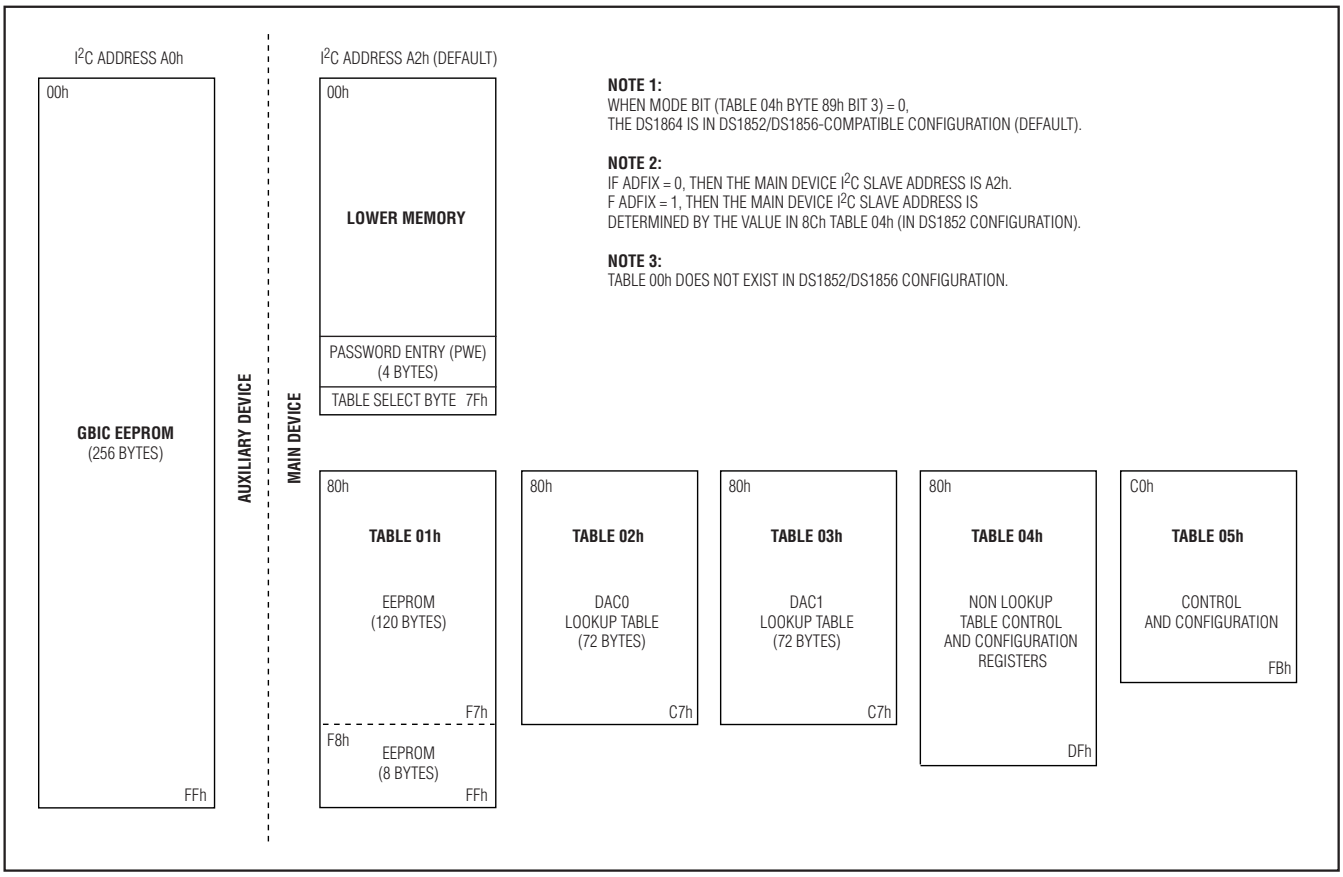

Figure 16. DS1852/DS1856-Compatible Configuration (Mode Bit = 0, Default)

EEPROM Write Disable

The $\overline{SEE}$ control bit resides in Table 04h (Table 01h in DS1859 configuration), register 80h, bit 2. By default ($\overline{SEE}$ bit = 0) these locations act as ordinary EEPROM. By setting $\overline{SEE}$ = 1, these locations function as SRAM memory allowing an infinite number of write cycles. This also eliminates the requirement for the EEPROM write time. Because changes made with $\overline{SEE}$ = 1 do not effect the EEPROM, these changes will not be retained through power cycles. The power-up value will be the last value written with $\overline{SEE}$ = 0.

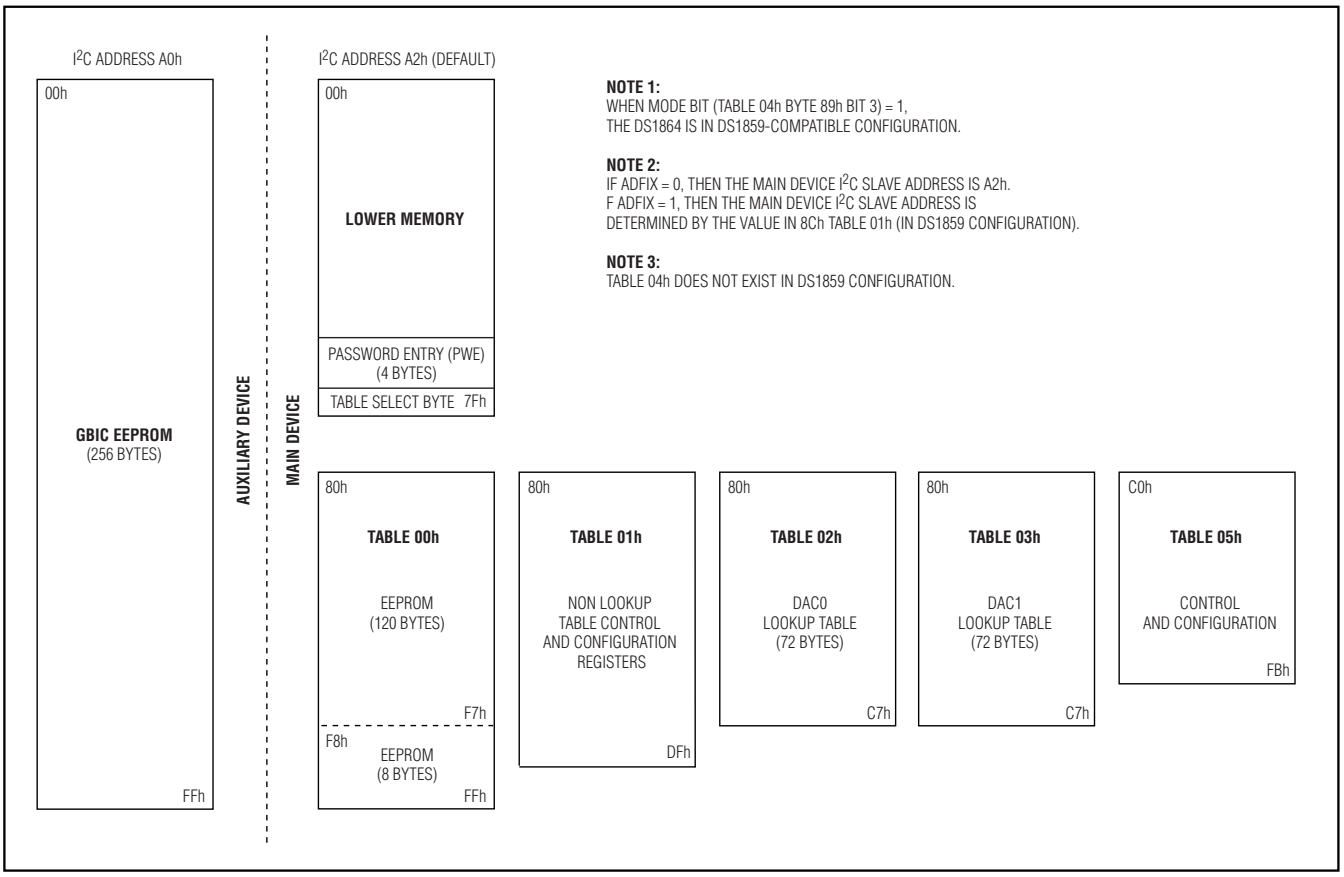

Figure 17. DS1859-Compatible Configuration (Mode Bit = 1)