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19-5044; Rev 1; 11/09

PON Triplexer Control and Monitoring Circuit

DS1865

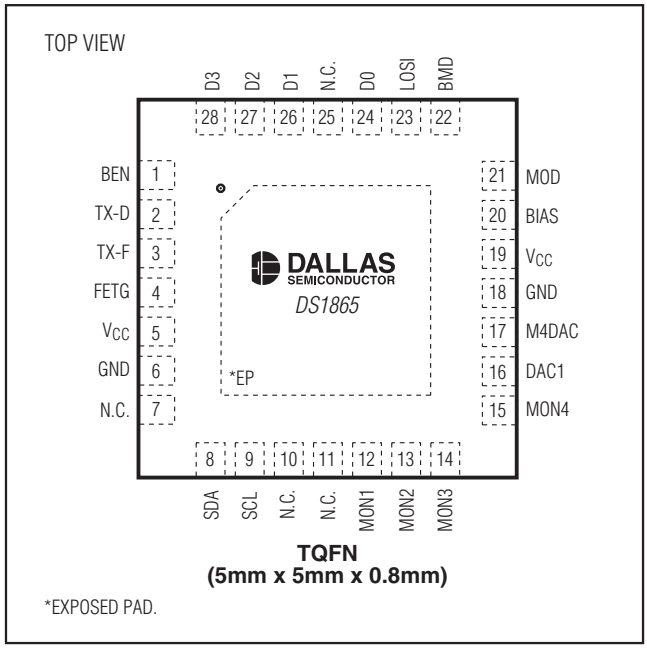
General Description

The DS1865 controls and monitors all the burst-mode transmitter and video receiver biasing functions for a passive optical network (PON) triplexer. It has an APC loop with tracking-error compensation that provides the reference for the laser driver bias current and a temperature-indexed lookup table (LUT) that controls the modulation current. It continually monitors for high output current, high bias current, and low and high transmit power with its internal fast comparators to ensure that laser shutdown for eye safety requirements are met without adding external components. Six ADC channels monitor V_{CC}, internal temperature, and four external monitor inputs (MON1–MON4) that can be used to meet transmitter and video receive signal monitoring requirements. Two digital-to-analog converter (DAC) outputs are available for biasing the video receiver channel, and five digital I/O pins are present to allow additional monitoring and configuration.

Applications

Optical Triplexers with GEPON, BPON, or GPON Transceiver

Pin Configuration



TQFN
(5mm x 5mm x 0.8mm)

*EXPOSED PAD.

Features

- **Meets GEPON, BPON, and GPON Timing Requirements for Burst-Mode Transmitters**
- **Bias Current Control Provided by APC Loop with Tracking-Error Compensation**
- **Modulation Current is Controlled by a Temperature-Indexed Lookup Table**
- **Laser Power Leveling from -6dB to +0dB**
- **Two 8-Bit Analog Outputs, One is Controlled by MON4 Voltage for Video Amplifier Gain Control**
- **Internal Direct-to-Digital Temperature Sensor**
- **Six Analog Monitor Channels: Temperature, V_{CC}, MON1, MON2, MON3, and MON4**
- **Five Digital I/O Pins for Additional Control and Monitoring Functions**
- **Comprehensive Fault Management System with Maskable Laser Shutdown Capability**
- **Two-Level Password Access to Protect Calibration Data**
- **120 Bytes of Password 1 Protected Nonvolatile Memory**
- **128 Bytes of Password 2 Protected Nonvolatile Memory in Main Device Address**
- **128 Bytes of Nonvolatile Memory Located at A0h Slave Address**
- **I^2C-Compatible Interface for Calibration and Monitoring**
- **Operating Voltage: 2.85V to 3.9V**
- **Operating Temperature Range: -40°C to +95°C**
- **Packaging: 28-Pin Lead-Free TQFN (5mm x 5mm x 0.8mm)**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
DS1865T+	-40°C to +95°C	28 TQFN-EP*
DS1865T+T&R	-40°C to +95°C	28 TQFN-EP*

+Denotes a lead(Pb)-free/RoHS-compliant package.
**EP = Exposed pad.*
T&R = Tape and reel.

PON Triplexer Control and Monitoring Circuit

ABSOLUTE MAXIMUM RATINGS

Voltage Range on MON1–MON4, BEN, BMD, and TX-D Pins Relative to Ground.....-0.5V to (V_{CC} + 0.5V) (subject to not exceeding +6V)
Voltage Range on V_{CC}, SDA, SCL, D0–D3, and TX-F Pins Relative to Ground .....-0.5V to +6V

Operating Temperature Range .....-40°C to +95°C
Programming Temperature Range .....0°C to +70°C
Storage Temperature Range .....-55°C to +125°C
Soldering Temperature.....See J-STD-020 Specification

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

(T_A = -40°C to +95°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	V_{CC}	(Note 1)	+2.85		+3.9	V
High-Level Input Voltage (SDA, SCL, BEN)	$V_{IH:1}$		0.7 x V_{CC}		V_{CC} + 0.3	V
Low-Level Input Voltage (SDA, SCL, BEN)	$V_{IL:1}$		-0.3		0.3 x V_{CC}	V
High-Level Input Voltage (TX-D, LOSI, D0, D1, D2, D3)	$V_{IH:2}$		2.0		V_{CC} + 0.3	V
Low-Level Input Voltage (TX-D, LOSI, D0, D1, D2, D3)	$V_{IL:2}$		-0.3		0.8	V

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = +2.85V to +3.9V, T_A = -40°C to +95°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current	I_{CC}	(Notes 1, 2)		5	10	mA
Output Leakage (SDA, TX-F, D0, D1, D2, D3)	I_{LO}				1	µA
Low-Level Output Voltage (SDA, TX-F, FETG, D0, D1, D2, D3)	V_{OL}	I_{OL} = 4mA			0.4	V
		I_{OL} = 6mA			0.6	
High-Level Output Voltage (FETG)	V_{OH}	I_{OH} = 4mA	V_{CC} - 0.4			V
FETG Before Recall		(Note 3)		10	100	nA
Input-Leakage Current (SCL, BEN, TX-D, LOSI)	I_{LI}				1	µA
Digital Power-On Reset	POD		1.0		2.2	V
Analog Power-On Reset	POA		2.1		2.75	V

ELECTRICAL CHARACTERISTICS (DAC1 and M4DAC)

(V_{CC} = +2.85V to +3.9V, T_A = -40°C to +95°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DAC Output Range			0		2.5	V
DAC Output Resolution				8		Bits
DAC Output Integral Nonlinearity			-2		+2	LSB
DAC Output Differential Nonlinearity			-1		+1	LSB
DAC Error		T_A = +25°C	-1.25		+1.25	LSB
DAC Temperature Drift			-2		+2	% FS
DAC Offset		V_{CC} = 2.85V to 3.6V	-20		+20	µV
Maximum Load			-500		+500	µA
Maximum Load Capacitance					250	pF

ANALOG INPUT CHARACTERISTICS (BMD, TXP-HI, TXP-LO, HBIAS)

(V_{CC} = +2.85V to +3.9V, T_A = -40°C to +95°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
BMD, TXP-HI, TXP-LO Full-Scale Voltage	V_{APC}	(Note 4)		2.5		V
HBIAS Full-Scale Voltage				1.25		mA
BMD Input Resistance			35	50	65	kΩ
Resolution		(Note 4)		8		Bits
Error		T_A = +25°C (Note 5)		±2		%FS
Integral Nonlinearity			-1		+1	LSB
Differential Nonlinearity			-1		+1	LSB
Temperature Drift			-2.5		+2.5	%FS

ANALOG OUTPUT CHARACTERISTICS

(V_{CC} = +2.85V to +3.9V, T_A = -40°C to +95°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
BIAS Current	I_{BIAS}	(Note 1)		1.2		mA
I_{BIAS} Shutdown Current	$I_{BIAS:OFF}$			10	100	nA
Voltage at I_{BIAS}			0.7	1.2	1.4	V
MOD Full-Scale Voltage	V_{MOD}	(Note 6)		1.25		V
MOD Output Impedance		(Note 7)		3		kΩ
V_{MOD} Error		T_A = +25°C (Note 8)	-2.5		+2.5	%FS
V_{MOD} Integral Nonlinearity			-3		+3	LSB
V_{MOD} Differential Nonlinearity			-1		+1	LSB
V_{MOD} Temperature Drift			-2		+2	%FS

PON Triplexer Control and Monitoring Circuit

ANALOG VOLTAGE MONITORING

(V_{CC} = +2.85V to +3.9V, T_A = -40°C to +95°C, unless otherwise noted.)

PARAMETER		SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Resolution		ΔVMON			610		µV
Supply Resolution		ΔV_{CC}			1.6		mV
Input/Supply Accuracy (MON1, MON2, MON3, MON4, V_{CC})		A_{CC}	At factory setting		0.25	0.5	% FS (full scale)
Update Rate for MON1, MON2, MON3, MON4 Temp, or V_{CC}		t_{FRAME}			30	45	ms
Input/Supply Offset (MON1, MON2, MON3, MON4, V_{CC})		V_{OS}	(Note 14)		0	5	LSB
Factory Setting	MON1, MON2, MON3, MON4				2.5		V
	V_{CC}				6.5536		

DIGITAL THERMOMETER

(V_{CC} = +2.85V to +3.9V, T_A = -40°C to +95°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Thermometer Error	T_{ERR}	-40°C to +95°C			±3.0	°C

TIMING CHARACTERISTICS (CONTROL LOOP AND QUICK-TRIP)

(V_{CC} = +2.85V to +3.9V, T_A = -40°C to +95°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
First MD Sample Following BEN	t_{FIRST}	(Note 9)				
Remaining Updates During BEN	t_{UPDATE}	(Note 9)				
BEN High Time	$t_{BEN:HIGH}$		400			ns
BEN Low Time	$t_{BEN:LOW}$		96			ns
Output-Enable Time Following POA	t_{INIT}		10			ms
BIAS and MOD Turn-Off Delay	t_{OFF}				5	µs
BIAS and MOD Turn-On Delay	t_{ON}				5	µs
FETG Turn-On Delay	$t_{FETG:ON}$				5	µs
FETG Turn-Off Delay	$t_{FETG:OFF}$				5	µs
Binary Search Time	t_{SEARCH}	(Note 10)	5		13	BIAS Samples
ADC Round-Robin Time	t_{RR}				75	ms

I²C AC ELECTRICAL CHARACTERISTICS

(V_{CC} = +2.85V to +3.9V, T_A = -40°C to +95°C, timing referenced to $V_{IL(MAX)}$ and $V_{IH(MIN)}$.) (See Figure 9.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SCL Clock Frequency	f_{SCL}	(Note 11)	0		400	kHz
Clock Pulse-Width Low	t_{LOW}		1.3			µs
Clock Pulse-Width High	t_{HIGH}		0.6			µs
Bus-Free Time Between STOP and START Condition	t_{BUF}		1.3			µs
Start Hold Time	$t_{HD:STA}$		0.6			µs
Start Setup Time	$t_{SU:STA}$		0.6			µs
Data in Hold Time	$t_{HD:DAT}$		0		0.9	µs
Data in Setup Time	$t_{SU:DAT}$		100			ns
Rise Time of Both SDA and SCL Signals	t_R	(Note 12)	$20 + 0.1C_B$		300	ns
Fall Time of Both SDA and SCL Signals	t_F	(Note 12)	$20 + 0.1C_B$		300	ns
STOP Setup Time	$t_{SU:STO}$		0.6			µs
Capacitive Load for Each Bus Line	C_B	(Note 12)			400	pF
EEPROM Write Time	t_W	(Note 13)			20	ms

NONVOLATILE MEMORY CHARACTERISTICS

(V_{CC} = +2.85V to +3.9V)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
EEPROM Write Cycles		At +70°C	50,000			

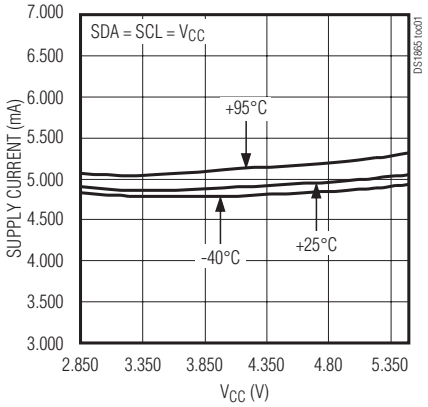
Note 1: All voltages are referenced to ground. Current into IC is positive, out of the IC is negative.
Note 2: Digital inputs are at rail. FETG is disconnected. SDA = SCL = V_{CC}. DAC1 and M4DAC are not loaded.
Note 3: See the *Safety Shutdown (FETG) Output* section for details.
Note 4: Eight ranges allow the full-scale range to change from 625mV to 2.5V.
Note 5: This specification applies to the expected full-scale value for the selected range. See the Comp Ranging byte for available full-scale ranges.
Note 6: Eight ranges allow the BMD full-scale range to change from 312.5mV to 1.25V.
Note 7: The output impedance of the DS1865 is proportional to its scale setting. For instance, if using the 1/2 scale, the output impedance would be approximately 1.56kΩ.
Note 8: This specification applies to the expected full-scale value for the selected range. See the Mod Ranging byte for available full-scale ranges.
Note 9: See the *APC and Quick-Trip Shared Comparator Timing* section for details.
Note 10: Assuming an appropriate initial step is programmed that would cause the power to exceed the APC set point within four steps, the bias current will be 1% within the time specified by the binary search time. See the *Bias and MOD Output During Power-Up* section.
Note 11: I²C interface timing shown is for fast-mode (400kHz) operation. This device is also backward-compatible with the I²C standard mode.
Note 12: C_B—total capacitance of one bus line in picofarads.
Note 13: EEPROM write begins after a STOP condition occurs.
Note 14: Guaranteed by design.

PON Triplexer Control and Monitoring Circuit

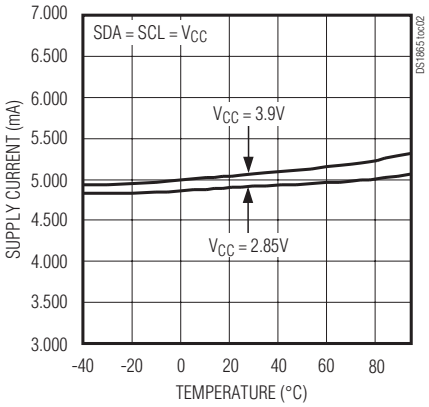
Typical Operating Characteristics

(V_{CC} = 3.3V, T_A = +25°C, unless otherwise noted.)

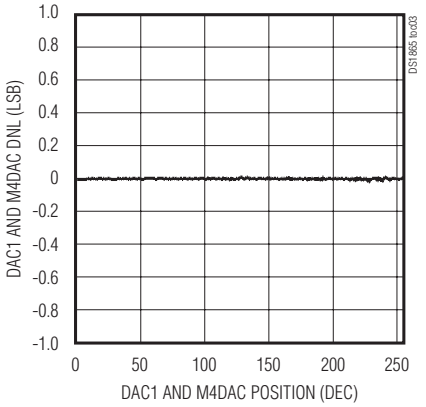
SUPPLY CURRENT vs. SUPPLY VOLTAGE



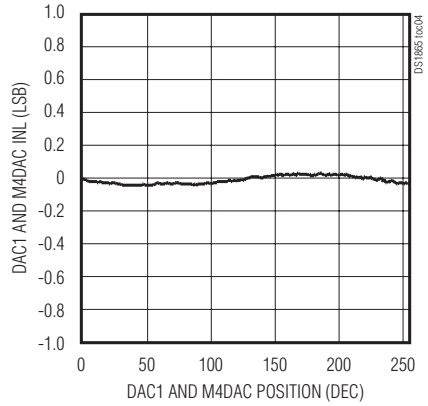
SUPPLY CURRENT vs. TEMPERATURE



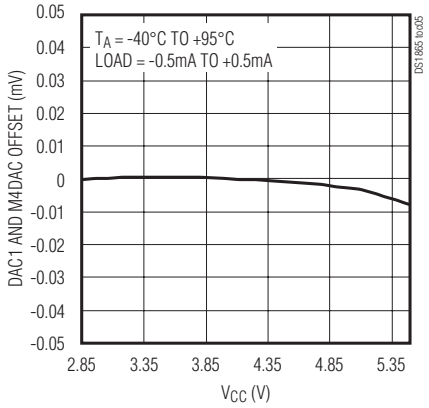
DAC1 AND M4DAC DNL



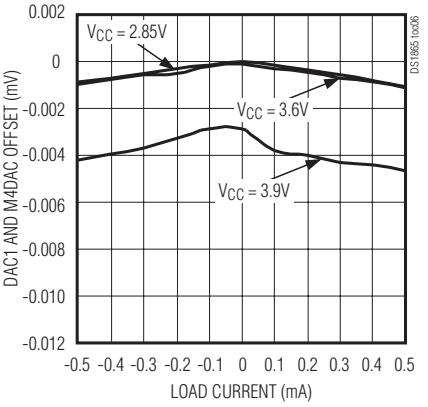
DAC1 AND M4DAC INL



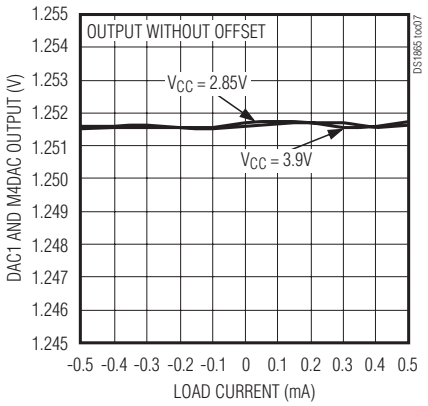
DAC1 AND M4DAC OFFSET vs. V_{CC}



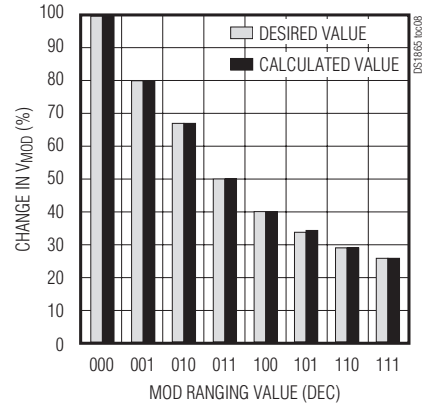
DAC1 AND M4DAC OFFSET VARIATION vs. LOAD CURRENT



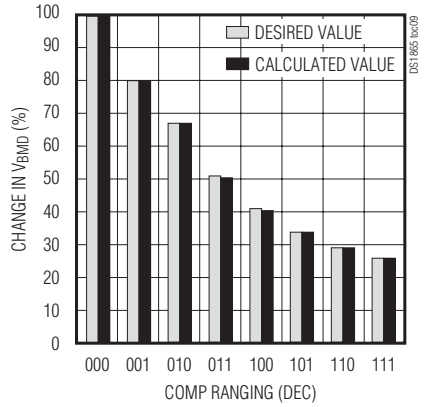
DAC1 AND M4DAC OUTPUT vs. LOAD CURRENT



CALCULATED AND DESIRED % CHANGE IN V_{MOD} vs. MOD RANGING



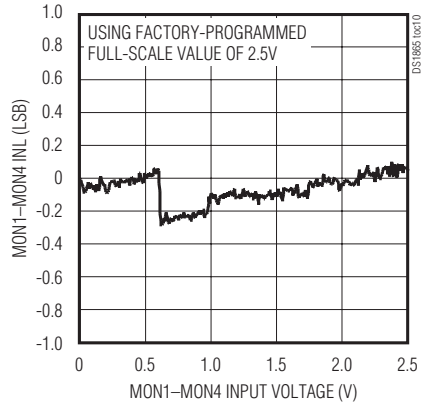
DESIRED AND CALCULATED CHANGE IN V_{BMD} vs. COMP RANGING



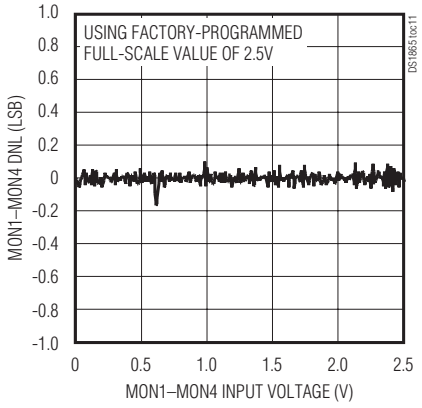
Typical Operating Characteristics (continued)

(V_{CC} = 3.3V, T_A = +25°C, unless otherwise noted.)

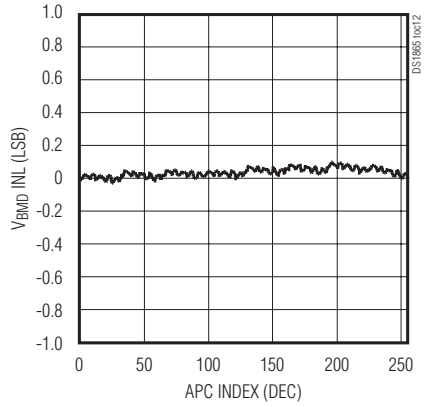
MON1–MON4 INL



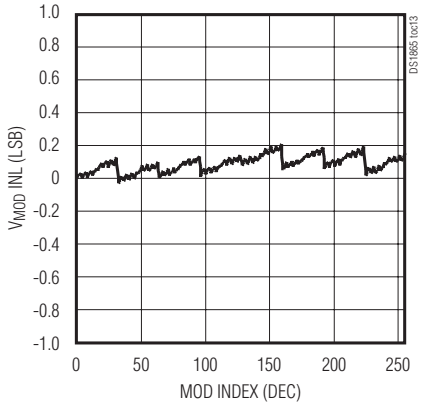
MON1–MON4 DNL



V_{BMD} INL vs. APC INDEX



V_{MOD} INL vs. MOD INDEX

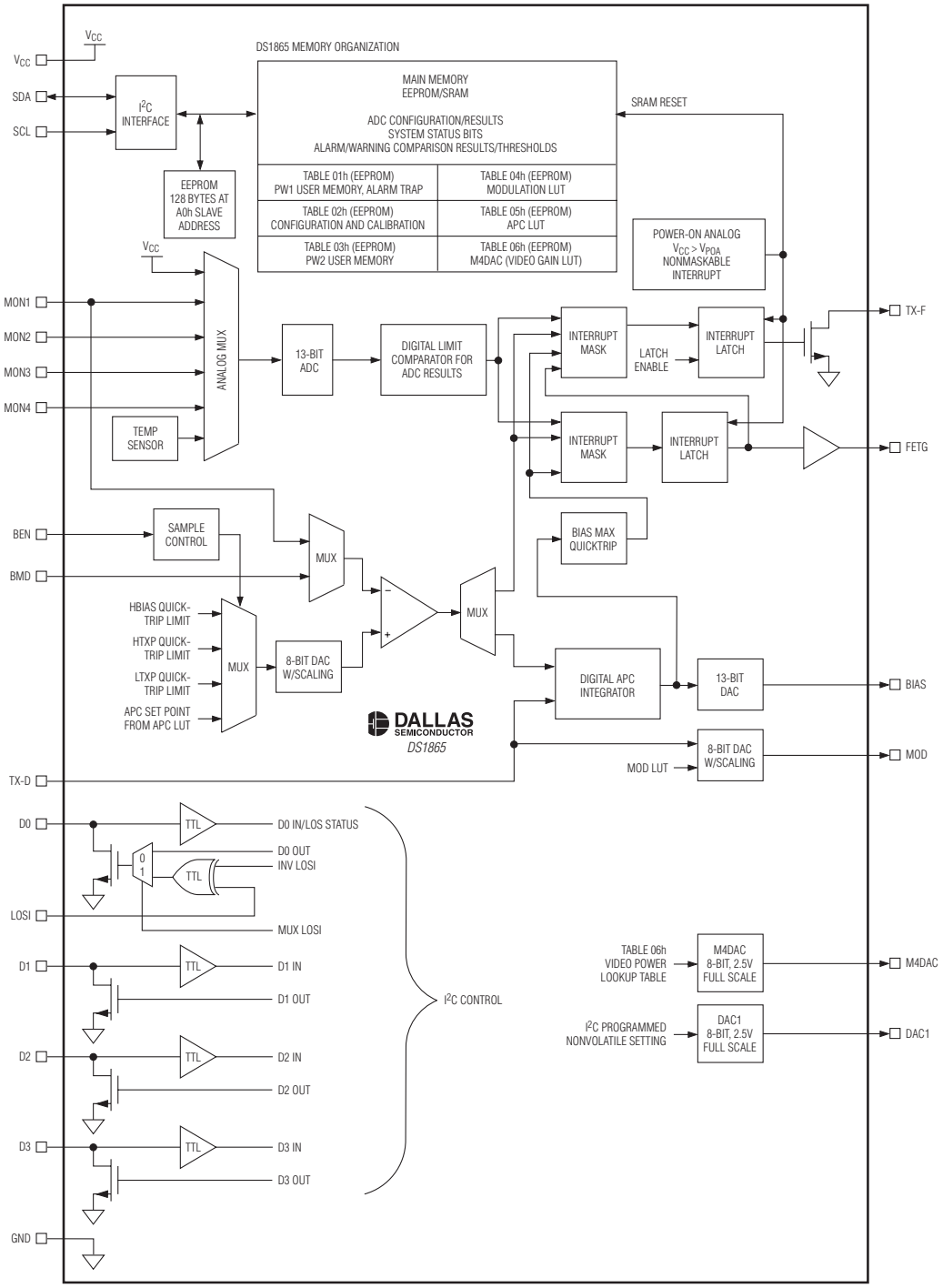


PON Triplexer Control and Monitoring Circuit

Pin Description

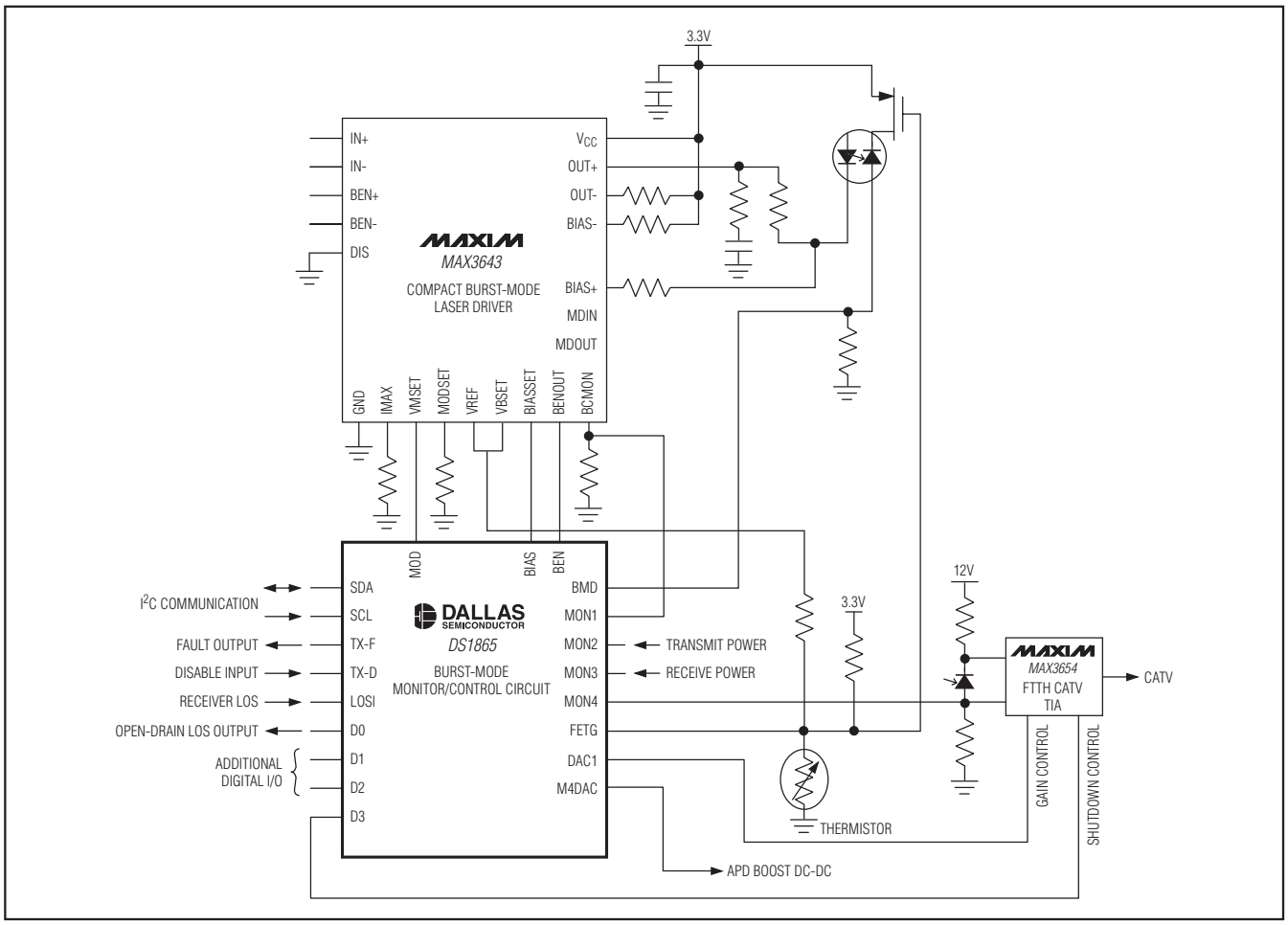
PIN	NAME	FUNCTION
1	BEN	Burst Enable Input. Triggers the sampling of the APC and quick-trip monitors.
2	TX-D	Transmit Disable Input. Disables BIAS and MOD outputs.
3	TX-F	Transmit Fault Output, Open Drain
4	FETG	Output to FET Gate. Signals an external n- or p-channel MOSFET to enable/disable the laser's current.
5, 19	V_{CC}	Supply Voltage
6, 18	GND	Ground
7, 10, 11, 25	N.C.	No Connection
8	SDA	I^2C Serial Data. Input/output for I^2C data.
9	SCL	I^2C Serial Clock. Input for I^2C clock.
12–15	MON1–MON4	External Monitor Input 1–4. The voltage at these pins are digitized by the internal analog-to-digital converter and can be read through the I^2C interface. Alarm and warning values can be assigned to interrupt the processor based on the ADC result.
16	DAC1	Digital-to-Analog Output DAC1 and M4DAC. Two 8-bit DAC outputs for generating analog voltages. Typically used to control the video photodiode bias. M4DAC is controlled by the input voltage on MON4 and Table 06h LUT.
17	M4DAC	
20	BIAS	Bias Current Output. This current DAC generates the bias current reference for the MAX3643.
21	MOD	Modulation Output Voltage. This 8-bit voltage output has eight full-scale ranges from 1.25V to 0.3125V. This pin is connected to the MAX3643's VMSET input to control the modulation current.
22	BMD	Monitor Diode Input (Feedback Voltage, Transmit Power Monitor)
23	LOSI	Loss-of-Signal Input. This input is accessible in the status register through the I^2C interface.
24	D0	Digital I/O 0. This signal is either the open-drain output driver for LOSI, or can be controlled by the OUT0 bit (D0OUT). The logic level of this pin is indicated by the D0IN and LOS status bits.
26, 27, 28	D1, D2, D3	Digital I/O 1–3. These are bidirectional pins controlled by internally addressable bits. The outputs are open-drain.
—	EP	Exposed Pad. This contact should be connected to GND.

Block Diagram



PON Triplexer Control and Monitoring Circuit

Typical Operating Circuit



Detailed Description

The DS1865 integrates the control and monitoring functionality required to implement a PON system using Maxim's MAX3643 compact burst-mode laser driver. The compact laser driver solution offers a considerable cost benefit by integrating control and monitoring features in the low-power CMOS process, while leaving only the high-speed portions to the laser driver. Key components of the DS1865 are shown in the *Block Diagram* and described in subsequent sections. Table 1 contains a list of acronyms used in this data sheet.

APC Control

BIAS current is controlled by an average power control (APC) loop. The APC loop uses digital techniques to overcome the difficulties associated with controlling burst-mode systems.

Table 1. Acronyms

ACRONYM	DEFINITION
ADC	Analog-to-Digital Converter
APC	Average Power Control
ATB	Alarm Trap Bytes
DAC	Digital-to-Analog Converter
LUT	Lookup Table
NV	Nonvolatile
PON	Passive Optical Network
QT	Quick Trip
SEE	Shadowed EEPROM
TE	Tracking Error
TXP	Transmit Power

The APC loop's feedback is the monitor diode (BMD) current, which is converted to a voltage using an external resistor. The feedback voltage is compared to an 8-bit scaleable voltage reference that determines the APC set point of the system. Scaling of the reference voltage accommodates the wide range in photodiode sensitivities. This allows the application to take full advantage of the APC reference's resolution.

The DS1865 has an LUT to allow the APC set point to change as a function of temperature to compensate for tracking error (TE). The TE LUT (Table 05h) has 36 entries that determine the APC setting in 4°C windows between -40°C to +100°C. Ranging of the APC DAC is possible by programming a single byte in Table 02h.

Modulation Control

The MOD output is an 8-bit scaleable voltage output that interfaces with the MAX3643's VMSET input. An external resistor to ground from the MAX3643's MODSET pin sets the maximum current the voltage at VMSET input can produce for a given output range. This resistor value should be chosen to produce the maximum modulation current the laser type requires over temperature. Then the MOD output's scaling is used to calibrate the full-scale (FS) modulation output to a particular laser's requirements. This allows the application to take full advantage of the MOD output's resolution. The modulation LUT can be programmed in 2°C increments over the -40°C to +102°C range.

Ranging of the MOD DAC is possible by programming a single byte in Table 02h.

BIAS and MOD Output During Power-Up

On power-up, the modulation and bias outputs remain off until V_{CC} is above V_{POA} and a temperature conversion has been completed. If the V_{CC} LO ADC alarm is enabled, then a V_{CC} conversion above the customer-defined V_{CC} low alarm level is required before the outputs are enabled with the value determined by the temperature conversion and the modulation LUT.

When the MOD output is enabled and BEN is high, the BIAS output is turned on to a value equal to I_{STEP} (see Figure 1). The startup algorithm checks if this bias current causes a feedback voltage above the APC set point, and if it does not it continues increasing the BIAS by I_{STEP} until the APC set point is exceeded. When the APC set point is exceeded, the DS1865 begins a binary search to quickly reach the bias current corresponding to the proper power level. After the binary search is completed the APC integrator is enabled, and single LSB steps are taken to tightly control the average power.

All quick-trip alarm flags are masked until the binary search is completed. However, the BIAS MAX alarm is monitored during this time to prevent the bias output from exceeding MAX IBIAS. During the bias current initialization, the bias current is not allowed to exceed MAX IBIAS. If this occurs during the I_{STEP} sequence, the binary search routine begins. If MAX IBIAS is exceeded during the binary search, the next smaller step is activated. I_{STEP} or binary increments that would cause I_{BIAS} to exceed MAX IBIAS are not taken. Masking the alarms until the completion of the binary search prevents false trips during startup.

I_{STEP} is programmed by the customer using the Startup Step register. This value should be programmed to the maximum safe current increase that is allowable during startup. If this value is programmed too low, the DS1865 will still operate, but it could take significantly longer for the algorithm to converge and hence to control the average power.

If a fault is detected and TX-D is toggled to re-enable the outputs, the DS1865 powers up following a similar sequence to an initial power-up. The only difference is that the DS1865 already has determined the present temperature, so the t_{INIT} time is not required for the DS1865 to recall the APC and MOD set points from EEPROM.

If the Bias-En bit (Table 02h, Register 80h) is written to 0, the BIAS DAC is manually controlled by the MAN IBIAS register (Table 02h, Registers F8h–F9h).

BIAS and MOD Output as a Function of Transmit Disable (TX-D)

If the TX-D pin is asserted (logic 1) during normal operation, the outputs are disabled within t_{OFF}. When TX-D is deasserted (logic 0), the DS1865 turns on the MOD output with the value associated with the present temperature, and initializes the BIAS using the same search algorithm used at startup. When asserted, the soft TX-D (Lower Memory, Register 6Eh) offers a software control identical to the TX-D pin (see Figure 2).

APC and Quick-Trip Shared Comparator Timing

As shown in Figure 3, the DS1865's input comparator is shared between the APC control loop and the three quick-trip alarms (TXP-HI, TXP-LO, and BIAS HI). The comparator polls the alarms in a round-robin multiplexed sequence. Six of every eight comparator readings are used for APC loop-bias current control. The other two updates are used to check the HTXP/LTXP (monitor diode voltage) and the HBIAS (MON1) signals against the internal APC and BIAS reference. The HTXP/LTXP comparison checks HTXP to see if the last

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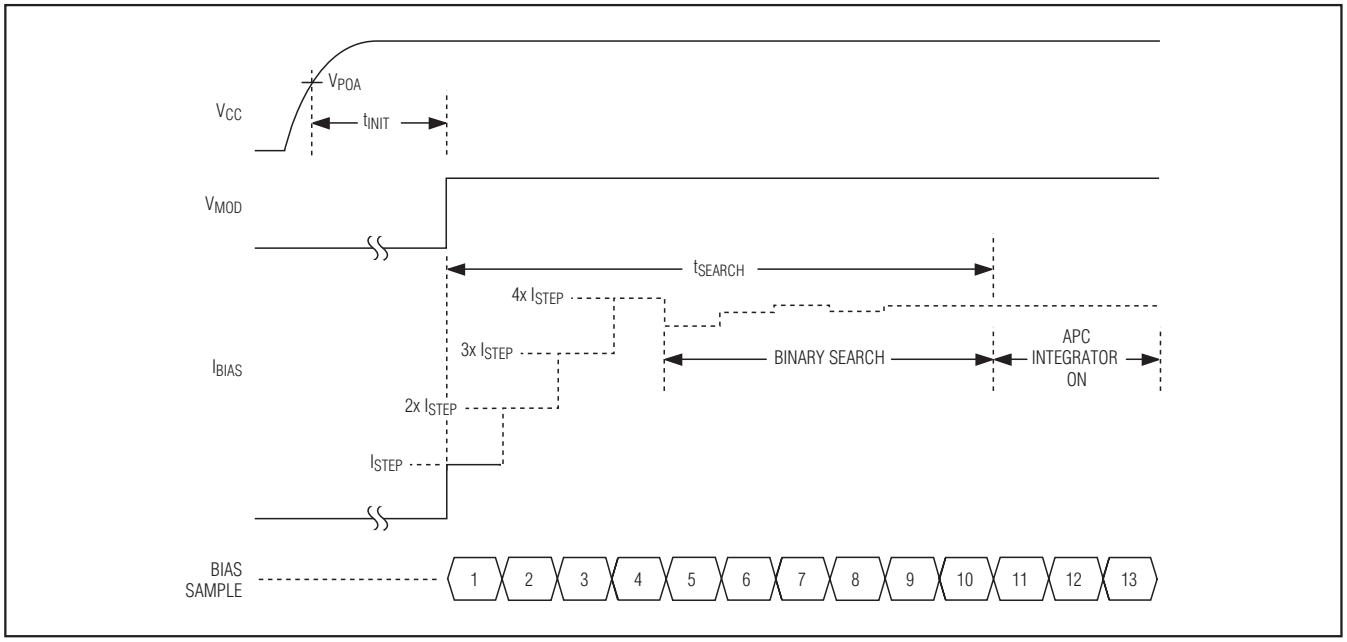

Figure 1. Power-Up Timing

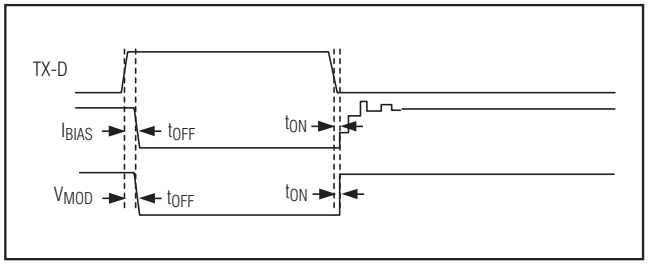

Figure 2. TX-D Timing (Normal Operating Conditions)

bias update comparison was above the APC set point, and checks LTXP to see if the last bias update comparison was below the APC set point. Depending on the results of the comparison, the corresponding alarms and warnings (TXP-HI, TXP-LO) are asserted or deasserted.

The DS1865 has a programmable comparator sample time based on an internally generated clock to facilitate a wide variety of external filtering options suitable for burst-mode transmitter data rates between 155Mbps and 1250Mbps. The rising edge of the burst enable (BEN) triggers the sample to occur, and the Update Rate register (Table 02h, Register 88h) determines the sampling time. The first sample occurs t_{FIRST} after the rising edge of BEN. The internal clock is asynchronous to BEN, causing a ±50ns uncertainty regarding when the first sample will occur following BEN. After the first sample occurs, subsequent samples occur on a regular interval, t_{REP}. Table 2 shows the sample rate options available.

Table 2. Update Rate Timing

SR_3–SR_0	MINIMUM TIME FROM BEN TO FIRST SAMPLE (t_{FIRST}) ±50ns	REPEATED SAMPLE PERIOD FOLLOWING FIRST SAMPLE (t_{REP})
0000b	350ns	800ns
0001b	550ns	1200ns
0010b	750ns	1600ns
0011b	950ns	2000ns
0100b	1350ns	2800ns
0101b	1550ns	3200ns
0110b	1750ns	3600ns
0111b	2150ns	4400ns
1000b	2950ns	6000ns
1001b*	3150ns	6400ns

**All codes greater than 1001b (1010b–1111b) use the maximum sample time of code 1001b.*

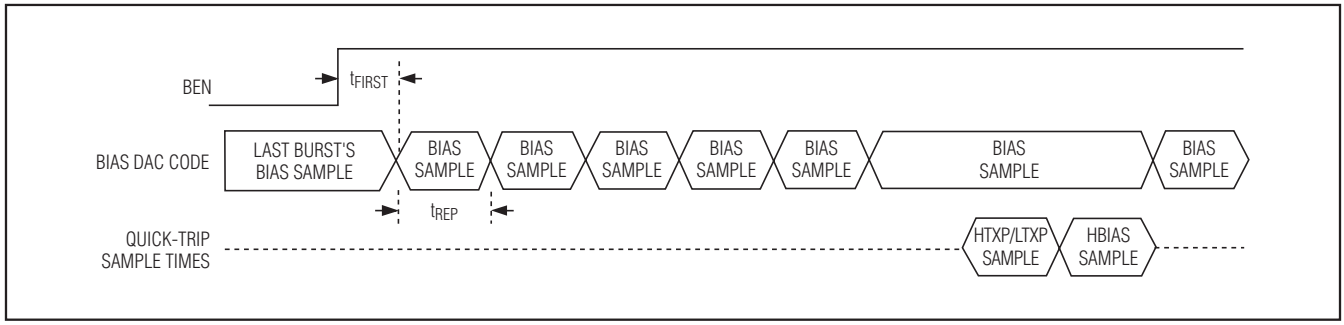

Figure 3. APC and Quick-Trip Alarm Sample Timing

Updates to the TXP-HI, TXP-LO, and BIAS HI quick-trip alarms do not occur during the burst-enable low time. Any quick-trip alarm that is detected by default remains active until a subsequent comparator sample shows the condition no longer exists.

A second bias-current monitor (BIAS MAX) compares the DS1865's BIAS DAC's code to a digital value stored in the MAX IBIAS register. This comparison is made every bias-current update to ensure that a high bias current is quickly detected.

Monitors and Fault Detection

Monitors

Monitoring functions on the DS1865 include four quick-trip comparators and six ADC channels. This monitoring, combined with the interrupt masks, determines when/if the DS1865 shuts down its outputs and triggers the TX-F and FETG outputs. All the monitoring levels and interrupt masks are user programmable.

Four Quick-Trip Monitors and Alarms

Four quick-trip monitors are provided to detect potential laser safety issues. These monitor:

1) High Bias Current (HBIAS)
2) Low Transmit Power (LTXP)
3) High Transmit Power (HTXP)
4) Max Output Current (MAX IBIAS)

The high and low transmit power quick-trip registers (HTXP and LTXP) set the thresholds used to compare against the BMD voltage to determine if the transmit power is within specification. The HBIAS quick-trip compares the MON1 input (generally from the MAX3643 bias monitor output) against its threshold setting to determine if the present bias current is above specification. The BIAS MAX quick-trip is a digital comparison that determines if the BIAS DAC indicates that the bias current is above specification. I_{BIAS} is not allowed to exceed the value set in the MAX IBIAS register. When the DS1865 detects that the bias is at the limit, it sets the BIAS MAX status bit and holds the bias current at the MAX IBIAS level. The quick-trips are routed to the TX-F and FETG outputs through interrupt masks to allow combinations of these alarms to be used to trigger these outputs. When FETG is triggered, the DS1865 also disables the MOD and BIAS outputs. See the *BIAS and MOD Output During Power-Up* section for details.

Six ADC Monitors And Alarms

The ADC monitors six channels that measure temperature (internal temp sensor), V_{CC}, MON1, MON2, MON3, and MON4 using an analog multiplexer to measure them round-robin with a single ADC. Each channel has a customer-programmable full-scale range and offset value that is factory programmed to a default value (see Table 3). Additionally, MON1–MON4 can right shift results by up to 7 bits before the results are compared to alarm thresholds or read over the I^2C bus. This allows customers with specified ADC ranges to calibrate the ADC full scale to a factor of $1/2^n$ of their specified range to measure small signals. The DS1865 can then right shift the results by n bits to maintain the bit weight of their specification.

Table 3. ADC Default Monitor Full-Scale Ranges

SIGNAL (UNITS)	+FS SIGNAL	+FS HEX	-FS SIGNAL	-FS HEX
Temperature (°C)	127.996	7FFF	-128	8000
V_{CC} (V)	6.5528	FFF8	0V	0000
MON1–MON4 (V)	2.4997	FFF8	0V	0000

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The ADC results (after right shifting, if used) are compared to high alarm thresholds, low alarm thresholds, and the warning threshold after each conversion, and the corresponding alarms are set, which can be used to trigger the TX-F or FETG outputs. These ADC thresholds are user programmable, as are the masking registers that can be used to prevent the alarms from triggering the TX-F and FETG outputs.

ADC Timing

There are six analog channels that are digitized in a round-robin fashion in the order as shown in Figure 4. The total time required to convert all six channels is t_{RR} (see *Timing Characteristics (Control Loop and Quick-Trip)* for details).

Right Shifting ADC Result

If the weighting of the ADC digital reading must conform to a predetermined full-scale value defined by a standard's specification, then right shifting can be used to adjust the predetermined full-scale analog measurement range while maintaining the weighting of the ADC results. The DS1865's range is wide enough to cover all requirements; when the maximum input value is far short of the FS value, right shifting can be used to obtain greater accuracy. For instance, the maximum voltage might be 1/8th the specified predetermined full-scale value, so only 1/8th the converter's range is used. An alternative is to calibrate the ADC's full-scale range to 1/8th the readable predetermined full-scale value and use a right-shift value of 3. With this implementation, the resolution of the measurement is increased by a factor of 8, and because the result is digitally divided by 8 by right shifting, the bit weight of the measurement still meets the standard's specification (i.e., SFF-8472).

The right-shift operation on the ADC result is carried out based on the contents of Right Shift Control registers (Table 02h, Registers 8Eh-8Fh) in EEPROM. Four analog channels, MON1–MON4, each have 3 bits allocated to set the number of right shifts. Up to 7 right-shift operations are allowed and are executed as a part of every conversion before the results are compared to the high and low alarm levels, or loaded into their corresponding measurement registers (Table 01h, Registers 62h–6Bh). This is true during the setup of internal calibration as well as during subsequent data conversions.

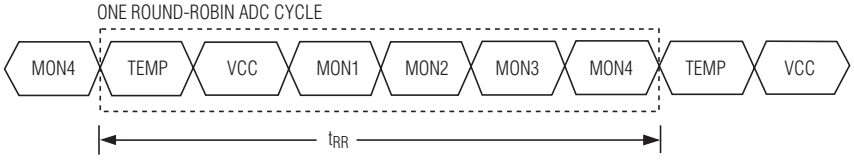
Transmit Fault (TX-F) Output

The TX-F output has masking registers for the six ADC alarms and the four QT alarms to select which comparisons cause it to assert. In addition, the FETG alarm is selectable through the TX-F mask to cause TX-F to assert. All alarms, with the exception of FETG, only cause TX-F to remain active while the alarm condition persists. However, the TX-F latch bit can enable the TX-F output to remain active until it is cleared by the TX-F reset bit, TX-D, soft TX-D, or by power cycling the part. If the FETG output is configured to trigger TX-F, it indicates that the DS1865 is in shutdown, and requires TX-D, soft TX-D, or cycling power to reset. The QT alarms are masked until the completion of the binary search. Only enabled alarms will activate TX-F. See Figure 5.

Table 4 shows TX-F as a function of TX-D and the alarm sources.

Safety Shutdown (FETG) Output

The FETG output has masking registers (separate from TX-F) for the five ADC alarms and the four QT alarms to select which comparisons cause it to assert. Unlike TX-F, the FETG output is always latched in case it is triggered by an unmasked alarm condition. Its output polarity is programmable to allow an external nMOSFET or pMOSFET to open during alarms to shut off the laser diode current. If the FETG output triggers, indicating that the DS1865 is in shutdown, it requires TX-D, soft TX-D, or cycling power to be reset. Under all conditions, when the analog outputs are reinitialized after being disabled, all the alarms with the exception of the V_{CC} low ADC alarm are cleared. The V_{CC} low alarm must remain active to prevent the output from attempting to operate when



NOTE: AT POWER-UP, IF THE V_{CC} LOW ALARM IS SET FOR EITHER THE TX-F OR FETG OUTPUT, THE ADC ROUND-ROBIN TIMING CYCLES BETWEEN TEMP AND V_{CC} ONLY UNTIL V_{CC} IS ABOVE THE V_{CC} LOW THRESHOLD.

Figure 4. ADC Round-Robin Timing

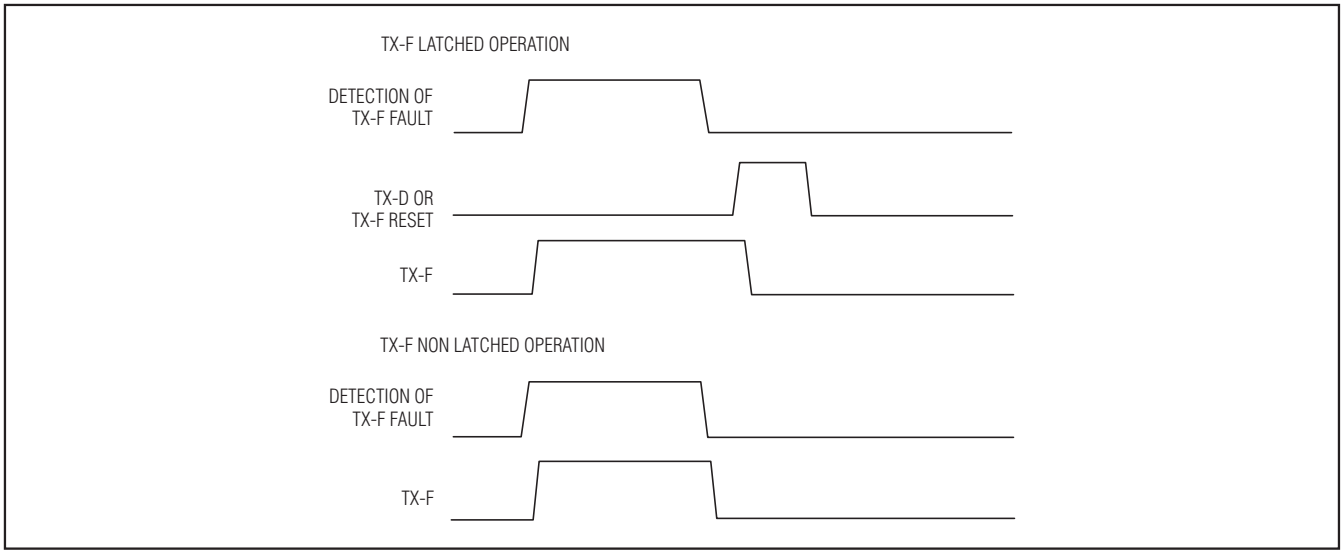


Figure 5. TX-F Timing

Table 4. TX-F as a Function of TX-D and Alarm Sources

$V_{CC} > V_{POA}$	TX-D	NONMASKED TX-F ALARM	TX-F
No	X	X	1
Yes	0	0	0
Yes	0	1	1
Yes	1	X	0

inadequate V_{CC} exists to operate the laser driver. Once adequate V_{CC} is present to clear the V_{CC} low alarm, the outputs are enabled following the same sequence as the power-up sequence.

As previously mentioned, the FETG is an output used to disable the laser current through a series nMOSFET or pMOSFET. This requires that the FETG output can sink or source current. Because the DS1865 does not know if it should sink or source current before V_{CC} exceeds V_{POA}, which triggers the EE recall, this output will be high impedance when V_{CC} is below V_{POA} (see the *Low-Voltage Operation* section for details and diagram). The application circuit must use a pullup or pulldown resistor on this pin that pulls FETG to the alarm/shutdown state (high for a pMOS, low for a nMOS). Once V_{CC} is above V_{POA}, the DS1865 pulls the FETG output to the state determined by the FETG DIR bit (Table 02h, Register 89h). FETG DIR is 0 if an nMOS is used and 1 if a pMOS is used.

Determining Alarm Causes Using the I²C Interface

To determine the cause of the TX-F or FETG alarm, the system processor can read the DS1865's Alarm Trap Bytes (ATB) through the I²C interface (in Table 01h). The ATB has a bit for each alarm. Any time an alarm occurs, regardless of the mask bit's state, the DS1865 sets the corresponding bit in the ATB. Active ATB bits remain set until written to zeros through the I²C interface. On power-up, the ATB is zeros until alarms dictate otherwise.

Die Identification

The DS1865 has an ID hard coded to its die. Two registers (Table 02h bytes 86h–87h) are assigned for this feature. Byte 86h reads 65h to identify the part as the DS1865, byte 87h reads the die revision.

Low-Voltage Operation

The DS1865 contains two power-on reset (POR) levels. The lower level is a digital POR (V_{POD}) and the higher level is an analog POR (V_{POA}). At startup, before the supply voltage rises above V_{POA}, the outputs are disabled (FETG and BIAS outputs are high impedance, MOD is low), all SRAM locations are low (including shadowed EEPROM), and all analog circuitry is disabled. When V_{CC} reaches V_{POA}, the SEE is recalled, and the analog circuitry is enabled. While V_{CC} remains above V_{POA}, the device is in its normal operating state, and it responds based on its nonvolatile configuration. If during operation V_{CC} falls below V_{POA} but is still above V_{POD}, the SRAM retains the SEE settings from

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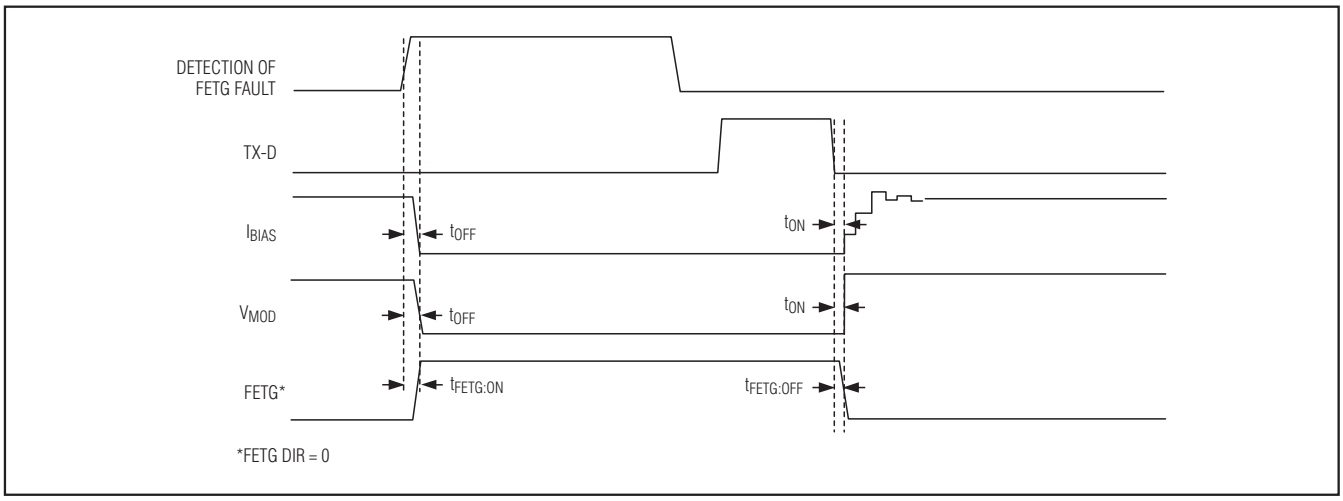

Figure 6. FETG/Modulation and Bias Timing (Fault Condition Detected)

Table 5. FETG, MOD, and BIAS Outputs as a Function of TX-D and Alarm Sources

$V_{CC} > V_{POA}$	TX-D	NONMASKED FETG ALARM	FETG	MOD AND BIAS OUTPUTS
Yes	0	0	FETG DIR	Enabled
Yes	0	1	$\overline{\text{FETG DIR}}$	Disabled
Yes	1	X	FETG DIR	Disabled

the first SEE recall, but the device analog is shut down and the outputs are disabled. FETG is driven to its alarm state defined by the FETG DIR bit (Table 02h, Register 89h). If the supply voltage recovers back above V_{POA}, the device immediately resumes normal functioning. If the supply voltage falls below V_{POD}, the device SRAM is placed in its default state and another SEE recall is required to reload the nonvolatile settings. The EEPROM recall occurs the next time V_{CC} exceeds V_{POA}. Figure 7 shows the sequence of events as the voltage varies.

Any time V_{CC} is above V_{POD}, the I^2C interface can be used to determine if V_{CC} is below the V_{POA} level. This is accomplished by checking the RDYB bit in the status (Lower Memory, Register 6Eh) byte. RDYB is set when V_{CC} is below V_{POA}. When V_{CC} rises above V_{POA}, RDYB is timed (within 500µs) to go to 0, at which point the part is fully functional.

For all device addresses sourced from EEPROM (Table 02h, Register 8Ch), the default device address is A2h until V_{CC} exceeds V_{POA} allowing the device address to be recalled from the EEPROM.

Power-On Analog (POA)

POA holds the DS1865 in reset until V_{CC} is at a suitable level ($V_{CC} > V_{POA}$) for the part to accurately measure with its ADC and compare analog signals with its quick-trip monitors. Because V_{CC} cannot be measured by the ADC when V_{CC} is less than V_{POA}, POA also asserts the V_{CC} low alarm, which is cleared by a V_{CC} ADC conversion greater than the customer-programmable V_{CC} low ADC limit. This prevents the TX-F and FETG outputs from glitching during a slow power-up. The TX-F and FETG outputs do not latch until there is a conversion above V_{CC} low limit.

The POA alarm is nonmaskable. The TX-F and FETG outputs are asserted when V_{CC} is below V_{POA}. See the *Low-Voltage Operation* section for more information.

DAC1 Output

The DAC1 output has a 0 to 2.5V range, 8 bits of resolution, and is programmed through the I^2C interface. The DAC1 setting is nonvolatile and password 2 (PW2) protected.

M4DAC Output

The M4DAC output has a 0 to 2.5V range, 8 bits of resolution, and is controlled by an LUT indexed by the MON4 voltage. The M4DAC LUT (Table 06h) is nonvolatile and PW2 protected. See the *Memory Organization* section for details.

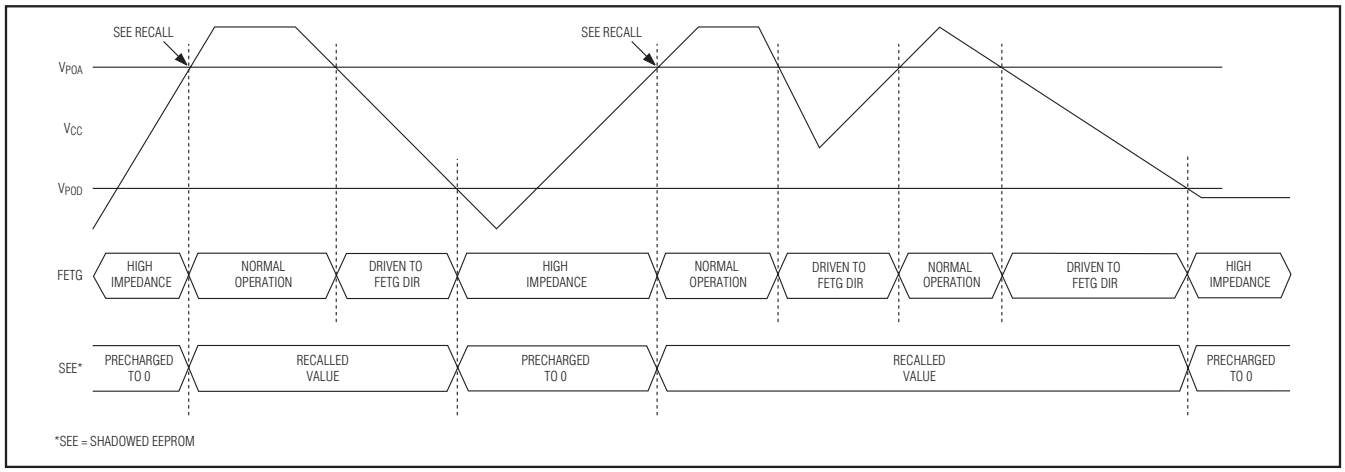

Figure 7. Low-Voltage Hysteresis Example

Digital I/O Pins

Five digital I/O pins are provided for additional monitoring and control of the triplexer. By default the LOSI pin is used to convert a standard comparator output for loss of signal (LOSI) to an open-collector output. This means the mux shown on the block diagram by default selects the LOSI pin as the source for the D0 output transistor. The level of the D0 pin can be read in the status byte (Lower Memory, Register 6Eh) as the LOS status bit. The LOS status bit reports back the logic level of the D0 pin, so an external pullup resistor must be provided for this pin to output a high level. The LOSI signal can be inverted before driving the open-drain output transistor using the XOR gate provided. The mux LOSI allows the D0 pin to be used identically to the D1, D2, and D3 pins. However, the mux setting (stored in the EEPROM) does not take effect until $V_{CC} > V_{POA}$, allowing the EEPROM to recall. This requires the LOSI pin to be grounded for D0 to act identical to the D1, D2, and D3 pins.

Digital pins D1, D2, and D3 can be used as inputs or outputs. External pullup resistors must be provided to realize high logic levels. The levels of these input pins can be read by reading the DIN byte (Lower Memory, Register 79h), and the open-drain outputs can be controlled using the DOUT byte (Lower Memory, Register 78h). When $V_{CC} < V_{POA}$, these outputs are high impedance. Once $V_{CC} \geq V_{POA}$, the outputs go to the power-on default state stored in the DPU byte (Table 02h, Register C0h). The EEPROM determined default state of the pin can be modified with PW2 access. After the default state has been recalled, the SRAM registers controlling outputs can be modified without password access. This allows the outputs to be used to control serial interfaces without wearing out the default EEPROM setting.

Memory Organization

The DS1865 features eight banks of memory composed of the following.

The **Lower Memory** is addressed from 00h to 7Fh and contains alarm and warning thresholds, flags, masks, several control registers, password entry area (PWE), and the table select byte. The table select byte determines which table (01h–06h) will be mapped into the upper memory locations, namely 80h–FFh (unless stated otherwise).

Table 01h primarily contains user EEPROM (with PW1 level access) as well as some alarm and warning status bytes.

Table 02h is a multifunction space that contains configuration registers, scaling and offset values, passwords, interrupt registers, as well as other miscellaneous control bytes.

Table 03h is strictly user EEPROM that is protected by a PW2 level access.

Table 04h contains a temperature-indexed LUT for control of the modulation voltage. The modulation LUT can be programmed in 2°C increments over the -40°C to +102°C range. This register is protected by a PW2 level access.

Table 05h contains another LUT, which allows the APC set point to change as a function of temperature to compensate for tracking error (TE). This TE LUT has 36 entries that determine the APC setting in 4°C windows between -40°C to +100°C. This register is protected by a PW2 level access.

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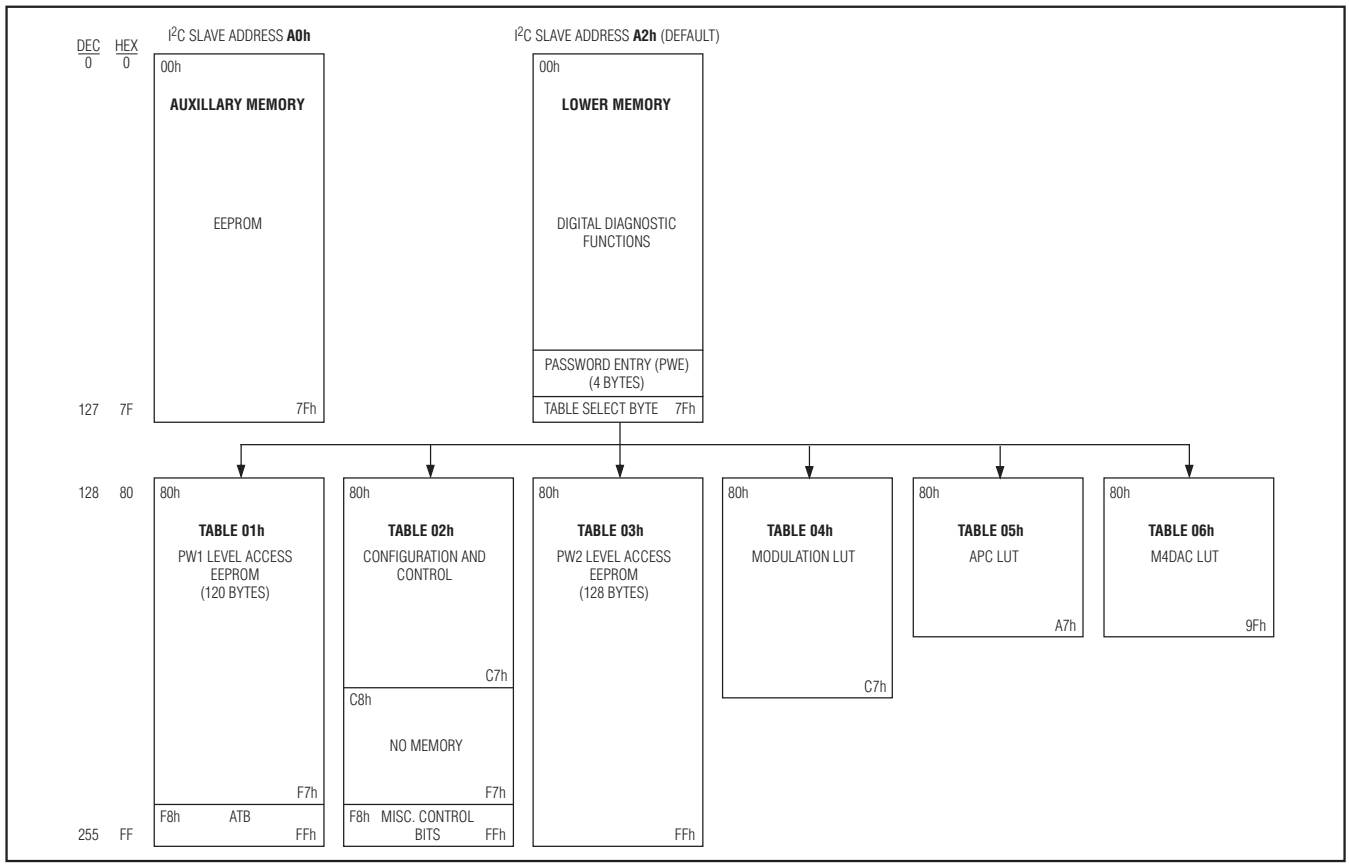

Figure 8. Memory Map

Table 06h contains a MON4-indexed LUT for control of the M4DAC voltage. The M4DAC LUT has 32 entries that are configurable to act as one 32-entry LUT or two 16-entry LUTs. When configured as one 32-byte LUT, each entry corresponds to an increment of 1/32 of the full scale. When configured as two 16-byte LUTs, the first 16 bytes and the last 16 bytes each correspond to 1/16 of full scale. Either of the two sections is selected with a separate configuration bit. This LUT is protected by a PW2 level access.

Auxiliary Memory is EEPROM accessible at the I²C slave address, A0h.

See the register map tables for a more complete detail of each byte's function, as well as for read/write permissions for each byte.

Shadowed EEPROM

In addition to volatile memory (SRAM) and nonvolatile memory (EEPROM), the DS1865 also features shadowed EEPROM. Shadowed EEPROM (SEE) can be configured as either volatile or nonvolatile memory using the SEEB bit in Table 02h, Register 80h.

The DS1865 uses shadowed EEPROM memory for key memory addresses that can be rewritten many times. By default the shadowed EEPROM bit, SEEB, is not set and these locations act as ordinary EEPROM. By setting SEEB, these locations function like SRAM cells, which allow an infinite number of write cycles without concern of wearing out the EEPROM. This also eliminates the requirement for the EEPROM write time, t_{WR}. Because changes made with SEEB enabled do not affect the EEPROM, these changes are not retained through power cycles. The power-up value is the last value written with SEEB disabled. This function can be used to limit the number of EEPROM writes during calibration or to change the monitor thresholds periodically during normal operation, helping to reduce the number of times EEPROM is written. The *Memory Organization* description indicates which locations are shadowed EEPROM.

I²C Definitions

The following terminology is commonly used to describe I²C data transfers.

Master Device: The master device controls the slave devices on the bus. The master device generates SCL clock pulses and START and STOP conditions.

Slave Devices: Slave devices send and receive data at the master's request.

Bus Idle or Not Busy: Time between STOP and START conditions when both SDA and SCL are inactive and in their logic-high states. When the bus is idle, it often initiates a low-power mode for slave devices.

START Condition: A START condition is generated by the master to initiate a new data transfer with a slave. Transitioning SDA from high to low while SCL remains high generates a START condition. See Figure 9 for applicable timing.

STOP Condition: A STOP condition is generated by the master to end a data transfer with a slave. Transitioning SDA from low to high while SCL remains high generates a STOP condition. See Figure 9 for applicable timing.

Repeated START Condition: The master can use a repeated START condition at the end of one data transfer to indicate that it will immediately initiate a new data transfer following the current one. Repeated START conditions are commonly used during read operations to identify a specific memory address to begin a data transfer. A repeated START condition is issued identically to a normal START condition. See Figure 9 for applicable timing.

Bit Write: Transitions of SDA must occur during the low state of SCL. The data on SDA must remain valid and unchanged during the entire high pulse of SCL plus the setup and hold-time requirements (Figure 9). Data is shifted into the device during the rising edge of the SCL.

Bit Read: At the end of a write operation, the master must release the SDA bus line for the proper amount of setup time before the next rising edge of SCL during a bit read. The device shifts out each bit of data on SDA at the falling edge of the previous SCL pulse and the data bit is valid at the rising edge of the current SCL pulse. Remember that the master generates all SCL clock pulses including when it is reading bits from the slave.

Acknowledgement (ACK and NACK): An acknowledgement (ACK) or not acknowledge (NACK) is always the 9th bit transmitted during a byte transfer. The device receiving data (the master during a read or the slave during a write operation) performs an ACK by transmitting a zero during the 9th bit. A device performs a NACK by transmitting a one during the 9th bit. Timing for the ACK and NACK is identical to all other bit writes. An ACK is the acknowledgment that the device is properly receiving data. A NACK is used to terminate a read sequence or as an indication that the device is not receiving data.

Byte Write: A byte write consists of 8 bits of information transferred from the master to the slave (most significant bit first) plus a 1-bit acknowledgement from the slave to the master. The 8 bits transmitted by the master are done according to the bit write definition and the acknowledgement is read using the bit read definition.

Byte Read: A byte read is an 8-bit information transfer from the slave to the master plus a 1-bit ACK or NACK from the master to the slave. The 8 bits of information that are transferred (most significant bit first) from the slave to the master are read by the master using the bit read definition, and the master transmits an ACK using the bit write definition to receive additional data bytes. The master must NACK the last byte read to terminate communication so the slave returns control of SDA to the master.

Slave Address Byte: Each slave on the I²C bus responds to a slave addressing byte (Figure 9) sent immediately following a START condition. The slave address byte contains the slave address in the most significant 7 bits and the R/$\overline{W}$ bit in the least significant bit.

The DS1865 responds to two slave addresses. The auxiliary memory always responds to a fixed I²C slave address, A0h. The Lower Memory and tables 01h–06h respond to I²C slave addresses that can be configured to any value between 00h–FEh using the Device Address byte (Table 02h, Register 8Ch). The user also must set the ASEL bit (Table 02h, Register 89h) for this address to be active. By writing the correct slave address with R/$\overline{W}$ = 0, the master indicates it will write data to the slave. If R/$\overline{W}$ = 1, the master reads data from the slave. If an incorrect slave address is written, the DS1865 assumes the master is communicating with another I²C device and ignores the communications until the next START condition is sent.

Memory Address: During an I²C write operation, the master must transmit a memory address to identify the memory location where the slave is to store the data. The memory address is always the second byte transmitted during a write operation following the slave address byte.

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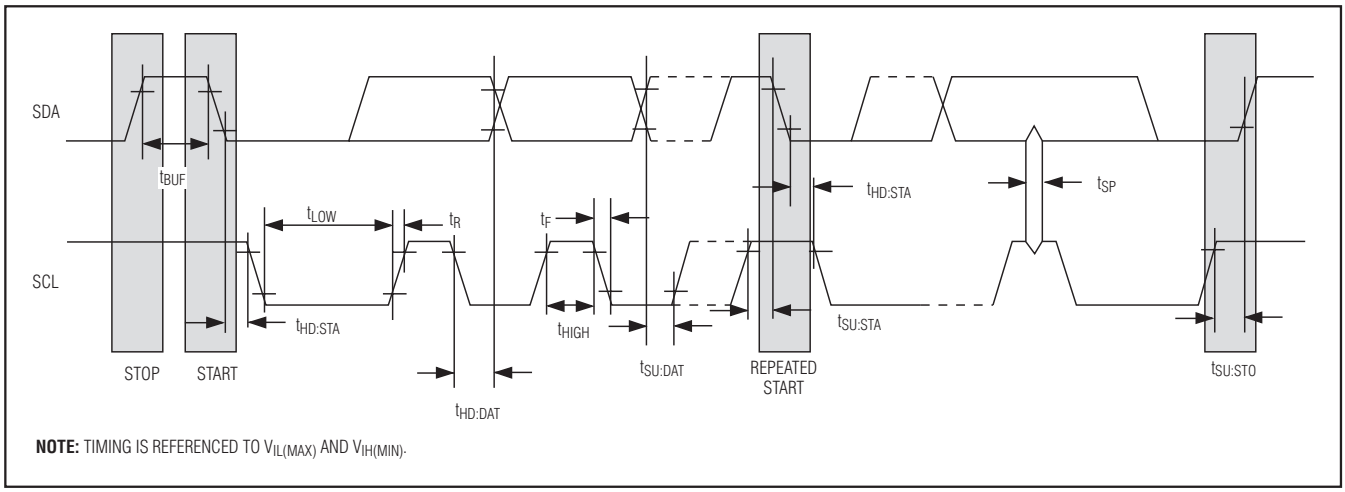

Figure 9. I²C Timing Diagram

I²C Communication

Writing a Single Byte to a Slave: The master must generate a START condition, write the I²C slave address byte (R/$\overline{W}$ = 0), write the byte of data, and generate a STOP condition. The master must read the slave's acknowledgement during all byte write operations.

Writing Multiple Bytes to a Slave: To write multiple bytes to a slave, the master generates a START condition, writes the slave address byte (R/$\overline{W}$ = 0), writes the memory address, writes up to 8 data bytes, and generates a STOP condition. The DS1865 writes 1 to 8 bytes (1 page or row) with a single write transaction. This is internally controlled by an address counter that allows data to be written to consecutive addresses without transmitting a memory address before each data byte is sent. The address counter limits the write to one 8-byte page (one row of the memory map). Attempts to write to additional pages of memory without sending a STOP condition between pages result in the address counter wrapping around to the beginning of the present row.

Example: A 3-byte write starts at address 06h and writes three data bytes (11h, 22h, and 33h) to three "consecutive" addresses. The result is that addresses 06h and 07h contain 11h and 22h, respectively, and the third data byte, 33h, is written to address 00h.

To prevent address wrapping from occurring, the master must send a STOP condition at the end of the page, then wait for the bus-free or EEPROM-write time to elapse. Then the master can generate a new START condition, and write the slave address byte (R/$\overline{W}$ = 0) and the first memory address of the next memory row before continuing to write data.

Acknowledge Polling: Any time an EEPROM location is written, the DS1865 requires the EEPROM write time (t_W) after the STOP condition to write the contents of the byte of data to EEPROM. During the EEPROM write time, the device does not acknowledge its slave address because it is busy. It is possible to take advantage of that phenomenon by repeatedly addressing the DS1865, which allows the next page to be written as soon as the DS1865 is ready to receive the data. The alternative to acknowledge polling is to wait for a maximum period of t_W to elapse before attempting to write again to the DS1865.

EEPROM Write Cycles: When EEPROM writes occur to the memory, the DS1865 writes to all three EEPROM memory locations, even if only a single byte was modified. Because all three bytes are written, the bytes that were not modified during the write transaction are still subject to a write cycle. This can result in all three bytes being worn out over time by writing a single byte repeatedly. The DS1865's EEPROM write cycles are specified in the *Nonvolatile Memory Characteristics* table. The specification shown is at the worst-case temperature. It can handle approximately 10 times that many writes at room temperature. Writing to SRAM-shadowed EEPROM memory with SEEB = 1 does not count as an EEPROM write cycle when evaluating the EEPROM's estimated lifetime.

Reading a Single Byte from a Slave: Unlike the write operation that uses the memory address byte to define where the data is to be written, the read operation occurs at the present value of the memory address counter. To read a single byte from the slave, the master generates a START condition, writes the slave address byte with R/$\overline{W}$ = 1, reads the data byte with a NACK to indicate the end of the transfer, and generates a STOP condition.

Manipulating the Address Counter for Reads: A dummy write cycle can be used to force the address pointer to a particular value. To do this, the master generates a START condition, writes the slave address byte (R/$\overline{W}$ = 0), writes the memory address where it desires to read, generates a repeated START condition, writes the slave address byte (R/$\overline{W}$ = 1), reads data with ACK or NACK as applicable, and generates a STOP condition.

Lower Memory Register Map

This register map shows each byte/word in terms of the row it is on in the memory. The first byte in the row is located in memory at the hexadecimal row address in the left-most column. Each subsequent byte on the row is one/two memory locations beyond the previous byte/word's address. A total of 8 bytes are present on each row. For more information about each of these bytes, see the corresponding register description in the following tables.

LOWER MEMORY									
ROW (HEX)	ROW NAME	WORD 0		WORD 1		WORD 2		WORD 3	
		BYTE 0/8	BYTE 1/9	BYTE 2/A	BYTE 3/B	BYTE 4/C	BYTE 5/D	BYTE 6/E	BYTE 7/F
00	<1>THRESHOLD$_0$	TEMP ALARM HI		TEMP ALARM LO		TEMP WARN HI		TEMP WARN LO	
08	<1>THRESHOLD$_1$	V_{CC} ALARM HI		V_{CC} ALARM LO		V_{CC} WARN HI		V_{CC} WARN LO	
10	<1>THRESHOLD$_2$	MON1 ALARM HI		MON1 ALARM LO		MON1 WARN HI		MON1 WARN LO	
18	<1>THRESHOLD$_3$	MON2 ALARM HI		MON2 ALARM LO		MON2 WARN HI		MON2 WARN LO	
20	<1>THRESHOLD$_4$	MON3 ALARM HI		MON3 ALARM LO		MON3 WARN HI		MON3 WARN LO	
28	<1>THRESHOLD$_5$	MON4 ALARM HI		MON4 ALARM LO		MON4 WARN HI		MON4 WARN LO	
30	<1>PW2 EE	EE	EE	EE	EE	EE	EE	EE	EE
38	<1>PW2 EE	EE	EE	EE	EE	EE	EE	EE	EE
40	<1>PW2 EE	EE	EE	EE	EE	EE	EE	EE	EE
48	<1>PW2 EE	EE	EE	EE	EE	EE	EE	EE	EE
50	<1>PW2 EE	EE	EE	EE	EE	EE	EE	EE	EE
58	<1>PW2 EE	EE	EE	EE	EE	EE	EE	EE	EE
60	<2>ADC VALUES$_0$	TEMP VALUE		V_{CC} VALUE		MON1 VALUE		MON2 VALUE	
68	<0> ADC VALUES$_1$	<2>MON3 VALUE		<2> MON4 VALUE		<2>RESERVED		<0>STATUS	<3>UPDATE
70	<2>ALARM/WARN	ALARM$_3$	ALARM$_2$	ALARM$_1$	ALARM$_0$	WARN$_3$	WARN$_2$	RESERVED	
78	<0>TABLE SELECT	<2>DOUT	<2>DIN	<6>RESERVED	<6>PWE MSB		<6>PWE LSB		<5>TBL SEL

ACCESS CODE	<0>	<1>	<2>	<3>	<4>	<5>	<6>	<7>	<8>	<9>	<10>	<11>
Read Access	See each bit/byte separately	All	All	All	PW2	All	N/A	PW1	PW2	N/A	PW2	All
Write Access		PW2	N/A	All and DS1865 hardware	PW2 + mode bit	All	All	PW1	PW2	PW2	N/A	PW1

Table 01h Register Map

TABLE 01h (PW1)									
ROW (HEX)	ROW NAME	WORD 0		WORD 1		WORD 2		WORD 3	
		BYTE 0/8	BYTE 1/9	BYTE 2/A	BYTE 3/B	BYTE 4/C	BYTE 5/D	BYTE 6/E	BYTE 7/F
80	<7>PW1 EE	EE	EE	EE	EE	EE	EE	EE	EE
88	<7>PW1 EE	EE	EE	EE	EE	EE	EE	EE	EE
90	<7>PW1 EE	EE	EE	EE	EE	EE	EE	EE	EE
98	<7>PW1 EE	EE	EE	EE	EE	EE	EE	EE	EE
A0	<7>PW1 EE	EE	EE	EE	EE	EE	EE	EE	EE
A8	<7>PW1 EE	EE	EE	EE	EE	EE	EE	EE	EE
B0	<7>PW1 EE	EE	EE	EE	EE	EE	EE	EE	EE
B8	<7>PW1 EE	EE	EE	EE	EE	EE	EE	EE	EE
C0	<7>PW1 EE	EE	EE	EE	EE	EE	EE	EE	EE
C8	<7>PW1 EE	EE	EE	EE	EE	EE	EE	EE	EE
D0	<7>PW1 EE	EE	EE	EE	EE	EE	EE	EE	EE
D8	<7>PW1 EE	EE	EE	EE	EE	EE	EE	EE	EE
E0	<7>PW1 EE	EE	EE	EE	EE	EE	EE	EE	EE
E8	<7>PW1 EE	EE	EE	EE	EE	EE	EE	EE	EE
F0	<7>PW1 EE	EE	EE	EE	EE	EE	EE	EE	EE
F8	<11>ALARM TRAP	$ALARM_3$	$ALARM_2$	$ALARM_1$	$ALARM_0$	$WARN_3$	$WARN_2$	RESERVED	

ACCESS CODE	<0>	<1>	<2>	<3>	<4>	<5>	<6>	<7>	<8>	<9>	<10>	<11>
Read Access	See each bit/byte separately	All	All	All	PW2	All	N/A	PW1	PW2	N/A	PW2	All
Write Access		PW2	N/A	All and DS1865 hardware	PW2 + mode bit	All	All	PW1	PW2	PW2	N/A	PW1

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Table 02h Register Map

TABLE 02h (PW2)									
ROW (HEX)	ROW NAME	WORD 0		WORD 1		WORD 2		WORD 3	
		BYTE 0/8	BYTE 1/9	BYTE 2/A	BYTE 3/B	BYTE 4/C	BYTE 5/D	BYTE 6/E	BYTE 7/F
80	<0> $CONFIG_0$	<8>MODE	<4>T INDEX	<4> MOD DAC	<4> APC DAC	<4> V INDEX	<4> M4DAC	<10> DEVICE ID	<10> DEVICE VER
88	<8> $CONFIG_1$	UPDATE RATE	CONFIG	STARTUP STEP	MOD RANGING	DEVICE ADDRESS	COMP RANGING	$RSHIFT_1$	$RSHIFT_0$
90	<8> $SCALE_0$	RESERVED		V_{CC} SCALE		MON1 SCALE		MON2 SCALE	
98	<8> $SCALE_1$	MON3 SCALE		MON4 SCALE		RESERVED		RESERVED	
A0	<8> $OFFSET_0$	RESERVED		V_{CC} OFFSET		MON1 OFFSET		MON2 OFFSET	
A8	<8> $OFFSET_1$	MON3 OFFSET		MON4 OFFSET		RESERVED		INTERNAL TEMP OFFSET*	
B0	<9> PWD VALUE	PW1 MSW		PW1 LSW		PW2 MSW		PW2 LSW	
B8	<8> INTERRUPT	FETG EN_1	FETG EN_0	TX-F EN_1	TX-F EN_0	HTXP	LTXP	HBIAS	MAX IBIAS
C0	<8> CNTL OUT	DPU	RESERVED	RESERVED	RESERVED	DAC1	RESERVED	RESERVED	M4 LUT CNTL
C8-F7	EMPTY	EMPTY	EMPTY	EMPTY	EMPTY	EMPTY	EMPTY	EMPTY	EMPTY
F8	<0> MAN IBIAS	<4> MAN $IBIAS_1$	<4> MAN $IBIAS_0$	<4> MAN_CNTL	<10> BIAS DAC_1	<10> BIAS DAC_0	RESERVED	RESERVED	RESERVED

**The final result must be XORed with BB40h before writing to this register.*

ACCESS CODE	<0>	<1>	<2>	<3>	<4>	<5>	<6>	<7>	<8>	<9>	<10>	<11>
Read Access	See each bit/byte separately	All	All	All	PW2	All	N/A	PW1	PW2	N/A	PW2	All
Write Access		PW2	N/A	All and DS1865 hardware	PW2 + mode bit	All	All	PW1	PW2	PW2	N/A	PW1

Table 03h Register Map

TABLE 03h (PW3)									
ROW (HEX)	ROW NAME	WORD 0		WORD 1		WORD 2		WORD 3	
		BYTE 0/8	BYTE 1/9	BYTE 2/A	BYTE 3/B	BYTE 4/C	BYTE 5/D	BYTE 6/E	BYTE 7/F
80	<8>PW2 EE	EE	EE	EE	EE	EE	EE	EE	EE
88	<8>PW2 EE	EE	EE	EE	EE	EE	EE	EE	EE
90	<8>PW2 EE	EE	EE	EE	EE	EE	EE	EE	EE
98	<8>PW2 EE	EE	EE	EE	EE	EE	EE	EE	EE
A0	<8>PW2 EE	EE	EE	EE	EE	EE	EE	EE	EE
A8	<8>PW2 EE	EE	EE	EE	EE	EE	EE	EE	EE
B0	<8>PW2 EE	EE	EE	EE	EE	EE	EE	EE	EE
B8	<8>PW2 EE	EE	EE	EE	EE	EE	EE	EE	EE
C0	<8>PW2 EE	EE	EE	EE	EE	EE	EE	EE	EE
C8	<8>PW2 EE	EE	EE	EE	EE	EE	EE	EE	EE
D0	<8>PW2 EE	EE	EE	EE	EE	EE	EE	EE	EE
D8	<8>PW2 EE	EE	EE	EE	EE	EE	EE	EE	EE
E0	<8>PW2 EE	EE	EE	EE	EE	EE	EE	EE	EE
E8	<8>PW2 EE	EE	EE	EE	EE	EE	EE	EE	EE
F0	<8>PW2 EE	EE	EE	EE	EE	EE	EE	EE	EE
F8	<8>PW2 EE	EE	EE	EE	EE	EE	EE	EE	EE

ACCESS CODE	<0>	<1>	<2>	<3>	<4>	<5>	<6>	<7>	<8>	<9>	<10>	<11>
Read Access	See each bit/byte separately	All	All	All	PW2	All	N/A	PW1	PW2	N/A	PW2	All
Write Access		PW2	N/A	All and DS1865 hardware	PW2 + mode bit	All	All	PW1	PW2	PW2	N/A	PW1