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19-4986; Rev 1; 11/09

EVALUATION KIT AVAILABLE

SFP+ Controller with Analog LDD Interface

DS1873

General Description

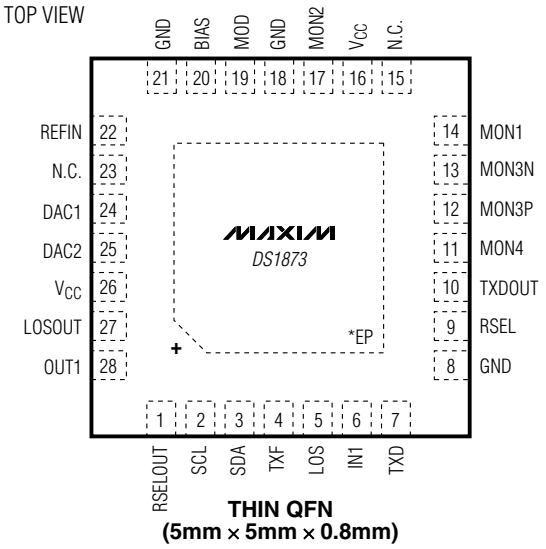
The DS1873 controls and monitors all functions for SFF, SFP, and SFP+ modules including all SFF-8472 functionality. The DS1873 provides APC loop, modulation current control, and eye safety functionality. The DS1873 continuously monitors for high output current, high bias current, and low and high transmit power to ensure that laser shutdown for eye safety requirements are met without adding external components.

Six ADC channels monitor V_{CC}, temperature, and four external monitor inputs (MON1–MON4) that can be used to meet all monitoring requirements. MON3 is differential with support for common mode to V_{CC}. Two digital-to-analog (DAC) outputs with temperature-indexed lookup tables (LUTs) are available for additional monitoring and control functionality.

Applications

SFF, SFP, and SFP+ Transceiver Modules

Pin Configuration



THIN QFN
(5mm × 5mm × 0.8mm)

*EXPOSED PAD.

Features

- **Meets All SFF-8472 Control and Monitoring Requirements**
- **Six Analog Monitor Channels: Temperature, V_{CC}, MON1–MON4**
  - **MON1–MON4 Support Internal and External Calibration**
  - **Scalable Dynamic Range**
  - **Internal Direct-to-Digital Temperature Sensor**
  - **Alarm and Warning Flags for All Monitored Channels**
- **Four 10-Bit Delta-Sigma Outputs with 36 Entry Temperature LUTs**
  - **Laser Bias Controlled by APC Loop and Temperature LUT to Compensate for Tracking Error**
  - **Laser Modulation Controlled by 72-Entry Temperature LUT**
  - **Two Additional DACs Controlled by One 72-Entry and One 36-Entry Temperature LUT**
- **Digital I/O Pins: Five Inputs, Five Outputs**
- **Comprehensive Fault-Measurement System with Maskable Laser Shutdown Capability**
- **Flexible, Two-Level Password Scheme Provides Three Levels of Security**
- **120 Bytes of Password-1 Protected Memory**
- **128 Bytes of Password-2 Protected Memory in Main Device Address**
- **256 Additional Bytes Located at A0h Slave Address**
- **I^2C-Compatible Interface**
- **+2.85V to +3.9V Operating Voltage Range**
- **-40°C to +95°C Operating Temperature Range**
- **28-Pin TQFN (5mm x 5mm) Package**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
DS1873T+	-40°C to +95°C	28 TQFN-EP*
DS1873T+T&R	-40°C to +95°C	28 TQFN-EP*

+Denotes a lead(Pb)-free/RoHS-compliant package.
T&R = Tape and reel.
**EP = Exposed pad.*

For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.

SFP+ Controller with Analog LDD Interface

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ABSOLUTE MAXIMUM RATINGS

Voltage Range on MON1–MON4, RSEL, IN1, LOS, TXF, and TXD Pins Relative to Ground .....-0.5V to (V_{CC} + 0.5V)*
Voltage Range on V_{CC}, SDA, SCL, OUT1, RSELOUT, and LOSOUT Pins Relative to Ground.....-0.5V to +4.2V

Operating Temperature Range .....-40°C to +95°C
Programming Temperature Range .....0°C to +95°C
Storage Temperature Range .....-55°C to +125°C
Soldering Temperature.....Refer to the IPC/JEDEC J-STD-020 Specification.

**Subject to not exceeding +4.2V.*

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

(T_A = -40°C to +95°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Main Supply Voltage	V_{CC}	(Note 1)	+2.85		+3.9	V
High-Level Input Voltage (SDA, SCL)	$V_{IH:1}$		0.7 x V_{CC}		V_{CC} + 0.3	V
Low-Level Input Voltage (SDA, SCL)	$V_{IL:1}$		-0.3		0.3 x V_{CC}	V
High-Level Input Voltage (TXD, TXF, RSEL, IN1, LOS)	$V_{IH:2}$		2.0		V_{CC} + 0.3	V
Low-Level Input Voltage (TXD, TXF, RSEL, IN1, LOS)	$V_{IL:2}$		-0.3		+0.8	V

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = +2.85V to +3.9V, T_A = -40°C to +95°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current	I_{CC}	(Notes 1, 2)		2.5	10	mA
Output Leakage (SDA, OUT1, RSELOUT, LOSOUT, TXF)	I_{LO}				1	µA
Low-Level Output Voltage (SDA, MOD, BIAS, OUT1, RSELOUT, LOSOUT, TXDOUT, DAC1, DAC2, TXF)	V_{OL}	I_{OL} = 4mA			0.4	V
		I_{OL} = 6mA			0.6	
High-Level Output Voltage (MOD, BIAS, DAC1, DAC2, TXDOUT)	V_{OH}	I_{OH} = 4mA	V_{CC} - 0.4			V
TXDOUT Before EEPROM Recall		See Figure 13		10	100	nA
MOD, BIAS, DAC1, and DAC2 Before LUT Recall		See Figure 12		10	100	nA
Input Leakage Current (SCL, TXD, LOS, RSEL, IN1)	I_{LI}				1	µA
Digital Power-On Reset	POD		1.0		2.2	V
Analog Power-On Reset	POA		2.0		2.75	V

MOD, BIAS, DAC1, DAC2 ELECTRICAL CHARACTERISTICS

(V_{CC} = +2.85V to +3.9V, T_A = -40°C to +95°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Main Oscillator Frequency	f_{OSC}			5		MHz
Delta-Sigma Input-Clock Frequency	f_{DS}			$f_{OSC}/2$		MHz
Reference Voltage Input (REFIN)	V_{REFIN}	Minimum 0.1µF to GND	2		V_{CC}	V
Output Range			0		V_{REFIN}	V
Output Resolution					10	Bits
Output Impedance	R_{DS}			35	100	Ω

ANALOG QUICK TRIP CHARACTERISTICS

(V_{CC} = +2.85V to +3.9V, T_A = -40°C to +95°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
MON2, TXP HI, TXP LO Full-Scale Voltage	V_{APC}			2.5		V
HBIAS LOS Full-Scale Voltage				1.25		V
MON2 Input Resistance			35	50	65	kΩ
Resolution				8		Bits
Error		T_A = +25°C		±2		%FS
Integral Nonlinearity			-1		+1	LSB
Differential Nonlinearity			-1		+1	LSB
Temperature Drift			-2.5		+2.5	%FS
LOS Offset				-5		mV

ANALOG VOLTAGE MONITORING CHARACTERISTICS

(V_{CC} = +2.85V to +3.9V, T_A = -40°C to +95°C, unless otherwise noted.)

PARAMETER		SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ADC Resolution					13		Bits
Input/Supply Accuracy (MON1–MON4, V_{CC})		ACC	At factory setting		0.25	0.50	%FS
Update Rate for Temperature, MON1–MON4, and V_{CC}		t_{RR}			64	75	ms
Input/Supply Offset (MON1–MON4, V_{CC})		V_{OS}	(Note 3)		0	5	LSB
Factory Setting	MON1–MON4		(Note 4)		2.5		V
	V_{CC}				6.5536		
	MON3 Fine				312.5		µV

DIGITAL THERMOMETER CHARACTERISTICS

(V_{CC} = +2.85V to +3.9V, T_A = -40°C to +95°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Thermometer Error	T_{ERR}	-40°C to +95°C	-3		+3	°C

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = +2.85V to +3.9V, T_A = -40°C to +95°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
TXD Enable	t_{OFF}	From ↑ TXD to BIAS DAC and MOD DAC disable			5	µs
Recovery from TXD Disable (Figure 13)	t_{ON}	From ↓ TXD to BIAS DAC and MOD DAC enable			5	µs
Recovery After Power-Up	t_{INIT_DAC}	From ↑ V_{CC} > VCC LO alarm (Note 5)		20		ms
Fault Reset Time (to TXF = 0)	t_{INITR1}	From ↓ TXD		131		ms
	t_{INITR2}	From ↑ V_{CC} > VCC LO alarm (Note 5)		161		
Fault Assert Time (to TXF = 1)	t_{FAULT}	After HTXP, LTXP, HBATH, IBIASMAX (Note 6)			15	µs
LOSOUT Assert Time	t_{LOSS_ON}	LLOS (Notes 6, 7)			15	µs
LOSOUT Deassert Time	t_{LOSS_OFF}	HLOS (Notes 6, 8)			15	µs

TIMING CHARACTERISTICS (CONTROL LOOP AND QUICK TRIP)

(V_{CC} = +2.85V to +3.9V, T_A = -40°C to +95°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output-Enable Time Following POA	t_{INIT}	(Note 5)		20		ms
Binary Search Time	t_{SEARCH}	(Note 9)	8		10	BIAS Samples

I²C AC ELECTRICAL CHARACTERISTICS

(V_{CC} = +2.85V to +3.9V, T_A = -40°C to +95°C, timing referenced to $V_{IL(MAX)}$ and $V_{IH(MIN)}$, unless otherwise noted.) (See Figure 16.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SCL Clock Frequency	f_{SCL}	(Note 10)	0		400	kHz
Clock Pulse-Width Low	t_{LOW}		1.3			µs
Clock Pulse-Width High	t_{HIGH}		0.6			µs
Bus-Free Time Between STOP and START Condition	t_{BUF}		1.3			µs
START Hold Time	$t_{HD:STA}$		0.6			µs
START Setup Time	$t_{SU:STA}$		0.6			µs
Data Out Hold Time	$t_{HD:DAT}$		0		0.9	µs
Data In Setup Time	$t_{SU:DAT}$		100			ns
Rise Time of Both SDA and SCL Signals	t_R	(Note 11)	20 + 0.1C_B		300	ns
Fall Time of Both SDA and SCL Signals	t_F	(Note 11)	20 + 0.1C_B		300	ns
STOP Setup Time	$t_{SU:STO}$		0.6			µs
EEPROM Write Time	t_{WR}	(Note 12)			20	ms
Capacitive Load for Each Bus Line	C_B				400	pF

NONVOLATILE MEMORY CHARACTERISTICS

(V_{CC} = +2.85V to +3.9V, unless otherwise noted.)

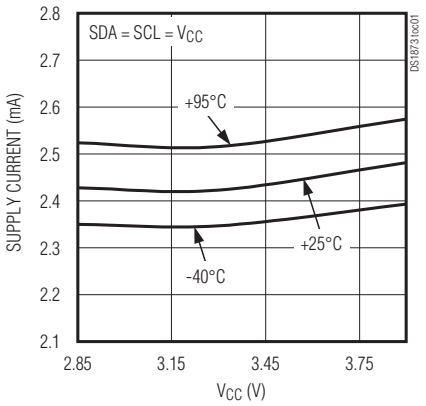
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
EEPROM Write Cycles		At +25°C	200,000			
		At +85°C	50,000			

Note 1: All voltages are referenced to ground. Current into the IC is positive, and current out of the IC is negative.
Note 2: Inputs are at supply rail. Outputs are not loaded.
Note 3: This parameter is guaranteed by design.
Note 4: Full-scale is user programmable.
Note 5: A temperature conversion is completed and the MOD DAC value is recalled from the LUT and V_{CC} has been measured to be above VCC LO alarm.
Note 6: The sampling time is 1.6µs per cycle. Each input is sampled every 8 cycles.
Note 7: This specification is the time it takes from MON3 voltage falling below the LLOS trip threshold to LOSOUT asserted high.
Note 8: This specification is the time it takes from MON3 voltage rising above the HLOS trip threshold to LOSOUT asserted low.
Note 9: Assuming an appropriate initial step is programmed that would cause the power to exceed the APC set point within four steps, the bias output will be within 3% within the time specified by the binary search time. See the *BIAS and MOD Output Control During Power-Up* section.
Note 10: I²C interface timing shown is for fast mode (400kHz). This device is also backward compatible with I²C standard mode timing.
Note 11: C_B—the total capacitance of one bus line in pF.
Note 12: EEPROM write begins after a STOP condition occurs.

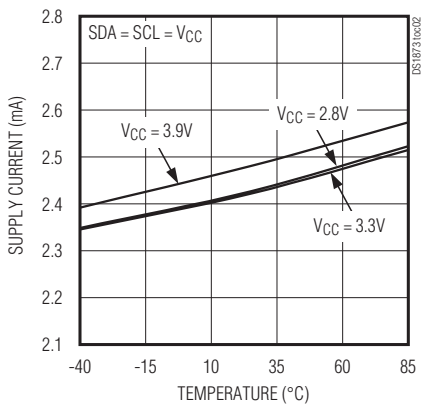
Typical Operating Characteristics

(V_{CC} = +2.85V to +3.9V, T_A = +25°C, unless otherwise noted.)

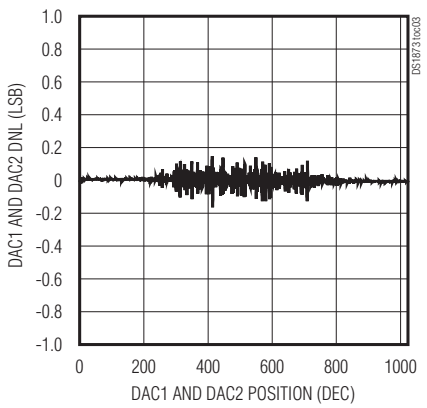
SUPPLY CURRENT vs. SUPPLY VOLTAGE



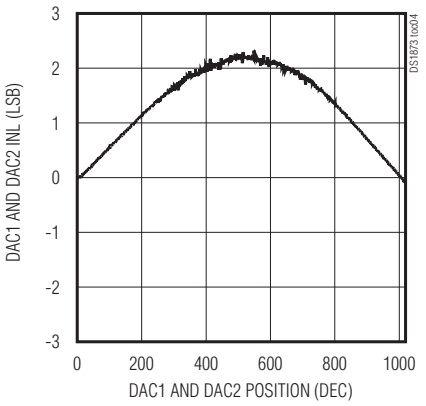
SUPPLY CURRENT vs. TEMPERATURE



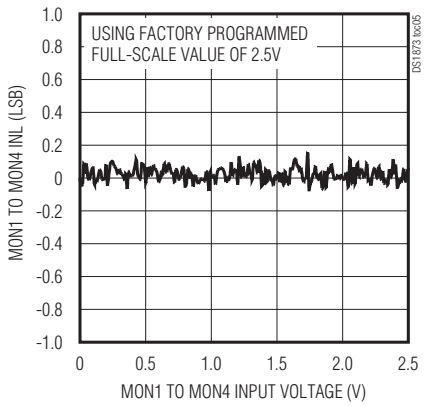
DAC1 AND DAC2 DNL



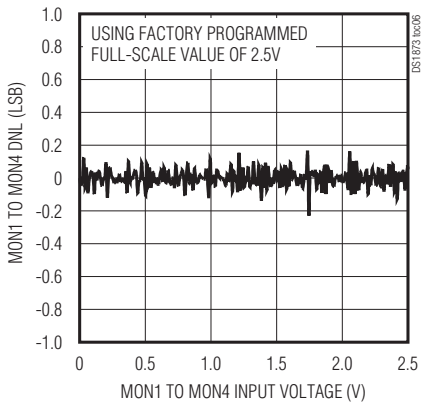
DAC1 AND DAC2 INL



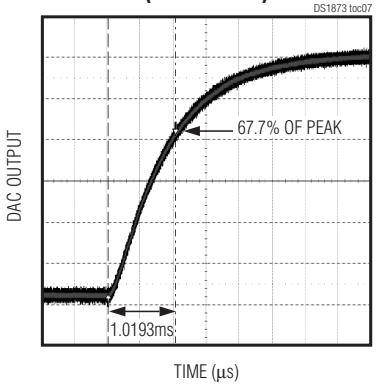
MON1 TO MON4 INL



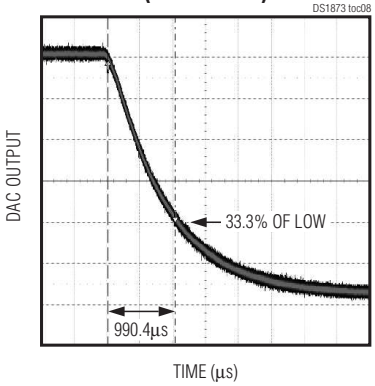
MON1 TO MON4 DNL



DAC SETTLING TIME (40% TO 60%)



DAC SETTLING TIME (60% TO 40%)

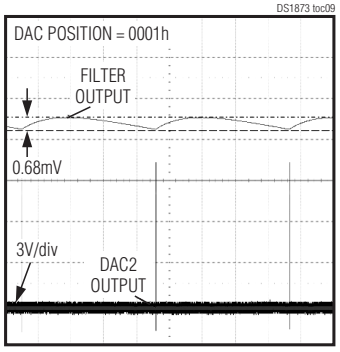


SFP+ Controller with Analog LDD Interface

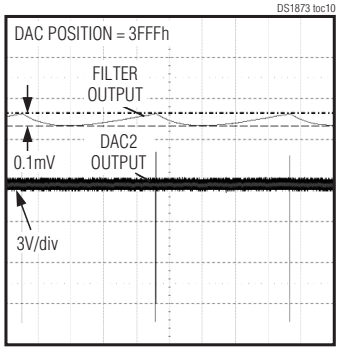
Typical Operating Characteristics (continued)

(V_{CC} = +2.85V to +3.9V, T_A = +25°C, unless otherwise noted.)

DAC OUTPUT RIPPLE AT 0001h



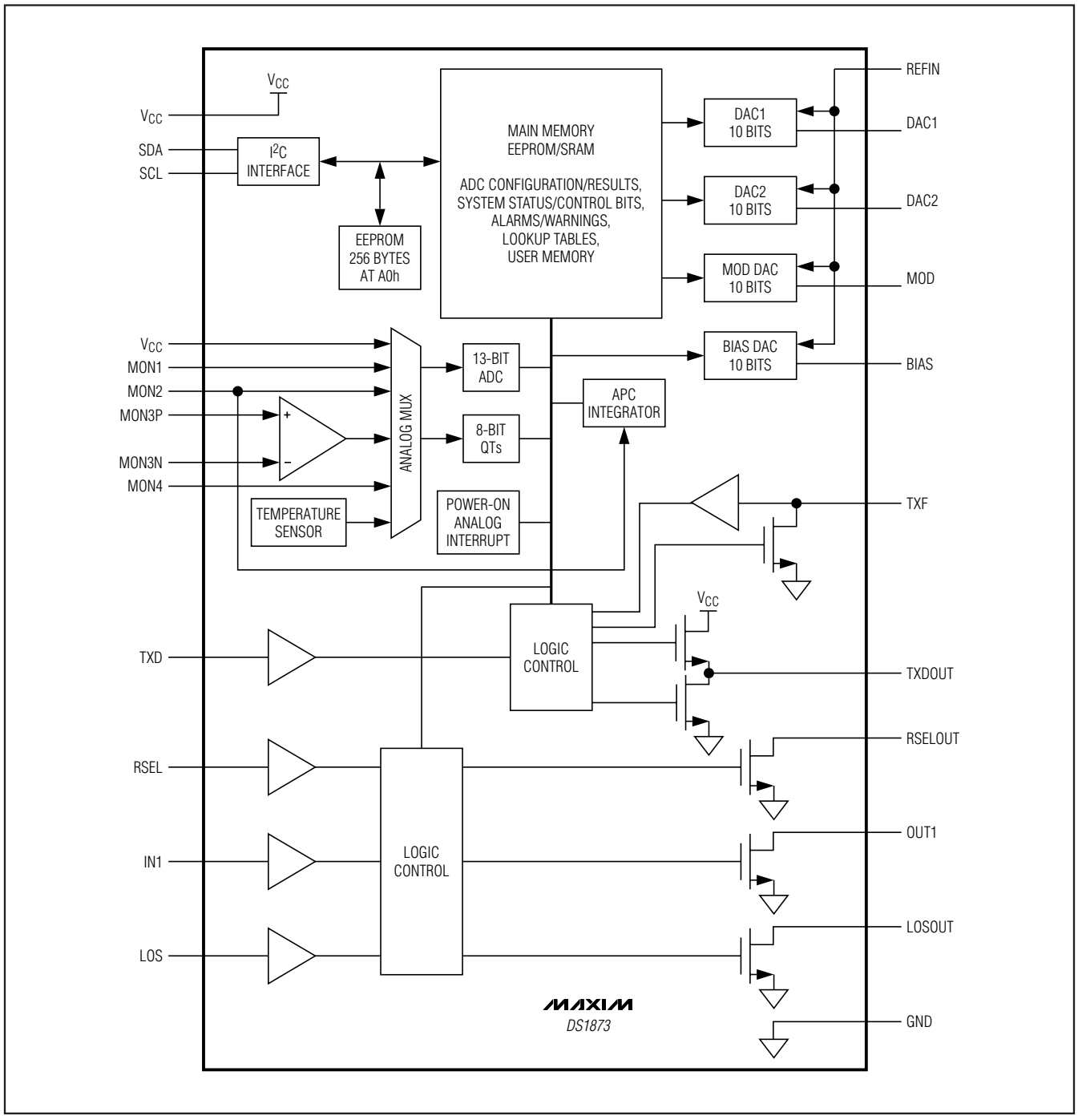
DAC OUTPUT RIPPLE AT 3FFFh



Pin Description

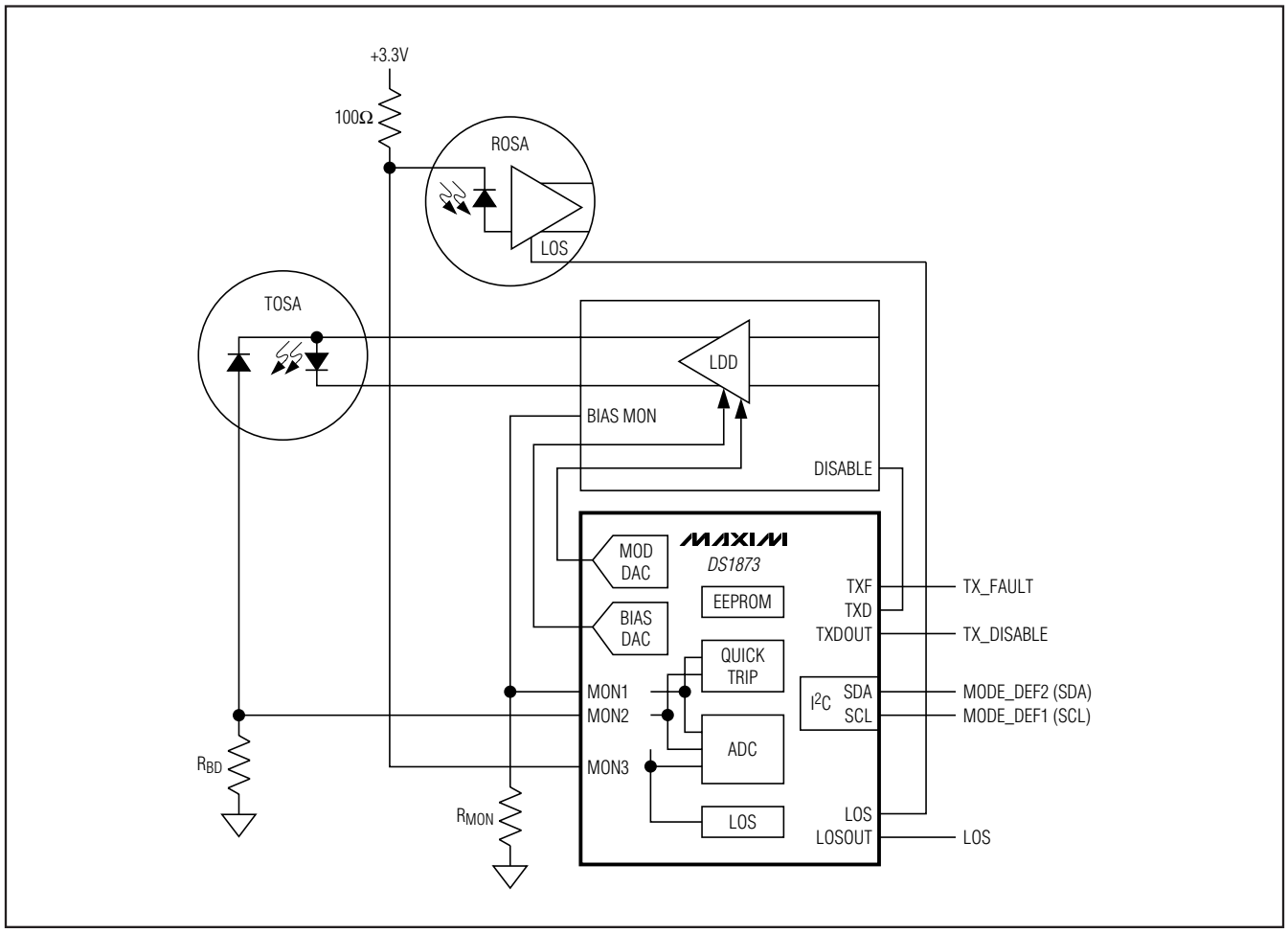
PIN	NAME	FUNCTION
1	RSELOUT	Open-Drain Rate-Select Output
2	SCL	I^2C Serial-Clock Input
3	SDA	I^2C Serial-Data Input/Output
4	TXF	Transmit-Fault Input and Output. The output is open drain.
5	LOS	Loss-of-Signal Input
6	IN1	Digital Input. General-purpose input with AS1 in SFF-8079 or RS1 in SFF-8431.
7	TXD	Transmit-Disable Input
8, 18, 21	GND	Ground Connection
9	RSEL	Rate-Select Input
10	TXDOUT	Transmit-Disable Output
11	MON4	External Monitor Input 4
12, 13	MON3P, MON3N	Differential External Monitor Input 3 and LOS LO Quick Trip
14	MON1	External Monitor Input 1 and HBATH Quick Trip
15, 23	N.C.	No Connection
16, 26	V_{CC}	Power-Supply Input
17	MON2	External Monitor Input 2. Feedback voltage for APC loop and HTXP/LTXP quick trip.
19	MOD	MOD DAC, Delta-Sigma Output
20	BIAS	BIAS DAC, Delta-Sigma Output
22	REFIN	Reference Input for DAC1 and DAC2
24, 25	DAC1, DAC2	Delta-Sigma Output 1/2
27	LOSOUT	Open-Drain Receive Loss-of-Signal Output
28	OUT1	Open-Drain Digital Output. General-purpose output with AS1 output in SFF-8079 or RS1 output in SFF-8431.
—	EP	Exposed Pad (Connect to GND)

Block Diagram



SFP+ Controller with Analog LDD Interface

Typical Operating Circuit



Detailed Description

The DS1873 integrates the control and monitoring functionality required to implement an SFP or SFP+ system. Key components of the DS1873 are shown in the *Block Diagram* and described in subsequent sections.

BIAS DAC/APC Control

The DS1873 controls its laser bias current using its BIAS DAC and the APC loop. The APC loop's feedback to the DS1873 is the monitor diode (MON2) current, which is converted to a voltage using an external resistor. The feedback is sampled by a comparator and compared to a digital set-point value. The output of the comparator has three states: up, down, or no-operation. The no-operation state prevents the output from excessive toggling once steady state is reached. As long as the comparator output is in either the up or down states, the bias is adjusted by incrementing and decrementing the BIAS DAC setting.

The DS1873 has an LUT to allow the APC set point to change as a function of temperature to compensate for tracking error (TE). The TE LUT has 36 entries that determine the APC setting in 4°C windows between -40°C to +100°C.

Table 1. Acronyms

ACRONYM	DEFINITION
ADC	Analog-to-Digital Converter
AGC	Automatic Gain Control
APC	Automatic Power Control
APD	Avalanche Photodiode
ATB	Alarm Trap Bytes
BM	Burst Mode
DAC	Digital-to-Analog Converter
LOS	Loss of Signal
LUT	Lookup Table
NV	Nonvolatile
QT	Quick Trip
TE	Tracking Error
TIA	Transimpedance Amplifier
ROSA	Receiver Optical Subassembly
SEE	Shadowed EEPROM
SFF	Small Form Factor
SFF-8472	Document Defining Register Map of SFPs and SFFs
SFP	Small Form Factor Pluggable
SFP+	Enhanced SFP
TOSA	Transmit Optical Subassembly
TXP	Transmit Power

BIAS and MOD Output Control During Power-Up

On power-up, the DS1873 sets the MOD and BIAS DACs to 0. After a temperature conversion is completed and if the VCC LO alarm is enabled, an additional V_{CC} conversion above the customer-defined VCC LO alarm level is required before the MOD DAC is updated with the value determined by the temperature conversion and the modulation LUT.

When the MOD DAC is set, the BIAS DAC is set to a value equal to ISTEP (see Figure 1). The startup algorithm checks if this bias current causes a feedback voltage above the APC set point, and if not, it continues increasing the BIAS DAC by ISTEP until the APC set-point is exceeded. When the APC set point is exceeded, the device begins a binary search to quickly reach the bias current corresponding to the proper power level. After the binary search is completed, the APC integrator is enabled and single LSB steps are used to tightly control the average power.

The TXP HI, TXP LO, HBAL, and BIAS MAX QT alarms are masked until the binary search is completed. However, the BIAS MAX alarm is monitored during this time to prevent the BIAS DAC from exceeding IBIASMAX. During the bias current initialization, the BIAS DAC is not allowed to exceed IBIASMAX. If this occurs during the ISTEP sequence, then the binary search routine is

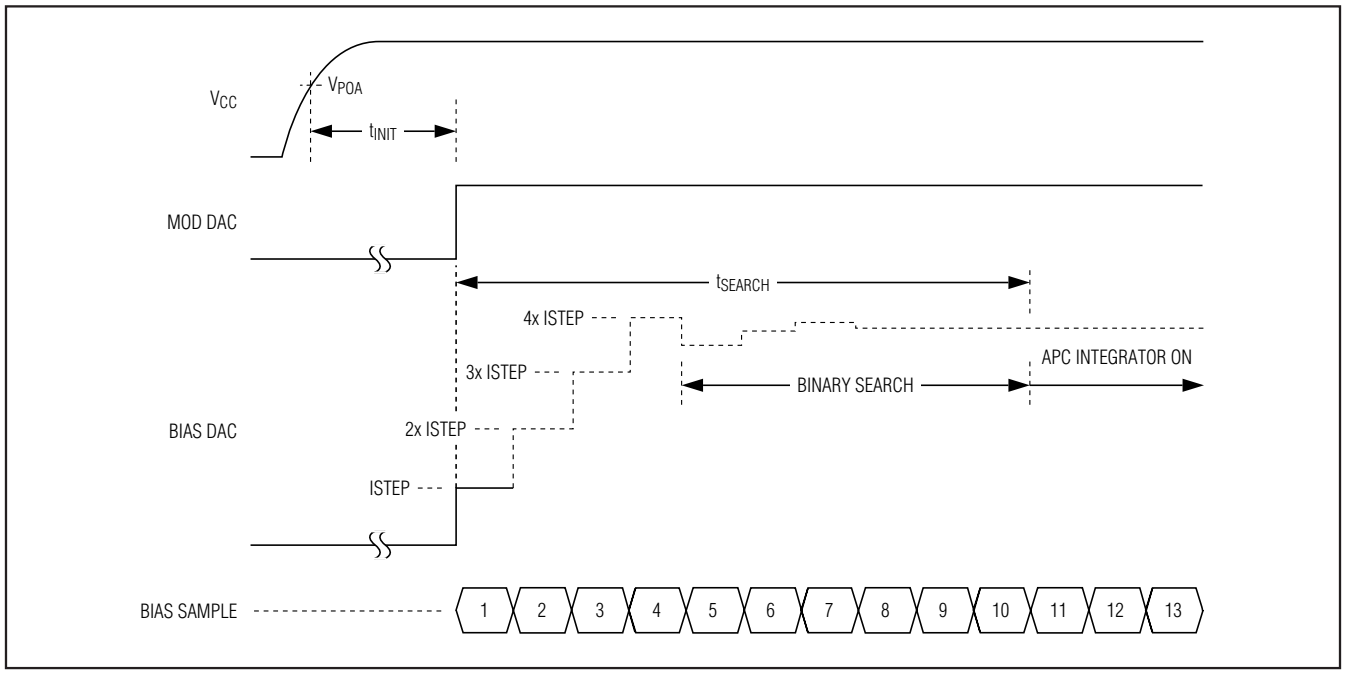


Figure 1. Power-Up Timing

enabled. If IBIASMAX is exceeded during the binary search, the next smaller step is activated. ISTEP or binary increments that would cause the BIAS DAC to exceed IBIASMAX are not taken. Masking the alarms until the completion of the binary search prevents false positive alarms during startup.

ISTEP is programmed by the customer using Table 02h, Register BBh. ISTEP should be programmed to the maximum safe increase that is allowable during startup. If this value is programmed too low, the DS1873 still operates, but it could take significantly longer for the algorithm to converge and hence to control the average power.

If a fault is detected, and TXD is toggled to reenable the outputs, the DS1873 powers up following a similar sequence to an initial power-up. The only difference is that the DS1873 already has determined the present temperature, so the t_{INIT} time is not required for the DS1873 to recall the APC and MOD set points from EEPROM.

BIAS and MOD DACs as a Function of Transmit Disable (TXD)

If TXD is asserted (logic 1) during normal operation, the outputs are disabled within t_{OFF}. When TXD is deasserted (logic 0), the DS1873 sets the MOD DAC register with the value associated with the present temperature, and initializes the BIAS DAC using the same search algorithm as done at startup. When asserted, soft TXD (TXDC) (Lower Memory, Register 6Eh) would allow a software control identical to the TXD pin (see Figure 2).

APC and Quick-Trip Timing

As shown in Figure 3, the DS1873's input comparator is shared between the APC control loop and the quick-trip alarms (TXP HI, TXP LO, LOS LO, and BIAS HI). The comparator polls the alarms in a multiplexed sequence. Five of every eight comparator readings are used for APC loop bias-current control. The other three updates are used to check the HTXP/LTXP (monitor diode voltage), the HBATH (MON1), and LOS (MON3) signals against the internal APC, BIAS, and MON3 reference, respectively. If the last APC comparison was higher than the APC set point, it makes an HTXP comparison, and if it is lower, it makes an LTXP comparison. Depending on the results of the comparison, the corresponding alarms and warnings (TXP HI, TXP LO) are asserted or deasserted.

The DS1873 has a programmable comparator sample time based on an internally generated clock to facilitate a wide variety of external filtering options and time delays. The UPDATE RATE register (Table 02h, Register 88h) determines the sampling time. Samples occur at a regular interval, t_{REP}, which is set at 1.6µs. Table 2 shows the sample rate options available. Any quick-trip alarm that is detected by default remains active until a subsequent comparator sample shows the condition no longer exists. A second bias current monitor (BIAS MAX) compares the BIAS DAC's code to a digital value stored in the IBIASMAX register. This comparison is made at every bias current update to ensure that a high-bias current is quickly detected.

The quick-trip comparator uses a 1.6µs window to sample each input. After an APC comparison that requires

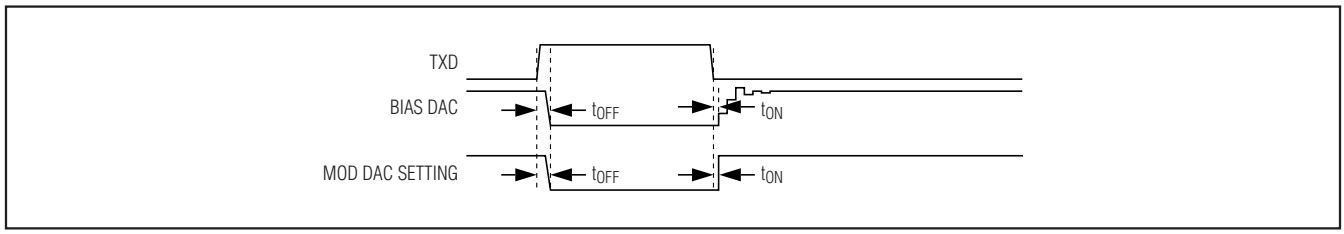


Figure 2. TXD Timing

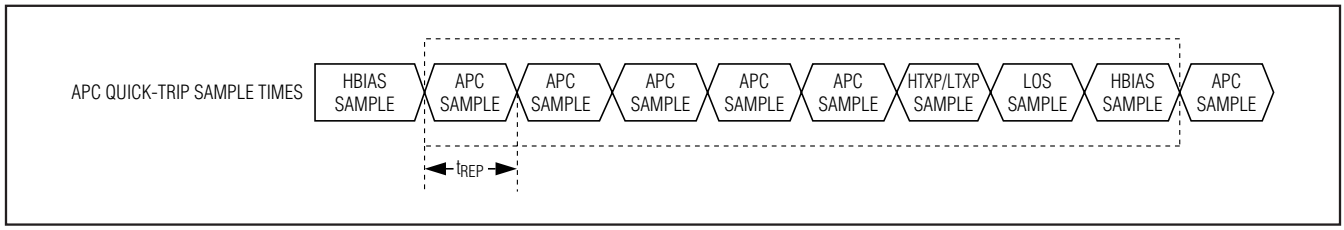


Figure 3. APC Loop and Quick-Trip Sample Timing

an update to the BIAS DAC, a settling time (as calculated below) is required to allow for the feedback on BMD (MON2) to stabilize. This time is dependent on the time constant of the filter pole used for the delta-to-sigma BIAS output. During the timing of the settling rate, comparisons of APC comparisons of BMD are ignored until 32 sample periods (t_{REP}) have passed.

SettlingTime = 51.2µs x (APC_SR[3:0] + 1)

Monitors and Fault Detection

Monitors

Monitoring functions on the DS1873 include five quick-trip comparators and six ADC channels. This monitoring combined with the alarm enables (Table 01h/05h) determines when/if the DS1873 turns off the MOD and BIAS DACs and triggers the TXF and TXDOUT outputs. All the monitoring levels and interrupt masks are user programmable.

Five Quick-Trip Monitors and Alarms

Five quick-trip monitors are provided to detect potential laser safety issues and LOS status. These monitor the following:

1) High Bias Current (HBATH)
2) Low Transmit Power (LTXP)
3) High Transmit Power (HTXP)
4) Max Output Current (IBIASMAX)
5) Loss-of-Signal (LOS LO)

The high-transmit and low-transmit power quick-trip registers (HTXP and LTXP) set the thresholds used to compare against the MON2 voltage to determine if the transmit power is within specification. The HBATH quick trip compares the MON1 input (generally from the laser driver's bias monitor output) against its threshold setting to determine if the present bias current is above specification. The BIAS MAX quick trip determines if the BIAS DAC is above specification (IBIASMAX). When the new BIAS DAC value is calculated, it is compared against the IBIASMAX register. The BIAS DAC is not allowed to exceed the value set in the IBIASMAX register. When the DS1873 detects that the bias is at the limit, it sets the BIASMAX status bit and holds the BIAS DAC setting at the IBIASMAX level. The bias and power quick trips are routed to the TXF through interrupt masks to allow combinations of these alarms to be used to trigger these outputs. The user can program up to eight different temperature-indexed threshold levels for MON1 (Table 02h, Register D1h). The LOS LO quick trip compares the MON3 input against its threshold setting to determine if the present received power is below the specification. The LOS LO quick trip can be used to set the LOSOUT pin.

Six ADC Monitors and Alarms

The ADC monitors six channels that measure temperature (internal temp sensor), V_{CC}, and MON1–MON4 using an analog multiplexer to measure them round robin with a single ADC (see the *ADC Timing* section). The five voltage channels have a customer-programmable full-scale range and all channels have a customer-programmable offset value that is factory programmed to default value (see Table 2). Additionally, MON1–MON4 can right-shift results by up to 7 bits before the results are compared to alarm thresholds or read over the I^2C bus. This allows customers with specified ADC ranges to calibrate the ADC full scale to a factor of $1/2^n$ of their specified range to measure small signals. The DS1873 can then right-shift the results by n bits to maintain the bit weight of their specification (see the *Right-Shifting ADC Result* and *Enhanced RSSI Monitoring (Dual-Range Functionality)* sections).

Table 2. ADC Default Monitor Full-Scale Ranges

SIGNAL	+FS SIGNAL	+FS hex	-FS SIGNAL	-FS hex
Temperature (°C)	127.996	7FFF	-128	8000
V_{CC} (V)	6.5528	FFF8	0	0000
MON1–MON4 (V)	2.4997	FFF8	0	0000

The ADC results (after right-shifting, if used) are compared to the alarm and warning thresholds after each conversion, and the corresponding alarms are set, which can be used to trigger the TXF output. These ADC thresholds are user programmable, as are the masking registers that can be used to prevent the alarms from triggering the TXF output.

ADC Timing

There are six analog channels that are digitized in a round-robin fashion in the order shown in Figure 4. The total time required to convert all six channels is t_{RR} (see the *Analog Voltage Monitoring Characteristics* for details).

Right-Shifting ADC Result

If the weighting of the ADC digital reading must conform to a predetermined full-scale (PFS) value defined by a standard's specification (e.g., SFF-8472), then right-shifting can be used to adjust the PFS analog measurement range while maintaining the weighting of

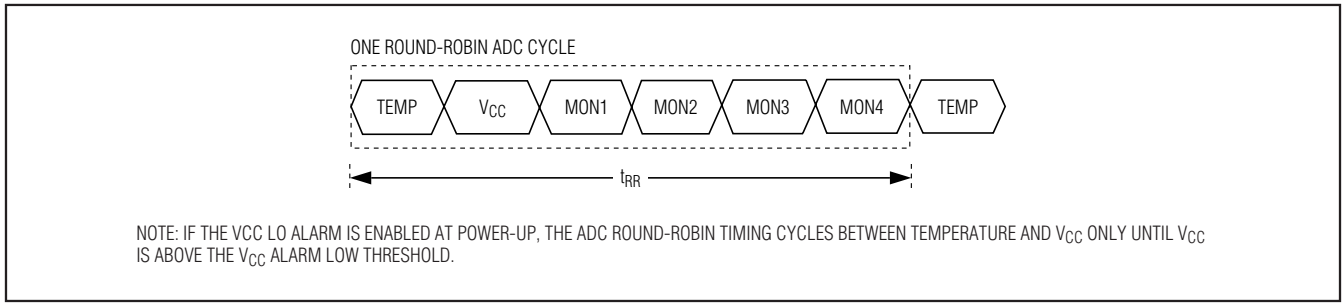


Figure 4. ADC Round-Robin Timing

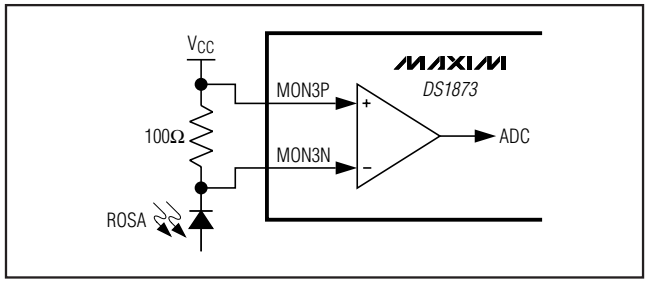


Figure 5. MON3 Differential Input for High-Side RSSI

the ADC results. The DS1873's range is wide enough to cover all requirements; when the maximum input value is ≤ 1/2 of the FS value, right-shifting can be used to obtain greater accuracy. For instance, the maximum voltage might be 1/8 the specified PFS value, so only 1/8 the converter's range is effective over this range. An alternative is to calibrate the ADC's full-scale range to 1/8 the readable PFS value and use a right-shift value of 3. With this implementation, the resolution of the measurement is increased by a factor of 8, and because the result is digitally divided by 8 by right-shifting, the bit weight of the measurement still meets the standard's specification (i.e., SFF-8472).

The right-shift operation on the ADC result is carried out based on the contents of right-shift control registers (Table 02h, Registers 8Dh–8Fh) in EEPROM. Four analog channels, MON1–MON4, each have 3 bits allocated to set the number of right-shifts. Up to 7 right-shift operations are allowed and are executed as a part of every conversion before the results are compared to the high-alarm and low-alarm levels, or loaded into their corresponding measurement registers (Lower Memory, Registers 64h–6Bh). This is true during the setup of internal calibration as well as during subsequent data conversions.

Differential MON3 Input

The DS1873 offers a fully differential input for MON3. This enables high-side monitoring of RSSI, as shown in Figure 5. This reduces board complexity by eliminating the need for a high-side differential amplifier or a current mirror.

Enhanced RSSI Monitoring (Dual-Range Functionality)

The DS1873 offers a feature to improve the accuracy and range of MON3, which is most commonly used for monitoring RSSI. The accuracy of the RSSI measurements is increased at the small cost of reduced range (of input signal swing). The DS1873 eliminates this trade-off by offering "dual range" calibration on the MON3 channel (see Figure 5). This feature enables right-shifting (along with its gain and offset settings) when the input signal is below a set threshold (within the range that benefits using right-shifting) and then automatically disables right-shifting (recalling different gain and offset settings) when the input signal exceeds the threshold. Also, to prevent "chattering," hysteresis prevents excessive switching between modes in addition to ensuring that continuity is maintained. Dual-range operation is enabled by default (factory programmed in EEPROM). However, it can easily be disabled through the RSSI_FC and RSSI_FF bits, which are described in the *Register Descriptions* section. When dual-range operation is disabled, MON3 operates identically to the other MON channels, although featuring a differential input.

Dual-range functionality consists of two modes of operation: fine mode and coarse mode. Each mode is calibrated for a unique transfer function, hence the term, dual range. Table 4 highlights the registers related to MON3. Fine mode is equivalent to the other MON channels. Fine mode is calibrated using the gain, offset, and right-shifting registers at locations shown in Table 4 and is ideal for relatively small analog input voltages. Coarse mode is automatically switched to when the input exceeds a threshold (to be discussed in a subsequent paragraph). Coarse mode is calibrated using different gain and offset registers, but lacks right-shifting (since coarse mode is only used on large input signals). The gain and offset registers for coarse mode are also shown in Table 4.

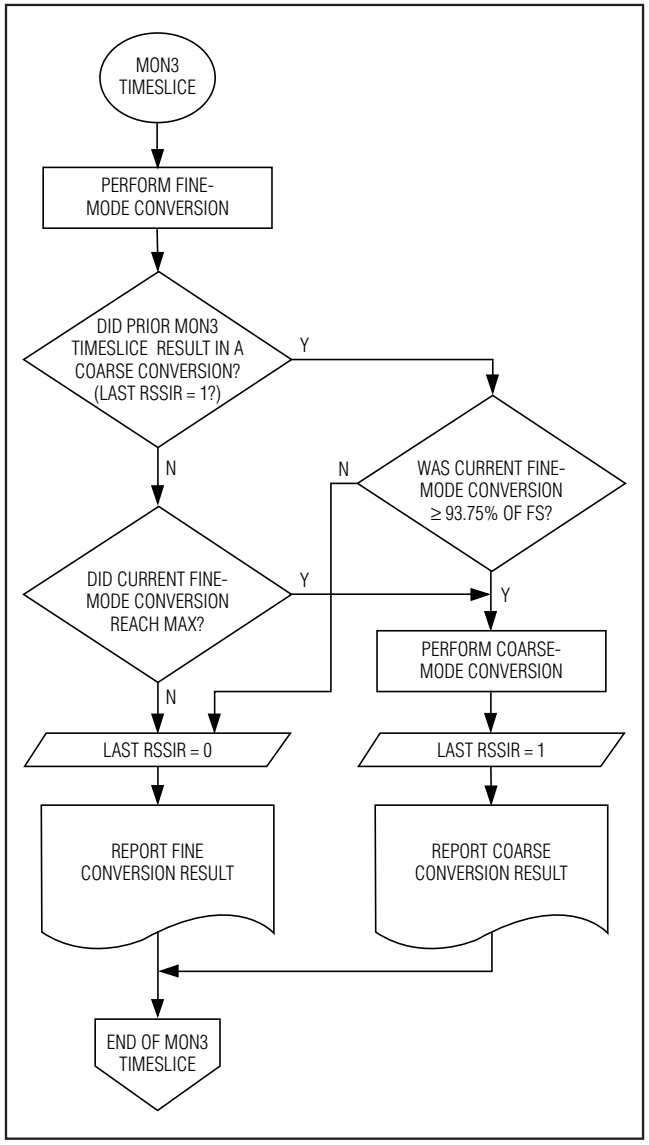


Figure 6. RSSI Flowchart

Additional information for each of the registers can be found in the *Register Descriptions* section.

Dual-range operation is transparent to the end user. The results of MON3 analog-to-digital conversions are still stored/reported in the same memory locations (68h–69h, Lower Memory) regardless of whether the conversion was performed in fine mode or coarse mode. The only way to tell which mode generated the digital result is by reading the RSSIR bit.

When the DS1873 is powered up, analog-to-digital conversions begin in a round-robin fashion. Every MON3 timeslice begins with a fine mode analog-to-digital conversion (using fine mode's gain, offset, and right-shifting settings). See the flowchart in Figure 6 for more details. Then, depending on whether the last MON3 timeslice resulted in a coarse-mode conversion and also depending on the value of the current fine conversion, decisions are made whether to use the current fine-mode conversion result or to make an additional conversion (within the same MON3 timeslice), using coarse mode (using coarse mode's gain and offset settings and no right-shifting) and reporting the coarse-mode result. The flowchart in Figure 6 also illustrates how hysteresis is implemented. The fine-mode conversion is compared to one of two thresholds. The actual threshold values are a function of the number of right-shifts being used. With the use of right-shifting, the fine mode full-scale is programmed to (1/2^nth) of the coarse mode full-scale. The DS1873 now auto ranges to choose the range that gives the best resolution for the measurement. Hysteresis is applied to eliminate chatter when the input resides at the boundary of the two ranges. See Figure 6 for details. Table 3 shows the threshold values for each possible number of right-shifts.

Table 3. MON3 Hysteresis Threshold Values

NUMBER OF RIGHT-SHIFTS	FINE MODE MAX (hex)	COARSE MODE MIN* (hex)
0	FFF8	F000
1	7FFC	7800
2	3FFE	3C00
3	1FFF	1E00
4	0FFF	0F00
5	07FF	0780
6	03FF	03C0
7	01FF	01E0

**This is the minimum reported coarse-mode conversion.*

Table 4. MON3 Configuration Registers

REGISTER	FINE MODE	COARSE MODE
GAIN	98h–99h, Table 02h	9Ch–9Dh, Table 02h
OFFSET	A8h–A9h, Table 02h	ACh–ADh, Table 02h
RIGHT-SHIFT$_0$	8Fh, Table 02h	—
CNFGC	8Bh, Table 02h	
UPDATE (RSSIR BIT)	6Fh, Lower Memory	
MON3 VALUE	68h–69h, Lower Memory	

The RSSI_FF and RSSI_FC bits are used to force fine-mode or coarse-mode conversions, or to disable the dual-range functionality. Dual-range functionality is enabled by default (both RSSI_FC and RSSI_FF are factory programmed to 0 in EEPROM). It can be disabled by setting RSSI_FC to 0 and RSSI_FF to 1. These bits are also useful when calibrating MON3. For additional information, see Figure 18. The dual-range calibration can operate in two modes: crossover enabled and crossover disabled.

- **Crossover Enabled:** For systems with nonlinear relationships between the ADC input and the desired ADC result, the mode should be set to crossover enabled. The RSSI measurement of an APD receiver is one such application. Using the crossover-enabled mode allows a piecewise linear approximation of the nonlinear response of the APD's gain factor. The crossover point is the point between fine and coarse points. The ADC result transitions between the fine and coarse ranges with no hysteresis. Right-shifting, slope adjustment, and offset are configurable for both the fine and coarse ranges. See Figure 7.
- **Crossover Disabled:** The crossover-disabled mode is intended for systems with a linear relationship between the MON3 input and the desired ADC result. Hysteresis allows for a nonjittery response when the input is at the crossover boundary of the fine and coarse ADC. In a nonlinear system, the hysteresis could cause significant errors in the ADC result. See Figure 8.

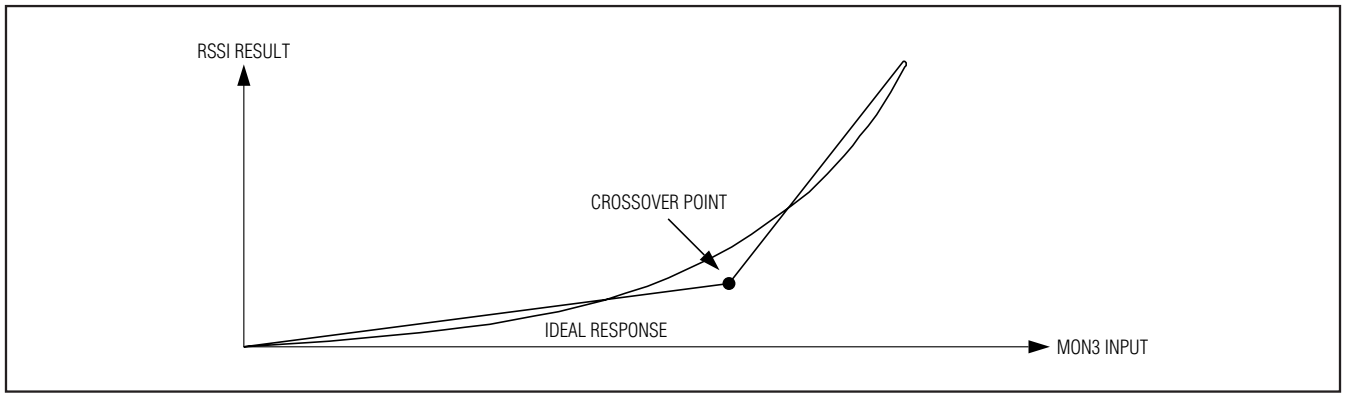


Figure 7. RSSI with Crossover Enabled

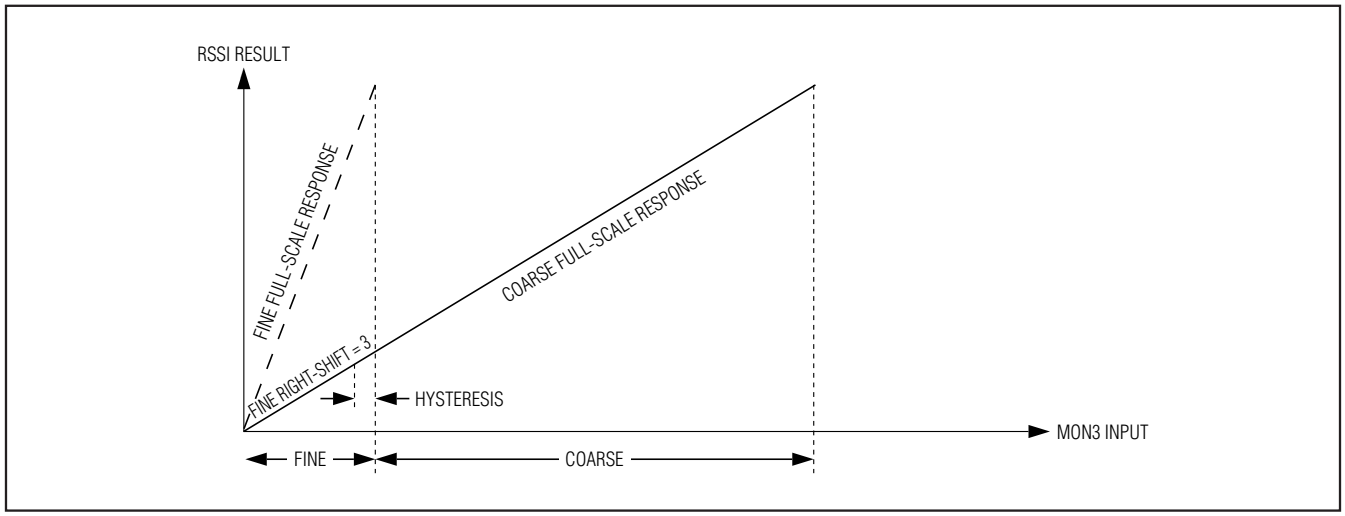


Figure 8. RSSI with Crossover Disabled

Low-Voltage Operation

The DS1873 contains two power-on reset (POR) levels. The lower level is a digital POR (POD) and the higher level is an analog POR (POA). At startup, before the supply voltage rises above POA, the outputs are disabled, all SRAM locations are set to their defaults, shadowed EEPROM (SEE) locations are zero, and all analog circuitry is disabled. When V_{CC} reaches POA, the SEE is recalled, and the analog circuitry is enabled. While V_{CC} remains above POA, the device is in its normal operating state, and it responds based on its nonvolatile configuration. If during operation V_{CC} falls below POA, but is still above POD, then the SRAM retains the SEE settings from the first SEE recall, but the device analog is shut down and the outputs disabled. If the supply voltage recovers back above POA, then the device immediately resumes normal operation. If the supply voltage falls below POD, then the device SRAM is placed in its default state and another SEE recall is required to reload the nonvolatile settings. The EEPROM recall occurs the next time V_{CC} exceeds POA. Figure 9 shows the sequence of events as the voltage varies.

Any time V_{CC} is above POD, the I^2C interface can be used to determine if V_{CC} is below the POA level. This is accomplished by checking the RDYB bit in the STATUS (Lower Memory, Register 6Eh) byte. RDYB is set when V_{CC} is below POA; when V_{CC} rises above POA, RDYB is timed (within 500µs) to go to 0, at which point the part is fully functional.

For all device addresses sourced from EEPROM (Table 02h, Register 8Ch), the default device address is A2h until V_{CC} exceeds POA, allowing the device address to be recalled from the EEPROM.

Power-On Analog (POA)

POA holds the DS1873 in reset until V_{CC} is at a suitable level (V_{CC} > POA) for the device to accurately measure with its ADC and compare analog signals with its quick-trip monitors. Because V_{CC} cannot be measured by the ADC when V_{CC} is less than POA, POA also asserts the VCC LO alarm, which is cleared by a V_{CC} ADC conversion greater than the customer-programmable V_{CC} alarm LO ADC limit. This allows a programmable limit to ensure that the headroom requirements of the transceiver are satisfied during a slow power-up. The TXF output does not latch until there is a conversion above V_{CC} low limit. The POA alarm is nonmaskable. The TXF output is asserted when V_{CC} is below POA. See the *Low-Voltage Operation* section for more information.

Delta-Sigma Outputs

Four delta-sigma outputs are provided: MOD DAC, BIAS DAC, DAC1, and DAC2. With the addition of an external RC filter, these outputs provide 10-bit resolution analog outputs with the full-scale range set by the input REFIN. Each output is either manually controlled or controlled using a temperature-indexed LUT, or in the case of the BIAS DAC, controlled by the APC loop. A delta-sigma is a digital output using pulse-density modulation. It provides much lower output ripple than a

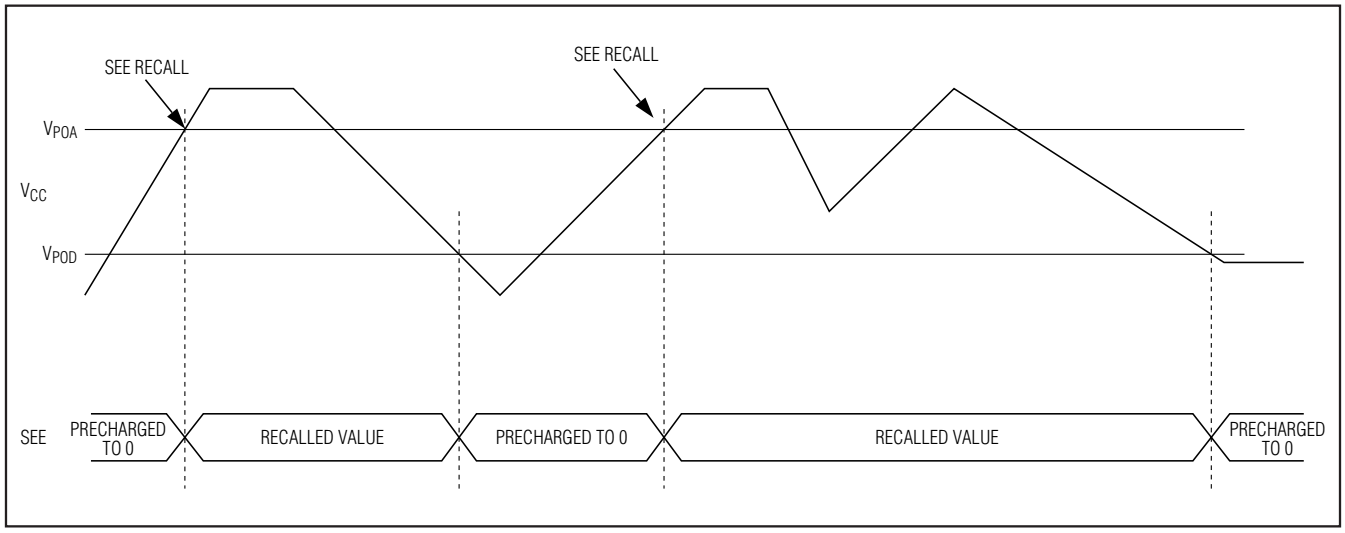


Figure 9. Low-Voltage Hysteresis Example

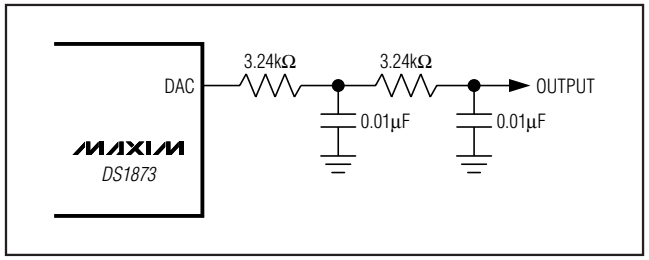


Figure 10. Recommended RC Filter for DAC1/DAC2

standard digital PWM output given the same clock rate and filter components. Before t_{INIT}, the DAC outputs are high impedance.

The external RC filter components are chosen based on ripple requirements, output load, delta-sigma frequency, and desired response time. A recommended filter is shown in Figure 10.

The DS1873's delta-sigma outputs are 10 bits. For illustrative purposes, a 3-bit example is provided. Each possible output of this 3-bit delta-sigma DAC is given in Figure 11.

In LUT mode, MOD, DAC1, and DAC2 are each controlled by an LUT with high-temperature resolution and an OFFSET LUT with lower temperature resolution. The MOD and DAC1 high-resolution LUTs each have 2°C resolution. The DAC2 high-resolution LUT has 4°C resolution. The OFFSET LUTs are located in the upper eight registers (F8h–FFh) of the table containing each high-resolution LUT. MOD DAC, DAC1 VALUE, and DAC2 VALUE are determined as follows:

MOD DAC = MOD LUT + 4 x (MOD OFFSET LUT)

DAC1 VALUE = DAC1 LUT + 4 x (DAC1 OFFSET LUT)

DAC2 VALUE = DAC1 LUT + 4 x (DAC1 OFFSET LUT)

Example calculation for MOD DAC:

Assumptions:

1) Temperature is 43°C.
2) Table 04h (MOD OFFSET LUT), Register FCh = 2Ah.
3) Table 04h (MOD LUT), Register A9h = 7Bh.

Because the temperature is 43°C, the MOD LUT index is A9h and the MOD OFFSET LUT index is FCh.

MOD DAC = 7Bh + 4 x 2Ah = 123h = 291

When temperature controlled, the DACs are updated after each temperature conversion.

The reference input, REFIN, is the supply voltage for all four DACs. The voltage connected to REFIN and its decoupling must be able to support the edge rate requirements of the delta-sigma outputs.

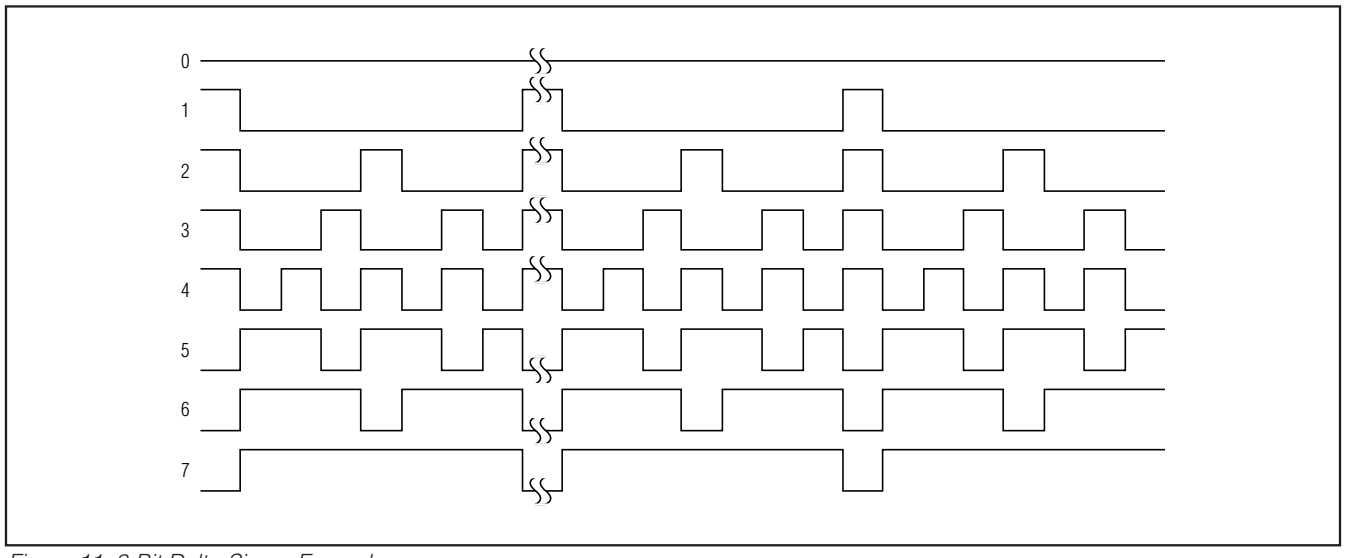


Figure 11. 3-Bit Delta-Sigma Example

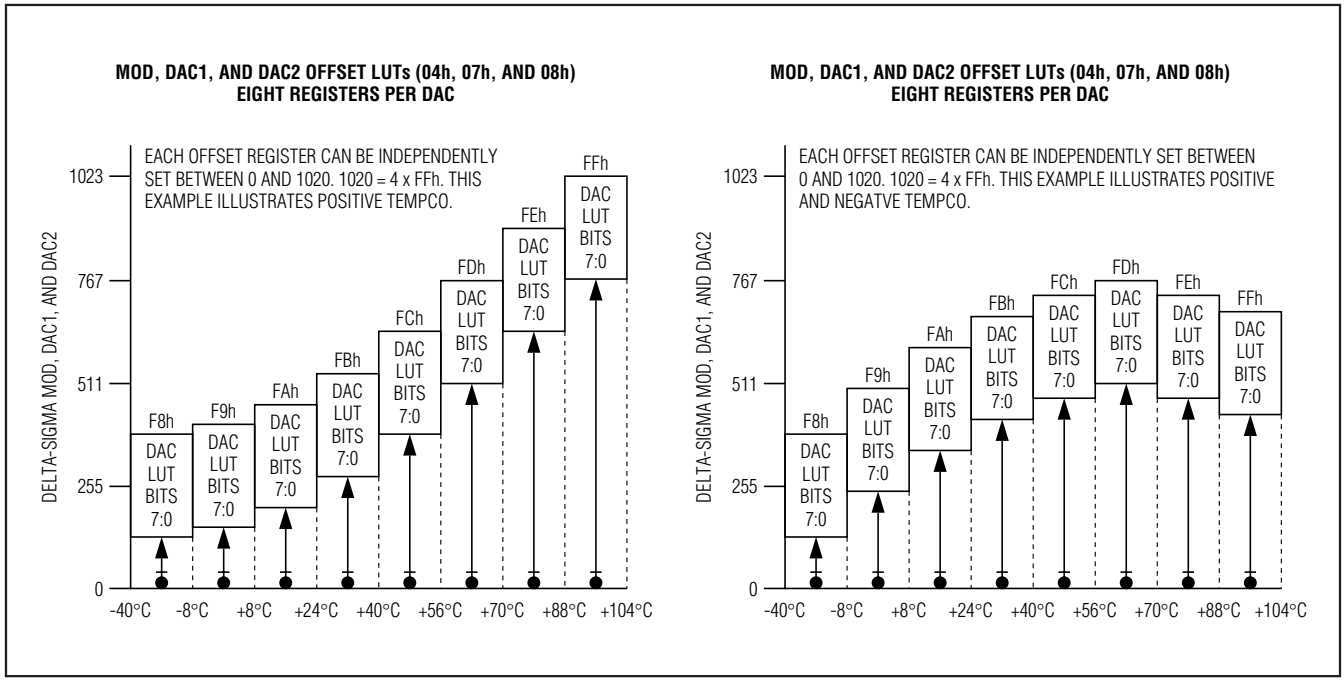


Figure 12. MOD, DAC1, and DAC2 Offset LUTs

Digital I/O Pins

Five digital input and five digital output pins are provided for monitoring and control.

LOS, LOSOUT

By default (LOSC = 1, Table 02h, Register 89h), the LOS pin is used to convert a standard comparator output for loss of signal (LOS) to an open-collector output. This means the mux shown in the *Block Diagram* by default selects the LOS pin as the source for the LOSOUT output transistor. The output of the mux can be read in the STATUS byte (Lower Memory, Register 6Eh) as the RXL bit. The RXL signal can be inverted (INV LOS = 1) before driving the open-drain output transistor using the XOR gate provided. Setting LOSC = 0 configures the mux to be controlled by LOS LO, which is driven by the output of the LOS quick trip (Table 02h, Registers BEh and BFh). The mux setting (stored in EEPROM) does not take effect until V_{CC} > POA, allowing the EEPROM to recall.

IN1, RSEL, OUT1, RSELOUT

The digital input IN1 and RSEL pins primarily serve to meet the rate-select requirements of SFP and SFP+. They also serve as general-purpose inputs. OUT1 and RSELOUT are driven by a combination of the IN1, RSEL, and logic dictated by control registers in the EEPROM (Figure 14). The levels of IN1 and RSEL can be read using the STATUS register (Lower Memory, Register 6Eh). The open-drain output OUT1 can be controlled and/or inverted using the CNFGB register (Table 02h, Register 8Ah). The open-drain RSELOUT output is software-controlled and/or inverted through the STATUS register and CNFGA register (Table 02h, Register 89h). External pullup resistors must be provided on OUT1 and RSELOUT to realize high logic levels.

SFP+ Controller with Analog LDD Interface

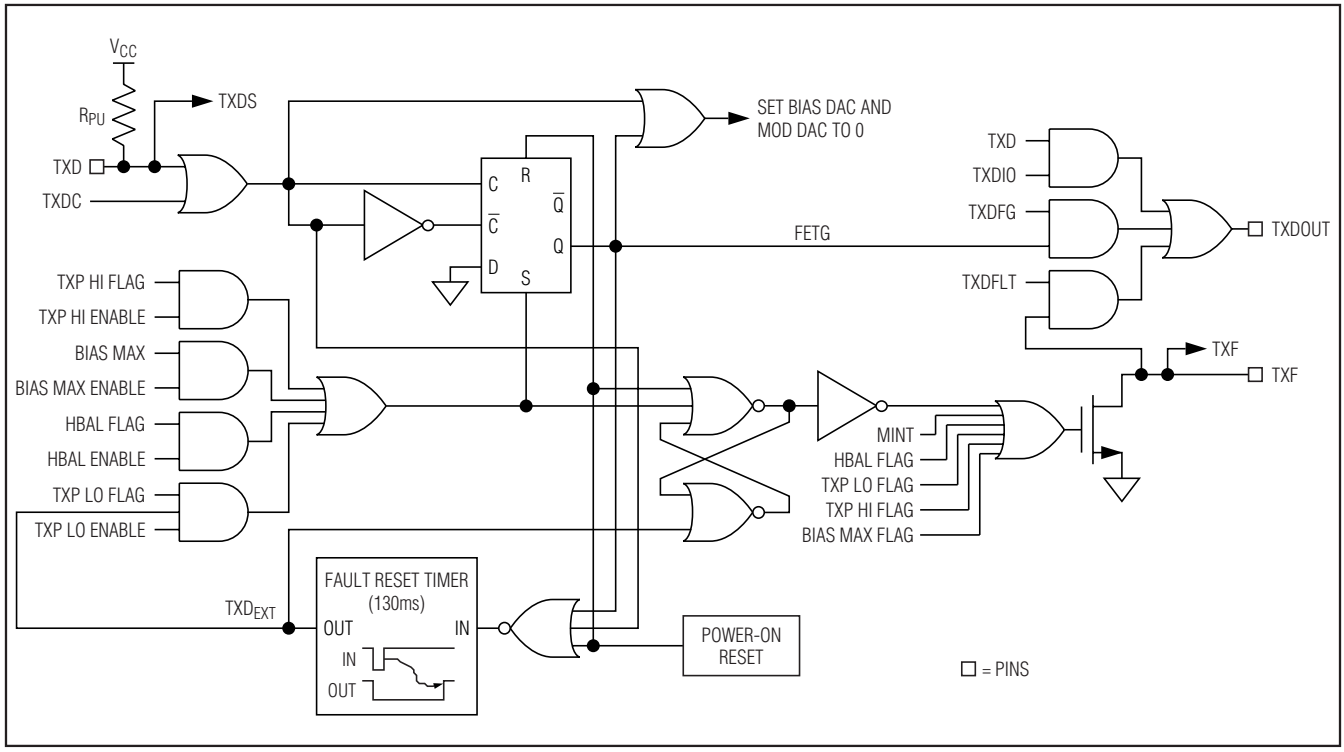


Figure 13. Logic Diagram 1

TXF, TXD, TXDOUT

TXDOUT is generated from a combination of TXF, TXD, and the internal signal FETG. A software control identical to TXD is available (TXDC, Lower Memory, Register 6Eh). A TXD pulse is internally extended (TXD_{EXT}) by time t_{INITR1} to inhibit the latching of low alarms and warnings related to the APC loop to allow for the loop to stabilize. The nonlatching alarms and warnings are TXP LO, LOS LO, and MON1–MON4 LO alarms and warnings. In addition, TXP LO is disabled from creating FETG. TXF is both an input and an output (Figure 13). See the *Transmit Fault (TXF) Output* section for a detailed explanation of TXF. Figure 13 shows that the same signals and faults can also be used to generate the internal signal FETG (Table 01h/05h, Registers FAh and FBh). FETG is used to send a fast "turn-off" command to the laser driver. The intended use is a direct connection to the laser driver's TXD input if this is desired. When V_{CC} < POA, TXDOUT is high impedance.

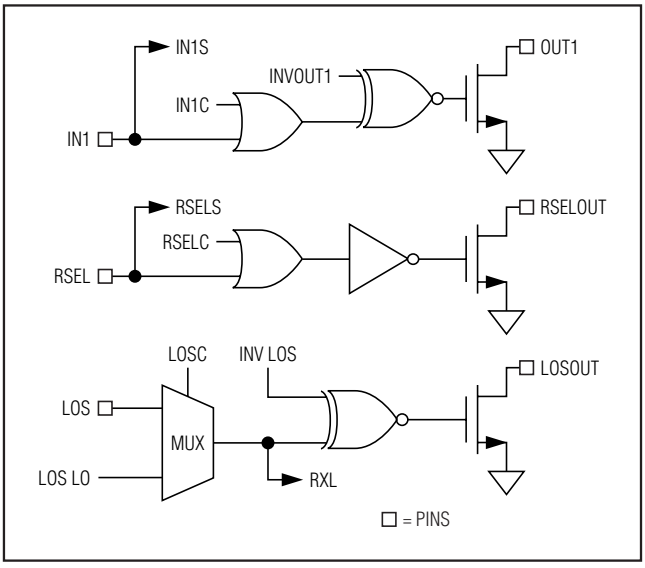


Figure 14. Logic Diagram 2

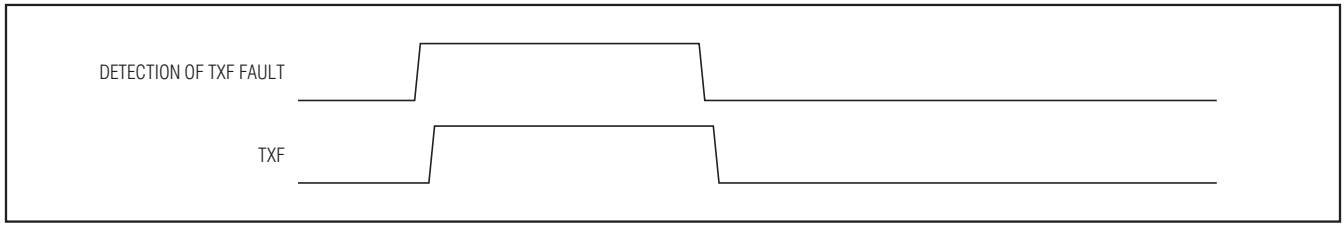


Figure 15a. TXF Nonlatched Operation

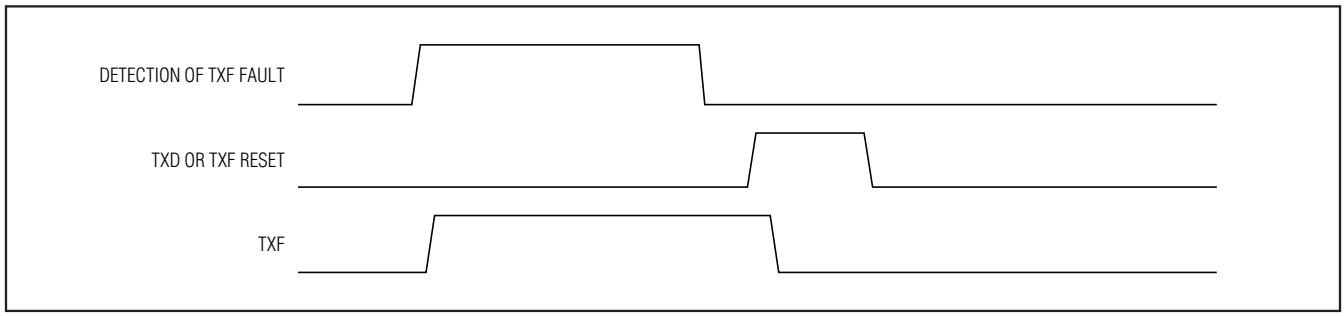


Figure 15b. TXF Latched Operation

Transmit Fault (TXF) Output

TXF can be triggered by all alarms, warnings, and quick trips (Figure 13). The six ADC alarms, warnings, and the LOS quick trips require enabling (Table 01h/05h, Registers F8h and FDh). See Figures 15a and 15b for nonlatched and latched operation. Latching of the alarms is controlled by the CNFGB and CNFGC registers (Table 02h, Registers 8Ah–8Bh).

Die Identification

The DS1873 has an ID hardcoded in its die. Two registers (Table 02h, Registers CEh–CFh) are assigned for this feature. The CEh register reads 73h to identify the part as the DS1873, while the CFh register reads the current device version.

I²C Communication

I²C Definitions

The following terminology is commonly used to describe I²C data transfers.

Master device: The master device controls the slave devices on the bus. The master device generates SCL clock pulses and START and STOP conditions.

Slave devices: Slave devices send and receive data at the master's request.

Bus idle or not busy: Time between STOP and START conditions when both SDA and SCL are inactive and in their logic-high states.

START condition: A START condition is generated by the master to initiate a new data transfer with a slave. Transitioning SDA from high to low while SCL remains high generates a START condition. See Figure 16 for applicable timing.

STOP condition: A STOP condition is generated by the master to end a data transfer with a slave. Transitioning SDA from low to high while SCL remains high generates a STOP condition. See Figure 16 for applicable timing.

Repeated START condition: The master can use a repeated START condition at the end of one data transfer to indicate that it will immediately initiate a new data transfer following the current one. Repeated STARTs are commonly used during read operations to identify a specific memory address to begin a data transfer. A repeated START condition is issued identically to a normal START condition. See Figure 16 for applicable timing.

Bit write: Transitions of SDA must occur during the low state of SCL. The data on SDA must remain valid and unchanged during the entire high pulse of SCL plus the setup and hold time requirements (Figure 16). Data is shifted into the device during the rising edge of the SCL.

Bit read: At the end a write operation, the master must release the SDA bus line for the proper amount of setup time (Figure 16) before the next rising edge of SCL during a bit read. The device shifts out each bit of data on SDA at the falling edge of the previous SCL pulse and the data bit is valid at the rising edge of the current SCL pulse. Remember that the master generates all SCL clock pulses, including when it is reading bits from the slave.

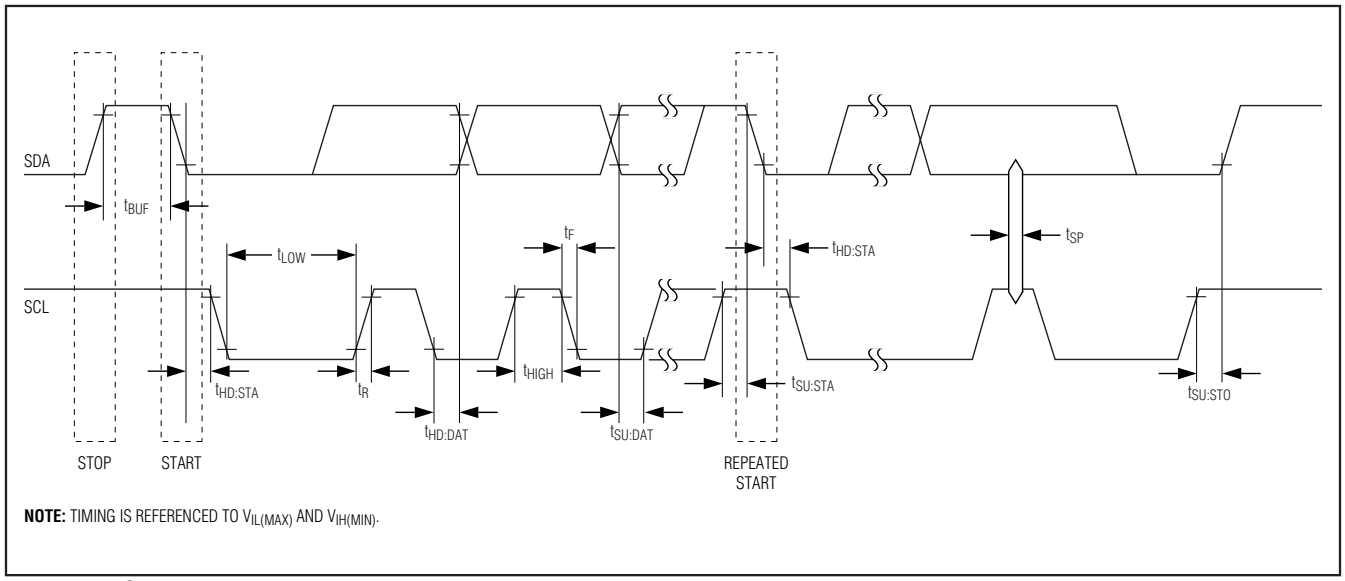
Acknowledgement (ACK and NACK): An acknowledgement (ACK) or not acknowledge (NACK) is always the ninth bit transmitted during a byte transfer. The device receiving data (the master during a read or the slave during a write operation) performs an ACK by transmitting a zero during the ninth bit. A device performs a NACK by transmitting a one during the 9th bit. Timing (Figure 16) for the ACK and NACK is identical to all other bit writes. An ACK is the acknowledgment that the device is properly receiving data. A NACK is used to terminate a read sequence or as an indication that the device is not receiving data.

Byte write: A byte write consists of 8 bits of information transferred from the master to the slave (most significant bit first) plus a 1-bit acknowledgement from the slave to the master. The 8 bits transmitted by the master are done according to the bit-write definition and the acknowledgement is read using the bit-read definition.

Byte read: A byte read is an 8-bit information transfer from the slave to the master plus a 1-bit ACK or NACK from the master to the slave. The 8 bits of information that are transferred (most significant bit first) from the slave to the master are read by the master using the bit-read definition, and the master transmits an ACK using the bit-write definition to receive additional data bytes. The master must NACK the last byte read to terminate communication so the slave returns control of SDA to the master.

Slave address byte: Each slave on the I²C bus responds to a slave address byte sent immediately following a START condition. The slave address byte contains the slave address in the most significant 7 bits and the R/$\overline{W}$ bit in the least significant bit.

The DS1873 responds to two slave addresses. The auxiliary memory always responds to a fixed I²C slave address, A0h. The Lower Memory and Tables 00h–08h respond to I²C slave addresses that can be configured to any value between 00h–FEh using the DEVICE ADDRESS byte (Table 02h, Register 8Ch). The user also must set the ASEL bit (Table 02h, Register 89h) for this address to be active. By writing the correct slave address with R/$\overline{W}$ = 0, the master indicates it will write data to the slave. If R/$\overline{W}$



NOTE: TIMING IS REFERENCED TO $V_{IL(MAX)}$ AND $V_{IH(MIN)}$.

Figure 16. I²C Timing

= 1, the master reads data from the slave. If an incorrect slave address is written, the DS1873 assumes the master is communicating with another I²C device and ignores the communications until the next START condition is sent. If the main device's slave address is programmed to be A0h, access to the auxiliary memory is disabled.

Memory address: During an I²C write operation to the DS1873, the master must transmit a memory address to identify the memory location where the slave is to store the data. The memory address is always the second byte transmitted during a write operation following the slave address byte.

I²C Protocol

Writing a single byte to a slave: The master must generate a START condition, write the slave address byte (R/$\overline{W}$ = 0), write the memory address, write the byte of data, and generate a STOP condition. Remember the master must read the slave's acknowledgement during all byte-write operations.

Writing multiple bytes to a slave: To write multiple bytes to a slave, the master generates a START condition, writes the slave address byte (R/$\overline{W}$ = 0), writes the memory address, writes up to 8 data bytes, and generates a STOP condition. The DS1873 writes 1 to 8 bytes (one page or row) with a single write transaction. This is internally controlled by an address counter that allows data to be written to consecutive addresses without transmitting a memory address before each data byte is sent. The address counter limits the write to one 8-byte page (one row of the memory map). Attempts to write to additional pages of memory without sending a STOP condition between pages results in the address counter wrapping around to the beginning of the present row.

For example, a 3-byte write starts at address 06h and writes three data bytes (11h, 22h, and 33h) to three "consecutive" addresses. The result is that addresses 06h and 07h would contain 11h and 22h, respectively, and the third data byte, 33h, would be written to address 00h.

To prevent address wrapping from occurring, the master must send a STOP condition at the end of the page, then wait for the bus-free or EEPROM write time to elapse. Then the master can generate a new START condition and write the slave address

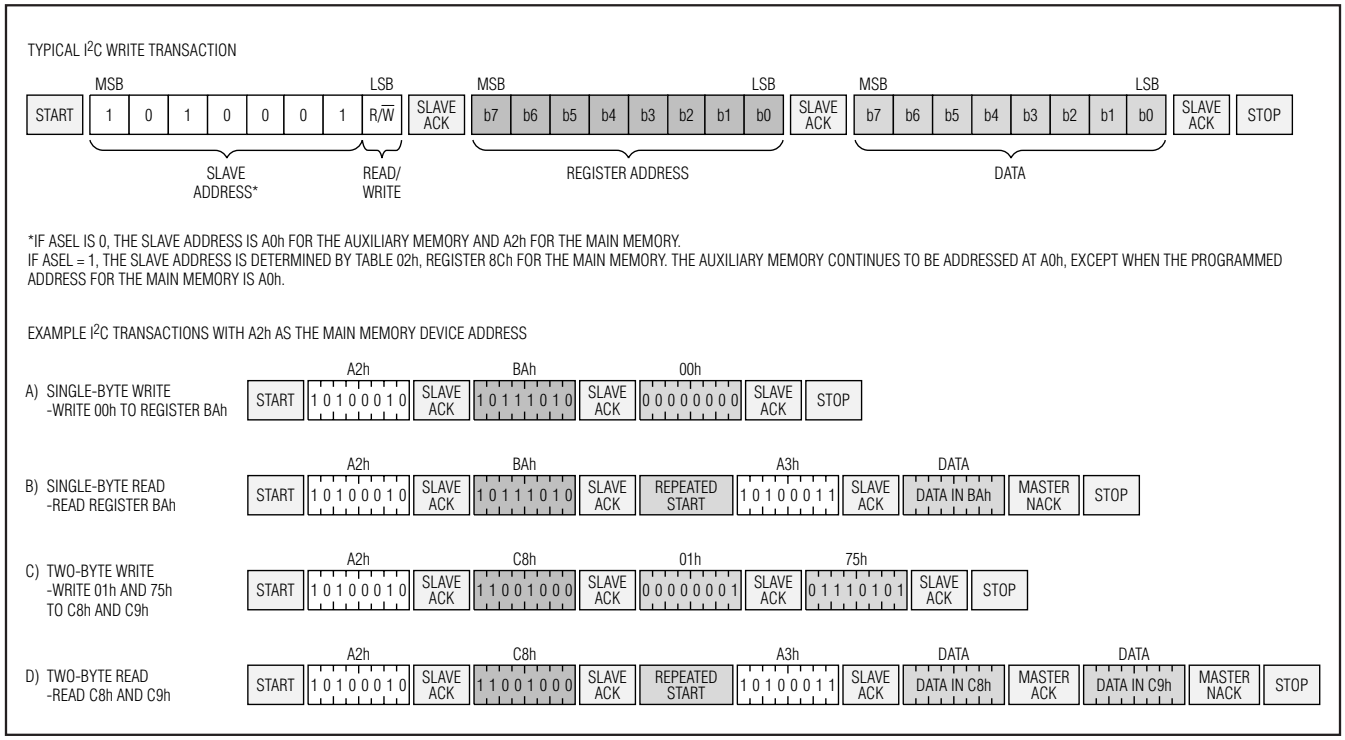


Figure 17. Example I²C Timing