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19-4691; Rev 0; 6/09

SFP+ Controller with Digital LDD Interface

DS1874

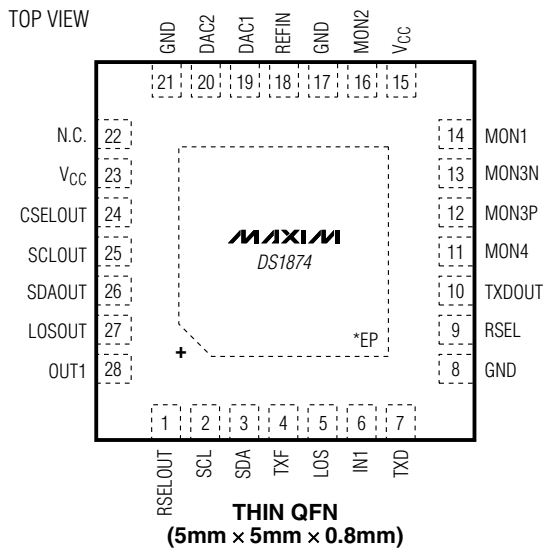
General Description

The DS1874 controls and monitors all functions for SFF, SFP, and SFP+ modules including all SFF-8472 functionality. The combination of the DS1874 with the MAX3798/MAX3799 laser driver/limiting amplifier provides APC loop, modulation current control, and eye safety functionality. The DS1874 continuously monitors for high output current, high bias current, and low and high transmit power to ensure that laser shutdown for eye safety requirements are met without adding external components. Six ADC channels monitor V_{CC}, temperature, and four external monitor inputs (MON1–MON4) that can be used to meet all monitoring requirements. MON3 is differential with support for common mode to V_{CC}. Two digital-to-analog (DAC) outputs with temperature-indexed lookup tables (LUTs) are available for additional monitoring and control functionality.

Applications

SFF, SFP, and SFP+ Transceiver Modules

Pin Configuration



THIN QFN
(5mm × 5mm × 0.8mm)

*EXPOSED PAD.

Features

- **Meets All SFF-8472 Control and Monitoring Requirements**
- **Laser Bias Controlled by APC Loop and Temperature LUT to Compensate for Tracking Error**
- **Laser Modulation Controlled by Temperature LUT**
- **Six Analog Monitor Channels: Temperature, V_{CC}, MON1–MON4**
  - **MON1–MON4 Support Internal and External Calibration**
  - **Scalable Dynamic Range**
  - **Internal Direct-to-Digital Temperature Sensor**
  - **Alarm and Warning Flags for All Monitored Channels**
- **Two 9-Bit Delta-Sigma Outputs with 36 Entry Temperature LUTs**
- **Digital I/O Pins: Five Inputs, Five Outputs**
- **Comprehensive Fault-Measurement System with Maskable Laser Shutdown Capability**
- **Flexible, Two-Level Password Scheme Provides Three Levels of Security**
- **256 Additional Bytes Located at A0h Slave Address**
- **I^2C-Compatible Interface**
- **3-Wire Master to Communicate with the MAX3798/MAX3799 Laser Driver/Limiting Amplifier**
- **+2.85V to +3.9V Operating Voltage Range**
- **-40°C to +95°C Operating Temperature Range**
- **28-Pin TQFN (5mm x 5mm) Package**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
DS1874T+	-40°C to +95°C	28 TQFN-EP*
DS1874T+T&R	-40°C to +95°C	28 TQFN-EP*

+Denotes a lead(Pb)-free/RoHS-compliant package.
T&R = Tape and reel.
**EP = Exposed pad.*

SFP+ Controller with Digital LDD Interface

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SFP+ Controller with Digital LDD Interface

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ABSOLUTE MAXIMUM RATINGS

Voltage Range on MON1–MON4, RSEL, IN1, LOS, TXF, and TXD Pins Relative to Ground .....-0.5V to (V_{CC} + 0.5V)*
Voltage Range on V_{CC}, SDA, SCL, OUT1, RSELOUT, and LOSOUT Pins Relative to Ground.....-0.5V to +6V

Operating Temperature Range .....-40°C to +95°C
Programming Temperature Range .....0°C to +95°C
Storage Temperature Range .....-55°C to +125°C
Soldering Temperature.....Refer to the IPC/JEDEC J-STD-020 Specification.

**Subject to not exceeding +6V.*

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

(T_A = -40°C to +95°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Main Supply Voltage	V_{CC}	(Note 1)	+2.85		+3.9	V
High-Level Input Voltage (SDA, SCL, SDAOUT)	$V_{IH:1}$		0.7 x V_{CC}		V_{CC} + 0.3	V
Low-Level Input Voltage (SDA, SCL, SDAOUT)	$V_{IL:1}$		-0.3		0.3 x V_{CC}	V
High-Level Input Voltage (TXD, TXF, RSEL, IN1, LOS)	$V_{IH:2}$		2.0		V_{CC} + 0.3	V
Low-Level Input Voltage (TXD, TXF, RSEL, IN1, LOS)	$V_{IL:2}$		-0.3		+0.8	V

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = +2.85V to +3.9V, T_A = -40°C to +95°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current	I_{CC}	(Notes 1, 2)		2.5	10	mA
Output Leakage (SDA, SDAOUT, OUT1, RSELOUT, LOSOUT, TXF)	I_{LO}				1	µA
Low-Level Output Voltage (SDA, SDAOUT, SCLOUT, CSELOUT, OUT1, RSELOUT, LOSOUT, TXDOUT, DAC1, DAC2, TXF)	V_{OL}	I_{OL} = 4mA			0.4	V
		I_{OL} = 6mA			0.6	
High-Level Output Voltage (DAC1, DAC2, SCLOUT, SDAOUT, CSELOUT, TXDOUT)	V_{OH}	I_{OH} = 4mA	V_{CC} - 0.4			V
TXDOUT Before EEPROM Recall				10	100	nA
DAC1 and DAC2 Before LUT Recall		Figure 11		10	100	nA
Input Leakage Current (SCL, TXD, LOS, RSEL, IN1)	I_{LI}				1	µA
Digital Power-On Reset	POD		1.0		2.2	V
Analog Power-On Reset	POA		2.0		2.75	V

DAC1, DAC2 ELECTRICAL CHARACTERISTICS

(V_{CC} = +2.85V to +3.9V, T_A = -40°C to +95°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Main Oscillator Frequency	f_{OSC}			5		MHz
Delta-Sigma Input-Clock Frequency	f_{DS}			$f_{OSC}/2$		MHz
Reference Voltage Input (REFIN)	V_{REFIN}	Minimum 0.1µF to GND	2		V_{CC}	V
Output Range			0		V_{REFIN}	V
Output Resolution		See the *Delta-Sigma Outputs (DAC1 and DAC2)* section for details.			9	Bits
Output Impedance	R_{DS}			35	100	Ω

ANALOG QUICK-TRIP CHARACTERISTICS

(V_{CC} = +2.85V to +3.9V, T_A = -40°C to +95°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
MON2, TXP HI, TXP LO Full-Scale Voltage	V_{APC}			2.5		V
HBIAS, LOS Full-Scale Voltage				1.25		V
MON2 Input Resistance			35	50	65	kΩ
Resolution				8		Bits
Error		T_A = +25°C		±2		%FS
Integral Nonlinearity			-1		+1	LSB
Differential Nonlinearity			-1		+1	LSB
Temperature Drift			-2.5		+2.5	%FS
LOS Offset				-5		mV

ANALOG VOLTAGE MONITORING CHARACTERISTICS

(V_{CC} = +2.85V to +3.9V, T_A = -40°C to +95°C, unless otherwise noted.)

PARAMETER		SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ADC Resolution					13		Bits
Input/Supply Accuracy (MON1–MON4, V_{CC})		ACC	At factory setting		0.25	0.50	%FS
Update Rate for Temperature, MON1–MON4, and V_{CC}		t_{RR}			64	75	ms
Input/Supply Offset (MON1–MON4, V_{CC})		V_{OS}	(Note 3)		0	5	LSB
Factory Setting	MON1–MON4		(Note 4)		2.5		V
	V_{CC}				6.5536		
	MON3 Fine				312.5		µV

DIGITAL THERMOMETER CHARACTERISTICS

(V_{CC} = +2.85V to +3.9V, T_A = -40°C to +95°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Thermometer Error	T_{ERR}	-40°C to +95°C	-3		+3	°C

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = +2.85V to +3.9V, T_A = -40°C to +95°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
TXD Enable	t_{OFF}	From ↑ TXD (Notes 5, 6)			5	µs
Recovery from TXD Disable (Figure 14)	t_{ON}	From ↓ TXD (Notes 5, 7)			1	ms
Recovery After Power-Up	t_{INIT_DAC}	From ↑ V_{CC} > VCC LO alarm (Notes 5, 8)		20		ms
Fault Reset Time (to TXF = 0)	t_{INITR1}	From ↓ TXD		131		ms
	t_{INITR2}	From ↑ V_{CC} > VCC LO alarm (Note 8)		161		
Fault Assert Time (to TXF = 1)	t_{FAULT}	After HTXP, LTXP, HBATH, IBIASMAX (Note 9)	6.4		55	µs
LOSOUT Assert Time	t_{LOSS_ON}	LLOS (Notes 9, 10)	6.4		55	µs
LOSOUT Deassert Time	t_{LOSS_OFF}	HLOS (Notes 9, 11)	6.4		55	µs

TIMING CHARACTERISTICS (CONTROL LOOP AND QUICK TRIP)

(V_{CC} = +2.85V to +3.9V, T_A = -40°C to +95°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output-Enable Time Following POA	t_{INIT}	(Note 8)		20		ms
Binary Search Time	t_{SEARCH}	(Note 12)	8		10	BIAS Samples

3-WIRE DIGITAL INTERFACE SPECIFICATION

(V_{CC} = +2.85V to +3.9V, T_A = -40°C to +95°C, timing referenced to $V_{IL(MAX)}$ and $V_{IH(MIN)}$, unless otherwise noted. See Figure 15.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SCLOUT Clock Frequency	f_{SCLOUT}	(Note 13)		833		kHz
SCLOUT Duty Cycle	t_{3WDC}			50		%
SDAOUT Setup Time	t_{DS}		100			ns
SDAOUT Hold Time	t_{DH}		100			ns
CSELOUT Pulse-Width Low	t_{CSW}		500			ns
CSELOUT Leading Time Before the First SCLOUT Edge	t_L		500			ns
CSELOUT Trailing Time After the Last SCLOUT Edge	t_T	(Note 14)	500			ns
SDAOUT, SCLOUT Load	C_{B3W}	Total bus capacitance on one line (Note 14)			10	pF

I²C AC ELECTRICAL CHARACTERISTICS

(V_{CC} = +2.85V to +3.9V, T_A = -40°C to +95°C, timing referenced to $V_{IL(MAX)}$ and $V_{IH(MIN)}$, unless otherwise noted. See Figure 17.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SCL Clock Frequency	f_{SCL}	(Note 13)	0		400	kHz
Clock Pulse-Width Low	t_{LOW}		1.3			µs
Clock Pulse-Width High	t_{HIGH}		0.6			µs
Bus-Free Time Between STOP and START Condition	t_{BUF}		1.3			µs
START Hold Time	$t_{HD:STA}$		0.6			µs
START Setup Time	$t_{SU:STA}$		0.6			µs
Data Out Hold Time	$t_{HD:DAT}$		0		0.9	µs
Data In Setup Time	$t_{SU:DAT}$		100			ns
Rise Time of Both SDA and SCL Signals	t_R	(Note 14)	20 + 0.1C_B		300	ns
Fall Time of Both SDA and SCL Signals	t_F	(Note 14)	20 + 0.1C_B		300	ns
STOP Setup Time	$t_{SU:STO}$		0.6			µs
EEPROM Write Time	t_W	(Note 15)			20	ms
Capacitive Load for Each Bus Line	C_B				400	pF

NONVOLATILE MEMORY CHARACTERISTICS

(V_{CC} = +2.85V to +3.9V, unless otherwise noted.)

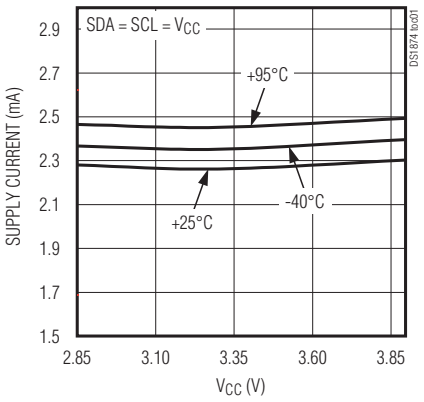
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
EEPROM Write Cycles		At +25°C	200,000			
		At +85°C	50,000			

Note 1: All voltages are referenced to ground. Current into the IC is positive, and current out of the IC is negative.
Note 2: Inputs are at supply rail. Outputs are not loaded.
Note 3: This parameter is guaranteed by design.
Note 4: Full-scale is user programmable.
Note 5: The DACs are the bias and modulation DACs found in the MAX3798/MAX3799 that are controlled by the DS1874.
Note 6: The DS1874 is configured with TXDOUT connected to the MAX3798/MAX3799 DISABLE input.
Note 7: This includes writing to the modulation DAC and the initial step written to the bias DAC.
Note 8: A temperature conversion is completed and the modulation register value is recalled from the LUT and V_{CC} has been measured to be above V_{CC} LO alarm.
Note 9: The timing is determined by the choice of the update rate setting (see Table 02h, Register 88h).
Note 10: This specification is the time it takes from MON3 voltage falling below the LLOS trip threshold to LOSOUT asserted high.
Note 11: This specification is the time it takes from MON3 voltage rising above the HLOS trip threshold to LOSOUT asserted low.
Note 12: Assuming an appropriate initial step is programmed that would cause the power to exceed the APC set point within four steps, the bias current will be within 3% within the time specified by the binary search time. See the *BIAS and MODULATION Control During Power-Up* section.
Note 13: I²C interface timing shown is for fast mode (400kHz). This device is also backward compatible with I²C standard mode timing.
Note 14: C_B—the total capacitance of one bus line in pF.
Note 15: EEPROM write begins after a STOP condition occurs.

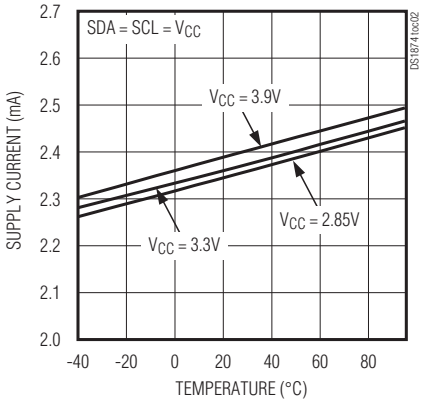
Typical Operating Characteristics

(V_{CC} = +2.85V to +3.9V, T_A = +25°C, unless otherwise noted.)

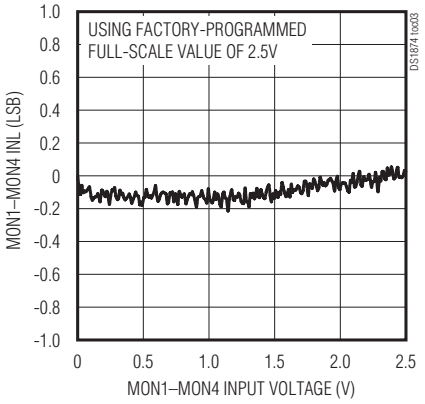
SUPPLY CURRENT vs. SUPPLY VOLTAGE



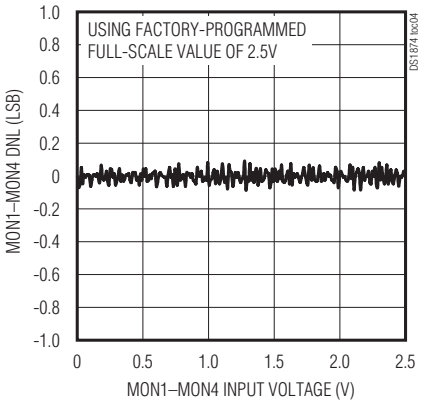
SUPPLY CURRENT vs. TEMPERATURE



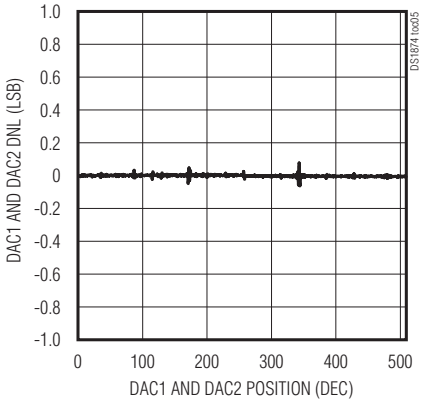
MON1–MON4 INL



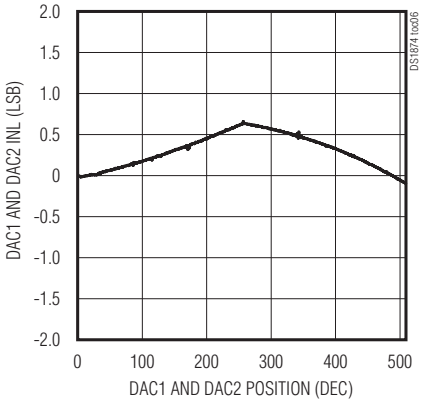
MON1–MON4 DNL



DAC1 AND DAC2 DNL



DAC1 AND DAC2 INL

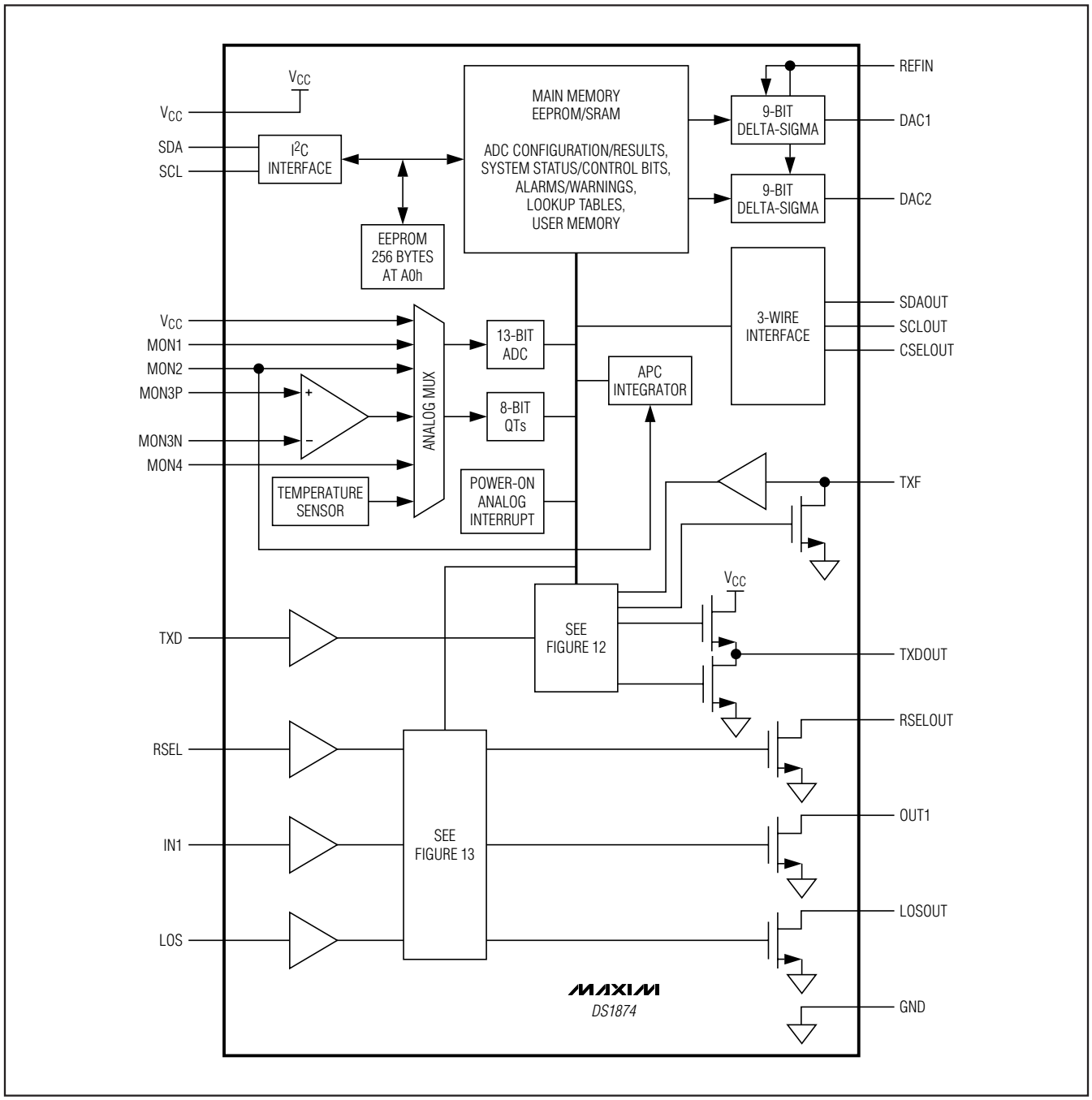


SFP+ Controller with Digital LDD Interface

Pin Description

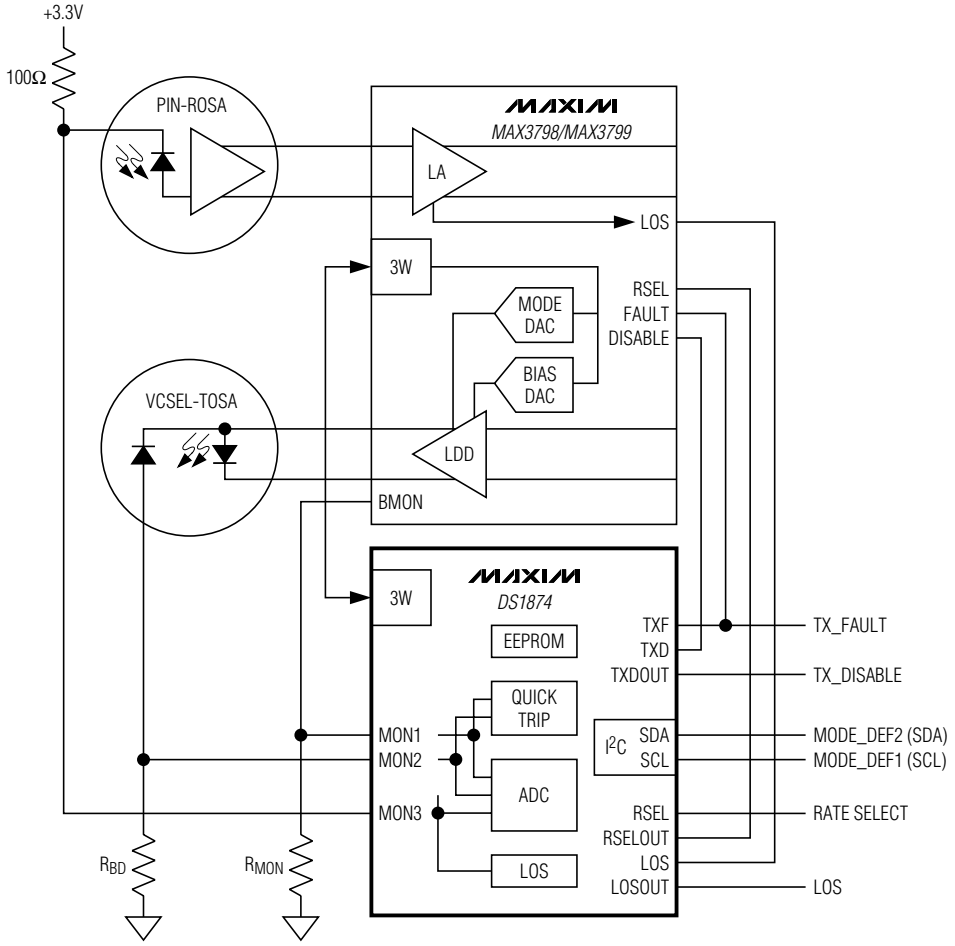
PIN	NAME	FUNCTION
1	RSELOUT	Rate-Select Output
2	SCL	I^2C Serial-Clock Input
3	SDA	I^2C Serial-Data Input/Output
4	TXF	Transmit-Fault Input and Output. The output is open drain.
5	LOS	Loss-of-Signal Input
6	IN1	Digital Input. General-purpose input with AS1 in SFF-8079 or RS1 in SFF-8431.
7	TXD	Transmit-Disable Input
8, 17, 21	GND	Ground Connection
9	RSEL	Rate-Select Input
10	TXDOUT	Transmit-Disable Output
11	MON4	External Monitor Input 4
12, 13	MON3P, MON3N	Differential External Monitor Input 3 and LOS Quick Trip
14	MON1	External Monitor Input 1 and HBATH Quick Trip
15, 23	V_{CC}	Power-Supply Input
16	MON2	External Monitor Input 2. Feedback voltage for APC loop and HTXP/LTXP quick trip.
18	REFIN	Reference Input for DAC1 and DAC2
19, 20	DAC1, DAC2	Delta-Sigma Output 1/2
22	N.C.	No Connection
24	CSELOUT	Chip-Select Output. Part of the 3-wire interface to the MAX3798/MAX3799 laser driver/limiting amplifier.
25	SCLOUT	Serial-Clock Output. Part of the 3-wire interface to the MAX3798/MAX3799 laser driver/limiting amplifier.
26	SDAOUT	Serial-Data Input/Output. Part of the 3-wire interface to the MAX3798/MAX3799 laser driver/limiting amplifier.
27	LOSOUT	Open-Drain Receive Loss-of-Signal Output
28	OUT1	Digital Output. General-purpose output with AS1 output in SFF-8079 or RS1 output in SFF-8431.
—	EP	Exposed Pad

Block Diagram



SFP+ Controller with Digital LDD Interface

Typical Operating Circuit



Detailed Description

The DS1874 integrates the control and monitoring functionality required to implement a VCSEL-based SFP or SFP+ system using Maxim's MAX3798/MAX3799 combined limiting amplifier and laser driver. Key components of the DS1874 are shown in the *Block Diagram* and described in subsequent sections.

MAX3798/MAX3799 DAC Control

The DS1874 controls two 9-bit DACs inside the MAX3798/MAX3799. One DAC is used for laser bias control while the other is used for laser modulation control. The DS1874 communicates with the MAX3798/MAX3799 over a 3-wire digital interface (see the *3-Wire Master for Controlling the MAX3798/MAX3799* section). The communication between the DS1874 and MAX3798/MAX3799 is transparent to the end user.

BIAS Register/APC Control

The MAX3798/MAX3799 control their laser bias current DAC using the APC loop within the DS1874. The APC loop's feedback to the DS1874 is the monitor diode (MON2) current, which is converted to a voltage using

Table 1. Acronyms

ACRONYM	DEFINITION
ADC	Analog-to-Digital Converter
AGC	Automatic Gain Control
APC	Automatic Power Control
APD	Avalanche Photodiode
ATB	Alarm Trap Bytes
BM	Burst Mode
DAC	Digital-to-Analog Converter
LOS	Loss of Signal
LUT	Lookup Table
NV	Nonvolatile
QT	Quick Trip
TE	Tracking Error
TIA	Transimpedance Amplifier
ROSA	Receiver Optical Subassembly
SEE	Shadowed EEPROM
SFF	Small Form Factor
SFF-8472	Document Defining Register Map of SFPs and SFFs
SFP	Small Form Factor Pluggable
SFP+	Enhanced SFP
TOSA	Transmit Optical Subassembly
TXP	Transmit Power

an external resistor. The feedback is sampled by a comparator and compared to a digital set-point value. The output of the comparator has three states: up, down, or no-operation. The no-operation state prevents the output from excessive toggling once steady state is reached. As long as the comparator output is in either the up or down states, the bias is adjusted by writing increment and decrement values to the MAX3798/MAX3799 through the BIASINC register (3-wire address 13h).

The DS1874 has an LUT to allow the APC set point to change as a function of temperature to compensate for tracking error (TE). The TE LUT has 36 entries that determine the APC setting in 4°C windows between -40°C to +100°C.

MODULATION Control

The MAX3798/MAX3799 control the laser modulation using the internal temperature-indexed LUT within the DS1874. The modulation LUT is programmed in 2°C increments over the -40°C to +102°C range to provide temperature compensation for the laser's modulation. The modulation is updated after each temperature conversion using the 3-wire interface that connects to the MAX3798/MAX3799. The MAX3798/MAX3799 include a 9-bit DAC. The modulation LUT is 8 bits.

Figure 1 demonstrates how the 8-bit LUT controls the 9-bit DAC with the use of a temperature control bit (MODTC, Table 02h, Register C6h) and a temperature index register (MODTI, Table 02h, Register C2h).

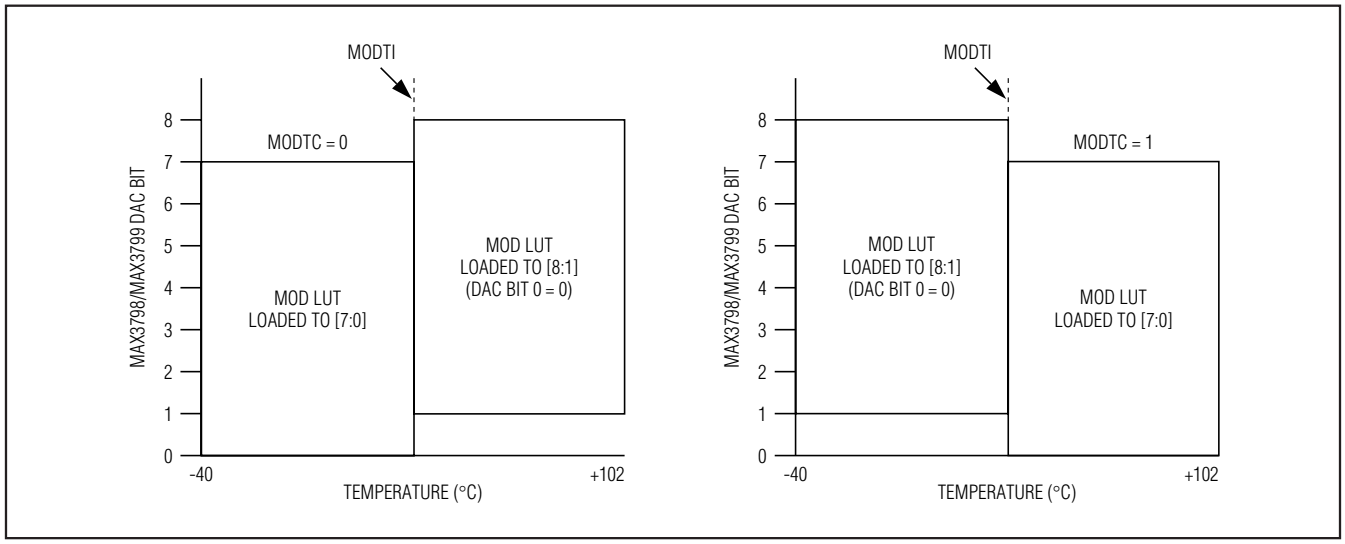


Figure 1. Modulation LUT Loading to MAX3798/MAX3799 MOD DAC

BIAS and MODULATION Control During Power-Up

The DS1874 has two internal registers, MODULATION and BIAS, that represent the values written to the MAX3798/MAX3799's modulation DAC and bias DAC through the 3-wire interface. On power-up, the DS1874 sets the MODULATION and BIAS registers to 0. When V_{CC} is above POA, the DS1874 initializes the MAX3798/MAX3799. After a temperature conversion is completed and if the VCC LO alarm is enabled, an additional V_{CC} conversion above the customer-defined VCC LO alarm level is required before the MAX3798/MAX3799 MODULATION register is updated with the value determined by the temperature conversion and the modulation LUT.

When the MODULATION register is set, the BIAS register is set to a value equal to ISTEP (see Figure 2). The startup algorithm checks if this bias current causes a feedback voltage above the APC set point, and if not, it continues increasing the BIAS register by ISTEP until the APC set point is exceeded. When the APC set point is exceeded, the device begins a binary search to quickly reach the bias current corresponding to the proper power level. After the binary search is completed, the APC integrator is enabled and single LSB steps are used to tightly control the average power.

The TXP HI, TXP LO, HBAL, and BIAS MAX QT alarms are masked until the binary search is completed. However, the BIAS MAX alarm is monitored during this time to prevent the BIAS register from exceeding IBIASMAX. During the bias current initialization, the BIAS register is not allowed to exceed IBIASMAX. If this occurs during the ISTEP sequence, then the binary search routine is enabled. If IBIASMAX is exceeded during the binary search, the next smaller step is activated. ISTEP or binary increments that would cause the BIAS register to exceed IBIASMAX are not taken. Masking the alarms until the completion of the binary search prevents false positive alarms during startup.

ISTEP is programmed by the customer using Table 02h, Register BBh. During the first steps, the MAX3798/MAX3799's bias DAC is directly written using SET_IBIAS (3-wire address 09h). ISTEP should be programmed to the maximum safe increase that is allowable during startup. If this value is programmed too low, the DS1874 still operates, but it could take significantly longer for the algorithm to converge and hence to control the average power.

If a fault is detected, and TXD is toggled to reenable the outputs, the DS1874 powers up following a similar sequence to an initial power-up. The only difference is that the DS1874 already has determined the present temperature, so the t_{INIT} time is not required for the DS1874 to recall the APC and MOD set points from EEPROM.

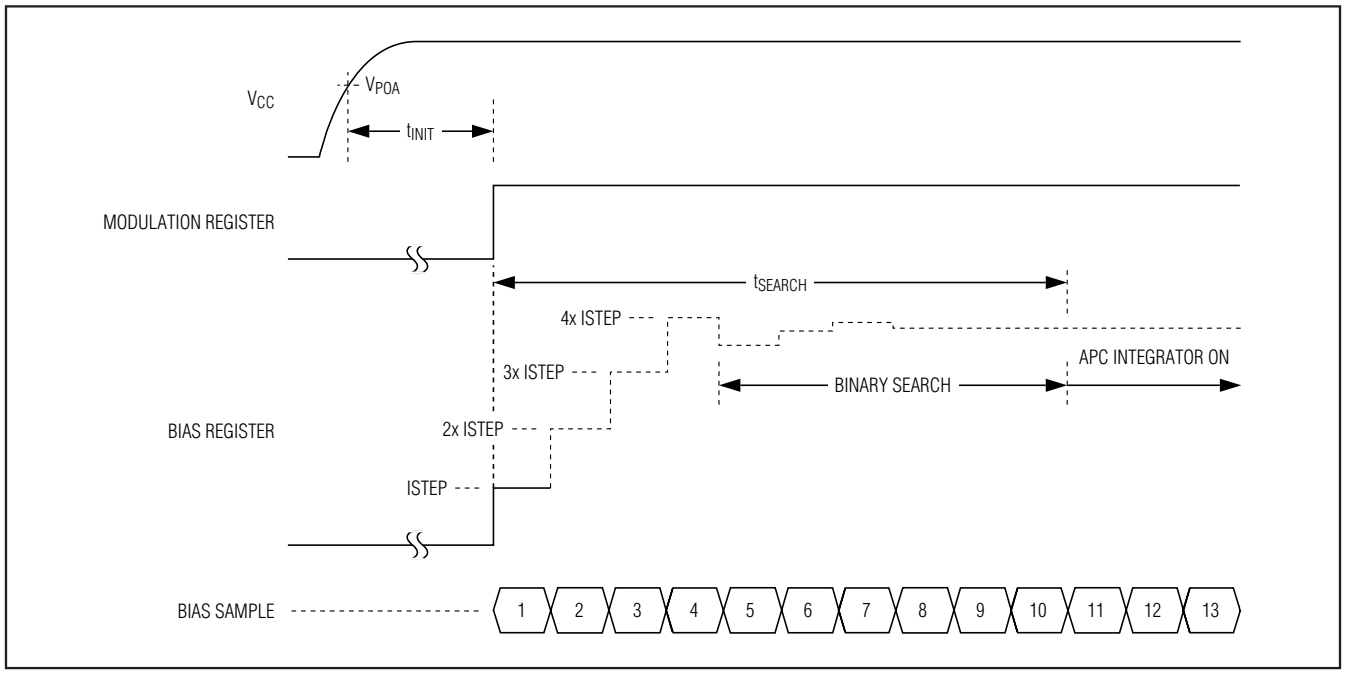


Figure 2. Power-Up Timing

BIAS and MODULATION Registers as a Function of Transmit Disable (TXD)

If TXD is asserted (logic 1) during normal operation, the outputs are disabled within t_{OFF}. When TXD is deasserted (logic 0), the DS1874 sets the MODULATION register with the value associated with the present temperature, and initializes the BIAS register using the same search algorithm as done at startup. When asserted, soft TXD (TXDC) (Lower Memory, Register 6Eh) would allow a software control identical to the TXD pin (see Figure 3).

APC and Quick-Trip Timing

As shown in Figure 4, the DS1874's input comparator is shared between the APC control loop and the quick-trip alarms (TXP HI, TXP LO, LOS, and BIAS HI). The comparator polls the alarms in a multiplexed sequence. Five of every eight comparator readings are used for APC loop bias-current control. The other three updates are used to check the HTXP/LTXP (monitor diode voltage), the HBATH (MON1), and LOS (MON3) signals against the internal APC, BIAS, and MON3 reference, respectively. If the last APC comparison was higher than the APC set point, it makes an HTXP comparison, and if it is lower, it makes an LTXP comparison. Depending on the results of the comparison, the corresponding alarms and warnings (TXP HI, TXP LO) are asserted or deasserted.

The DS1874 has a programmable comparator sample time based on an internally generated clock to facilitate a wide variety of external filtering options and time delays resulting from writing values to the MAX3798/MAX3799's bias DAC. The UPDATE RATE register (Table 02h, Register 88h) determines the sampling time. Samples occur at a regular interval, t_{REP}. Table 2 shows the sample rate options available. Any quick-trip alarm that is detected by default remains active until a subsequent comparator sample shows the condition no longer exists. A second bias current monitor (BIAS MAX) compares the MAX3798/MAX3799's BIAS DAC's code to a digital value stored in the IBIASMAX register. This comparison is made at every bias current update to ensure that a high-bias current is quickly detected.

An APC sample that requires an update of the BIAS register causes subsequent APC samples to be

Table 2. Update Rate Timing

APC_SR[2:0]	SAMPLE PERIOD (t_{REP}) (ns)
000b	800
001b	1200
010b	1600
011b	2000
100b	2800
101b	3200
110b	4400
111b	6400

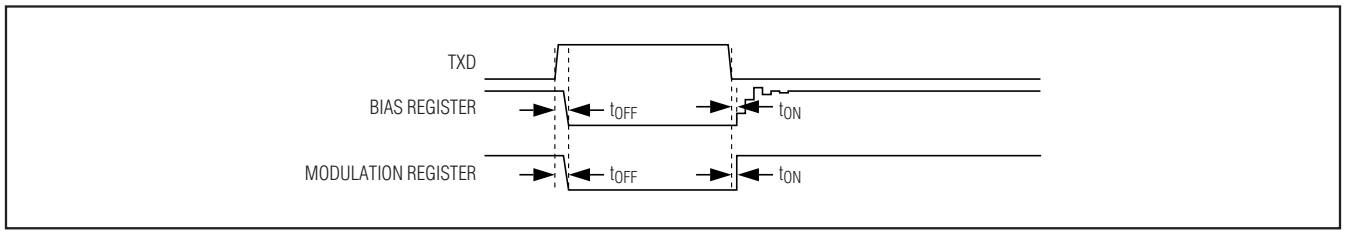


Figure 3. TXD Timing

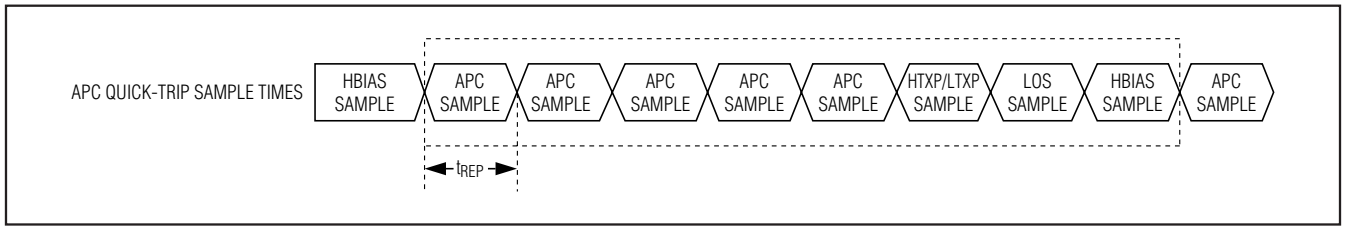


Figure 4. APC Loop and Quick-Trip Sample Timing

ignored until the end of the 3-wire communication that updates the MAX3798/MAX3799's BIAS DAC, plus an additional 16 sample periods (t_{REP}).

Monitors and Fault Detection

Monitors

Monitoring functions on the DS1874 include five quick-trip comparators and six ADC channels. This monitoring combined with the alarm enables (Table 01h/05h) determines when/if the DS1874 turns off the MAX3798/MAX3799 DACs and triggers the TXF and TXDOUT outputs. All the monitoring levels and interrupt masks are user programmable.

Five Quick-Trip Monitors and Alarms

Five quick-trip monitors are provided to detect potential laser safety issues and LOS status. These monitor the following:

1) High Bias Current (HBATH)
2) Low Transmit Power (LTXP)
3) High Transmit Power (HTXP)
4) Max Output Current (IBIASMAX)
5) Loss-of-Signal (LOS LO)

The high-transmit and low-transmit power quick-trip registers (HTXP and LTXP) set the thresholds used to compare against the MON2 voltage to determine if the transmit power is within specification. The HBATH quick trip compares the MON1 input (generally from the MAX3798/MAX3799 bias monitor output) against its threshold setting to determine if the present bias current is above specification. The BIAS MAX quick trip determines if the BIAS register is above specification. The BIAS register is not allowed to exceed the value set in the IBIASMAX register. When the DS1874 detects that the bias is at the limit it sets the BIAS MAX status bit and holds the BIAS register setting at the IBIASMAX level. The bias and power quick trips are routed to the TXF through interrupt masks to allow combinations of these alarms to be used to trigger these outputs. The user can program up to eight different temperature-indexed threshold levels for MON1 (Table 02h, Registers D0h–D7h). The LOS LO quick trip compares the MON3 input against its threshold setting to determine if the present received power is below the specification. The LOS LO quick trip can be used to set the LOSOUT pin. These alarms can be latched using Table 02h, Register 8Ah.

Six ADC Monitors and Alarms

The ADC monitors six channels that measure temperature (internal temp sensor), V_{CC}, and MON1–MON4 using an analog multiplexer to measure them round robin with a single ADC (see the *ADC Timing* section). The five voltage channels have a customer-programmable full-scale range and all channels have a customer-programmable offset value that is factory programmed to default value (see Table 3). Additionally, MON1–MON4 can right-shift results by up to 7 bits before the results are compared to alarm thresholds or read over the I^2C bus. This allows customers with specified ADC ranges to calibrate the ADC full scale to a factor of $1/2^n$ of their specified range to measure small signals. The DS1874 can then right-shift the results by n bits to maintain the bit weight of their specification (see the *Right-Shifting ADC Result* and *Enhanced RSSI Monitoring (Dual-Range Functionality)* sections).

Table 3. ADC Default Monitor Full-Scale Ranges

SIGNAL	+FS SIGNAL	+FS hex	-FS SIGNAL	-FS hex
Temperature (°C)	127.996	7FFF	-128	8000
V_{CC} (V)	6.5528	FFF8	0	0000
MON1–MON4 (V)	2.4997	FFF8	0	0000

The ADC results (after right-shifting, if used) are compared to the alarm and warning thresholds after each conversion, and the corresponding alarms are set, which can be used to trigger the TXF output. These ADC thresholds are user programmable, as are the masking registers that can be used to prevent the alarms from triggering the TXF output.

ADC Timing

There are six analog channels that are digitized in a round-robin fashion in the order shown in Figure 5. The total time required to convert all six channels is t_{RR} (see the *Analog Voltage Monitoring Characteristics* for details).

Right-Shifting ADC Result

If the weighting of the ADC digital reading must conform to a predetermined full-scale (PFS) value defined by a standard's specification (e.g., SFF-8472), then right-shifting can be used to adjust the PFS analog measurement range while maintaining the weighting of the ADC results. The DS1874's range is wide enough to cover all requirements; when the maximum input value is ≤ 1/2 of the FS value, right-shifting can be used to obtain greater accuracy. For instance, the maximum voltage might be 1/8 the specified PFS value, so only 1/8 the converter's range is effective over this range. An alternative is to calibrate the ADC's full-scale range to 1/8 the readable PFS value and use a right-shift value of 3. With this implementation, the resolution of

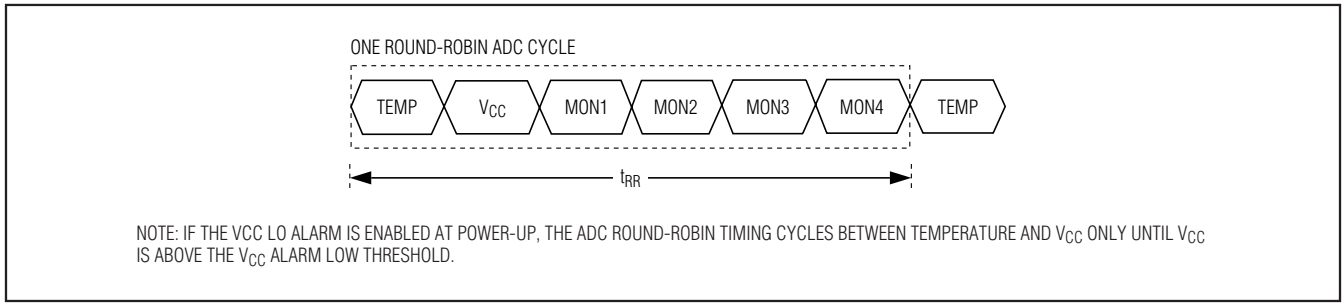


Figure 5. ADC Round-Robin Timing

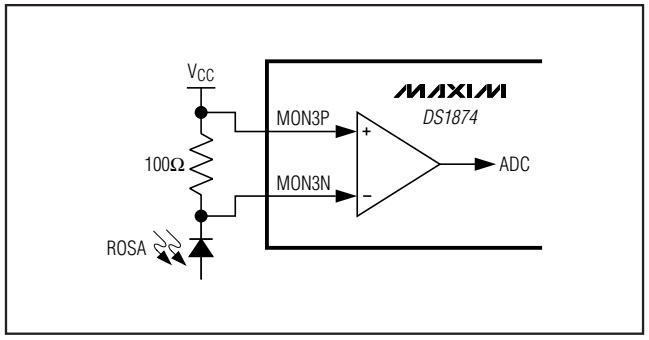


Figure 6. MON3 Differential Input for High-Side RSSI

the measurement is increased by a factor of 8, and because the result is digitally divided by 8 by right-shifting, the bit weight of the measurement still meets the standard's specification (i.e., SFF-8472).

The right-shift operation on the ADC result is carried out based on the contents of right-shift control registers (Table 02h, Registers 8Eh–8Fh) in EEPROM. Four analog channels, MON1–MON4, each have 3 bits allocated to set the number of right-shifts. Up to seven right-shift operations are allowed and are executed as a part of every conversion before the results are compared to the high-alarm and low-alarm levels, or loaded into their corresponding measurement registers (Lower Memory, Registers 64h–6Bh). This is true during the setup of internal calibration as well as during subsequent data conversions.

Enhanced RSSI Monitoring (Dual-Range Functionality)

The DS1874 offers a feature to improve the accuracy and range of MON3, which is most commonly used for monitoring RSSI. The accuracy of the RSSI measurements is increased at the small cost of reduced range (of input signal swing). The DS1874 eliminates this trade-off by offering "dual range" calibration on the MON3 channel (see Figure 6). This feature enables right-shifting (along with its gain and offset settings) when the input signal is below a set threshold (within the range that benefits using right-shifting) and then automatically disables right-shifting (recalling different gain and offset settings) when the input signal exceeds the threshold. Also, to prevent "chattering," hysteresis prevents excessive switching between modes in addition to ensuring that continuity is maintained. Dual-range operation is enabled by default (factory programmed in EEPROM). However, it can easily be disabled through the RSSI_FC and RSSI_FF bits, which are described in the *Register Descriptions* section. When dual-range operation is disabled, MON3 operates identically to the other MON channels, although featuring a differential input.

Dual-range functionality consists of two modes of operation: fine mode and coarse mode. Each mode is calibrated for a unique transfer function, hence the term, dual range. Table 5 highlights the registers related to MON3. Fine mode is equivalent to the other MON channels. Fine mode is calibrated using the gain, offset, and right-shifting registers at locations shown in Table 5 and is ideal for relatively small analog input voltages. Coarse mode is automatically switched to when the input exceeds a threshold (to be discussed in a subsequent paragraph). Coarse mode is calibrated using different gain and offset registers, but lacks right-shifting (since coarse mode is only used on large input signals). The gain and offset registers for coarse mode are also shown in Table 5. Additional information for each of the registers can be found in the *Register Descriptions* section.

Dual-range operation is transparent to the end user. The results of MON3 analog-to-digital conversions are still stored/reported in the same memory locations (68h–69h, Lower Memory) regardless of whether the conversion was performed in fine mode or coarse mode. The only way to tell which mode generated the digital result is by reading the RSSIR bit.

When the DS1874 is powered up, analog-to-digital conversions begin in a round-robin fashion. Every MON3 timeslice begins with a fine mode analog-to-digital conversion (using fine mode's gain, offset, and right-shifting settings). See the flowchart in Figure 7 for more details.

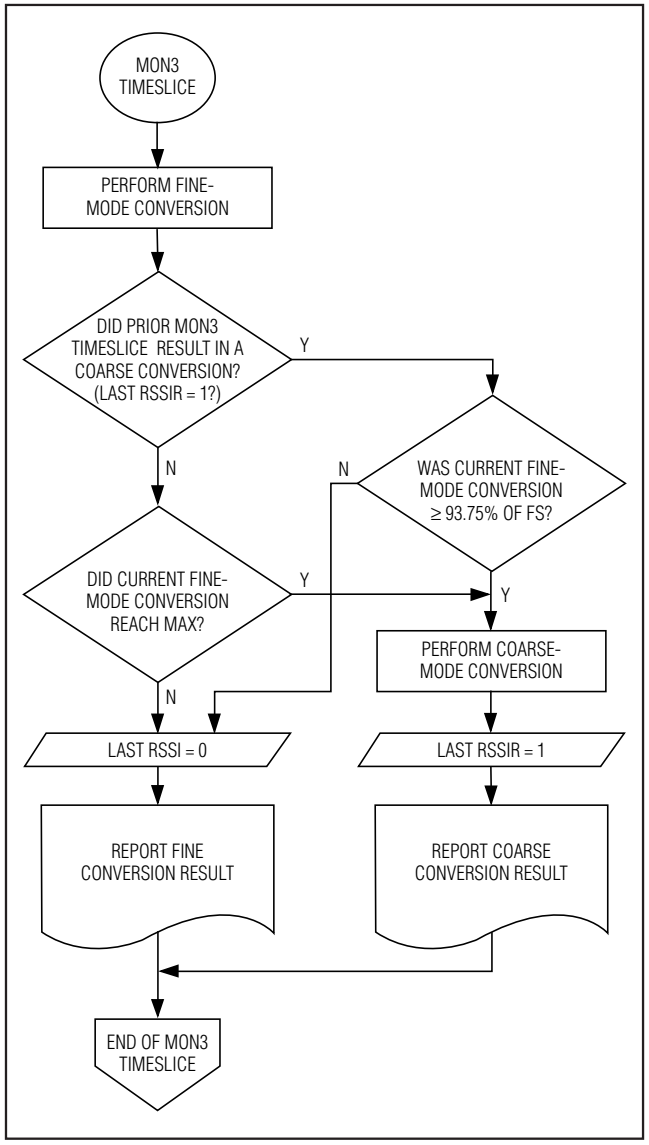


Figure 7. RSSI Flowchart

Then, depending on whether the last MON3 timeslice resulted in a coarse-mode conversion and also depending on the value of the current fine conversion, decisions are made whether to use the current fine-mode conversion result or to make an additional conversion (within the same MON3 timeslice), using coarse mode (using coarse mode's gain and offset settings and no right-shifting) and reporting the coarse-mode result. The flowchart in Figure 7 also illustrates how hysteresis is implemented. The fine-mode conversion is compared to one of two thresholds. The actual threshold values are a function of the number of right-shifts being used. With the use of right-shifting, the fine mode full-scale is programmed to (1/2^nth) of the coarse mode full-scale. The DS1874 now auto ranges to choose the range that gives the best resolution for the measurement. Hysteresis is applied to eliminate chatter when the input resides at the boundary of the two ranges. See Figure 7 for details. Table 4 shows the threshold values for each possible number of right-shifts.

The RSSI_FF and RSSI_FC bits are used to force fine-mode or coarse-mode conversions, or to disable the dual-range functionality. Dual-range functionality is enabled by default (both RSSI_FC and RSSI_FF are factory programmed to 0 in EEPROM). It can be disabled by setting RSSI_FC to 0 and RSSI_FF to 1. These bits are also useful when calibrating MON3. For additional information, see Figure 19.

Table 4. MON3 Hysteresis Threshold Values

NUMBER OF RIGHT-SHIFTS	FINE MODE MAX (hex)	COARSE MODE MIN* (hex)
0	FFF8	F000
1	7FFC	7800
2	3FFE	3C00
3	1FFF	1E00
4	0FFF	0F00
5	07FF	0780
6	03FF	03C0
7	01FF	01E0

**This is the minimum reported coarse-mode conversion.*

Table 5. MON3 Configuration Registers

REGISTER	FINE MODE	COARSE MODE
GAIN	98h–99h, Table 02h	9Ch–9Dh, Table 02h
OFFSET	A8h–A9h, Table 02h	ACh–ADh, Table 02h
$RIGHT\text{-}SHIFT_0$	8Fh, Table 02h	—
CNFGC	8Bh, Table 02h	
UPDATE (RSSIR BIT)	6Fh, Lower Memory	
MON3 VALUE	68h–69h, Lower Memory	

Low-Voltage Operation

The DS1874 contains two power-on reset (POR) levels. The lower level is a digital POR (POD) and the higher level is an analog POR (POA). At startup, before the supply voltage rises above POA, the outputs are disabled, all SRAM locations are set to their defaults, shadowed EEPROM (SEE) locations are zero, and all analog circuitry is disabled. When V_{CC} reaches POA, the SEE is recalled, and the analog circuitry is enabled. While V_{CC} remains above POA, the device is in its normal operating state, and it responds based on its nonvolatile configuration. If during operation V_{CC} falls below POA, but is still above POD, then the SRAM retains the SEE settings from the first SEE recall, but the device analog is shut down and the outputs disabled. If the supply voltage recovers back above POA, then the device immediately resumes normal operation. If the supply voltage falls below POD, then the device SRAM is placed in its default state and another SEE recall is required to reload the nonvolatile settings. The EEPROM recall occurs the next time V_{CC} exceeds POA. Figure 8 shows the sequence of events as the voltage varies.

Any time V_{CC} is above POD, the I^2C interface can be used to determine if V_{CC} is below the POA level. This is accomplished by checking the RDYB bit in the STATUS (Lower Memory, Register 6Eh) byte. RDYB is set when V_{CC} is below POA; when V_{CC} rises above POA, RDYB is timed (within 500µs) to go to 0, at which point the part is fully functional.

For all device addresses sourced from EEPROM (Table 02h, Register 8Ch), the default device address is A2h until V_{CC} exceeds POA, allowing the device address to be recalled from the EEPROM.

Power-On Analog (POA)

POA holds the DS1874 in reset until V_{CC} is at a suitable level (V_{CC} > POA) for the device to accurately measure with its ADC and compare analog signals with its quick-trip monitors. Because V_{CC} cannot be measured by the ADC when V_{CC} is less than POA, POA also asserts the VCC LO alarm, which is cleared by a V_{CC} ADC conversion greater than the customer-programmable V_{CC} alarm low ADC limit. This allows a programmable limit to ensure that the headroom requirements of the transceiver are satisfied during a slow power-up. The TXF output does not latch until there is a conversion above V_{CC} low limit. The POA alarm is nonmaskable. The TXF output is asserted when V_{CC} is below POA. See the *Low-Voltage Operation* section for more information.

Delta-Sigma Outputs (DAC1 and DAC2)

Two delta-sigma outputs are provided, DAC1 and DAC2. With the addition of an external RC filter, these outputs provide two 9-bit resolution analog outputs with the full-scale range set by the input REFIN. Each output

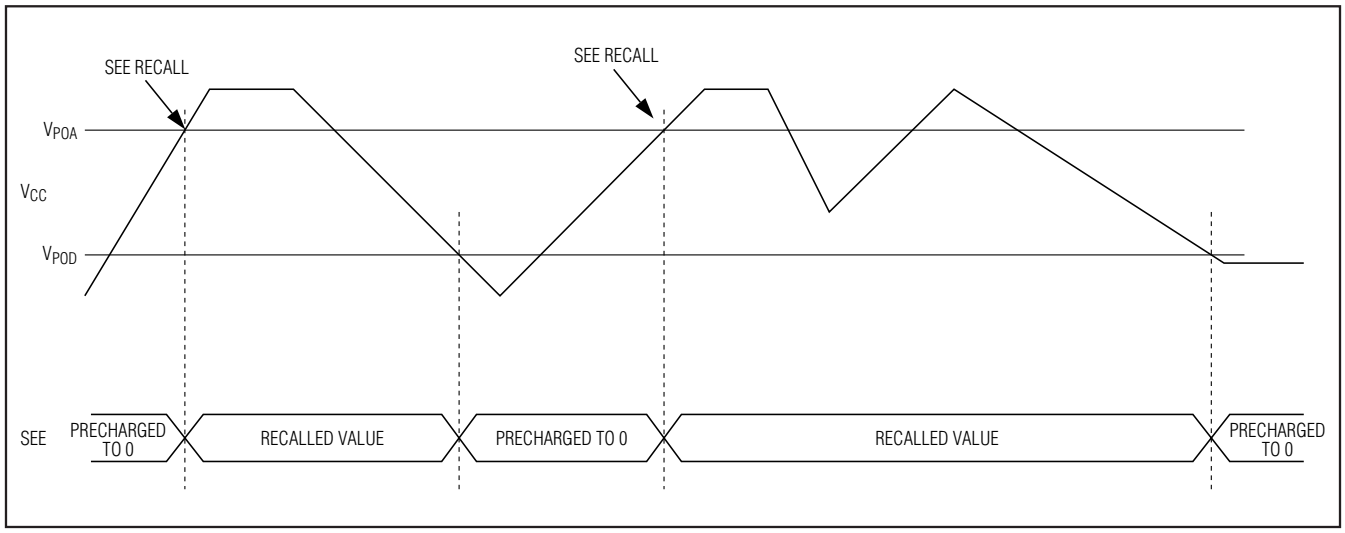


Figure 8. Low-Voltage Hysteresis Example

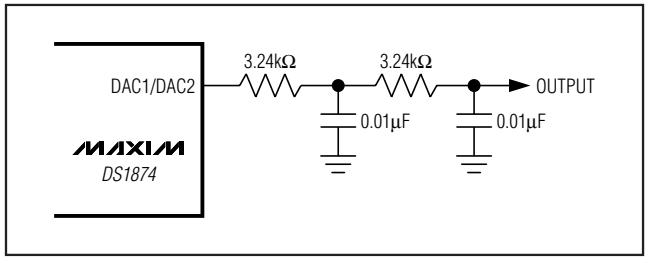


Figure 9. Recommended RC Filter for DAC1/DAC2

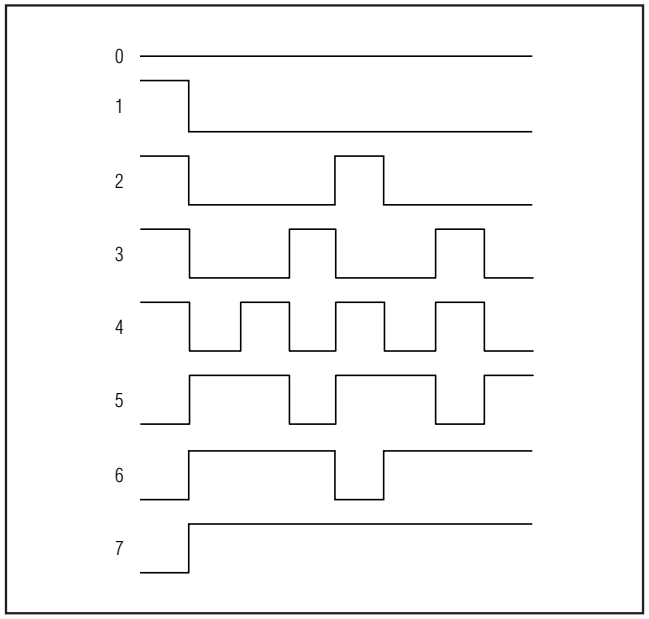


Figure 10. Delta-Sigma Outputs

is either manually controlled or controlled using a temperature-indexed LUT. A delta-sigma is a digital output using pulse-density modulation. It provides much lower output ripple than a standard digital PWM output given the same clock rate and filter components. Before t_{INIT}, the DAC1 and DAC2 outputs are high impedance.

The external RC filter components are chosen based on ripple requirements, output load, delta-sigma frequency, and desired response time. A recommended filter is shown in Figure 9.

The DS1874's delta-sigma outputs are 9 bits. For illustrative purposes, a 3-bit example is provided. Each possible output of this 3-bit delta-sigma DAC is given in Figure 10.

In LUT mode, DAC1 and DAC2 are each controlled by a separate 8-bit, 4°C-resolution, temperature-addressed LUT. The delta-sigma outputs use a 9-bit structure. The 8-bit LUTs are either loaded directly into the MSBs (8:1) or the LSBs (7:0). This is determined by DAC1TI (Table 02h, Register C3h), DAC2TI (Table 02h, Register C4h), DAC1TC (Table 02h, Register C6h, bit 6), and DAC2TC (Table 02h, Register C6h, bit 5). See Figure 11 for more details. The DAC1 LUT (Table 07h) and DAC2 LUT (Table 08h) are nonvolatile and password-2 protected.

The reference input, REFIN, is the supply voltage for the output buffer of DAC1 and DAC2. The voltage connected to REFIN must be able to support the edge rate requirements of the delta-sigma outputs. In a typical application, a 0.1µF capacitor should be connected between REFIN and ground.

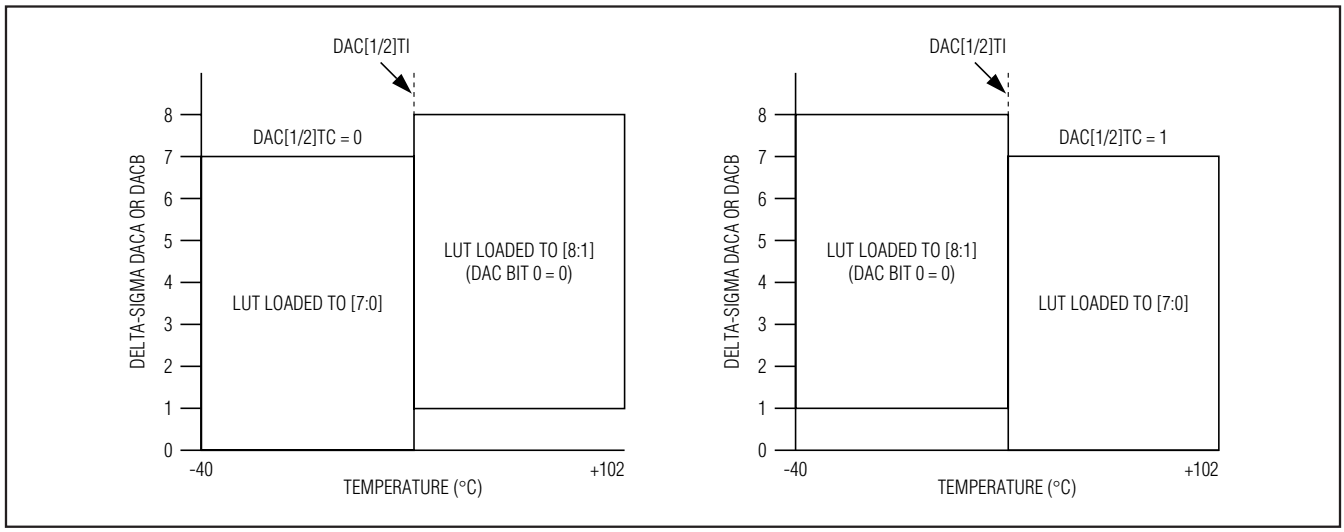


Figure 11. DAC1/DAC2 LUT Assignments

Digital I/O Pins

Five digital input and five digital output pins are provided for monitoring and control.

LOS, LOSOUT

By default (LOSC = 1, Table 02h, Register 89h), the LOS pin is used to convert a standard comparator output for loss of signal (LOS) to an open-collector output. This means the mux shown in the *Block Diagram* by default selects the LOS pin as the source for the LOSOUT output transistor. The output of the mux can be read in the STATUS byte (Lower Memory, Register 6Eh) as the RXL bit. The RXL signal can be inverted (INV LOS = 1) before driving the open-drain output transistor using the XOR gate provided. Setting LOSC = 0 configures the mux to be controlled by LOS LO, which is driven by the output of the LOS quick trip (Table 02h, Registers BEh and BFh). The mux setting (stored in EEPROM) does not take effect until V_{CC} > POA, allowing the EEPROM to recall.

IN1, RSEL, OUT1, RSELOUT

The digital input IN1 and RSEL pins primarily serve to meet the rate-select requirements of SFP and SFP+. They also serve as general-purpose inputs. OUT1 and RSELOUT are driven by a combination of the IN1, RSEL, and logic dictated by control registers in the EEPROM (Figure 13). The levels of IN1 and RSEL can be read using the STATUS register (Lower Memory, Register 6Eh). The open-drain output OUT1 can be controlled and/or inverted using the CNFGB register (Table 02h, Register 8Ah). The open-drain RSELOUT output is software-controlled and/or inverted through the Status register and CNFGA register (Table 02h, Register 89h). External pullup resistors must be provided on OUT1 and RSELOUT to realize high logic levels.

TXF, TXD, TXDOUT

TXDOUT is generated from a combination of TXF, TXD, and the internal signal FETG. A software control identical to TXD is available (TXDC, Lower Memory, Register 6Eh). A TXD pulse is internally extended (TXD_{EXT}) by time t_{INITR1} to inhibit the latching of low alarms and warnings related to the APC loop to allow for the loop to stabilize. The nonlatching alarms and warnings are TXP LO, LOS LO, and MON1–MON4 LO alarms and warnings. In addition, TXP LO is disabled from creating FETG. TXF is both an input and an output (Figure 12). See the *Transmit Fault (TXF) Output* section for a detailed explanation of TXF. Figure 12 shows that the

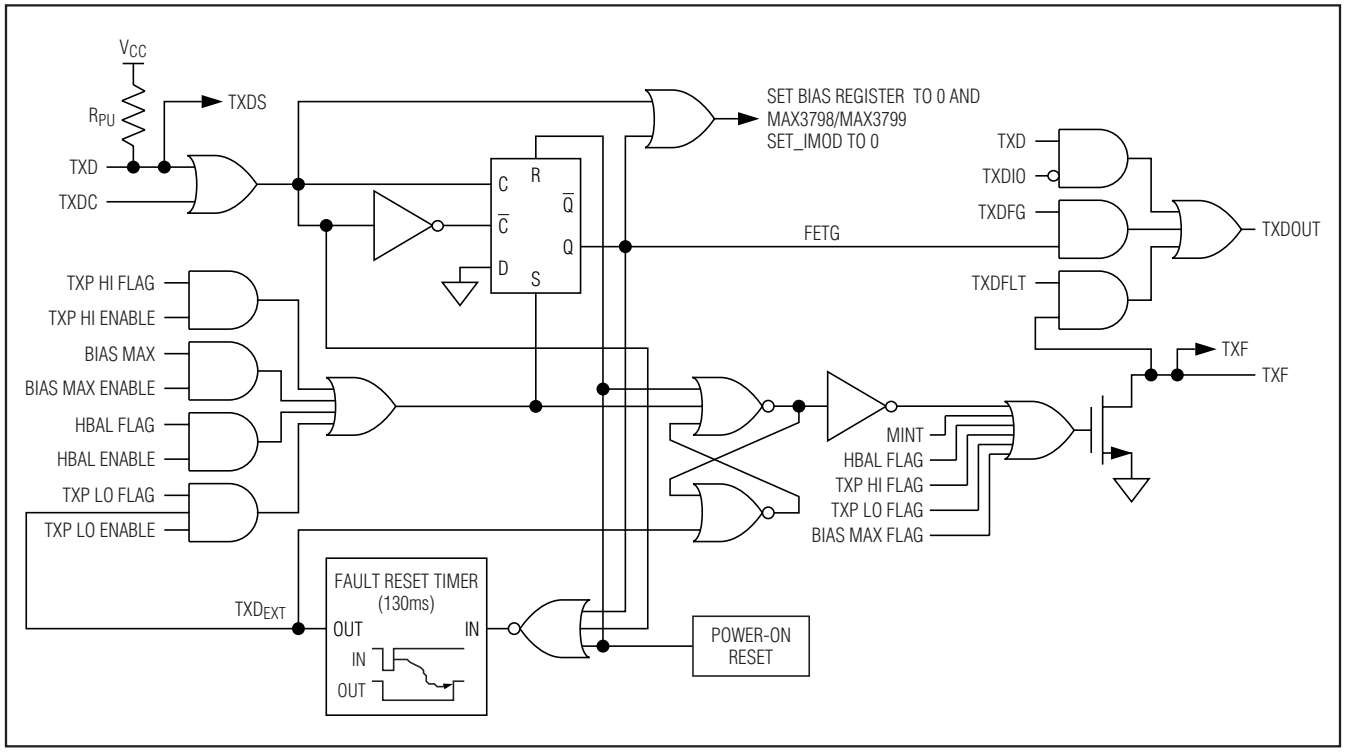


Figure 12. Logic Diagram 1

SFP+ Controller with Digital LDD Interface

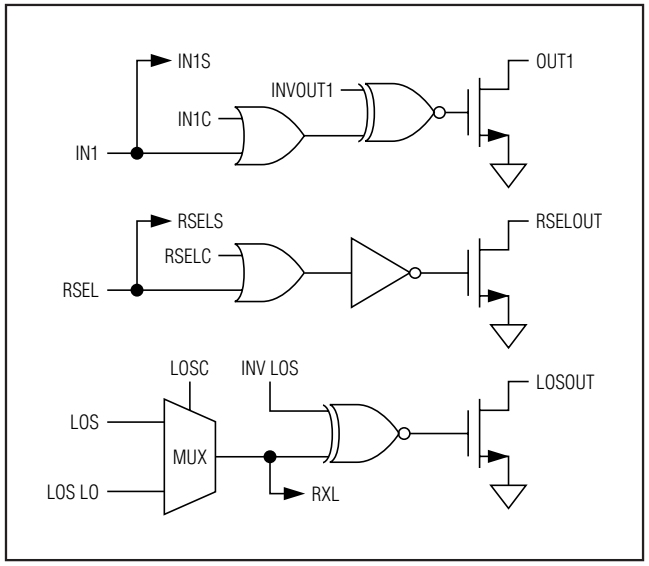


Figure 13. Logic Diagram 2

same signals and faults can also be used to generate the internal signal FETG (Table 01h/05h, Registers FAh and FBh). FETG is used to send a fast "turn-off" command to the laser driver. The intended use is a direct connection to the MAX3798/MAX3799's TXD input if this is desired. When V_{CC} < POA, TXDOUT is high impedance.

Transmit Fault (TXF) Output

TXF can be triggered by all alarms, warnings, and quick trips (Figure 12). The six ADC alarms, warnings, and the LOS quick trips require enabling (Table 01h/05h, Registers F8h and FDh). See Figures 14a and 14b for nonlatched and latched operation. Latching of the alarms is controlled by the CNFGB and CNFGC registers (Table 02h, Registers 8Ah–8Bh).

Die Identification

The DS1874 has an ID hardcoded in its die. Two registers (Table 02h, Registers CEh–CFh) are assigned for this feature. The CEh register reads 74h to identify the part as the DS1874, while the CFh register reads the current device version.

3-Wire Master for Controlling the MAX3798/MAX3799

The DS1874 controls the MAX3798/MAX3799 over a proprietary 3-wire interface. The DS1874 acts as the master, initiating communication with and generating the clock for the MAX3798/MAX3799. It is a 3-pin interface consisting of SDAOUT (a bidirectional data line), an SCLOUT clock signal, and a CSELOUT chip-select output (active high).

Protocol

The DS1874 initiates a data transfer by asserting the CSELOUT pin. It then starts to generate a clock signal

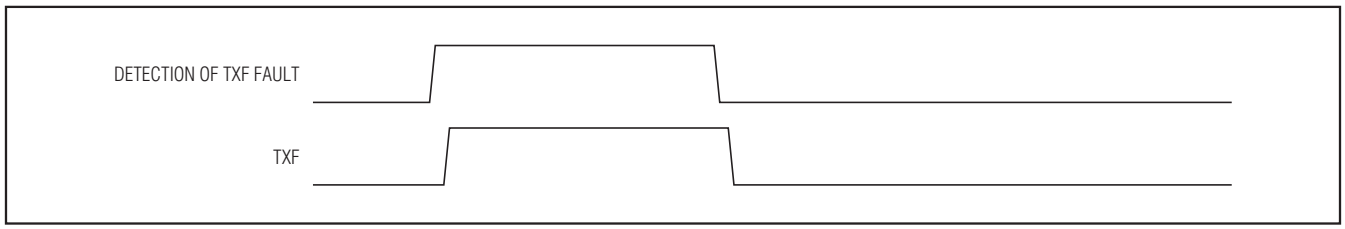


Figure 14a. TXF Nonlatched Operation

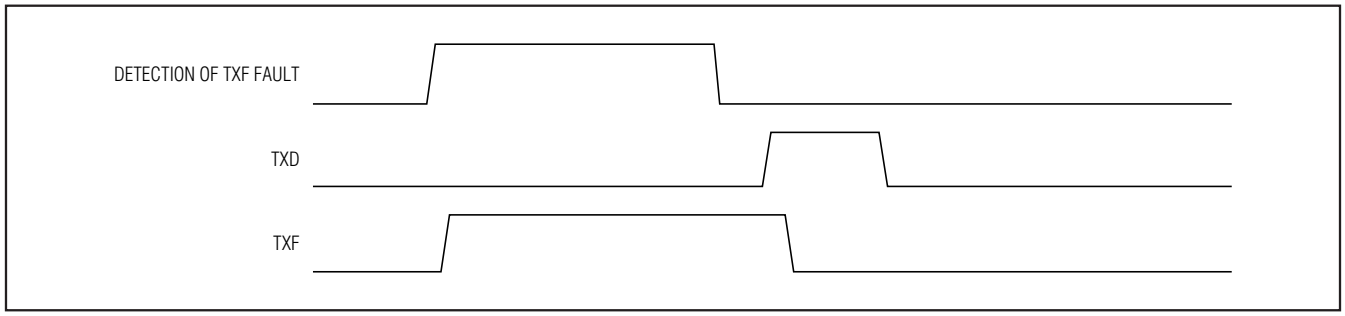


Figure 14b. TXF Latched Operation

after the CSELOUT has been set to 1. Each operation consists of 16-bit transfers (15-bit address/data, 1-bit RWN). All data transfers are MSB first.

BIT	NAME	DESCRIPTION
15:9	Address	7-bit internal register address
8	RWN	0: write; 1: read
7:0	Data	8-bit read or write data

Write Mode (RWN = 0): The master generates 16 clock cycles at SCLOUT in total. It outputs 16 bits (MSB first) to the SDAOUT line at the falling edge of the clock. The master closes the transmission by setting the CSELOUT to 0.

Read Mode (RWN = 1): The master generates 16 clock cycles at SCLOUT in total. It outputs 8 bits (MSB first) to the SDAOUT line at the falling edge of the clock. The SDAOUT line is released after the RWN bit has been transmitted. The slave outputs 8 bits of data (MSB first) at the rising edge of the clock. The master samples SDAOUT at the falling edge of SCLOUT. The master closes the transmission by setting the CSELOUT to 0.

3-Wire Interface Timing

Figure 15 shows the 3-wire interface timing. Figure 16 shows the 3-wire state machine. See the *3-Wire Digital Interface Specification* table for more information.

DS1874 and MAX3798/MAX3799 Communication

Normal Operation

The majority of the communication between the two devices consists of bias adjustments for the APC loop. After each temperature conversion, the laser modulation setting must be updated. Status registers TXSTAT1 and TXSTAT2 are read between temperature updates at a regular interval: t_{RR} (see the *Analog Voltage Monitoring Characteristics* table). The results are stored in TXSTAT1 and TXSTAT2 (Table 02h, FCh–FDh).

Manual Operation

The MAX3798/MAX3799 are manually controllable using four registers in the DS1874: 3WCTRL, ADDRESS, WRITE, and READ. Commands can be manually issued while the DS1874 is in normal operation mode. It is also possible to suspend normal 3-wire commands so that only manual operation commands are sent (3WCTRL, Table 02h, Register F8h).

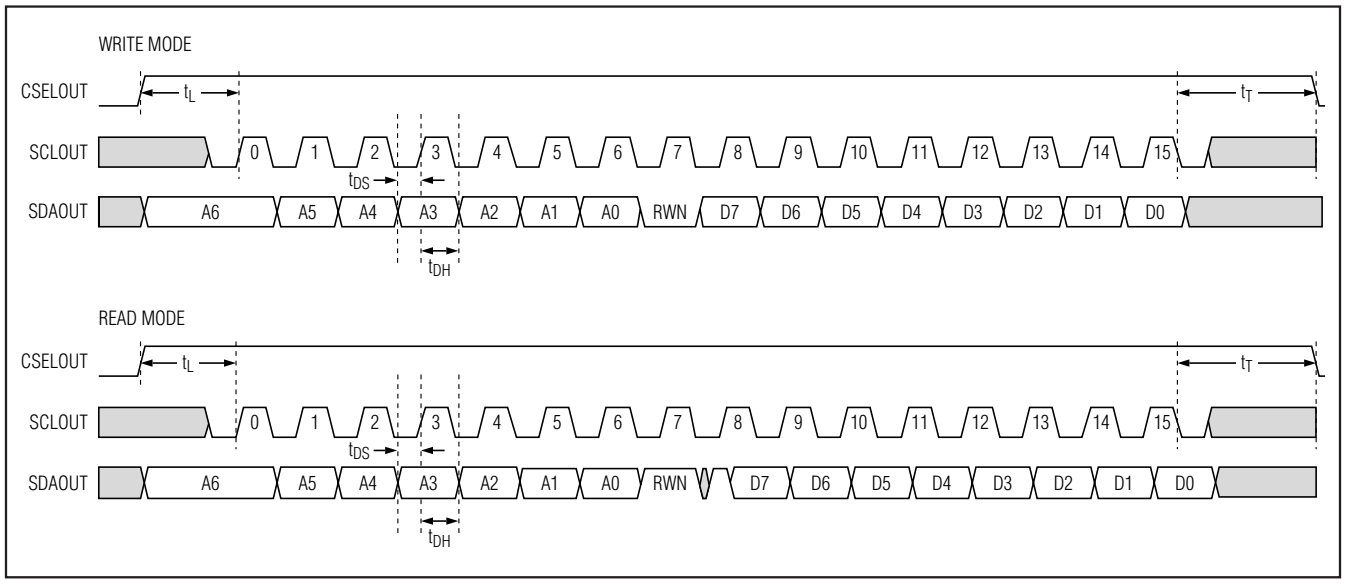


Figure 15. 3-Wire Timing

SFP+ Controller with Digital LDD Interface

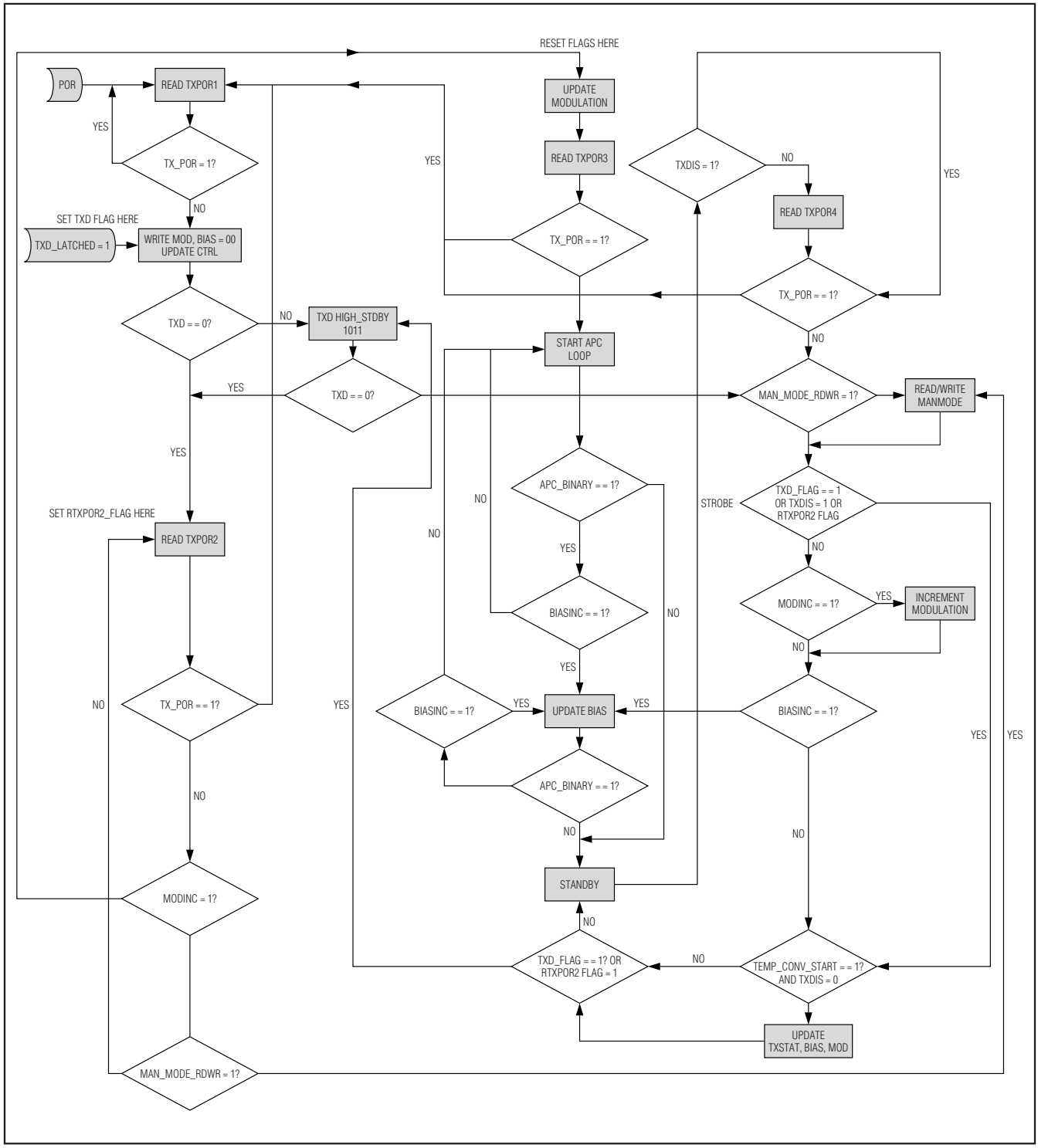


Figure 16. 3-Wire State Machine

Initialization

During initialization, the DS1874 transfers all its 3-wire EEPROM control registers to the MAX3798/MAX3799.

The 3-wire control registers include the following:

- RXCTRL1
- RXCTRL2
- SET_CML
- SET_LOS
- TXCTRL
- IMODMAX
- IBIASMAX
- SET_PWCTRL
- SET_TXDE

The control registers are first written when V_{CC} exceeds POA. They are also written if the MAX3798/MAX3799 TX_POR bit is set high (visible in 3W TXSTAT1, bit 7). In the MAX3798/MAX3799, this bit is "sticky" (latches high and is cleared on a read). They are also updated on a rising edge of TXD. Any time one of these events occurs, the DS1874 reads and updates TXSTAT1 and TXSTAT2 and sets SET_IBIAS and SET_IMOD in the MAX3798/MAX3799 to 0.

MAX3798/MAX3799 Register Map and DS1874 Corresponding Location

MAX3798/MAX3799 REGISTER FUNCTION	REGISTER NAME	DS1874 LOCATION
Receiver Control 1	RXCTRL1	Table 02h, E8h
Receiver Control 2	RXCTRL2	Table 02h, E9h
Receiver Status	RXSTAT	Lower Memory, 6Eh, Bit1
Output CML Level Setting	SET_CML	Table 02h, EAh
LOS Threshold Level Setting	SET_LOS	Table 02h, EBh
Transmitter Control	TXCTRL	Table 02h, ECh
Transmitter Status 1	TXSTAT1	Table 02h, FCh
Transmitter Status 2	TXSTAT2	Table 02h, FDh
Bias Current Setting	SET_IBIAS/BIAS	Table 02h, CBh–CCh
Modulation Current Setting	SET_IMOD/MODULATION	Table 02h, 82h–83h
Maximum Modulation Current Setting	IMODMAX	Table 02h, EDh
Maximum Bias Current Setting	IBIASMAX	Table 02h, EEh
Modulation Current Increment Setting	MODINC	(see Note)
Bias Current Increment Setting	BIASINC	Automatically performed by APC loop. Disable APC before using 3-wire manual mode. Manual Mode: Table 02h, F8h–FBh
Mode Control	MODECTRL	(see Note)
Transmitter Pulse-Width Control	SET_PWCTRL	Table 02h, EFh
Transmitter Deemphasis Control	SET_TXDE	Table 02h, F0h

Note: *This register is not present in the DS1874. To access this register, use manual operation (see the* Manual Operation *section).*