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Rev 1; 10/08

PON Triplexer and SFP Controller

General Description

The DS1875 controls and monitors all functions for burst-mode transmitters, APD receivers, and video receivers. It also includes a power-supply controller for APD bias generation, and provides all SFF-8472 diagnostic and monitoring functionality. The combined solution of the DS1875 and the MAX3643 laser driver provides APC loop, modulation current control, and eye safety functionality. Ten ADC channels monitor V_{CC}, temperature (both internal signals), and eight external monitor inputs (MON1–MON8) that can be used to meet transmitter, digital receiver, video receiver, and APD receiver-signal monitoring requirements. Four total DAC outputs are available. A PWM controller with feedback and compensation pins can be used to generate the bias for an APD or as a step-down converter. Five I/O pins allow additional monitoring and configuration.

Applications

BPON, GPON, or EPON Optical Triplexers

SFF, SFP, and SFP+ Transceiver Modules

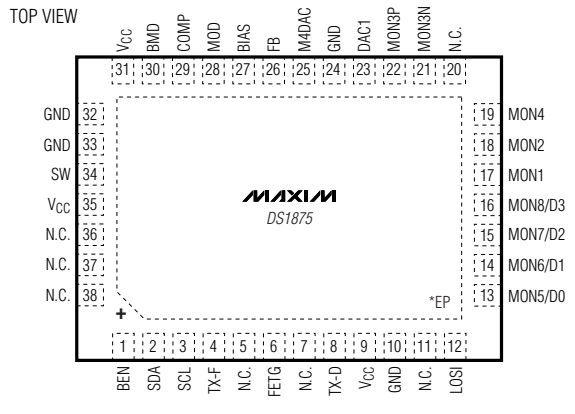
APD Controller

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
DS1875T+	-40°C to +95°C	38 TQFN-EP*
DS1875T+T&R	-40°C to +95°C	38 TQFN-EP*

+Denotes a lead-free/RoHS-compliant package.
T&R = Tape and reel.
**EP = Exposed pad.*

Pin Configuration



TQFN
(5mm × 7mm × 0.8mm)

*EXPOSED PAD.

Features

- **Meets All PON Burst-Timing Requirements for Burst-Mode Operation**
- **Laser Bias Controlled by APC Loop and Temperature Lookup Table (LUT)**
- **Laser Modulation Controlled by Temperature LUT**
- **Six Total DACs: Four External, Two Internal**
- **Two 8-Bit DACs, One of Which is Optionally Controlled by MON4 Voltage**
- **Internal 8-Bit DAC Controlled by a Temperature-Indexed LUT**
- **PWM Controller**
- **Boost or Buck Mode**
- **Boost Mode: Uses Optional External Components, Up to 90V Bias Generation**
- **131kHz, 262kHz, 525kHz, or 1050kHz Selectable-Switching Frequency**
- **APD Overcurrent Protection Using Optional Fast Shutdown**
- **10 Analog Monitor Channels: Temperature, V_{CC}, Eight Monitors**
- **Internal, Factory-Calibrated Temperature Sensor**
- **RSSI with 29dB Electrical Dynamic**
- **Five I/O Pins for Additional Control and Monitoring Functions, Four of Which are Either Digital I/O or Analog Monitors**
- **Comprehensive Fault-Measurement System with Maskable Laser Shutdown Capability**
- **Two-Level Password Access to Protect Calibration Data**
- **120 Bytes of Password-1 Protected Memory**
- **128 Bytes of Password-2 Protected Memory in Main Device Address**
- **256 Additional Bytes Located at A0h Slave Address**
- **I^2C-Compatible Interface for Calibration and Monitoring**
- **2.85V to 3.9V Operating Voltage Range**
- **-40°C to +95°C Operating Temperature Range**
- **38-Pin TQFN (5mm x 7mm) Package**

For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.

PON Triplexer and SFP Controller

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Voltage Range on MON1–MON8, BEN, BMD, and TX-D Pins Relative to Ground .....-0.5V to (V_{CC} + 0.5V)*
Voltage Range on V_{CC}, SDA, SCL, D0–D3, and TX-F Pins Relative to Ground.....-0.5V to 6V

Operating Temperature Range .....-40°C to +95°C
Programming Temperature Range .....0°C to +85°C
Storage Temperature Range .....-55°C to +125°C
Soldering Temperature.....Refer to the IPC/JEDEC J-STD-020 Specification.

**Subject to not exceeding +6V.*

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

(T_A = -40°C to +95°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Main Supply Voltage	V_{CC}	(Note 1)	+2.85		+3.9	V
High-Level Input Voltage (SDA, SCL, BEN)	$V_{IH:1}$		0.7 x V_{CC}		V_{CC} + 0.3	V
Low-Level Input Voltage (SDA, SCL, BEN)	$V_{IL:1}$		-0.3		0.3 x V_{CC}	V
High-Level Input Voltage (TX-D, LOSI, D0, D1, D2, D3)	$V_{IH:2}$		2.0		V_{CC} + 0.3	V
Low-Level Input Voltage (TX-D, LOSI, D0, D1, D2, D3)	$V_{IL:2}$		-0.3		+0.8	V

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = +2.85V to +3.9V, T_A = -40°C to +95°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current	I_{CC}	(Notes 1, 2)		5.5	10	mA
Output Leakage (SDA, TX-F, D0, D1, D2, D3)	I_{LO}	(Note 2)			1	µA
Low-Level Output Voltage (SDA, TX-F, FETG, D0, D1, D2, D3)	V_{OL}	I_{OL} = 4mA			0.4	V
		I_{OL} = 6mA			0.6	
High-Level Output Voltage (FETG)	V_{OH}	I_{OH} = 4mA	V_{CC} - 0.4			V
FETG Before Recall		(Note 3)		10	100	nA
Input Leakage Current (SCL, BEN, TX-D, LOSI)	$I_{LI:1}$				1	µA
Digital Power-On Reset	POD		1.0		2.2	V
Analog Power-On Reset	POA		2.1		2.75	V

ELECTRICAL CHARACTERISTICS (DAC1 AND M4DAC)

(V_{CC} = +2.85V to +3.9V, T_A = -40°C to +95°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DAC Output Range				2.5		V
DAC Output Resolution				8		Bits
DAC Output Integral Nonlinearity			-1		+1	LSB
DAC Output Differential Nonlinearity			-1		+1	LSB
DAC Error		T_A = +25°C	-1.25		+1.25	%FS
DAC Temperature Drift			-2		+2	%FS
DAC Offset			-12		+12	mV
Maximum Load			-500		+500	µA
Maximum Load Capacitance					250	pF

ANALOG INPUT CHARACTERISTICS (BMD, TXP HI, TXP LO, HBIAS)

(V_{CC} = +2.85V to +3.9V, T_A = -40°C to +95°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
BMD, TXP HI, TXP LO Full-Scale Voltage	V_{APC}	(Note 4)		2.5		V
HBIAS Full-Scale Voltage		(Note 5)		1.25		V
BMD Input Resistance			35	50	65	kΩ
Resolution				8		Bits
Error		T_A = +25°C (Note 6)		±2		%FS
Integral Nonlinearity			-1		+1	LSB
Differential Nonlinearity			-1		+1	LSB
Temperature Drift			-2.5		+2.5	%FS

ANALOG OUTPUT CHARACTERISTICS

(V_{CC} = +2.85V to +3.9V, T_A = -40°C to +95°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
BIAS Current	I_{BIAS}	(Note 1)		1.2		mA
I_{BIAS} Shutdown Current	$I_{BIAS:OFF}$			10	100	nA
Voltage at I_{BIAS}			0.7	1.2	1.4	V
MOD Full-Scale Voltage	V_{MOD}	(Note 5)		1.25		V
MOD Output Impedance		(Note 7)		3		kΩ
V_{MOD} Error		T_A = +25°C (Note 8)	-1.25		+1.25	%FS
V_{MOD} Integral Nonlinearity			-1		+1	LSB
V_{MOD} Differential Nonlinearity			-1		+1	LSB
V_{MOD} Temperature Drift			-2		+2	%FS

PWM CHARACTERISTICS

(V_{CC} = +2.85V to +3.9V, T_A = -40°C to +95°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
PWM-DAC Full-Scale Voltage	$V_{PWM-DAC}$			1.25		V
PWM-DAC Resolution					8	Bits
$V_{PWM-DAC}$ Full-Scale Voltage Error		T_A = +25°C		1.25		%
$V_{PWM-DAC}$ Integral Nonlinearity			-1		1	LSB
$V_{PWM-DAC}$ Differential Nonlinearity			-1		1	LSB
$V_{PWM-DAC}$ Temperature Drift			-2		+2	%FS
SW Output Impedance					20	Ω
SW Frequency Error	f_{SWER}	(Note 9)	-5		+7	%
SW Duty Cycle	D_{MAX}		89	90	91	%
Error-Amplifier Source Current				-10		µA
Error-Amplifier Sink Current				+10		µA
COMP High-Voltage Clamp				2.1		V
COMP Low-Voltage Clamp				0.8		V
Error-Amplifier Transconductance	G_M			425		µS
Error-Amplifier Output Impedance	R_{EA}			260		MΩ
FB Pin Capacitance				5		pF

TIMING CHARACTERISTICS (CONTROL LOOP AND QUICK TRIP)

(V_{CC} = +2.85V to +3.9V, T_A = -40°C to +95°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
First BMD Sample Following BEN	t_{FIRST}	(Note 10)				
Remaining Updates During BEN	t_{UPDATE}	(Note 10)				
BEN High Time	$t_{BEN:HIGH}$		400			ns
BEN Low Time	$t_{BEN:LOW}$		96			ns
Output-Enable Time Following POA	t_{INIT}		10			ms
BIAS and MOD Turn-Off Delay	t_{OFF}				5	µs
BIAS and MOD Turn-On Delay	t_{ON}				5	µs
FETG Turn-On Delay	$t_{FETG:ON}$				5	µs
FETG Turn-Off Delay	$t_{FETG:OFF}$				5	µs

ANALOG VOLTAGE MONITORING

(V_{CC} = +2.85V to +3.9V, T_A = -40°C to +95°C, unless otherwise noted.)

PARAMETER		SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ADC Resolution					13		Bits
Input/Supply Accuracy (MON1–MON8, V_{CC})		ACC	At factory setting		0.25	0.50	%FS
Update Rate for Temp, MON1–MON4, and V_{CC}		$t_{FRAME:1}$			78	95	ms
Update Rate for MON5–MON8		$t_{FRAME:2}$	Bit EN5TO8B is enabled in Table 02h, Register 89h		156	190	ms
Input/Supply Offset (MON1–MON8, V_{CC})		V_{OS}	(Note 11)		0	5	LSB
Factory Setting	MON1–MON8		Full scales are user programmable		2.5		V
	V_{CC}				6.5536		
	MON3 Fine				312.5		µV

DIGITAL THERMOMETER

(V_{CC} = +2.85V to +3.9V, T_A = -40°C to +95°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Thermometer Error	T_{ERR}	-40°C to +95°C			±3.0	°C

NONVOLATILE MEMORY CHARACTERISTICS

(V_{CC} = +2.85V to +3.9V, T_A = -40°C to +95°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
EEPROM Write Cycles		At +85°C (Note 11)	50,000			
		At +25°C (Note 11)	200,000			

I²C TIMING SPECIFICATIONS

(V_{CC} = +2.85V to +3.9V, T_A = -40°C to +95°C, timing referenced to $V_{IL(MAX)}$ and $V_{IH(MIN)}$.) (See Figure 15.)

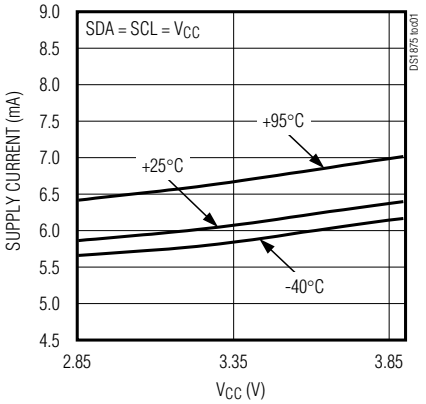
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SCL Clock Frequency	f_{SCL}	(Note 12)	0		400	kHz
Clock Pulse-Width Low	t_{LOW}		1.3			µs
Clock Pulse-Width High	t_{HIGH}		0.6			µs
Bus-Free Time Between STOP and START Condition	t_{BUF}		1.3			µs
START Hold Time	$t_{HD:STA}$		0.6			µs
START Setup Time	$t_{SU:STA}$		0.6			µs
Data in Hold Time	$t_{HD:DAT}$		0		0.9	µs
Data in Setup Time	$t_{SU:DAT}$		100			ns
Capacitive Load for Each Bus Line	C_B				400	pF
Rise Time of Both SDA and SCL Signals	t_R	(Note 13)	$20 + 0.1C_B$		300	ns
Fall Time of Both SDA and SCL Signals	t_F	(Note 13)	$20 + 0.1C_B$		300	ns
STOP Setup Time	$t_{SU:STO}$		0.6			µs
EEPROM Write Time	t_W	(Note 14)			20	ms

Note 1: All voltages are referenced to ground. Current into IC is positive, and current out of the IC is negative.
Note 2: Digital inputs are at rail. FETG is disconnected. SDA = SCL = V_{CC}. SW, DAC1, and M4DAC are not loaded.
Note 3: See the *Safety Shutdown (FETG) Output* section for details.
Note 4: Eight ranges allow the full scale to change from 625mV to 2.5V.
Note 5: Eight ranges allow the full scale to change from 312.5mV to 1.25V.
Note 6: This specification applies to the expected full-scale value for the selected range. See the COMP RANGING register description for available full-scale ranges.
Note 7: The output impedance of the DS1875 is proportional to its scale setting. For instance, if using the 1/2 scale, the output impedance would be approximately 1.56kΩ.
Note 8: This specification applies to the expected full-scale value for the selected range. See the MOD RANGING register description for available full-scale ranges.
Note 9: The switching frequency is selectable between four values: 131.25kHz, 262.5kHz, 525kHz, and 1050kHz.
Note 10: See the *APC and Quick-Trip Shared Comparator Timing* section for details.
Note 11: Guaranteed by design.
Note 12: I²C interface timing shown is for fast-mode (400kHz) operation. This device is also backward compatible with I²C standard mode.
Note 13: C_B—Total capacitance of one bus line in pF.
Note 14: EEPROM write begins after a STOP condition occurs.

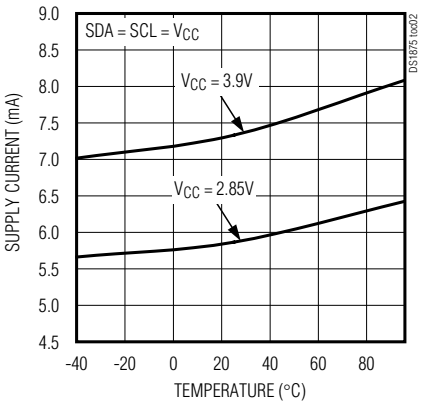
Typical Operating Characteristics

(V_{CC} = +2.85V to +3.9V, T_A = +25°C, unless otherwise noted.)

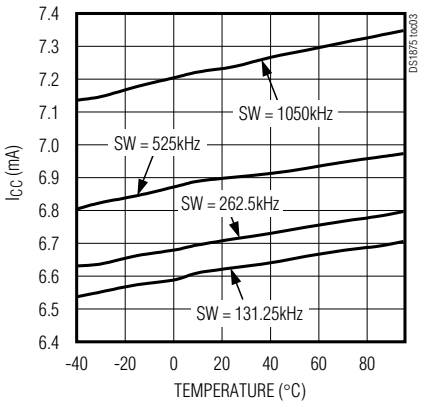
SUPPLY CURRENT vs. SUPPLY VOLTAGE



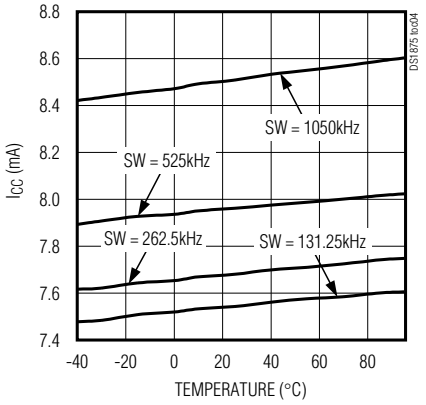
SUPPLY CURRENT vs. TEMPERATURE



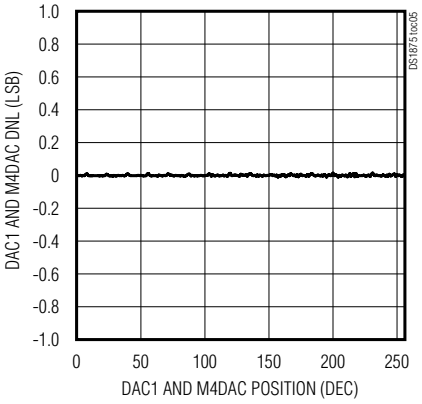
SUPPLY CURRENT vs. TEMPERATURE VCC = 3.3V, NO BIAS CURRENT



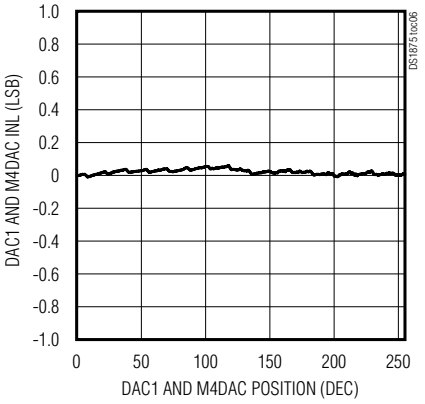
SUPPLY CURRENT vs. TEMPERATURE VCC = 5V, NO BIAS CURRENT



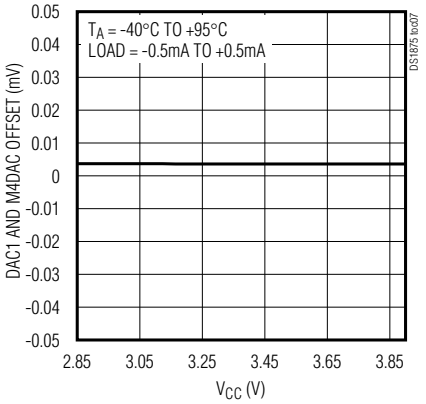
DAC1 AND M4DAC DNL



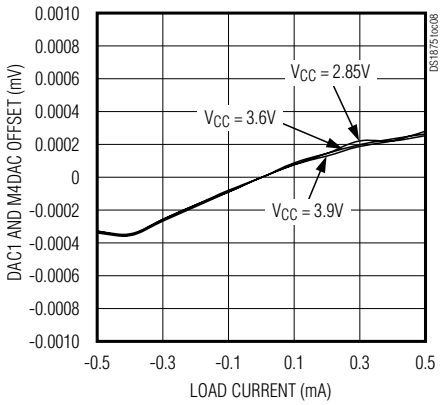
DAC1 AND M4DAC INL



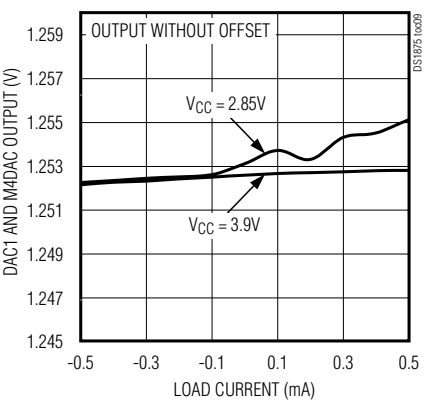
DAC1 AND M4DAC OFFSET vs. VCC



DAC1 AND M4DAC OFFSET VARIATION vs. LOAD CURRENT



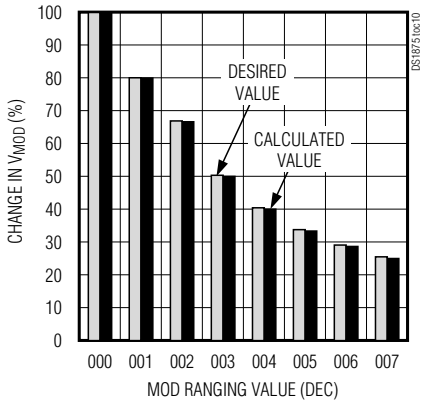
DAC1 AND M4DAC OUTPUT vs. LOAD CURRENT



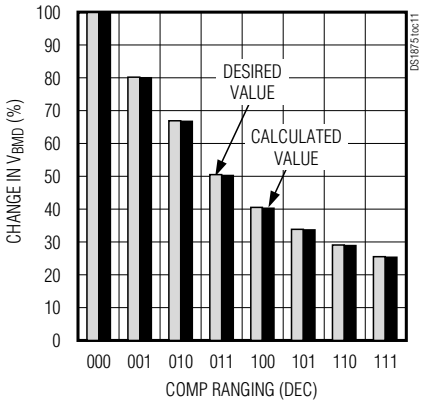
Typical Operating Characteristics (continued)

(V_{CC} = +2.85V to +3.9V, T_A = +25°C, unless otherwise noted.)

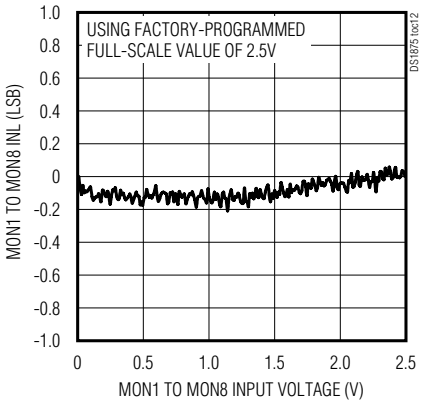
CALCULATED AND DESIRED % CHANGE IN V_{MOD} vs. MOD RANGING



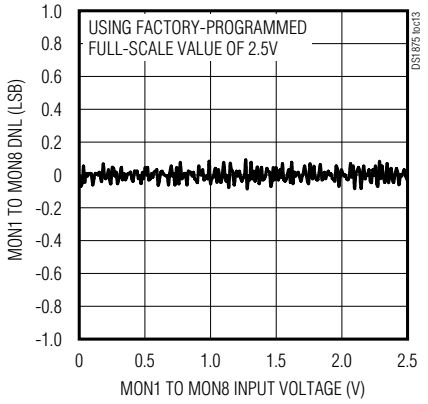
DESIRED AND CALCULATED CHANGE IN V_{BMD} vs. COMP RANGING



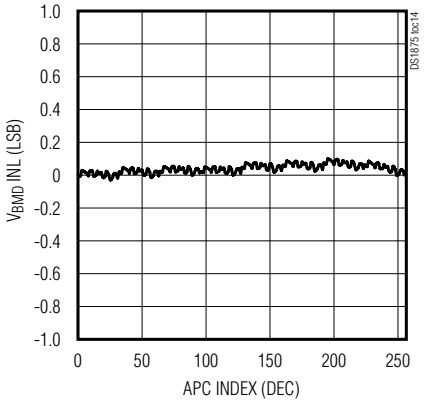
MON1 TO MON8 INL



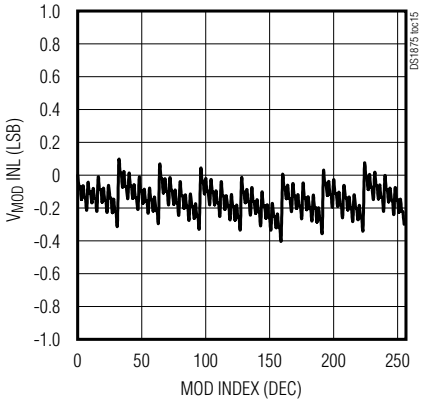
MON1 TO MON8 DNL



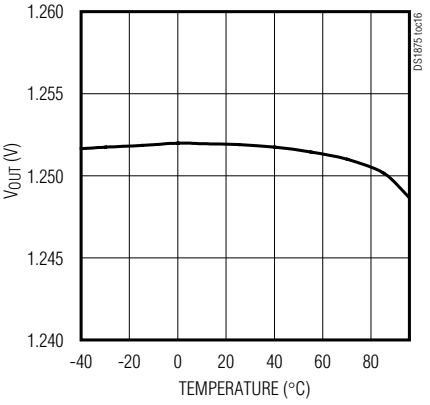
V_{BMD} INL vs. APC INDEX



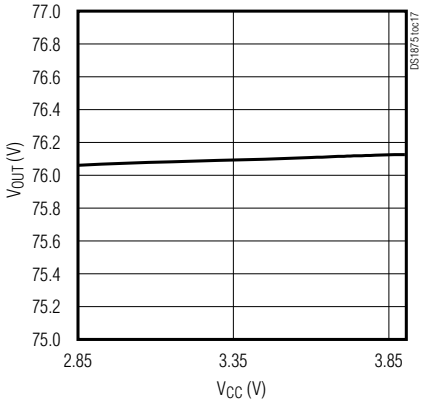
V_{MOD} INL vs. MOD INDEX



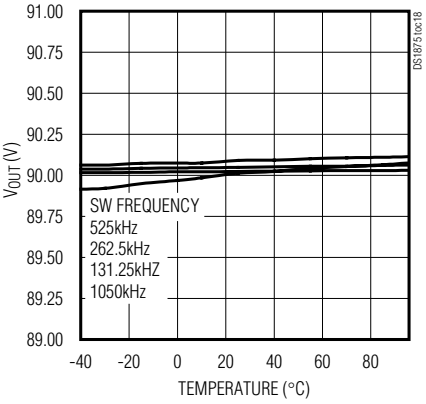
FB VOLTAGE vs. TEMPERATURE PWM DAC = FFh



V_{OUT} vs. V_{CC} V_{IN} = 3.3V



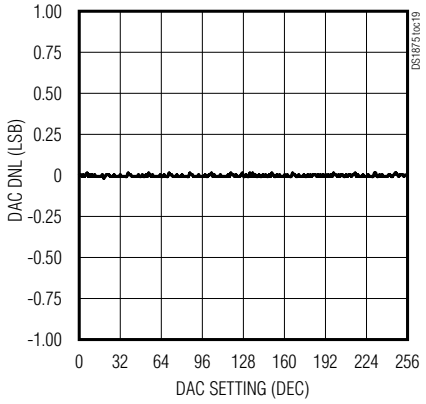
DUTY-CYCLE LIMIT vs. TEMPERATURE



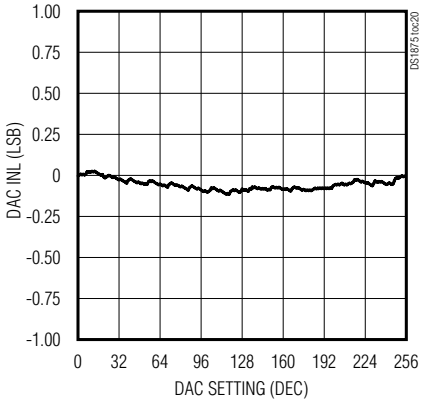
Typical Operating Characteristics (continued)

(V_{CC} = +2.85V to +3.9V, T_A = +25°C, unless otherwise noted.)

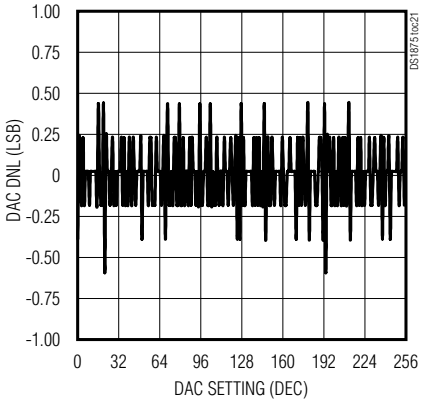
PWM DAC DNL



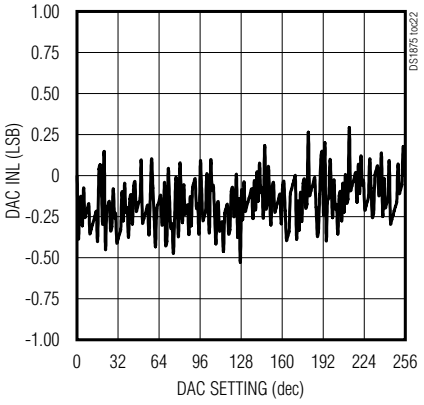
PWM DAC INL



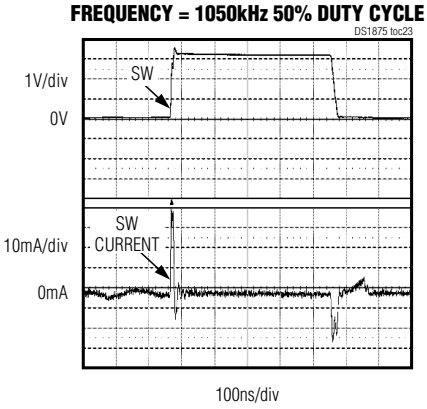
M3QT DAC DNL



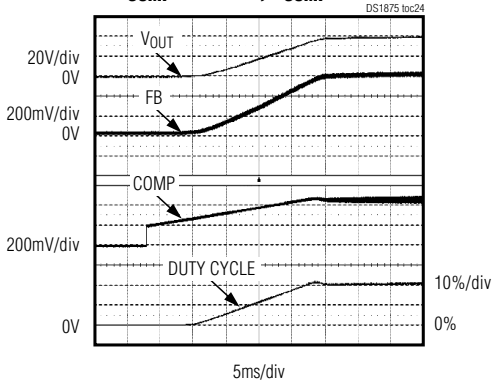
M3QT DAC INL



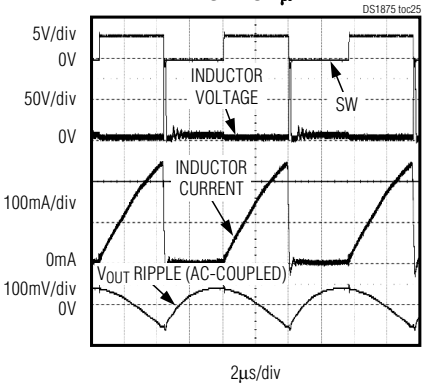
SW CURRENT INTO BSS123 FET
FREQUENCY = 1050kHz 50% DUTY CYCLE



PWM DAC CHANGING FROM 00h TO 80h
R_{COMP} = 24.3kΩ, C_{COMP} = 220nF



SWITCHING WAVEFORMS
V_{IN} = 3.3V, V_{OUT} ~ 90V, I_{OUT} ~ 1.25mA,
C2 = 0.1µF

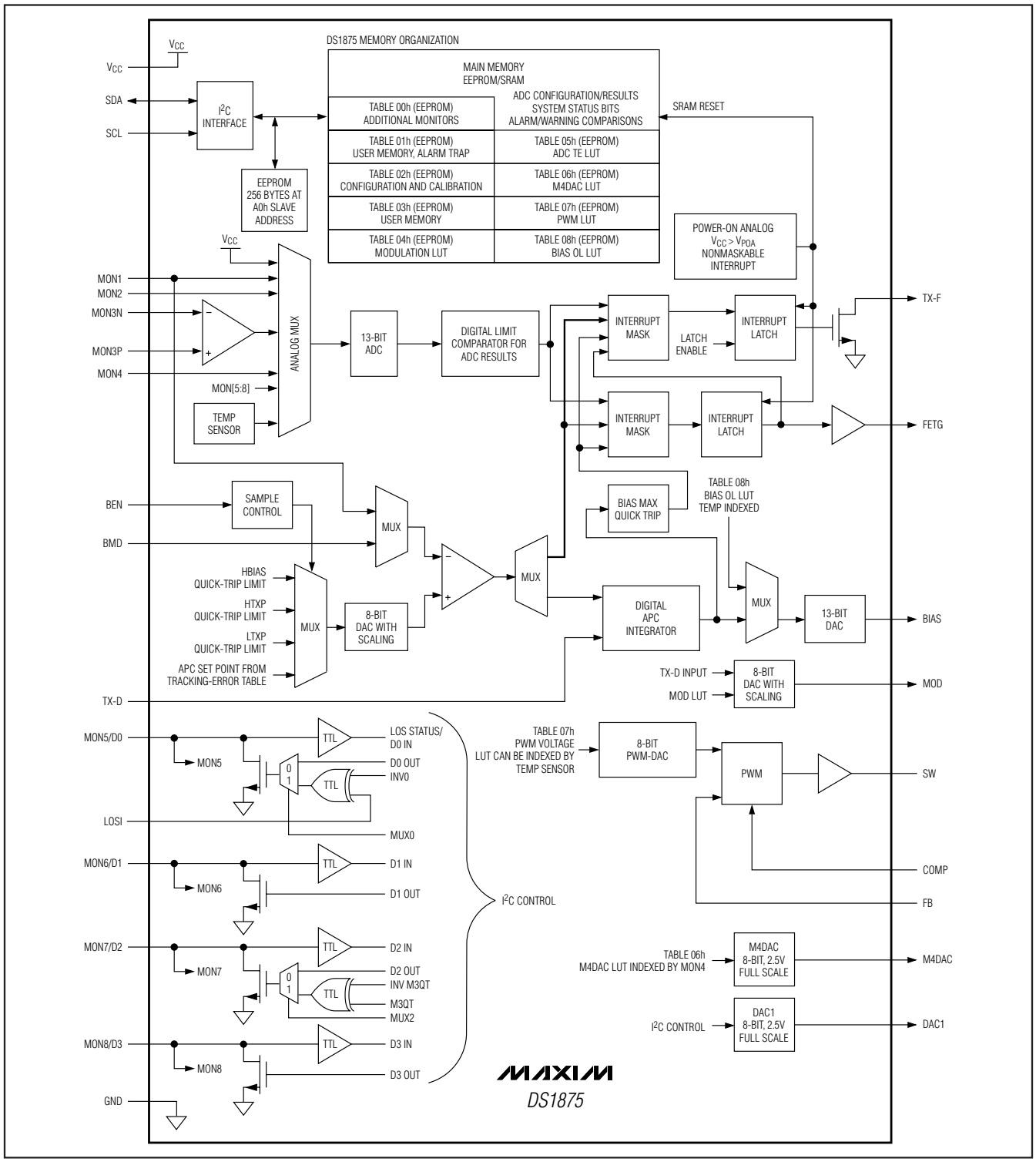


Pin Description

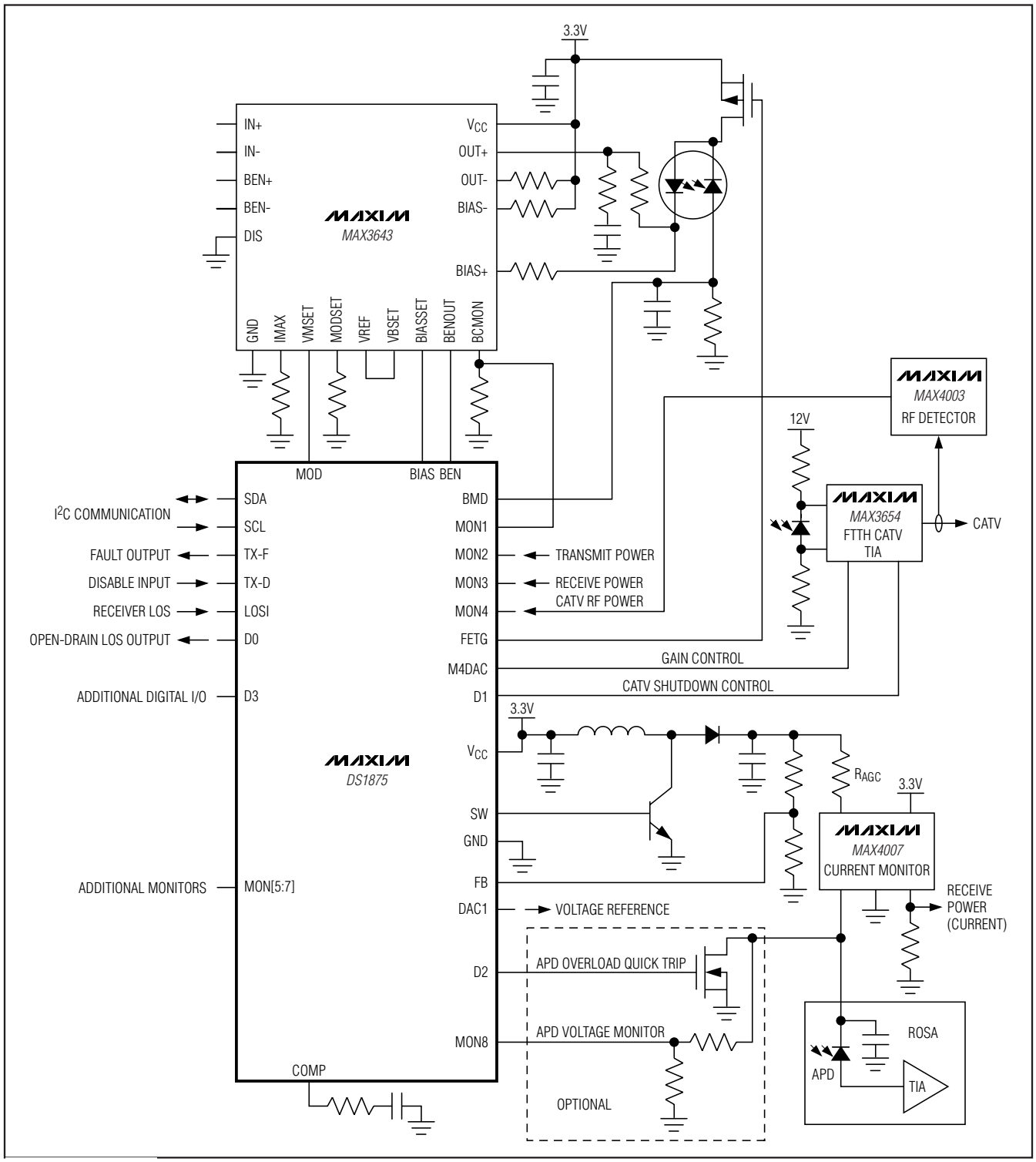
PIN	NAME	FUNCTION
1	BEN	Burst-Enable Input. Triggers the samples for the APC and quick-trip monitors.
2	SDA	I^2C Serial-Data Input/Output
3	SCL	I^2C Serial-Clock Input
4	TX-F	Transmit-Fault Output
5, 7, 11, 20, 36, 37, 38	N.C.	No Connection
6	FETG	FET Gate Output. Signals an external n-channel or p-channel MOSFET to enable/disable the laser's current.
8	TX-D	Transmit-Disable Input. Disables analog outputs.
9, 31, 35	V_{CC}	Power-Supply Input (2.85V to 3.9V)
10, 24, 32, 33	GND	Ground Connection
12	LOSI	Loss-of-Signal Input. Open-collector buffer for external loss-of-signal input. This input is accessible in the status register through the I^2C interface.
13	MON5/D0	External Monitor Input 5 or Digital I/O 0. This signal is the open-collector output driver for IN. It can also be controlled by the MUX0 and OUT0 bits. The voltage level of this pin can be read at IN0. In analog input mode, the voltage at this pin is digitized by the internal 13-bit analog-to-digital converter and can be read through the I^2C interface. Alarm and warning values can be assigned to interrupt the processor based on the ADC result.
14, 15, 16	MON6/D1, MON7/D2, MON8/D3	External Monitor Inputs 6, 7, and 8 or Digital I/O 1, 2, and 3. In digital mode, these open-collector outputs are controlled by the OUTx bits, and their voltage levels can be read at the INx bits. In analog input mode, the voltages at these pins are digitized by the internal 13-bit analog-to-digital converter and can be read through the I^2C interface. Alarm and warning values can be assigned to interrupt the processor based on the ADC result. D2 is configurable as a quick-trip output for MON3.
17, 18, 19	MON1, MON2, MON4	External Monitor Input 1, 2, and 4. The voltage at these pins is digitized by the internal 13-bit analog-to-digital converter and can be read through the I^2C interface. Alarm and warning values can be assigned to interrupt the processor based on the ADC result.
21, 22	MON3N, MON3P	External Monitor Input 3. This is a differential input that is digitized by the internal 13-bit ADC and can be read through the I^2C interface. Alarm and warning values can be assigned to interrupt the processor based on the ADC result. When used as a single-ended input, connect MON3N to ground.
23	DAC1	8-Bit DAC Output. Driven either by I^2C interface or temperature-indexed LUT.
25	M4DAC	8-Bit DAC Output for Generating Analog Voltage. Can be controlled by a LUT indexed by the voltage applied to MON4.
26	FB	Converter Feedback. Input to error amplifier. The other input to the error amplifier is an 8-bit DAC. The DAC can be driven by a temperature-indexed LUT. The output of the error amplifier is the input of the comparator used to create the PWM signal.
27	BIAS	Bias-Current Output. This 13-bit current output generates the bias current reference for the MAX3643.
28	MOD	Modulation Output Voltage. This 8-bit voltage output has eight full-scale ranges from 1.25V to 0.3125V. This pin is connected to the MAX3643's VMSET input to control the modulation current.
29	COMP	Compensation for Error Amplifier in PWM Controller
30	BMD	Back Monitor Diode Input (Feedback Voltage, Transmit Power Monitor)
34	SW	PWM Output. This is typically the switching node of a PWM converter. In conjunction with FB, a boost converter, buck converter, or analog 8-bit output can be created.
—	EP	Exposed Pad

PON Triplexer and SFP Controller

Block Diagram



Typical Operating Circuit



PON Triplexer and SFP Controller

Detailed Description

The DS1875 integrates the control and monitoring functionality required to implement a PON system using Maxim's MAX3643 compact burst-mode laser driver. The compact laser-driver solution offers a considerable cost benefit by integrating control and monitoring features in the low-power CMOS process, while leaving only the high-speed portions to the laser driver. Key components of the DS1875 are shown in the *Block Diagram* and described in subsequent sections. Table 1 contains a list of acronyms used in this data sheet.

Table 1. DS1875 Acronyms

ACRONYM	DEFINITION
10GEPON	10-Gigabit Ethernet PON
ADC	Analog-to-Digital Converter
AGC	Automatic Gain Control
APC	Automatic Power Control
APD	Avalanche Photodiode
BM	Burst Mode
BPON	Broadband PON
CATV	Cable Television
EPON	Ethernet PON
ER	Extinction Ratio
DAC	Digital-to-Analog Converter
FTTH	Fiber-to-the-Home
FTTX	Fiber-to-the-X
GEPON	Gigabit Ethernet PON
GPON	Gigabit PON
LOS	Loss of Signal
LUT	Lookup Table
TE	Tracking Error
TIA	Transimpedance Amplifier
ROSA	Receiver Optical Subassembly
RSSI	Receive Signal Strength Indicator
PON	Passive Optical Network
PWM	Pulse-Width Modulation
SFF	Small Form Factor
SFF-8472	Document Defining Register Map of SFPs and SFFs
SFP	Small Form Factor Pluggable
SFP+	Enhanced SFP
TOSA	Transmit Optical Subassembly

Bias Control

Bias current is controlled by an APC loop. The APC loop uses digital techniques to overcome the difficulties associated with controlling burst-mode systems.

Autodetect Bias Control

This is the default mode of operation. In autodetect bias control, transmit burst length is monitored. A "short burst" is declared when the burst is shorter than expected based on the sample rate setting in Table 02h, Register 88h. In the case that 32 consecutive short bursts are transmitted, the integrator is disabled and the BIAS DAC is loaded from the BIAS LUT (Table 08h). Any single burst of adequate burst length re-enables the APC integrator.

Open-Loop Bias Control

Open-loop control is configured by setting FBOL in Table 02h, Register C7h. In this mode, the BIAS LUT (Table 08h) is directly loaded to the BIAS DAC output. The BIAS LUT can be programmed in 2°C increments over the 40°C to +102°C range. It is left-shifted so that the LUT value is loaded to either the DAC MSB or the DAC MSB-1 (Bit BOLFS, Table 02h, Register 89h).

Closed-Loop Bias Control

The closed-loop control requires a burst length long enough to satisfy the sample rate settings in Table 02h, Register 88h (APC_SR[3:0]). Closed-loop control is configured by setting FBCL in Table 02h, Register C7h. In this mode, the APC integrator is enabled, which controls the BIAS DAC.

The APC loop begins by loading the value from the BIAS LUT (Table 08h) indexed by the present temperature conversion. The feedback for the APC loop is the monitor diode (BMD) current, which is converted to a voltage using an external resistor. The feedback voltage is compared to an 8-bit scaleable voltage reference, which determines the APC set point of the system. Scaling of the reference voltage accommodates the wide range in photodiode sensitivities. This allows the application to take full advantage of the APC reference's resolution.

The DS1875 has an LUT to allow the APC set point to change as a function of temperature to compensate for TE. The TE LUT (Table 05h) has 36 entries that determine the APC setting in 4°C windows between -40°C to +100°C. Ranging of the APC DAC is possible by programming a single byte in Table 02h, Register 8Dh.

DC Operation

When using autodetect mode or closed-loop mode, BEN should be equal to V_{CC} or long burst. In open-loop mode, BEN should be ground or any burst length.

Modulation Control

The MOD output is an 8-bit scaleable voltage output that interfaces with the MAX3643's VMSET input. An external resistor to ground from the MAX3643's MODSET pin sets the maximum current that the voltage at the VMSET input can produce for a given output range. This resistor value should be chosen to produce the maximum modulation current the laser type requires over temperature. Then the MOD output's scaling is used to calibrate the full-scale (FS) modulation output to a particular laser's requirements. This allows the application to take full advantage of the MOD output's resolution. The modulation LUT can be programmed in 2°C increments over the -40°C to +102°C range. Ranging of the MOD DAC is possible by programming a single byte in Table 02h, Register 8Bh.

BIAS and MOD Output During Power-Up

On power-up the modulation and bias outputs remain off until V_{CC} is above V_{POA}, a temperature conversion has been completed, and, if the V_{CC} ADC alarm is enabled, a V_{CC} conversion above the customer-defined V_{CC} low alarm level must clear the V_{CC} low alarm (t_{INIT}). Once all these conditions (t_{INIT}) are satisfied, the MOD output is enabled with the value determined by the temperature conversion and the modulation LUT (Table 04h).

When the MOD output is enabled, the BIAS output is turned on to a value equal to the temperature-indexed value in the BIAS LUT (Table 08h). Next, the APC integrator is enabled, and single LSB steps are taken to tightly control the average power.

If a fault is detected and TX-D is toggled to re-enable the outputs, the DS1875 powers up following a similar sequence to an initial power-up. The only difference is that the DS1875 already determined the present temperature, so the t_{INIT} time is not required for the DS1875 to recall the APC and MOD set points from EEPROM.

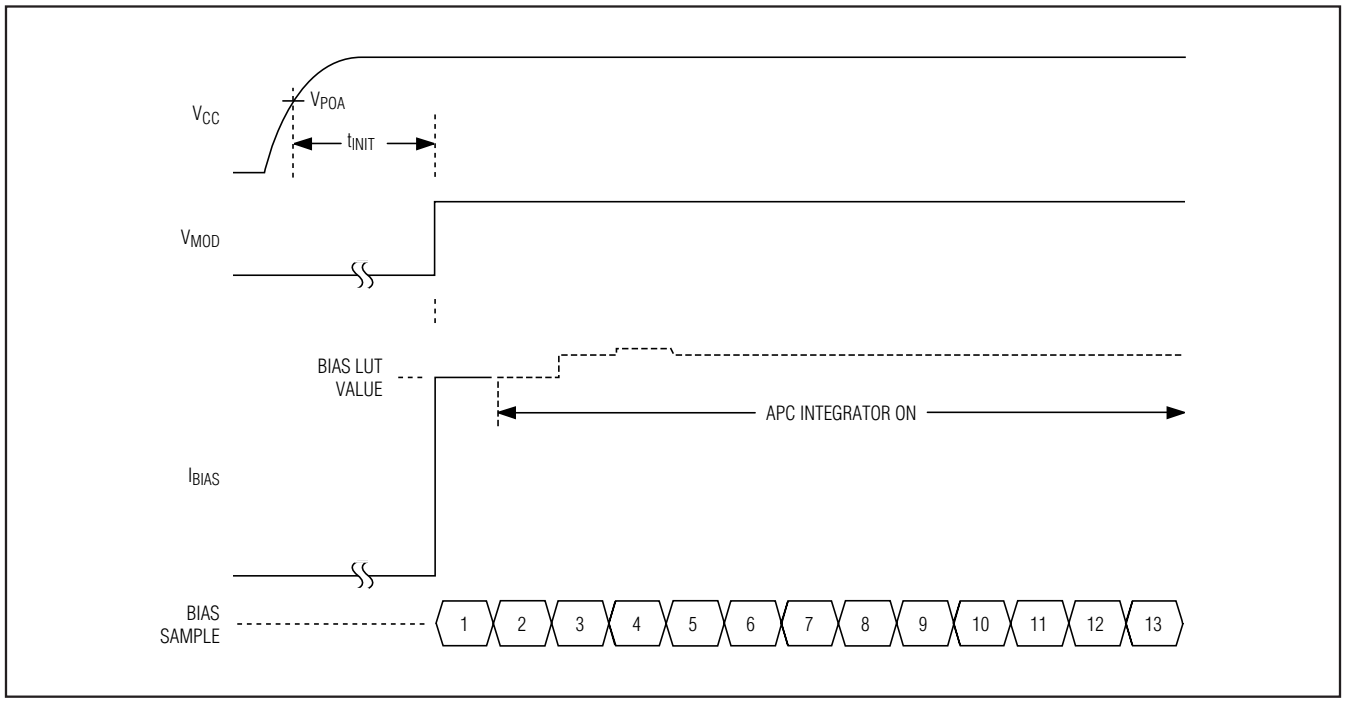


Figure 1. Power-Up Timing (BEN is a Long Burst)

BIAS and MOD Output as a Function of Transmit Disable (TX-D)

If the TX-D pin is asserted (logic 1) during normal operation, the outputs are disabled within t_{OFF}. When TX-D is deasserted (logic 0), the DS1875 turns on the MOD output with the value associated with the present temperature and initializes the BIAS using the same search algorithm used at startup. When asserted, the SOFT TX-D bit (Lower Memory, Register 6Eh) offers a software control identical to the TX-D pin (see Figure 2).

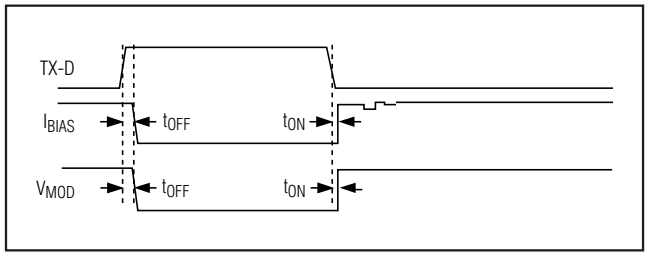


Figure 2. TX-D Timing

APC and Quick-Trip Shared Comparator Timing

As shown in Figure 3, the DS1875's input comparator is shared between the APC control loop and the three quick-trip alarms (TXP HI, TXP LO, and BIAS HI). The comparator polls the alarms in a multiplexed sequence. Six of every eight comparator readings are used for APC loop-bias current control. The other two updates are used to check the HTXP/LTXP (monitor diode voltage) and the HBIAS (MON1) signals against the internal APC and BIAS reference. If the last APC comparison was higher than the APC set point, it makes an HTXP comparison, and if it is lower, it makes an LTXP comparison. Depending on the results of the comparison, the corresponding alarms and warnings (TXP HI, TXP LO) are asserted or deasserted.

The DS1875 has a programmable comparator sample time based on an internally generated clock to facilitate a wide variety of external filtering options suitable for burst-mode transmitters. The rising edge of BEN triggers the sample to occur, and the Update Rate register (Table 02h, Register 88h) determines the sampling time. The first sample occurs (t_{FIRST}) after the rising edge of BEN. The internal clock is asynchronous to BEN, causing a ±50ns uncertainty regarding when the first sample will occur following BEN. After the first sample occurs, subsequent samples occur on a regular interval, t_{REP}. Table 2 shows the sample rate options available.

Updates to the TXP HI and TXP LO quick-trip alarms do not occur during the BEN low time. The BIAS HI quick trip can be sampled during the burst-low time. Any

Table 2. Update Rate Timing

APC_SR[3:0]	MINIMUM TIME FROM BEN TO FIRST SAMPLE (t_{FIRST}) ±50ns (ns)	REPEATED SAMPLE PERIOD FOLLOWING FIRST SAMPLE (t_{REP}) (ns)
0000b	350	800
0001b	550	1200
0010b	750	1600
0011b	950	2000
0100b	1350	2800
0101b	1550	3200
0110b	1750	3600
0111b	2150	4400
1000b	2950	6000
1001b*	3150	6400

**All codes greater than 1001b (1010b to 1111b) use the maximum sample time of code 1001b.*

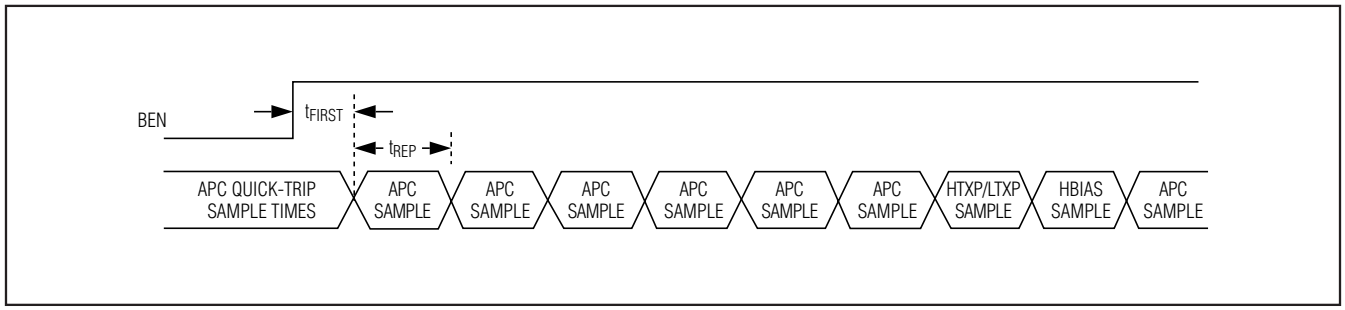


Figure 3. APC Loop and Quick-Trip Sample Timing

quick-trip alarm that is detected by default remains active until a subsequent comparator sample shows the condition no longer exists. A second bias-current monitor (BIAS MAX) compares the DS1875's BIAS DAC's code to a digital value stored in the MAX BIAS register. This comparison is made at every bias-current update to ensure that a high bias current is quickly detected.

Monitors and Fault Detection

Monitors

Monitoring functions on the DS1875 include a power-on analog (POA) V_{CC} comparison, five quick-trip comparators, and ADC channels. This monitoring combined with the interrupt masks determine if the DS1875 shuts down its outputs and triggers the TX-F and FETG outputs. All the monitoring levels and interrupt masks are user programmable with the exception of POA, which trips at a fixed range and is nonmaskable for safety reasons.

Power-On Analog (POA)

POA holds the DS1875 in reset until V_{CC} is at a suitable level ($V_{CC} > V_{POA}$) for the part to accurately measure with its ADC and compare analog signals with its quick-trip monitors. Because V_{CC} cannot be measured by the ADC when V_{CC} is less than V_{POA}, POA also asserts the V_{CC} low alarm, which is cleared by a V_{CC} ADC conversion greater than the customer-programmable V_{CC} low ADC limit. This allows a programmable limit to ensure that the head room requirements of the transceiver are satisfied during slow power-up. The TX-F and FETG outputs do not latch until there is a conversion above the V_{CC} low limit. The POA alarm is nonmaskable. The TX-F and FETG outputs are asserted when V_{CC} is below V_{POA}. See the *Low-Voltage Operation* section for more information.

Five Quick-Trip Monitors and Alarms

Five quick-trip monitors are provided to detect potential laser safety issues. These monitor:

1) High Bias Current (HBIAS)

2) Low Transmit Power (LTXP)

3) High Transmit Power (HTXP)

4) Max Output Current (BIAS MAX)

5) MON3 Quick Trip (M3QT)

The high- and low-transmit power quick-trip registers (HTXP and LTXP) set the thresholds used to compare against the BMD voltage to determine if the transmit power is within specification. The HBIAS quick trip compares the MON1 input (generally from the MAX3643 bias monitor output) against its threshold setting to determine if the present bias current is above specification. The BIAS MAX quick trip is a digital comparison that determines if the BIAS DAC indicates that the bias current is above specification. I_{BIAS} is not allowed to exceed the value set in the MAX BIAS register. When the DS1875 detects that the bias is at the limit, it sets the BIAS MAX status bit and clamps the bias current at the MAX BIAS level. In the closed-loop mode, if the recalled value from the BIAS LUT is greater than MAX BIAS then, the update is not done and I_{BIAS} reverts to the previous I_{BIAS} value. The quick trips are routed to the TX-F and FETG outputs through interrupt masks to allow combinations of these alarms to be used to trigger these outputs. When FETG is triggered, the DS1875 also disables the MOD and BIAS outputs. See the *BIAS and MOD Output During Power-Up* section for details.

MON3 Quick Trip

One additional quick trip is used to protect the APD from overcurrent. MON3P is used to monitor the current through the APD. When MON3P exceeds a threshold set by the M3QT DAC register (Table 02h, Register C3h), the PWM is shut down by blocking SW pulses. The MON3 comparison is single-ended referenced to ground. In the case where MON3 is used differentially and not referenced to ground, this must be considered when setting the MON3 quick-trip threshold. Additionally, the D2 pin can be driven either high or low as determined by INV M3QT and MUX M3QT bits in Lower Memory, Register 79h. An external switch controlled by pin D2 may be used to clamp the converter's output when MON3 quick trip occurs. This external switch discharges the output voltage much faster than allowing the load to discharge the rail. The MON3 quick-trip alarm can be latched by enabling M3QT LEN in Table 02h, Register 89h. The latch is reset by setting M3QT RESET in Lower Memory, Register 78h. A soft quick trip is performed by setting SOFT M3QT in Lower Memory, Register 78h (see Figure 4).

ADC Monitors and Alarms

The ADC monitors six channels that measure temperature (internal temp sensor), V_{CC}, and MON1–MON4 using an analog multiplexer to measure them round robin with a single ADC. Each channel has a customer-programmable full-scale range and offset value that is factory programmed to default value (see Table 3). Additionally, MON1–MON4 can right-shift results by up to 7 bits before the results are compared to alarm thresholds or read over the I^2C bus. This allows customers with specified ADC ranges to calibrate the ADC full scale to a factor of $1/2^n$ their specified range to measure small signals. The DS1875 can then right-shift the results by n bits to maintain the bit weight of their specification.

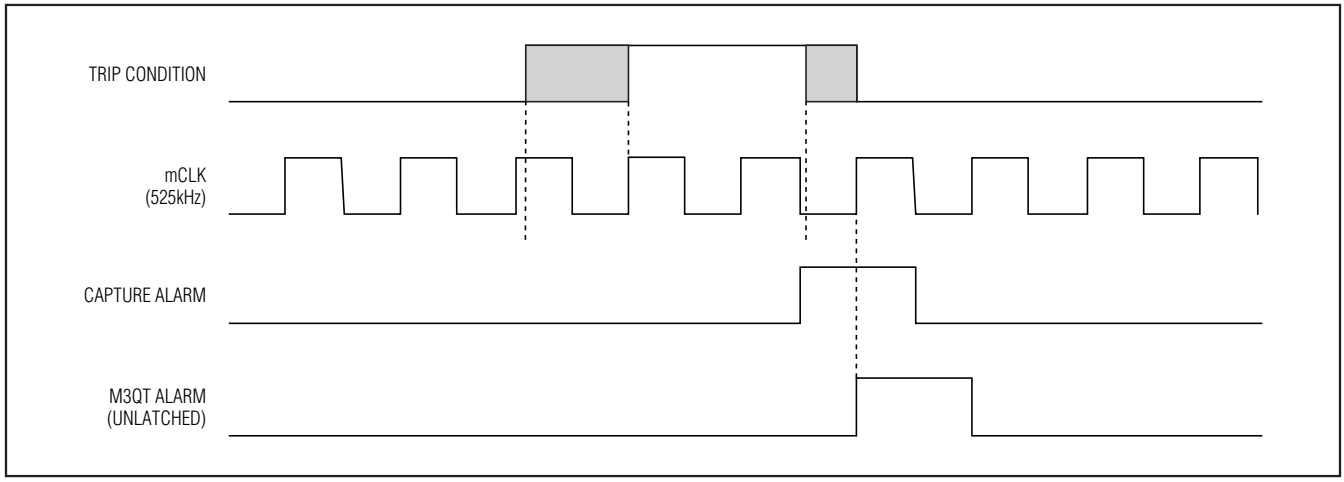


Figure 4. M3QT Timing

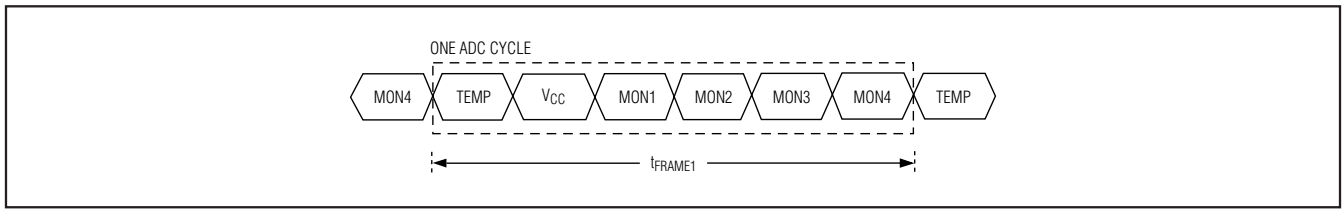


Figure 5. ADC Timing with EN5TO8B = 0

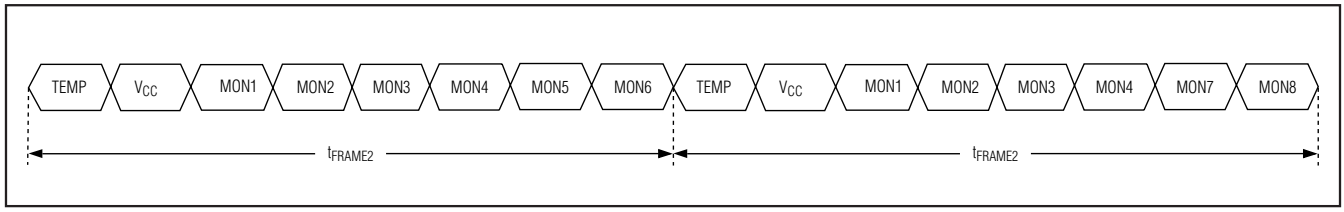


Figure 6. ADC Timing with EN5TO8B = 1

The ADC results (after right-shifting, if used) are compared to high and low alarm and warning thresholds after each conversion. The alarm values can be used to trigger the TX-F or FETG outputs. These ADC thresholds are user programmable through the I^2C interface, as well as masking registers that can be used to prevent the alarms from triggering the TX-F and FETG outputs.

Table 3. ADC Default Monitor Ranges

SIGNAL	+FS SIGNAL	+FS HEX	-FS SIGNAL	-FS HEX
Temperature (°C)	127.996	7FFF	-128	8000
V_{CC} (V)	6.5528	FFF8	0	0000
MON1–MON8 (V)	2.4997	FFF8	0	0000

ADC Timing

There are 10 analog channels that are digitized in a sequential fashion. The MON5–MON8 channels are sampled depending on the state of the EN5TO8B bit in Table 02h, Register 89h. If the bit is programmed to logic 0, the ADC cycles through temperature, V_{CC}, and MON1–MON4 (Figure 5). If the bit is programmed to logic 1, all 10 channels are digitized, including channels MON5–MON8 (Figure 6). In this mode (EN5TO8B = 0), each of MON5–MON8 is sampled on alternate cycles, as shown in Figure 5. The total time required to convert one set of channels is the sequential ADC cycle time, t_{FRAME1} or t_{FRAME2} (see Figure 6).

Right-Shifting ADC Result

If the weighting of the ADC digital reading must conform to a predetermined full-scale value defined by a standard's specification, then right-shifting can be used to adjust the predetermined full-scale analog measurement range while maintaining the weighting of the ADC results. The DS1875's range is wide enough to cover all requirements; when the maximum input value is ≤ 1/2 the FS value, right-shifting can be used to obtain greater accuracy. For instance, the maximum voltage might be 1/8th the specified predetermined full-scale value, so only 1/8th the converter's range is used. An alternative is to calibrate the ADC's full-scale range to 1/8th the readable predetermined full-scale value and use a right-shift value of 3. With this implementation, the resolution of the measurement is increased by a factor of 8, and because the result is digitally divided by 8 by right-shifting, the bit weight of the measurement still meets the standard's specification (i.e., SFF-8472).

The right-shift operation on the ADC result is carried out based on the contents of RIGHT SHIFT1/0 registers (Table 02h, Registers 8Eh–8Fh). Four analog channels, MON1–MON4, have 3 bits each allocated to set the number of right-shifts. Up to seven right-shift operations are allowed and are executed as a part of every conversion before the results are compared to the high and low alarm levels, or loaded into their corresponding measurement registers (Table 01h, Registers 62h–6Bh). This is true during the setup of internal calibration as well as during subsequent data conversions.

Transmit Fault (TX-F) Output

The TX-F output has masking registers for the ADC alarms and the QT alarms to select which comparisons cause it to assert. In addition, the FETG alarm is selectable through the TX-F mask to cause TX-F to assert. All alarms, with the exception of FETG, only cause TX-F to remain active while the alarm condition persists. However, the TX-F latch bit can enable the TX-F output to remain active until it is cleared by the TX-F reset bit, TX-D, SOFT TX-D, or by power cycling the part. If the FETG output is configured to trigger TX-F, it indicates that the DS1875 is in shutdown and requires TX-D, SOFT TX-D, or cycling power to reset. Only enabled alarms activate TX-F (see Figure 7). Table 4 shows TX-F as a function of TX-D and the alarm sources.

Table 4. TX-F as a Function of TX-D and Alarm Sources

$V_{CC} > V_{POA}$	TX-D	NONMASKED TX-F ALARM	TX-F
No	X	X	1
Yes	0	0	0
Yes	0	1	1
Yes	1	X	0

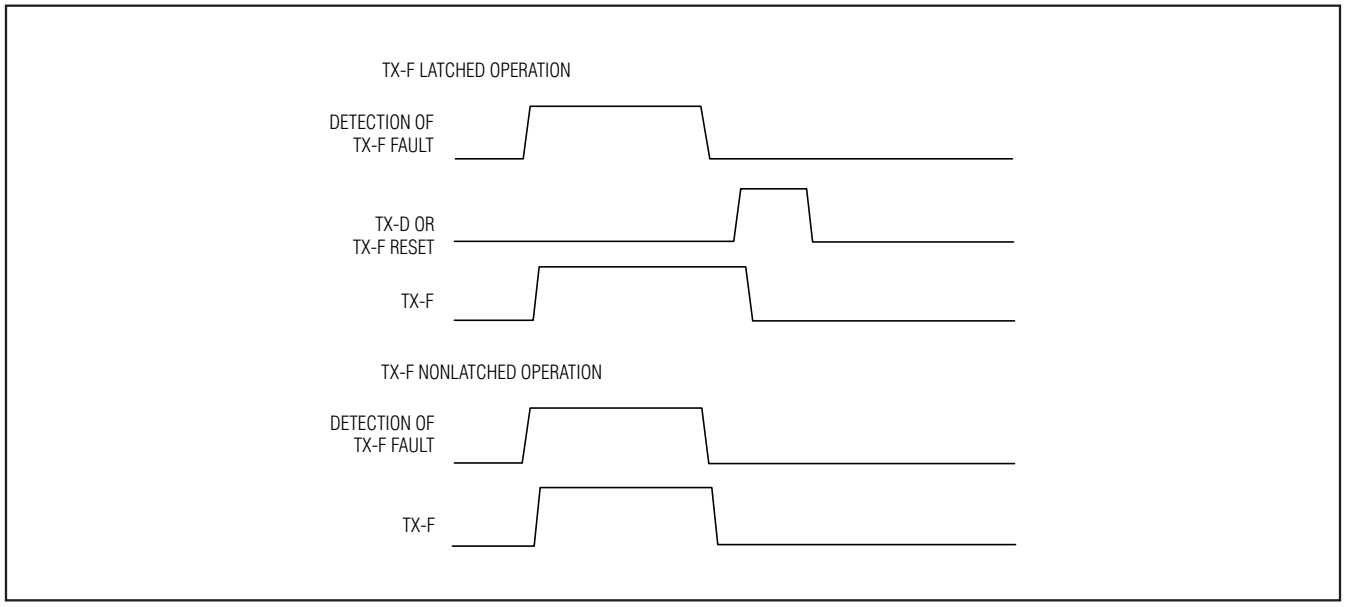


Figure 7. TX-F Timing

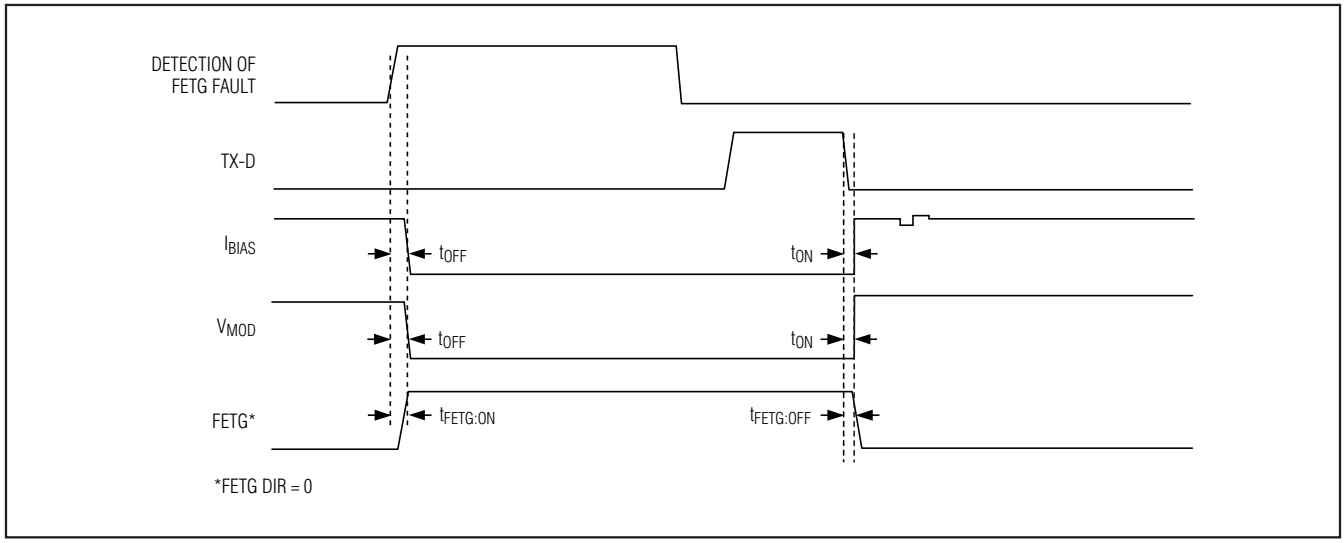


Figure 8. FETG/Output Disable Timing (Fault Condition Detected)

Safety Shutdown (FETG) Output

The FETG output has masking registers (separate from TX-F) for the ADC alarms and the QT alarms to select which comparisons cause it to assert. Unlike TX-F, the FETG output is always latched. Its output polarity is programmable to allow an external nMOS or pMOS to open during alarms to shut off the laser-diode current. If the FETG output triggers, indicating that the DS1875 is in shutdown, it requires TX-D, SOFT TX-D, or cycling power to be reset. Under all conditions, when the analog outputs are reinitialized after being disabled, all the alarms with the exception of the V_{CC} low ADC alarm are cleared. The V_{CC} low alarm must remain active to prevent the output from attempting to operate when inadequate V_{CC} exists to operate the laser driver. Once adequate V_{CC} is present to clear the V_{CC} low alarm, the outputs are enabled following the same sequence as the power-up sequence.

As previously mentioned, the FETG is an output used to disable the laser current through a series nMOS or pMOS. This requires that the FETG output can sink or source current. Because the DS1875 does not know if it should sink or source current before V_{CC} exceeds V_{POA}, which triggers the EE recall, this output is high impedance when V_{CC} is below V_{POA} (see the *Low-Voltage Operation* section for details and diagram). The application circuit should use a pullup or pulldown resistor on this pin that pulls FETG to the alarm/shutdown state (high for a pMOS, low for a nMOS). Once V_{CC} is above V_{POA}, the DS1875 pulls the FETG output to the state determined by the FETG DIR bit (Table 02h, Register 89h). Set FETG DIR to 0 if an nMOS is used and 1 if a pMOS is used.

Table 5. FETG, MOD, and BIAS Outputs as a Function of TX-D and Alarm Sources

$V_{CC} > V_{POA}$	TX-D	NONMASKED FETG ALARM	FETG	MOD AND BIAS OUTPUTS
Yes	0	0	FETG DIR	Enabled
Yes	0	1	FETG DIR	Disabled
Yes	1	X	FETG DIR	Disabled

Determining Alarm Causes Using the I²C Interface

To determine the cause of the TX-F or FETG alarm, the system processor can read the DS1875's alarm trap bytes (ATB) through the I²C interface (Table 01h, Registers F8h–FBh). The ATB has a bit for each alarm. Any time an alarm occurs, regardless of the mask bit's state, the DS1875 sets the corresponding bit in the ATB. Active ATB bits remain set until written to 0s through the I²C interface. On power-up, the ATB is 0s until alarms dictate otherwise. FETG causes additional alarms that make it difficult to determine the root cause of the problem. Therefore, no updates are made to the ATB when FETG occurs.

Die Identification

The DS1875 has an ID hard-coded to its die. Two registers (Table 02h, Registers 86h–87h) are assigned for this feature. Byte 86h reads 75h to identify the part as the DS1875; byte 87h reads the die revision.

Low-Voltage Operation

The DS1875 contains two power-on reset (POR) levels. The lower level is a digital POR (V_{POD}) and the higher level is an analog POR (V_{POA}). At startup, before the supply voltage rises above V_{POA}, the outputs are disabled (FETG and BIAS outputs are high impedance, MOD is low), all SRAM locations are low (including shadowed EEPROM (SEE)), and all analog circuitry is disabled. When V_{CC} reaches V_{POA}, the SEE is recalled, and the analog circuitry is enabled. While V_{CC} remains above V_{POA}, the device is in its normal operating state, and it responds based on its nonvolatile configuration. If during operation V_{CC} falls below V_{POA} but is still above V_{POD}, the SRAM retains the SEE settings from the first SEE recall, but the device analog is shut down and the outputs are disabled. FETG is driven to its alarm state defined by the FETG DIR bit (Table 02h, Register 89h). If the supply voltage recovers back above V_{POA}, the device immediately resumes normal functioning. When the supply voltage falls below V_{POD}, the device SRAM is placed in its default state and another SEE recall is required to reload the nonvolatile settings. The EEPROM recall occurs the next time V_{CC} exceeds V_{POA}. Figure 9 shows the sequence of events as the voltage varies.

Any time V_{CC} is above V_{POD}, the I^2C interface can be used to determine if V_{CC} is below the V_{POA} level. This is accomplished by checking the RDYB bit in the status (Lower Memory, Register 6Eh) byte. RDYB is set when V_{CC} is below V_{POA}. When V_{CC} rises above V_{POA}, RDYB is timed (within 500µs) to go to 0, at which point the part is fully functional.

For all device addresses sourced from EEPROM (Table 02h, Register 8Ch), the default device address is A2h until V_{CC} exceeds V_{POA}, allowing the device address to be recalled from the EEPROM.

Enhanced RSSI Monitoring (Dual Range Functionality)

The DS1875 offers a new feature to improve the accuracy and range of MON3, which is most commonly used for monitoring RSSI. This feature enables right-shifting (along with its gain and offset settings) when the input signal is below a set threshold (within the range that benefits using right-shifting) and then automatically disables right-shifting (recalling different gain and offset settings) when the input signal exceeds the threshold. Also, to prevent “chattering,” hysteresis prevents excessive switching between modes in addition to ensuring that continuity is maintained. Dual range operation is enabled by default (factory programmed in EEPROM). However, it can easily be disabled through the RSSI_FF and RSSI_FC bits. When dual range operation is disabled, MON3 operates identically to the other MON channels, although featuring a differential input.

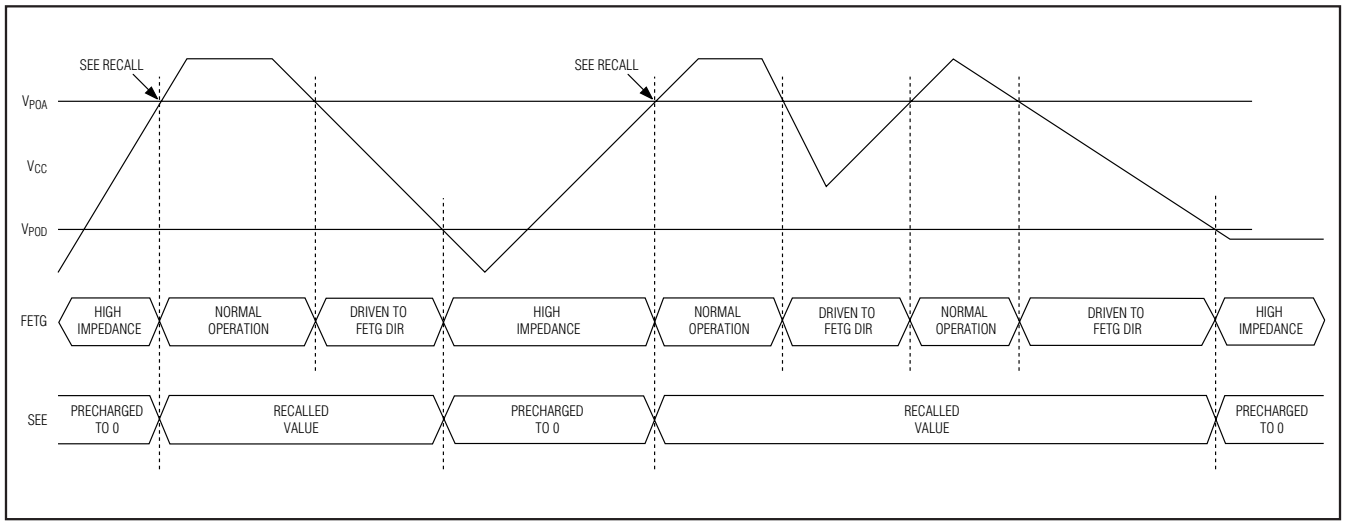


Figure 9. SEE Timing

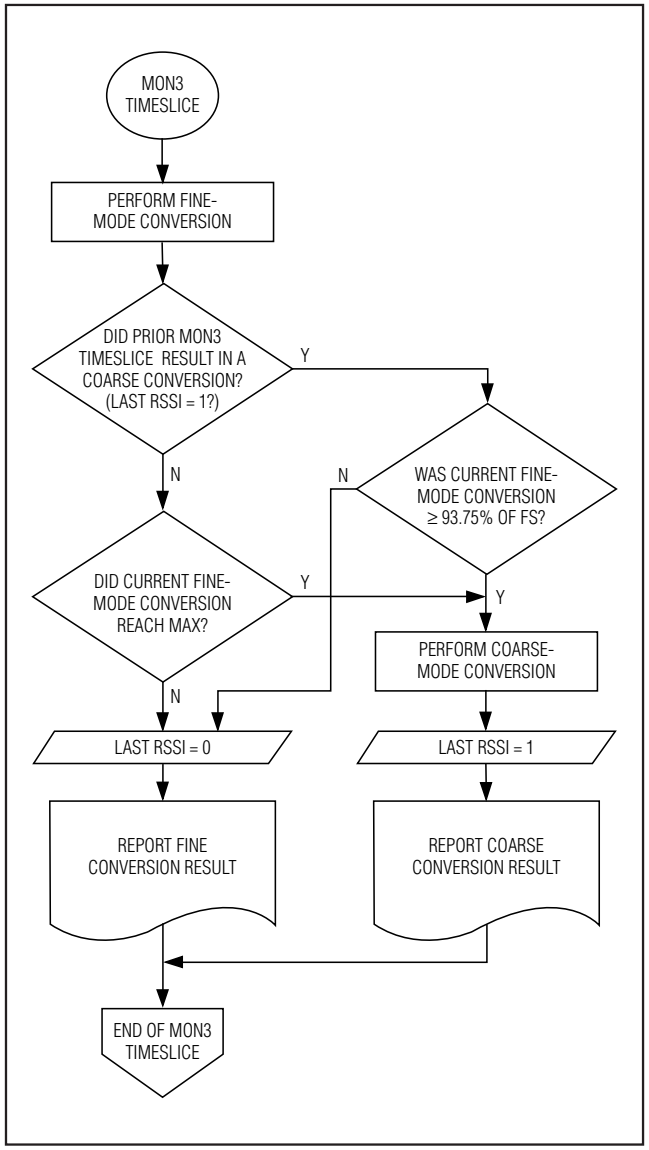


Figure 10. RSSI Flowchart

Dual-range functionality consists of two modes of operation: fine mode and coarse mode. Each mode is calibrated for a unique transfer function, hence the term, dual range. Table 6 highlights the registers related to MON3. Fine mode is equivalent to the other MON channels. Fine mode is calibrated using the gain, offset, and right-shifting registers at locations shown in Table 6 and is ideal for relatively small analog input voltages. Coarse mode is automatically switched to when the input exceeds the threshold (to be discussed in a subsequent paragraph). Coarse mode is calibrated using different gain and offset registers, but lacks right-shifting (since coarse mode is only used on large input signals). The gain and offset registers for coarse mode are also shown in Table 6. With the use of right-shifting, the fine mode full scale is programmed to (1/2N)th the coarse mode full scale. The DS1875 will now autorange to choose the range that gives the best resolution for the measurement. To eliminate chatter, 6.25% of hysteresis is applied when the input resides at the boundary of the two ranges. See Figure 10. Additional information for each of the registers can be found in the *Memory Map* section.

Dual range operation is transparent to the end user. The results of MON3 analog-to-digital conversions are still stored/reported in the same memory locations (68–69h, Lower Memory) regardless of whether the conversion was performed in fine mode or coarse mode.

When the DS1875 is powered up, analog-to-digital conversions begin in a round-robin fashion. Every MON3 timeslice begins with a fine mode analog-to-digital conversion (using fine mode's gain, offset, and right-shifting settings). See the flowchart in Figure 10. Then, depending on whether the last MON3 timeslice resulted in a coarse-mode conversion and also depending on the value of the current fine conversion, decisions are made whether to use the current fine-mode conversion result or to make an additional conversion (within the same MON3 timeslice), using coarse mode (using coarse mode's gain and offset settings, and no right-shifting) and reporting the coarse-mode result. The flowchart also illustrates how hysteresis is implemented. The fine-mode conversion is compared to one of

Table 6. MON3 Configuration Registers

REGISTER	FINE MODE	COARSE MODE
MON3 FINE SCALE	98h–99h, Table 02h	9Ch–9Dh, Table 02h
MON3 FINE OFFSET	A8h–A9h, Table 02h	ACh–ADh, Table 02h
RIGHT SHIFT0/1	8Eh–8Fh, Table 02h	—
CONFIG (RSSI_FC, RSSI_FF bits)	89h, Table 02h	
MON3 VALUE	68h–69h, Lower Memory	

Table 7. MON3 Hysteresis Threshold Values

NO. OF RIGHT-SHIFTS	FINE MODE (MAX)	COARSE MODE (MIN*)
0	FFF8h	F000h
1	7FFCh	7800h
2	3FFEh	3C00h
3	1FFFh	1E00h
4	0FFFh	0F00h
5	07FFh	0780h
6	03FFh	03C0h
7	01FFh	01E0h

**This is the minimum reported coarse-mode conversion.*

two thresholds. The actual threshold values are a function of the number of right-shifts being used. Table 7 shows the threshold values for each possible number of right-shifts.

The RSSI_FF and RSSI_FC (Table 02h, Register 89h) bits are used to force fine-mode or coarse-mode conversions, or to disable the dual-range functionality. Dual-range functionality is enabled by default (both RSSI_FC and RSSI_FF are factory programmed to 0 in EEPROM). It can be disabled by setting RSSI_FC to 0 and RSSI_FF to 1. These bits are also useful when calibrating MON3. For additional information, see the *Memory Map* section.

PWM Controller

The DS1875 has a PWM controller that, when used with external components, generates a low-noise, high-voltage output to bias APDs in optical receivers. The achievable boost voltage is determined by the external component selection. Figure 12 shows a typical schematic. Selection of switching frequency, external inductor, capacitors, resistor network, switching FET, and switch diode determine the performance of the DC-DC converter. The PWM controller can be configured in boost or buck mode. Both modes require an external nMOS or npn transistor.

The DS1875 PWM controller consists of several sections used to create a PWM signal to drive a DC-DC converter. Figure 11 is a block diagram of the DS1875 PWM controller. Following is a description of each block in the PWM controller and some guidelines for selecting components for the DC-DC converter.

The PWM DAC is used to set the desired output voltage of the DC-DC converter section. The feedback from the DC-DC converter is compared to the output from the PWM DAC by an error amplifier. If the FB level is less

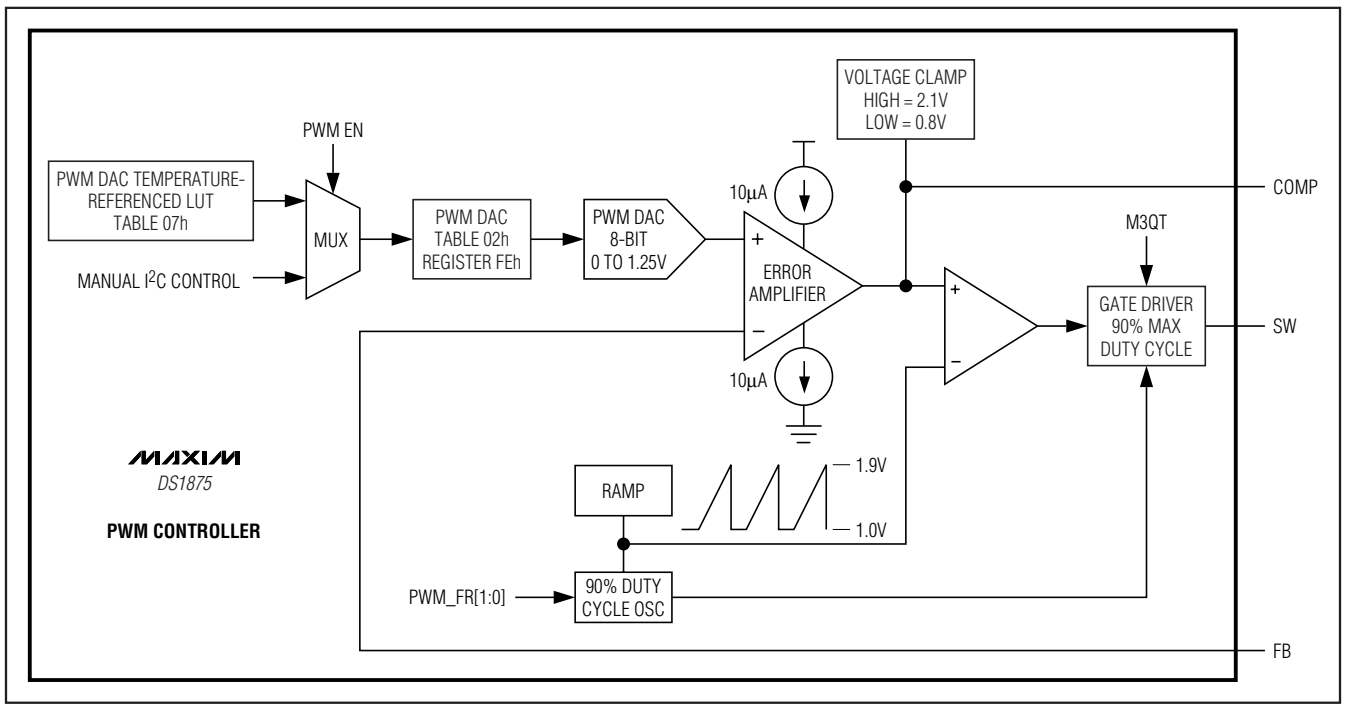


Figure 11. PWM Controller Diagram