DS1876

SFP Controller with Dual LDD Interface

General Description

The DS1876 controls and monitors all functions for dual transmitter modules. The memory map is based on SFF-8472. The DS1876 supports APC and modulation control and eye safety functionality for two laser drivers. It continually monitors for high output current, high bias current, and low and high transmit power to ensure that laser shutdown for eye safety requirements are met without adding external components. Six ADC channels monitor V_{CC}, temperature, and four external monitor inputs that can be used to meet all monitoring requirements.

Applications

Dual Tx Video SFP Modules

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
DS1876T+	-40°C to +95°C	28 TQFN-EP*
DS1876T+T&R	-40°C to +95°C	28 TQFN-EP*

+Denotes a lead(Pb)-free/RoHS-compliant package.
T&R = Tape and reel.
**EP = Exposed pad.*

Features

- **Meets All SFF-8472 Transmitter Control and Monitoring Requirements**
- **Six Analog Monitor Channels: Temperature, V_{CC}, PMON1, BMON1, PMON2, BMON2**
  - **PMON_ and BMON_ Support Internal and External Calibration**
  - **Scalable Dynamic Range**
  - **Internal Direct-to-Digital Temperature Sensor**
  - **Alarm and Warning Flags for All Monitored Channels**
- **Six Quick Trips for Fast Monitoring of Critical Functions for Laser Safety**
- **Four 10-Bit Delta-Sigma Outputs**
  - **Each Controlled by 72-Entry Temperature Lookup Table (LUT)**
- **Digital I/O Pins: Six Inputs, Five Outputs**
- **Comprehensive Fault Measurement System with Maskable Laser Shutdown Capability**
- **Flexible, Two-Level Password Scheme Provides Three Levels of Security**
- **256 Additional Bytes Located at A0h Slave Address**
- **Transmitter 1 is Accessed at A2h Slave Address**
- **Transmitter 2 is Accessed at B2h Slave Address**
- **I^2C-Compatible Interface**
- **+2.85V to +3.9V Operating Voltage Range**
- **-40°C to +95°C Operating Temperature Range**
- **28-Pin TQFN (5mm x 5mm x 0.8mm) Package**

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ABSOLUTE MAXIMUM RATINGS

Voltage Range on PMON_, BMON_, RSEL, IN1, TXF_, and TXD_ Pins Relative to Ground ....-0.5V to (V_{CC} + 0.5V)*
Voltage Range on V_{CC}, SDA, SCL, OUT1, RSELOUT, and TXFOUT Pins Relative to Ground ....-0.5V to +6V

**Subject to not exceeding +6V.*

Continuous Power Dissipation
28-Pin TQFN (derate 34.5mW/°C) above +70°C....2758.6mW
Operating Temperature Range..........................-40°C to +95°C
Programming Temperature Range .... 0°C to +95°C
Storage Temperature Range............................-55°C to +125°C
Soldering Temperature ....Refer to the IPC/JEDEC J-STD-020 Specification.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

(T_A = -40°C to +95°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Main Supply Voltage	V_{CC}	(Note 1)	+2.85		+3.9	V
High-Level Input Voltage (SDA, SCL)	$V_{IH:1}$		0.7 x V_{CC}		V_{CC} + 0.3	V
Low-Level Input Voltage (SDA, SCL)	$V_{IL:1}$		-0.3		0.3 x V_{CC}	V
High-Level Input Voltage (TXD_, TXF_, RSEL, IN1)	$V_{IH:2}$		2.0		V_{CC} + 0.3	V
Low-Level Input Voltage (TXD_, TXF_, RSEL, IN1)	$V_{IL:2}$		-0.3		+0.8	V

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = +2.85V to +3.9V, T_A = -40°C to +95°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current	I_{CC}	(Notes 1, 2)		2.5	10	mA
Output Leakage (SDA, OUT1, RSELOUT, TXFOUT)	I_{LO}				1	µA
Low-Level Output Voltage (SDA, OUT1, RSELOUT, TXDOUT_, MOD_, APC_, TXFOUT)	V_{OL}	I_{OL} = 4mA			0.4	V
		I_{OL} = 6mA			0.6	
High-Level Output Voltage (MOD_, APC_, TXDOUT_)	V_{OH}	I_{OH} = 4mA	V_{CC} - 0.4			V
TXDOUT_ Before EEPROM Recall				10	100	nA
MOD_, APC_ Before Recall		Figure 1		10	100	nA
Input Leakage Current (SCL, TXD_, RSEL, IN1, TXF_)	I_{LI}				1	µA
Digital Power-On Reset	POD		1.0		2.2	V
Analog Power-On Reset	POA		2.0		2.75	V

MOD_, APC_ ELECTRICAL CHARACTERISTICS

(V_{CC} = +2.85V to +3.9V, T_A = -40°C to +95°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Main Oscillator Frequency	f_{OSC}			5		MHz
Delta-Sigma Input-Clock Frequency	f_{DS}			f_{OSC}/2		MHz
Reference Voltage Input (REFIN)	V_{REFIN}	Minimum 0.1µF to GND	2		V_{CC}	V
Output Range			0		V_{REFIN}	V
Output Resolution		See the *Delta-Sigma Outputs* section for details			10	Bits
Output Impedance	R_{DS}			35	100	Ω

ANALOG QUICK-TRIP CHARACTERISTICS

(V_{CC} = +2.85V to +3.9V, T_A = -40°C to +95°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
TXP HI, TXP LO Full-Scale Voltage				2.507		V
HBIAS Full-Scale Voltage				1.25		V
PMON_ Input Resistance			35	50	65	kΩ
Resolution				8		Bits
Error		T_A = +25°C		±2		%FS
Integral Nonlinearity			-1		+1	LSB
Differential Nonlinearity			-1		+1	LSB
Temperature Drift			-2.5		+2.5	%FS
Offset			-5		+10	mV

ANALOG VOLTAGE MONITORING CHARACTERISTICS

(V_{CC} = +2.85V to +3.9V, T_A = -40°C to +95°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ADC Resolution				13		Bits
Input/Supply Accuracy (BMON_, PMON_, V_{CC})	ACC	At factory setting		0.25	0.5	%FS
Update Rate for Temperature, BMON_, PMON_, V_{CC}	t_{RR}			64	78	ms
Input/Supply Offset (BMON_, PMON_, V_{CC})	V_{OS}	(Note 3)		0	5	LSB
Factory Setting (Note 4)		BMON_, PMON_		2.5		V
		V_{CC}		6.5536		

DIGITAL THERMOMETER CHARACTERISTICS

(V_{CC} = +2.85V to +3.9V, T_A = -40°C to +95°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Thermometer Error	T_{ERR}	-40°C to +95°C	-3		+3	°C

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = +2.85V to +3.9V, T_A = -40°C to +95°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
TXD_ Enable	t_{OFF}	From ⊠ TXD_			5	µs
Recovery from TXD_ Disable (Figure 2)	t_{ON}	From ⊠ TXD_			1	ms
Fault Reset Time (to TXFOUT = 0)	t_{INITR1}	From ⊠ TXD_		131		ms
	t_{INITR2}	On power-up or ⊠ TXD_, when VCC LO alarm is detected (Note 5)		161		
Fault Assert Time (to TXFOUT = 1)	t_{FAULT}	After HTXP_, LTXP_, HBATH_	1.6		10.5	µs

QUICK-TRIP TIMING CHARACTERISTICS

(V_{CC} = +2.85V to +3.9V, T_A = -40°C to +95°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output-Enable Time Following POA	t_{INIT}			20		ms
Sample Time per Quick-Trip Comparison	t_{REP}			1.6		µs

I²C AC ELECTRICAL CHARACTERISTICS

(V_{CC} = +2.85V to +3.9V, T_A = -40°C to +95°C, timing referenced to $V_{IL(MAX)}$ and $V_{IH(MIN)}$, unless otherwise noted. See the *I²C Communication* section.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SCL Clock Frequency	f_{SCL}	(Note 6)	0		400	kHz
Clock Pulse-Width Low	t_{LOW}		1.3			µs
Clock Pulse-Width High	t_{HIGH}		0.6			µs
Bus Free Time Between STOP and START Condition	t_{BUF}		1.3			µs
START Hold Time	$t_{HD:STA}$		0.6			µs
START Setup Time	$t_{SU:STA}$		0.6			µs
Data Out Hold Time	$t_{HD:DAT}$		0		0.9	µs
Data In Setup Time	$t_{SU:DAT}$		100			ns
Rise Time of Both SDA and SCL Signals	t_R	(Note 7)	20 + $0.1C_B$		300	ns
Fall Time of Both SDA and SCL Signals	t_F	(Note 7)	20 + $0.1C_B$		300	ns
STOP Setup Time	$t_{SU:STO}$		0.6			µs
Capacitive Load for Each Bus Line	C_B				400	pF
EEPROM Write Time	t_{WR}	(Note 8)			20	ms

NONVOLATILE MEMORY CHARACTERISTICS

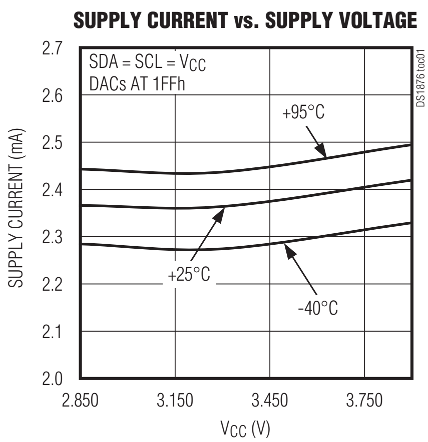
(V_{CC} = +2.85V to +3.9V, unless otherwise noted.)

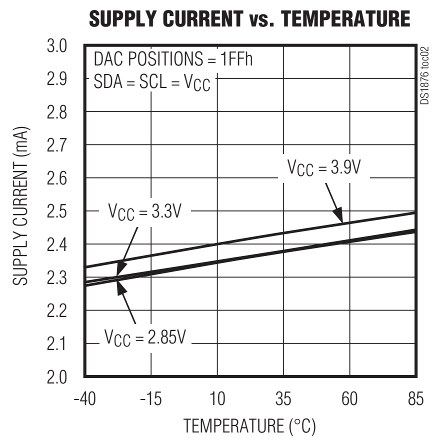
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
EEPROM Write Cycles		At +25°C	200,000			
		At +85°C	50,000			

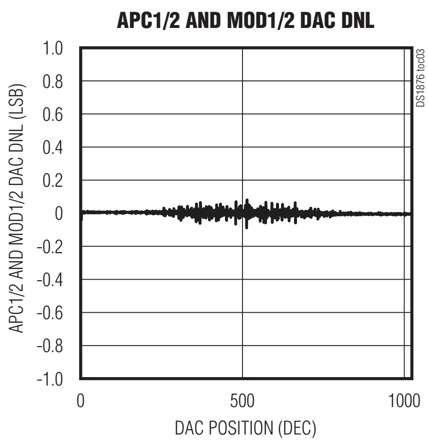
Note 1: All voltages are referenced to ground. Current into the IC is positive, and current out of the IC is negative.
Note 2: Inputs are at supply rail. Outputs are not loaded.
Note 3: This parameter is guaranteed by design.
Note 4: Full scale is user programmable.
Note 5: A temperature conversion is completed and MOD1 DAC, MOD2 DAC, APC1 DAC, and APC2 DAC values are recalled from the LUT and V_{CC} has been measured to be above VCC LO alarm, if the VCC LO alarm is enabled.
Note 6: I^2C interface timing shown is for fast-mode (400kHz) operation. This device is also backward compatible with I^2C standard mode.
Note 7: C_B—Total capacitance of one bus line in pF.
Note 8: EEPROM write begins after a STOP condition occurs.

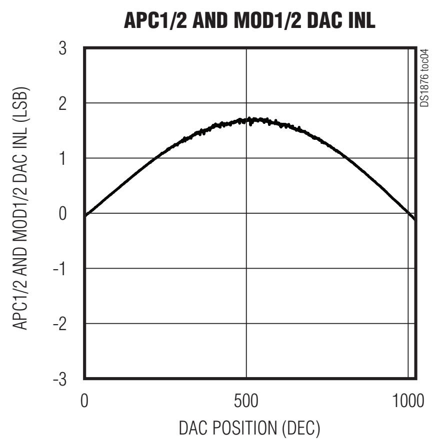
Typical Operating Characteristics

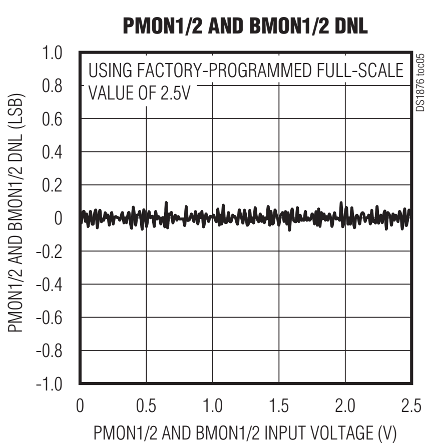
(V_{CC} = 3.3V, T_A = +25°C, unless otherwise noted.)

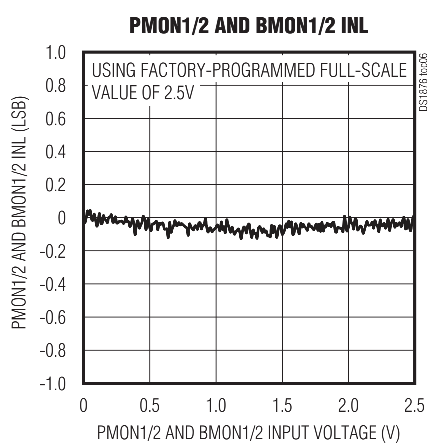




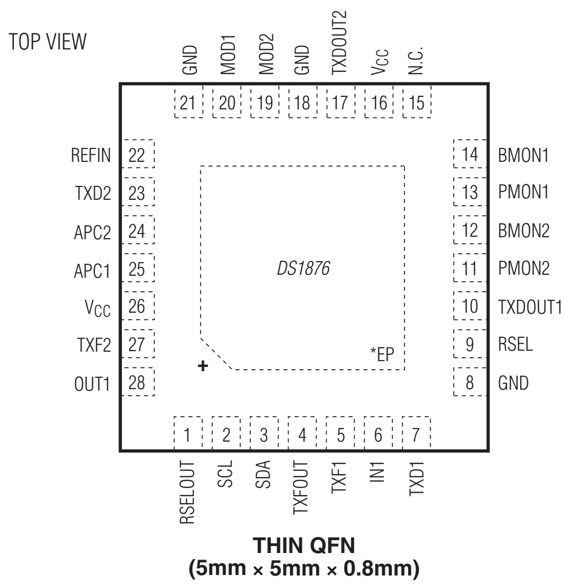








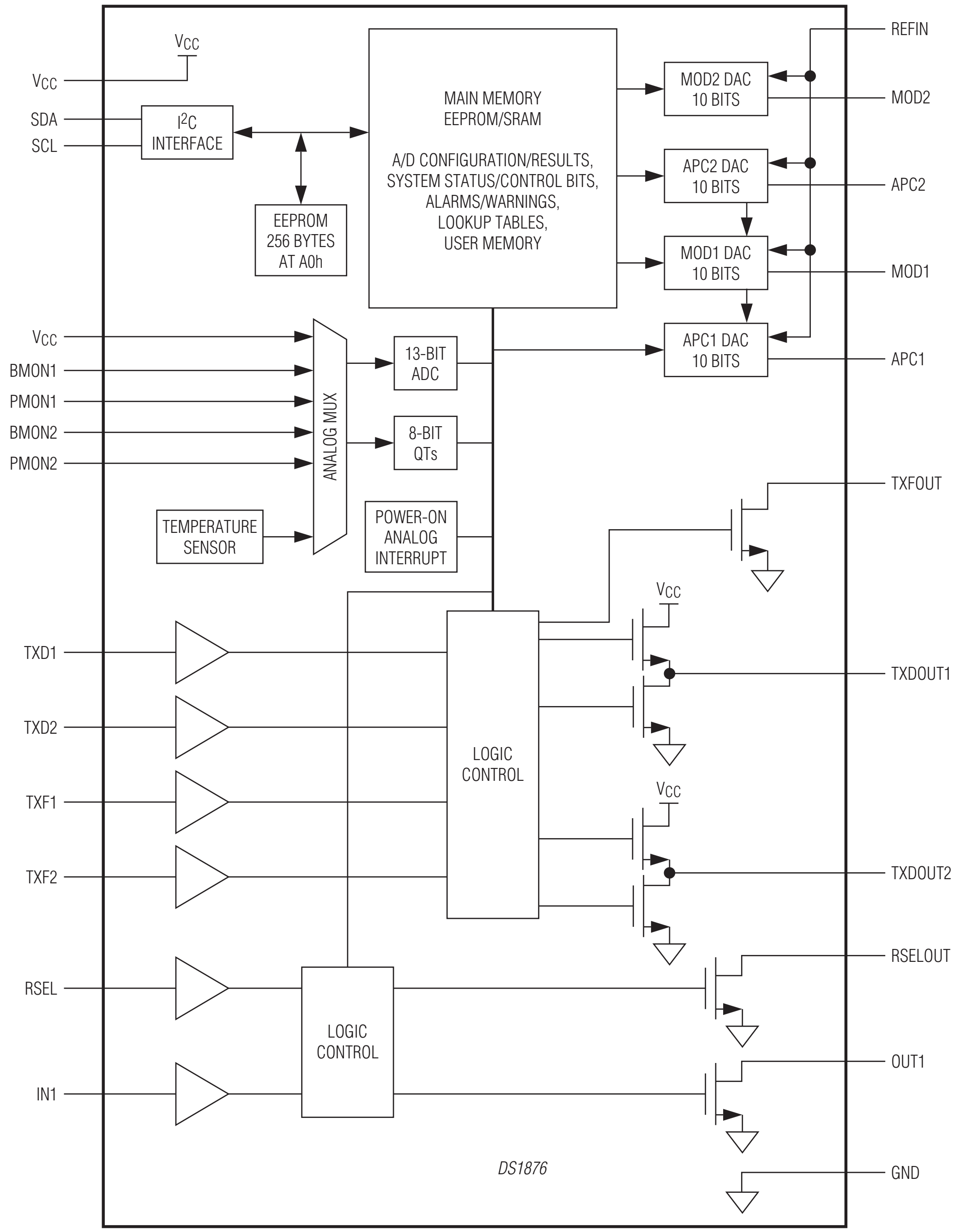
Pin Configuration



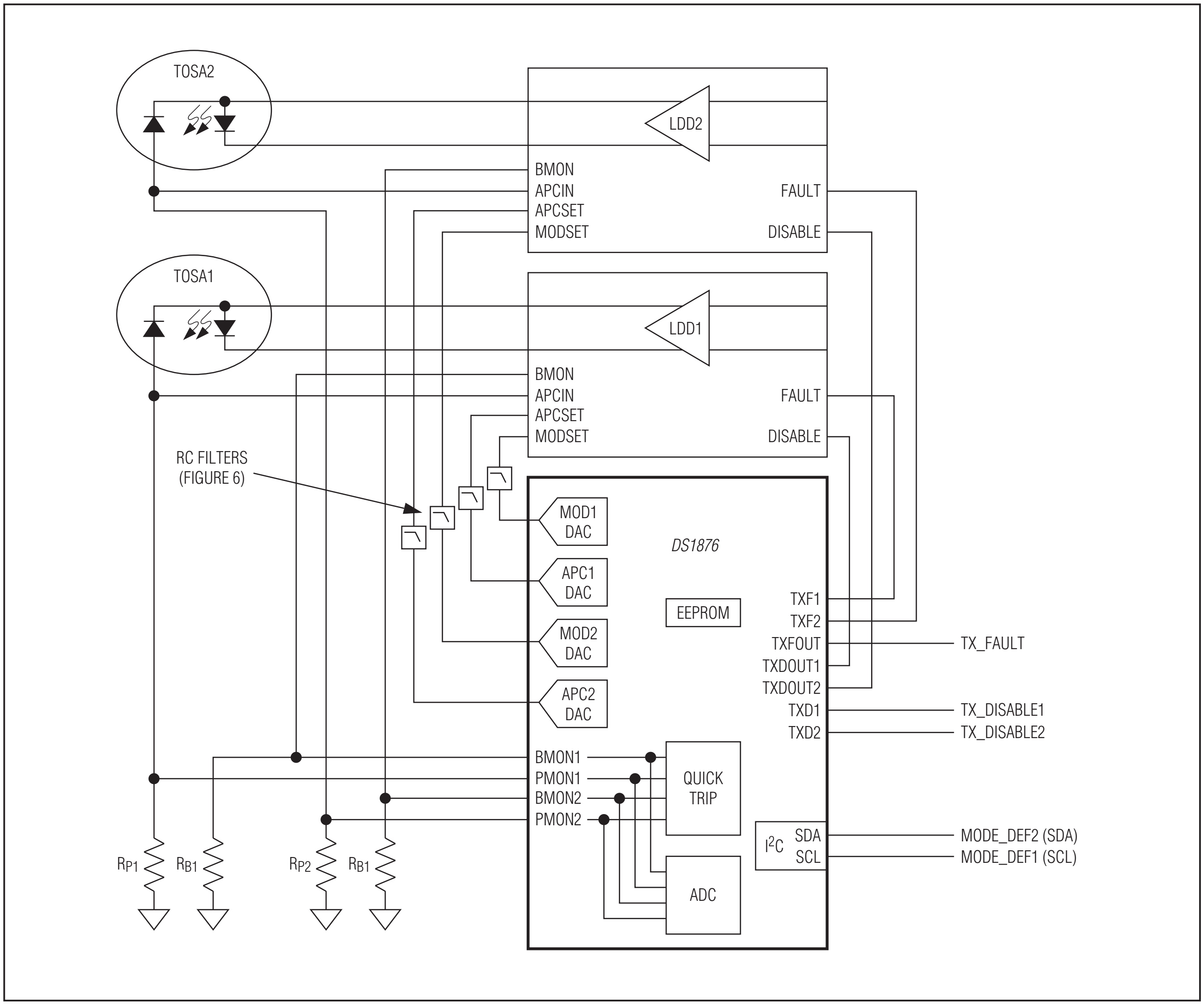
Pin Description

PIN	NAME	FUNCTION
1	RSELOUT	Rate-Select Output
2	SCL	I²C Serial-Clock Input
3	SDA	I²C Serial-Data Input/Output
4	TXFOUT	Transmit Fault Output, Open Drain
5	TXF1	Transmit Fault Input 1
6	IN1	Digital Input. General-purpose input, AS1 in SFF-8079, or RS1 in SFF-8431.
7	TXD1	Transmit Disable Input 1
8, 18, 21	GND	Ground Connection
9	RSEL	Rate-Select Input
10	TXDOUT1	Transmit Disable Output 1
11	PMON2	External Monitor Input PMON2 and HTXP2/LTXP2 Quick Trip
12	BMON2	External Monitor Input BMON2 and HBATH2 Quick Trip
13	PMON1	External Monitor Input PMON1 and HTXP1/LTXP1 Quick Trip
14	BMON1	External Monitor Input BMON1 and HBATH1 Quick Trip
15	N.C.	No Connection
16, 26	V_{CC}	Power-Supply Input
17	TXDOUT2	Transmit Disable Output 2
19	MOD2	MOD2 DAC, Delta-Sigma Output
20	MOD1	MOD1 DAC, Delta-Sigma Output
22	REFIN	Reference Input for DAC1 and DAC2
23	TXD2	Transmit Disable Input 2
24	APC2	APC2 DAC, Delta-Sigma Output
25	APC1	APC1 DAC, Delta-Sigma Output
27	TXF2	Transmit Fault Input 2
28	OUT1	Digital Output. General-purpose output, AS1 output in SFF-8079, or RS1 output in SFF-8431.
—	EP	Exposed Pad (Connect to GND)

Block Diagram



Typical Operating Circuit



Detailed Description

The DS1876 integrates the control and monitoring functionality required in a dual transmitter system. Key components of the DS1876 are shown in the *Block Diagram* and described in subsequent sections.

DACs During Power-Up

On power-up, the DS1876 sets the DACs to high impedance. After time t_{INIT}, the DACs are set to an initial condition set in EEPROM. After a temperature conversion is completed and if the VCC LO alarm is enabled, an additional V_{CC} conversion above the customer-defined VCC LO alarm level is required before the DACs are updated with the value determined by the temperature conversion and the DAC LUT.

If a fault is detected, and TXD1 and TXD2 are toggled to re-enable the outputs, the DS1876 powers up following a similar sequence to an initial power-up. The

Table 1. Acronyms

ACRONYM	DESCRIPTION
ADC	Analog-to-Digital Converter
AGC	Automatic Gain Control
APC	Automatic Power Control
APD	Avalanche Photodiode
ATB	Alarm Trap Bytes
DAC	Digital-to-Analog Converter
LOS	Loss of Signal
LUT	Lookup Table
NV	Nonvolatile
QT	Quick Trip
TE	Tracking Error
TIA	Transimpedance Amplifier
ROSA	Receiver Optical Subassembly
SEE	Shadowed EEPROM
SFF	Small Form Factor
SFF-8472	Document Defining Register Map of SFPs and SFFs
SFP	Small Form Factor Pluggable
SFP+	Enhanced SFP
TOSA	Transmit Optical Subassembly
TXP	Transmit Power

only difference is that the DS1876 already has determined the present temperature, so the t_{INIT} time is not required for the DS1876 to recall the APC and MOD set points from EEPROM. See Figure 1.

DACs as a Function of Transmit Disable (TXD1, TXD2)

If TXD1 or TXD2 are asserted (logic 1) during normal operation, the associated outputs are disabled within t_{OFF}. When TXD1 or TXD2 are deasserted (logic 0), the DS1876 sets the DACs with the value associated with the present temperature. When asserted, soft TXD1 or soft TXD2 (TXDC) (Lower Memory, Register 6Eh) would allow a software control identical to the TXD1 or TXD2 pin (Figure 2). The POLARITY register (Table 02h, Register C6h) determines if the off-state value of the DACs is V_{REFIN} or 0V.

Quick-Trip Timing

As shown in Figure 3, the DS1876's input comparator is shared among the six quick-trip alarms (TXP1 HI, TXP1 LO, TXP2 HI, TXP2 LO, BIAS1 HI, and BIAS2 HI). The comparator polls the alarms in a multiplexed sequence. The updates are used to compare the HTXP1, LTXP1, HTXP2, and LTXP2 (monitor diode voltages) and the HBATH1 and HBATH2 (BMON1, BMON2) signals against the internal APC and BIAS reference, respectively. Depending on the results of the comparison, the

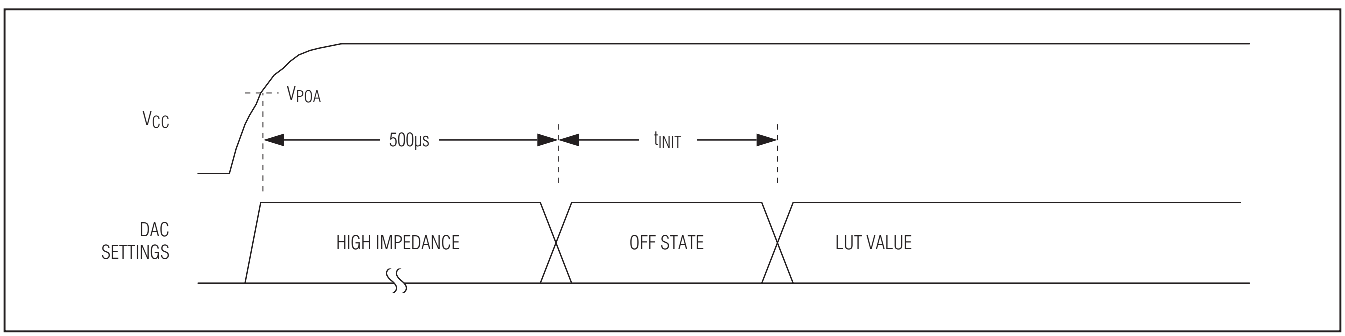


Figure 1. Power-Up Timing

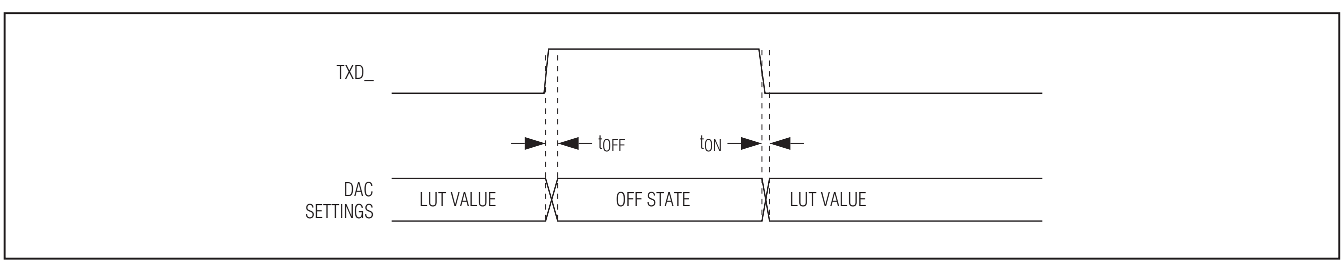


Figure 2. TXD1, TXD2 Timing

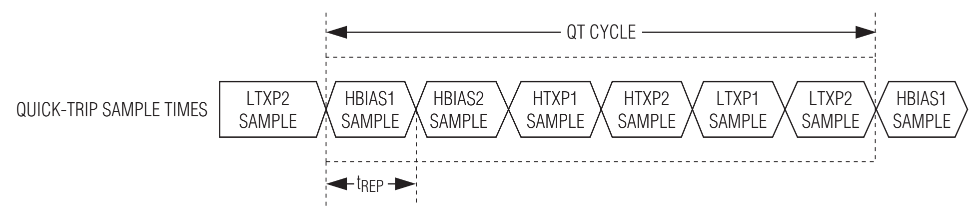


Figure 3. Quick-Trip Sample Timing

Table 2. ADC Default Monitor Full-Scale Ranges

SIGNAL (UNITS)	+FS SIGNAL	+FS HEX	-FS SIGNAL	-FS HEX
Temperature (°C)	127.996	7FFF	-128	8000
V_{CC} (V)	6.5528	FFF8	0	0000
PMON1, PMON2 and BMON1, BMON2 (V)	2.4997	FFF8	0	0000

corresponding alarms and warnings (TXP HI1, TXP LO1, TXP HI2, TXP LO2, BIAS HI1, and BIAS HI2) are asserted or deasserted.

After resetting, the device completes one QT cycle before making comparisons. The TXP LO quick-trip alarm updates its alarm bit, but does not create FETG until after TXD_{EXT}. TXP HI and BIAS HI can also be configured to wait for TXD_{EXT}; however, this can be disabled using QTHEXT_ (Table 02h, Register 88h).

Monitors and Fault Detection

Monitors

Monitoring functions on the DS1876 include six quick-trip comparators and six ADC channels. This monitoring combined with the alarm enables (Table 01h/05h) determines when/if the DS1876 turns off DACs and triggers the TXFOUT and TXDOUT1, TXDOUT2 outputs. All the monitoring levels and interrupt masks are user programmable.

Six Quick-Trip Monitors and Alarms

Six quick-trip monitors are provided to detect potential laser safety issues and LOS status. These monitor the following:

1) High Bias Current 1 (HBATH1), causing QT BIAS1 HI
2) Low Transmit Power 1 (LTXP1), causing QT TXP1 LO
3) High Transmit Power 1 (HTXP1), causing QT TXP1 HI
4) High Bias Current 2 (HBATH2), causing QT BIAS2 HI
5) Low Transmit Power 2 (LTXP2), causing QT TXP2 LO
6) High Transmit Power 2 (HTXP2), causing QT TXP2 HI

The high and low transmit power quick-trip registers (HTXP1, HTXP2, LTXP1, and LTXP2) set the thresholds used to compare against the PMON1 and PMON2 voltages to determine if the transmit power is within specification. The HBATH1 and HBATH2 QTs compare the BMON1 and BMON2 inputs (generally from the laser driver's bias monitor output) against their threshold settings to determine if the present bias current is above specification. The bias and power QTs are routed to FETG through interrupt masks to allow combinations of these alarms to be used to trigger FETG. The bias and power QTs are directly connected to TXFOUT (see Figure 9). The user can program up to eight different temperature-indexed threshold levels for HBATH1 and HBATH2 (Table 06h, Registers E0h–E7h).

Six ADC Monitors and Alarms

The ADC monitors six channels that measure temperature (internal temp sensor), V_{CC}, PMON1, PMON2, BMON1, and BMON2 using an analog multiplexer to measure them round-robin with a single ADC (see the *ADC Timing* section). The channels have a customer-programmable full-scale range, and all channels have a customer-programmable offset value that is factory programmed to a default value (see Table 2). Additionally, PMON1, PMON2 and BMON1, BMON2 can right-shift results by up to 7 bits before the results are compared to alarm thresholds or read over the I^2C bus. This allows customers with specified ADC ranges to calibrate the ADC full scale to a factor of $1/2^n$ of their specified range to measure small signals. The DS1876 can then right-shift the results by n bits to maintain the bit weight of their specification.

The ADC results (after right-shifting, if used) are compared to the alarm and warning thresholds after each conversion, and the corresponding alarms are set that can be used to trigger the TXFOUT output. These ADC thresholds are user programmable, as are the masking registers that can be used to prevent the alarms from triggering the TXFOUT output.

ADC Timing

There are six analog channels that are digitized in a round-robin fashion in the order as shown in Figure 4. The total time required to convert all six channels is t_{RR} (see the *Analog Voltage Monitoring Characteristics* table for details).

Right-Shifting ADC Result

If the weighting of the ADC digital reading must conform to a predetermined full-scale (PFS) value defined by a standard's specification (e.g., SFF-8472), then right-shifting can be used to adjust the PFS analog measurement range while maintaining the weighting of the ADC results. The DS1876's range is wide enough to cover all requirements; when the maximum input value is ≤ 1/2 the FS value, right-shifting can be used to obtain greater accuracy. For instance, the maximum voltage might be 1/8 the specified PFS value, so only 1/8 of the converter's range is effective over this range. An alternative is to calibrate the ADC's full-scale range to 1/8 the readable PFS value and use a right-shift value of 3. With this implementation, the resolution of the measurement is increased by a factor of 8, and because the result is digitally divided by 8 by right-shifting, the bit weight of the measurement still meets the standard's specification (i.e., SFF-8472).

The right-shift operation on the ADC result is carried out based on the contents of right-shift control registers (Table 02h, Registers 8Eh–8Fh) in EEPROM. Four analog channels—PMON1, PMON2, BMON1, and BMON2—each have 3 bits allocated to set the number of right-shifts. Up to seven right-shift operations are allowed and are executed as a part of every conversion before the results are compared to the high and low alarm levels, or loaded into their corresponding measurement registers (Lower Memory, Registers 64h–6Bh). This is true during the setup of internal calibration as well as during subsequent data conversions.

Low-Voltage Operation

The DS1876 contains two power-on reset (POR) levels. The lower level is a digital POR (POD) and the higher level is an analog POR (POA). At startup, before the supply voltage rises above POA, the outputs are disabled, all SRAM locations are set to their defaults, shadowed EEPROM (SEE) locations are zero, and all analog circuitry is disabled. When V_{CC} reaches POA, the SEE is recalled, and the analog circuitry is enabled. While V_{CC} remains above POA, the device is in its normal operating state, and it responds based on its nonvolatile configuration. If during operation V_{CC} falls below POA, but is still above POD, the SRAM retains the SEE settings from the first SEE recall, but the device analog is shut down and the outputs disabled. If the supply voltage recovers back above POA, the device immediately resumes normal operation. If the supply voltage falls below POD, the device SRAM is placed in its default state and another SEE recall is required to reload the nonvolatile settings. The EEPROM recall occurs the next time V_{CC} next exceeds POA. Figure 5 shows the sequence of events as the voltage varies.

Any time V_{CC} is above POD, the I^2C interface can be used to determine if V_{CC} is below the POA level. This is accomplished by checking the RDYB bit in the status byte (Lower Memory, Register 6Eh). RDYB is set when V_{CC} is below POA; when V_{CC} rises above POA, RDYB is timed (within 500μs) to go to 0, at which point the part is fully functional.

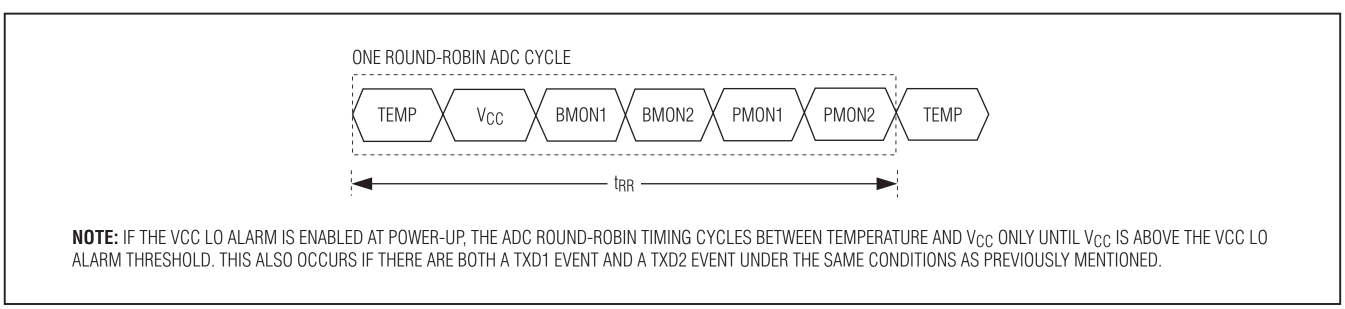


Figure 4. ADC Round-Robin Timing

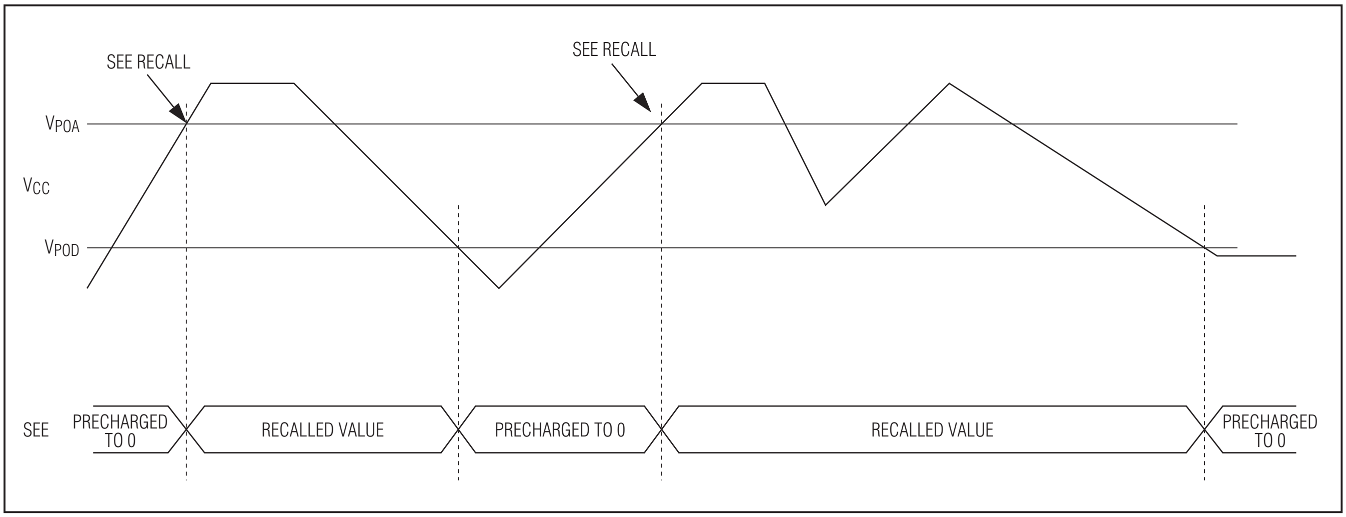


Figure 5. Low-Voltage Hysteresis Example

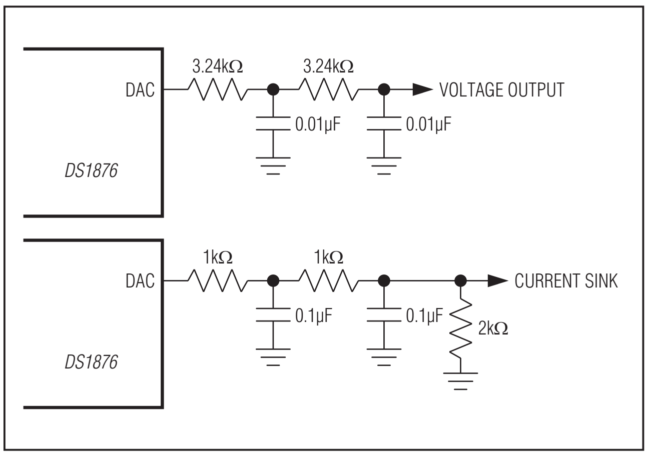


Figure 6. Recommended RC Filter for DAC Outputs in Voltage Mode and Current Sink Mode

For all device addresses sourced from EEPROM (Table 02h, Register 8Bh), the default device addresses are A2h and B2h until V_{CC} exceeds POA allowing the device address to be recalled from the EEPROM.

Delta-Sigma Outputs

Four delta-sigma outputs are provided: MOD1, MOD2, APC1, and APC2. With the addition of an external RC filter, these outputs provide 10-bit resolution analog outputs with the full-scale range set by the input REFIN. Each output is either manually controlled or controlled using a temperature-indexed LUT.

A delta-sigma DAC has a digital output using pulse-density modulation. It provides much lower output ripple than a standard digital PWM output given the same clock rate and filter components. Before t_{INIT}, the DAC outputs are high impedance. The external RC filter components are chosen based on ripple requirements, output load, delta-sigma frequency, and desired response time. Figure 6 shows a recommended filter.

For illustrative purposes, a 3-bit example is provided in Figure 7.

In LUT mode the DACs are each controlled by an LUT with high-temperature resolution and an OFFSET LUT with lower temperature resolution. The high-resolution LUTs each have 2°C resolutions. The OFFSET LUTs are located in the upper eight registers (F8h–FFh) of the table containing each high-resolution LUT. The DAC values are determined as follows:

DAC value = LUT + 4 x (OFFSET LUT)

An example calculation for MOD1 DAC is as follows:

Assumptions:

1) Temperature is +43°C
2) Table 04h (MOD1 OFFSET LUT), Register FCh = 2Ah
3) Table 04h (MOD1 LUT), Register AAh = 7Bh

Because the temperature is +43°C, the MOD1 LUT index is AAh and the MOD1 OFFSET LUT index is FCh.

MOD1 DAC = 7Bh + 4 x 2Ah = 123h = 291

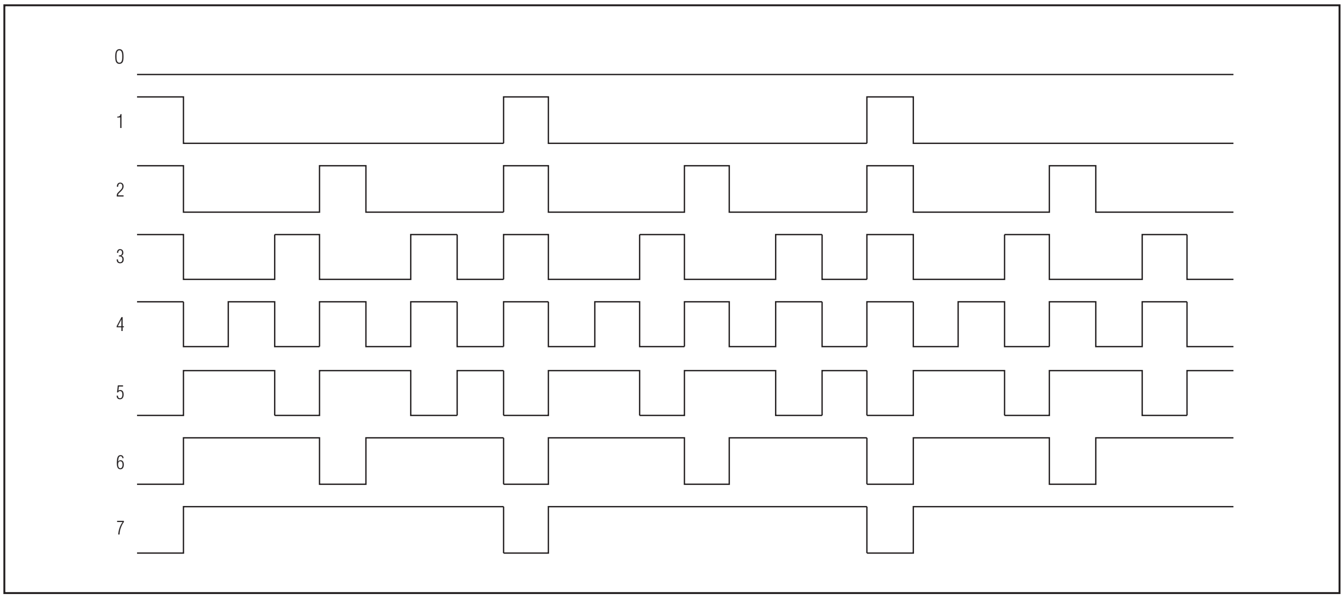


Figure 7. 3-Bit (8-Position) Delta-Sigma Example

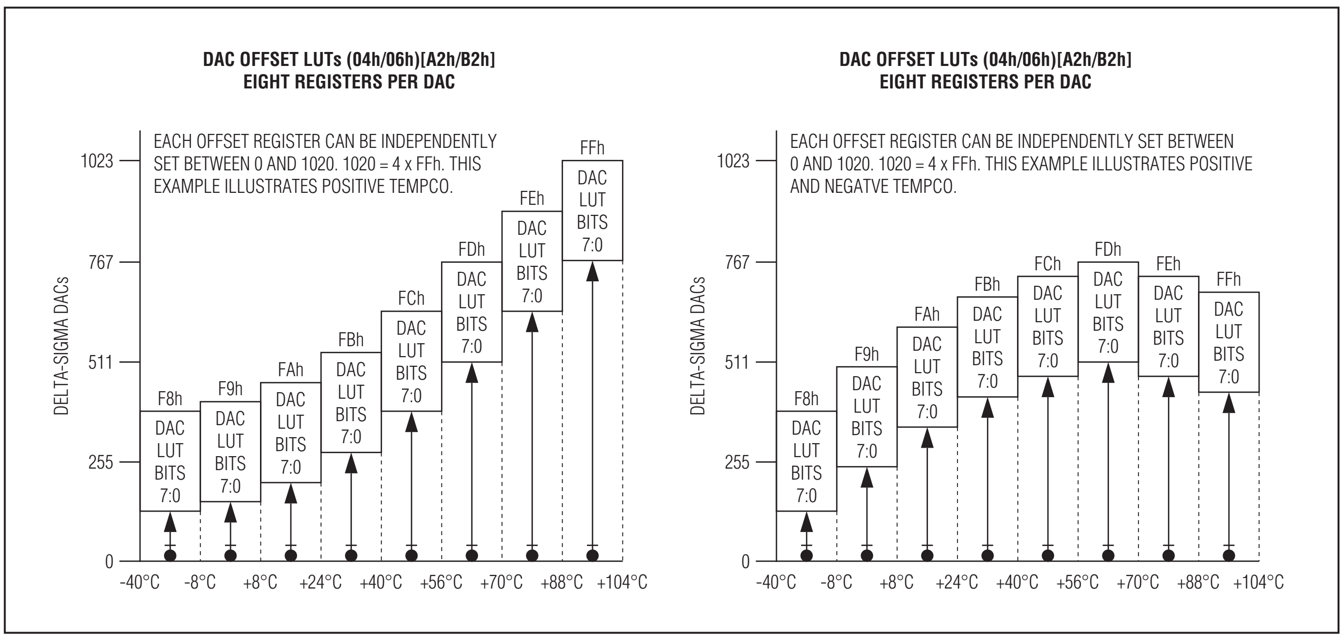


Figure 8. DAC OFFSET LUTs

When temperature controlled, the DACs are updated after each temperature conversion.

The reference input, REFIN, is the supply voltage for the output buffer of all four DACs. The voltage connected to REFIN and its decoupling must be able to support the edge rate requirements of the delta-sigma outputs. In a typical application, a 0.1µF capacitor should be connected between REFIN and ground.

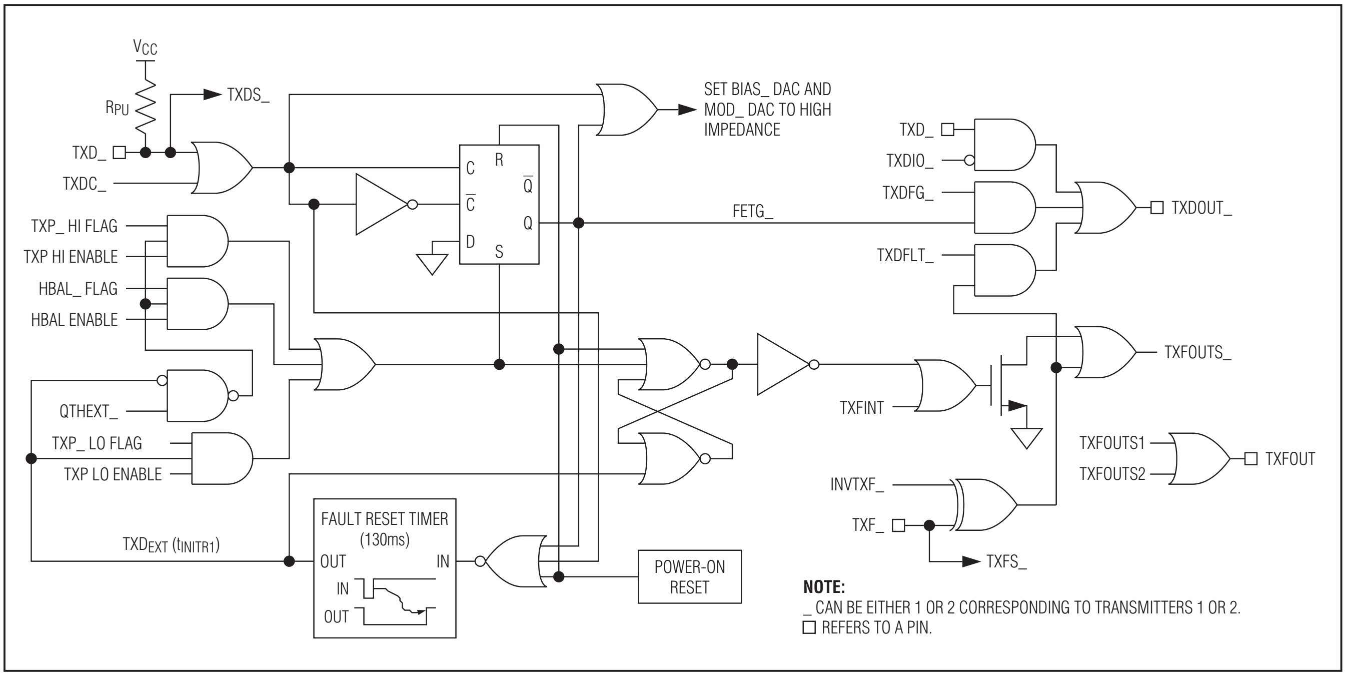


Figure 9. Logic Diagram 1

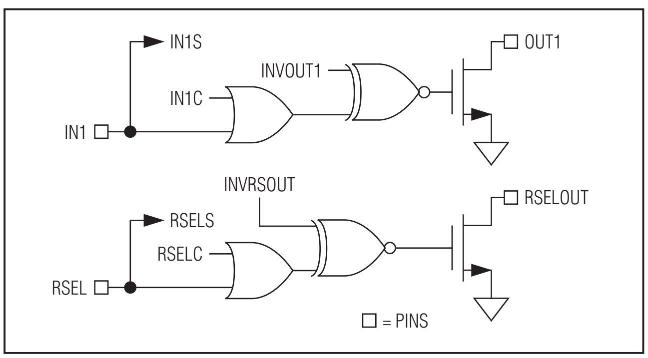


Figure 10. Logic Diagram 2

Digital I/O Pins

Six digital input pins and five digital output pins are provided for monitoring and control.

IN1, RSEL, OUT1, RSELOUT

Digital input pins IN1 and RSEL primarily serve to meet the rate-select requirements of SFP and SFP+. They can also serve as general-purpose inputs. OUT1 and RSELOUT are driven by a combination of the IN1, RSEL, and logic dictated by control registers in the EEPROM (see Figure 10). The levels of IN1 and RSEL can be read from the STATUS register (Lower Memory, Register 6Eh). The open-drain output OUT1 can be controlled and/or inverted using the CNFGB register (Table 02h, Register 89h). The open-drain RSELOUT output is software controlled and/or inverted through the STATUS register and CNFGA register (Table 02h, Register 88h). External pullup resistors must be provided on OUT1 and RSELOUT to realize high logic levels.

TXF1, TXF2, TXFOUT, TXD1, TXD2, TXDOUT1, TXDOUT2

TXDOUT1 and TXDOUT2 are generated from a combination of TXF1, TXF2, TXD1, TXD2, and the internal signals FETG1 and FETG2 (Table 02h, Register 8Ah). A software control identical to TXD1 and TXD2 is also available (TXDC1 and TXDC2, Lower Memory, Register 6Eh). A TXD1 or TXD2 pulse is internally extended (TXD_{EXT}) by time t_{INITR1} to inhibit the latching of low alarms and warnings related to the APC loop to allow for the loop to stabilize. The nonlatching alarms and warnings are TXP LO, BMON1 LO, BMON2 LO, PMON1 LO, and PMON2 LO. In addition, TXP LO is disabled from creating FETG. See the *Transmit Fault (TXFOUT) Output* section for a detailed explanation of TXFOUT. As shown in Figure 9, the same signals and faults can also be used to generate the internal signal FETG. FETG is used to send a fast "turn-off" command to the laser driver. The intended use is a direct connection to the laser driver's TXD1, TXD2 input if this is desired. When V_{CC} < POA, TXDOUT1 and TXDOUT2 are high impedance.

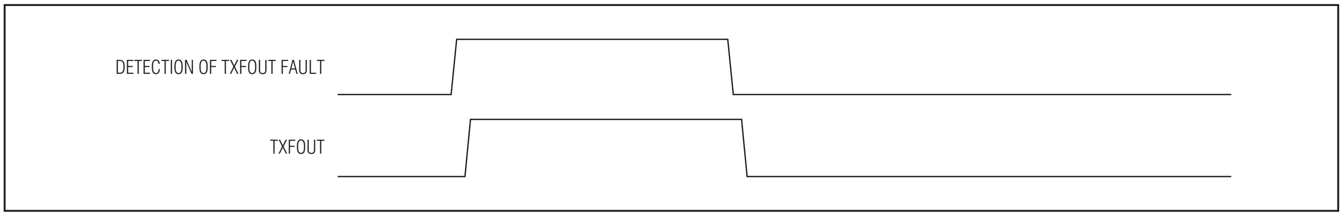


Figure 11a. TXFOUT Nonlatched Operation

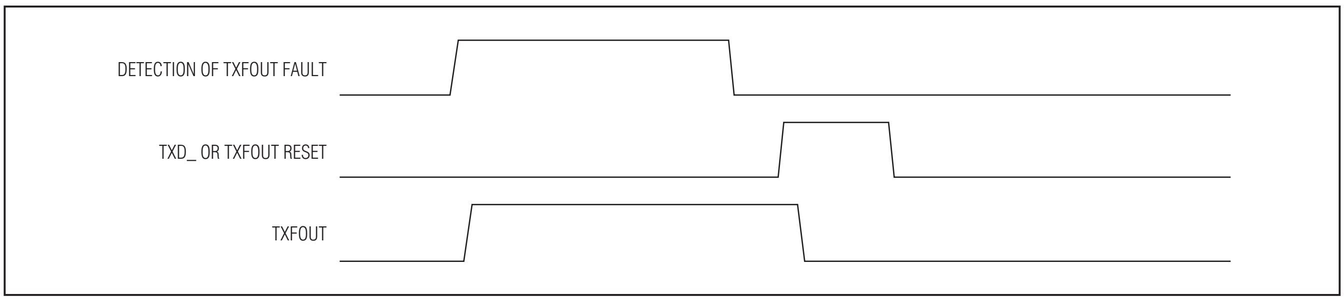


Figure 11b. TXFOUT Latched Operation

Transmit Fault (TXFOUT) Output

TXFOUT can be triggered by all alarms, warnings, QTs, TXD1, TXD2, TXF1, and TXF2 (see Figure 9). The six ADC alarms and warnings are controlled by enable bits (Table 01h/05h, Registers F8h and FCh). See Figures 11a and 11b for nonlatched and latched operation for TXFOUT. The CNFGB register (Table 02h, Register 89h) controls the latching of the alarms.

Die Identification

The DS1876 has an ID hardcoded in its memory. Two registers (Table 02h, Registers 86h–87h) are assigned for this feature. Register 86h reads 76h to identify the part as the DS1876; Register 87h reads the present device version.

I^2C Communication

I^2C Definitions

The following terminology is commonly used to describe I^2C data transfers.

Master Device: The master device controls the slave devices on the bus. The master device generates SCL clock pulses and START and STOP conditions.

Slave Devices: Slave devices send and receive data at the master's request.

Bus Idle or Not Busy: Time between STOP and START conditions when both SDA and SCL are inactive and in their logic-high states.

START Condition: A START condition is generated by the master to initiate a new data transfer with a slave. Transitioning SDA from high to low while SCL remains high generates a START condition. See Figure 12 for applicable timing.

STOP Condition: A STOP condition is generated by the master to end a data transfer with a slave. Transitioning SDA from low to high while SCL remains high generates a STOP condition. See Figure 12 for applicable timing.

Repeated START Condition: The master can use a repeated START condition at the end of one data transfer to indicate that it will immediately initiate a new data transfer following the current one. Repeated STARTs are commonly used during read operations to identify a specific memory address to begin a data transfer. A repeated START condition is issued identically to a normal START condition. See Figure 12 for applicable timing.

Bit Write: Transitions of SDA must occur during the low state of SCL. The data on SDA must remain valid and unchanged during the entire high pulse of SCL plus the setup and hold time requirements (Figure 12). Data is shifted into the device during the rising edge of the SCL.

Bit Read: At the end of a write operation, the master must release the SDA bus line for the proper amount of setup time (Figure 12) before the next rising edge of SCL during a bit read. The device shifts out each bit of data on SDA at the falling edge of the previous SCL pulse and the data bit is valid at the rising edge of the current SCL pulse. Remember that the master generates all SCL clock pulses, including when it is reading bits from the slave.

Acknowledgement (ACK and NACK): An acknowledgement (ACK) or not-acknowledge (NACK) is always the 9th bit transmitted during a byte transfer. The device receiving data (the master during a read or the slave during a write operation) performs an ACK by transmitting a zero during the 9th bit. A device performs a NACK by transmitting a one during the 9th bit. Timing (Figure 12) for the ACK and NACK is identical to all other bit writes. An ACK is the acknowledgment that the device is properly receiving data. A NACK is used to terminate a read sequence or as an indication that the device is not receiving data.

Byte Write: A byte write consists of 8 bits of information transferred from the master to the slave (most significant bit first) plus a 1-bit acknowledgement from the slave to the master. The 8 bits transmitted by the master are done according to the bit write definition and the acknowledgement is read using the bit read definition.

Byte Read: A byte read is an 8-bit information transfer from the slave to the master plus a 1-bit ACK or NACK from the master to the slave. The 8 bits of information that are transferred (most significant bit first) from the slave to the master are read by the master using the bit read definition, and the master transmits an ACK using the bit write definition to receive additional data bytes. The master must NACK the last byte read to terminate communication so the slave returns control of SDA to the master.

Slave Address Byte: Each slave on the I^2C bus responds to a slave address byte sent immediately following a START condition. The slave address byte contains the slave address in the most significant 7 bits and the $R/\overline{W}$ bit in the least significant bit.

The DS1876 responds to three slave addresses. The auxiliary memory always responds to a fixed I^2C slave address, A0h. (If the main device's slave address is programmed to be A0h, access to the auxiliary memory is disabled.) The Lower Memory and Tables 00h–06h respond to I^2C slave addresses whose lower 3 bits are configurable (A0h–AEh, B0h–BEh) using the DEVICE ADDRESS byte (Table 02h, Register 8Bh). The user also must set the ASEL bit (Table 02h, Register 88h) for this address to be active. By writing the correct slave address with $R/\overline{W} = 0$, the master indicates it writes data to the slave. If $R/\overline{W} = 1$, the master reads data from the slave. If an incorrect slave address is written, the DS1876 assumes the master is communicating with another I^2C device and ignores the communications until the next START condition is sent.

Memory Address: During an I^2C write operation to the DS1876, the master must transmit a memory address to identify the memory location where the slave is to store the data. The memory address is

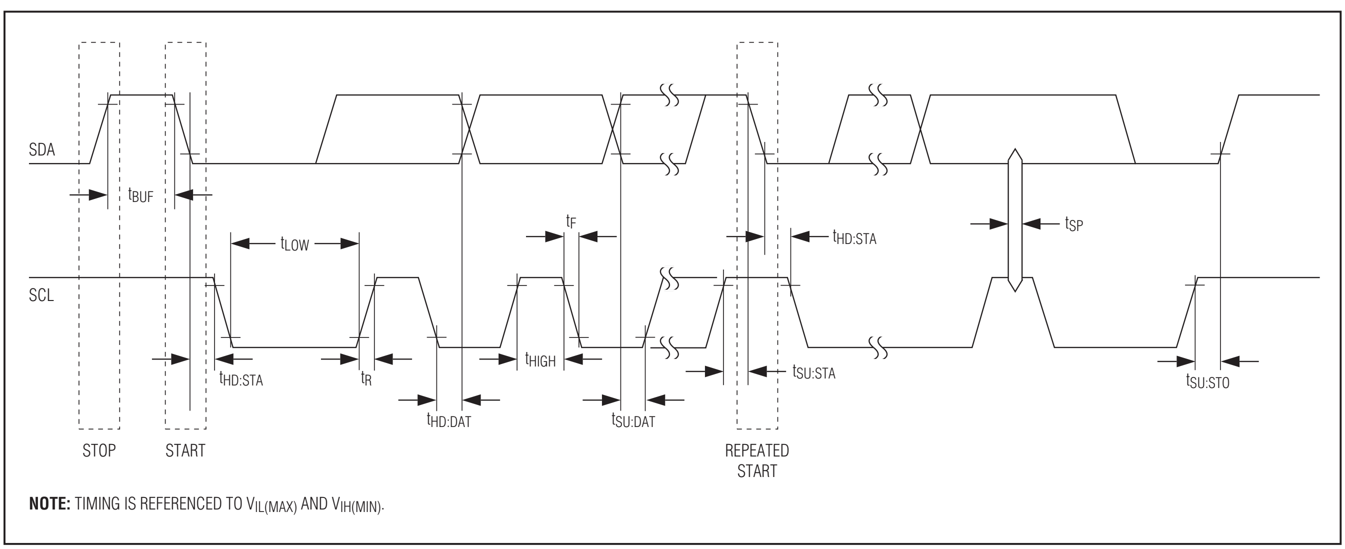


Figure 12. I^2C Timing

always the second byte transmitted during a write operation following the slave address byte.

I²C Protocol

See Figure 13 for an example of I²C timing.

Writing a Single Byte to a Slave: The master must generate a START condition, write the slave address byte (R/$\overline{W}$ = 0), write the memory address, write the byte of data, and generate a STOP condition. Remember that the master must read the slave's acknowledgement during all byte write operations.

Writing Multiple Bytes to a Slave: To write multiple bytes to a slave, the master generates a START condition, writes the slave address byte (R/$\overline{W}$ = 0), writes the memory address, writes up to 8 data bytes, and generates a STOP condition. The DS1876 writes 1 to 8 bytes (one page or row) with a single write transaction. This is internally controlled by an address counter that allows data to be written to consecutive addresses without transmitting a memory address before each data byte is sent. The address counter limits the write to one 8-byte page (one row of the memory map). Attempts to write to additional pages of memory without sending a STOP condition between pages result in the address counter wrapping around to the beginning of the present row.

For example: A 3-byte write starts at address 06h and writes three data bytes (11h, 22h, and 33h) to three "consecutive" addresses. The result is that addresses 06h and 07h would contain 11h and 22h, respectively, and the third data byte, 33h, would be written to address 00h.

To prevent address wrapping from occurring, the master must send a STOP condition at the end of the page, then wait for the bus-free or EEPROM write time to elapse. Then the master can generate a new START condition and write the slave address byte (R/$\overline{W}$ = 0) and the first memory address of the next memory row before continuing to write data.

Acknowledge Polling: Any time a EEPROM page is written, the DS1876 requires the EEPROM write time (t_{WR}) after the STOP condition to write the contents of the page to EEPROM. During the EEPROM write time, the DS1876 does not acknowledge its slave address because it is busy. It is possible to take advantage of that phenomenon by repeatedly addressing the DS1876, which allows the next page to be written as soon as the DS1876 is ready to receive the data. The alternative to acknowledge polling is to wait for maximum period of t_{WR} to elapse before attempting to write again to the DS1876.

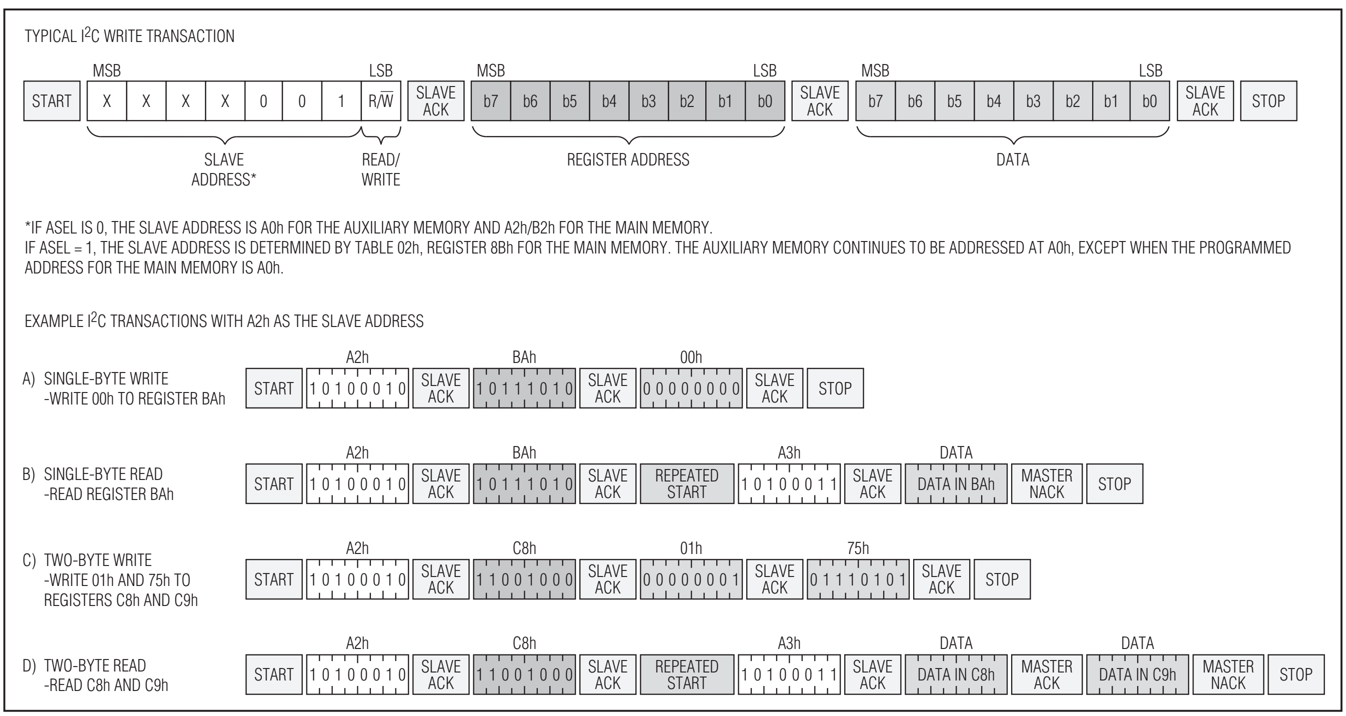


Figure 13. Example I²C Timing

EEPROM Write Cycles: When EEPROM writes occur, the DS1876 writes the whole EEPROM memory page, even if only a single byte on the page was modified. Writes that do not modify all 8 bytes on the page are allowed and do not corrupt the remaining bytes of memory on the same page. Because the whole page is written, bytes on the page that were not modified during the transaction are still subject to a write cycle. This can result in a whole page being worn out over time by writing a single byte repeatedly. Writing a page 1 byte at a time wears the EEPROM out 8x faster than writing the entire page at once. The DS1876's EEPROM write cycles are specified in the *Nonvolatile Memory Characteristics* table. The specification shown is at the worst-case temperature. It can handle approximately 10x that many writes at room temperature. Writing to SRAM-shadowed EEPROM memory with SEEB = 1 does not count as a EEPROM write cycle when evaluating the EEPROM's estimated lifetime.

Reading a Single Byte from a Slave: Unlike the write operation that uses the memory address byte to define where the data is to be written, the read operation occurs at the present value of the memory address counter. To read a single byte from the slave, the master generates a START condition, writes the slave address byte with $R/\overline{W}$ = 1, reads the data byte with a NACK to indicate the end of the transfer, and generates a STOP condition.

Manipulating the Address Counter for Reads: A dummy write cycle can be used to force the address pointer to a particular value. To do this, the master generates a START condition, writes the slave address byte ($R/\overline{W}$ = 0), writes the memory address where it desires to read, generates a repeated START condition, writes the slave address byte ($R/\overline{W}$ = 1), reads data with ACK or NACK as applicable, and generates a STOP condition.

Memory Organization

The DS1876 features nine separate memory tables that are internally organized into 8-byte rows. The main device located at A2h is used for overall device configuration and transmitter 1 control, calibration, alarms, warnings, and monitoring.

Lower Memory, A2h is addressed from 00h–7Fh and contains alarm and warning thresholds, flags, masks, several control registers, password entry area (PWE), and the table-select byte.

Table 01h, A2h primarily contains user EEPROM (with PW1 level access) as well as alarm and warning enable bytes.

Table 02h, A2h/B2h is a multifunction space that contains configuration registers, scaling and offset values, passwords, and interrupt registers as well as other miscellaneous control bytes. All functions and status can be written and read from either A2h or B2h addresses.

Table 04h, A2h contains a temperature-indexed LUT for control of the MOD1 voltage. The MOD1 LUT can be programmed in 2°C increments over the -40°C to +102°C range. This also contains a temperature-indexed LUT for the MOD1 offsets.

Table 05h, A2h is empty by default. It can be configured to contain the alarm and warning enable bytes from Table 01h, Registers F8h–FFh with the MASK bit enabled (Table 02h, Register 88h). In this case Table 01h is empty.

Table 06h, A2h contains a temperature-indexed LUT for control of the APC1 voltage. The APC1 LUT can be programmed in 2°C increments over the -40°C to +102°C range. This also contains a temperature-indexed LUT for the APC1 offsets.

The main device located at B2h is used for transmitter 2 control, calibration, alarms, warnings, and monitoring.

Lower Memory, B2h is addressed from 00h–7Fh and contains alarm and warning thresholds, flags, masks, several control registers, PWE, and the table-select byte.

Table 01h, B2h contains alarm and warning enable bytes.

Table 04h, B2h contains a temperature-indexed LUT for control of the MOD2 voltage. The MOD2 LUT can be programmed in 2°C increments over the -40°C to +102°C range. This also contains a temperature-indexed LUT for the MOD2 offsets.

Table 05h, B2h is empty by default. It can be configured to contain the alarm and warning enable bytes from Table 01h, Registers F8h–FFh with the MASK bit enabled (Table 02h, Register 88h). In this case Table 01h is empty.

Table 06h, B2h contains a temperature-indexed LUT for control of the APC2 voltage. The APC2 LUT can be programmed in 2°C increments over the -40°C to +102°C range. This also contains a temperature-indexed LUT for the APC2 offsets.

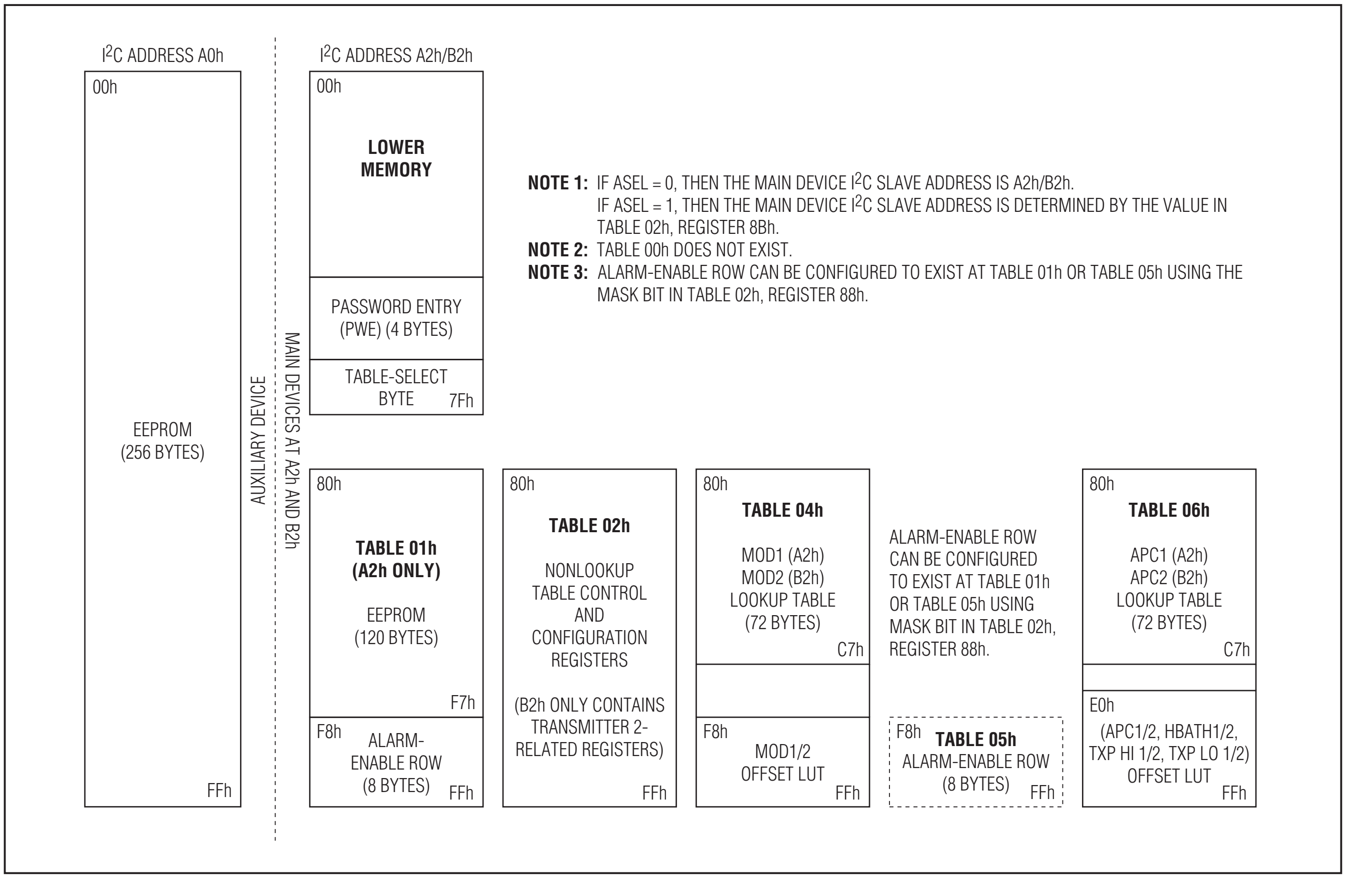


Figure 14. Memory Map

Auxiliary Memory (Device A0h) contains 256 bytes of EE memory accessible from address 00h–FFh. It is selected with the device address of A0h.

See the *Register Descriptions* section for a more complete detail of each byte's function, as well as for read/write permissions for each byte.

Shadowed EEPROM

Many nonvolatile memory locations (listed within the *Register Descriptions* section) are actually shadowed EEPROM and are controlled by the SEEB bit in Table 02h, Register 80h.

The DS1876 incorporates shadowed EEPROM memory locations for key memory addresses that can be written many times. By default the shadowed EEPROM bit, SEEB, is not set and these locations act as ordinary EEPROM. By setting SEEB, these locations function like SRAM cells, which allow an infinite number of write cycles without concern of wearing out the EEPROM. This also eliminates the requirement for the EEPROM write time, t_{WR}. Because changes made with SEEB enabled do not affect the EEPROM, these changes are not retained through power cycles. The power-on value is the last value written with SEEB disabled. This function can be used to limit the number of EEPROM writes during calibration or to change the monitor thresholds periodically during normal operation helping to reduce the number of times EEPROM is written. Figure 14 shows the memory map and indicates which locations are shadowed EEPROM.

Register Descriptions

The register maps show each byte/word (2 bytes) in terms of its row in the memory. The first byte in the row is located in memory at the row address (hexadecimal) in the leftmost column. Each subsequent byte on the row is one/two memory locations beyond the previous byte/word's address. A total of 8 bytes are present on each row. For more information about each of these bytes, see the corresponding register description.

Memory Map Access Codes

The following section provides the DS1876 register definitions. Each register or row of registers has an access descriptor that determines the password level required to read or write the memory. Level 2 password is intended for the module manufacture access only. Level 1 password allows another level of protection for items the end consumer wishes to protect. Many registers are always readable, but require password access to write. There are a few registers that cannot be read without password access. The following access codes describe each mode used by the DS1876 with factory settings for the PW_ENA and PW_ENB (Table 02h, Registers C0h–C1h) registers.

ACCESS CODE	READ ACCESS	WRITE ACCESS
<0/_>	At least 1 byte/bit in the row/byte is different than the rest of the row/byte, so look at each byte/bit separately for permissions.	
<1/_>	Read all	Write PW2
<2/_>	Read all	Write not applicable
<3/_>	Read all	Write all, but the DS1876 hardware also writes to these bytes/bits
<4/_>	Read PW2	Write PW2 + mode_bit
<5/_>	Read all	Write all
<6/_>	Read not applicable	Write all
<7/_>	Read PW1	Write PW1
<8/_>	Read PW2	Write PW2
<9/_>	Read not applicable	Write PW2
<10/_>	Read PW2	Write not applicable
<11/_>	Read all	Write PW1

Memory Addresses A0h, A2h, and B2h

There are three separate I^{2}C addresses in the DS1876: A0h, A2h, and B2h. A2h and B2h are used to configure and monitor two transmitters. Transmitter 1 is accessed using A2h. Transmitter 2 is accessed using B2h. Many of the registers in A2h and B2h are shared registers. These registers can be read and written from both A2h and B2h.

MEMORY CODE	A2h AND B2h REGISTERS
<C> or <_/C>	A common memory location is used for A2h and B2h device addresses. Reading or writing to these locations is identical, regardless of using A2h or B2h addresses.
<D> or <_/D>	Different memory locations are used for A2h and B2h device addresses.
<M> or <_/M>	Mixture of common and different memory locations for A2h and B2h device addresses. See the individual bytes within the row for clarification. If "M" is used on an individual byte, see the expanded bit descriptions to determine which bits are common vs. different.

Lower Memory Register Map

LOWER MEMORY									
ROW (HEX)	ROW NAME	WORD 0		WORD 1		WORD 2		WORD 3	
		BYTE 0/8	BYTE 1/9	BYTE 2/A	BYTE 3/B	BYTE 4/C	BYTE 5/D	BYTE 6/E	BYTE 7/F
00	<1/C> THRESHOLD$_0$	TEMP ALARM HI		TEMP ALARM LO		TEMP WARN HI		TEMP WARN LO	
08	<1/C > THRESHOLD$_1$	V_{CC} ALARM HI		V_{CC} ALARM LO		V_{CC} WARN HI		V_{CC} WARN LO	
10	<1/D> THRESHOLD$_2$	BMON ALARM HI		BMON ALARM LO		BMON WARN HI		BMON WARN LO	
18	<1/D> THRESHOLD$_3$	PMON ALARM HI		PMON ALARM LO		PMON WARN HI		PMON WARN LO	
20–40	<1/C > EEPROM	EE		EE		EE		EE	
48–50	<1/D > EEPROM	EE		EE		EE		EE	
58	<1/C > EEPROM	EE	EE	EE	EE	EE	EE	EE	EE
60	<2/M> ADC VALUES$_0$	<C>TEMP VALUE		<C> V_{CC} VALUE		<D>BMON VALUE		<D>PMON VALUE	
68	<0/M> ADC VALUES$_1$	RESERVED		RESERVED		RESERVED		<0/M>STATUS	<3/D> UPDATE
70	<5/D> ALARM/WARN	ALARM$_3$	ALARM$_2$	ALARM$_1$	RESERVED	WARN$_3$	RESERVED	RESERVED	RESERVED
78	<0/M> TABLE SELECT	RESERVED	RESERVED	RESERVED	<6/C> PWE MSW		<6/C> PWE LSW		<5/D> TBL SEL

<C> or <_/C> = Common, <D> or <_/D> = Different, <M> or <_/M> = Mixture of common and different.

Table 01h Register Map

TABLE 01h									
ROW (HEX)	ROW NAME	WORD 0		WORD 1		WORD 2		WORD 3	
		BYTE 0/8	BYTE 1/9	BYTE 2/A	BYTE 3/B	BYTE 4/C	BYTE 5/D	BYTE 6/E	BYTE 7/F
80–F7	<1/C> EEPROM	EE	EE	EE	EE	EE	EE	EE	EE
F8	<7/M>ALARM ENABLE	<M>ALARM EN$_3$	RESERVED	<D>ALARM EN$_1$	RESERVED	<M>WARN EN$_3$	RESERVED	RESERVED	RESERVED

<C> or <_/C> = Common, <D> or <_/D> = Different, <M> or <_/M> = Mixture of common and different.

***Note:** The ALARM ENABLE bytes (Registers F8h–FFh) can be configured to exist in Table 05h instead of here at Table 01h with the MASK bit (Table 02h, Register 88h). If the row is configured to exist in Table 05h, these location are empty in Table 01h.*

The access codes represent the factory default values of PW_ENA and PW_ENB (Table 02h, Registers C0h–C1h). These registers also allow for custom permissions.

ACCESS CODE	<0/_>	<1/_>	<2/_>	<3/_>	<4/_>	<5/_>	<6/_>	<7/_>	<8/_>	<9/_>	<10/_>	<11/_>
Read Access	See each bit/byte separately	All	All	All	PW2	All	N/A	PW1	PW2	N/A	PW2	All
Write Access		PW2	N/A	All and DS1876 Hardware	PW2 + mode bit	All	All	PW1	PW2	PW2	N/A	PW1