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DS1877

SFP Controller for Dual Rx Interface

General Description

The DS1877 controls and monitors all functions for SFF, SFP, and SFP+ modules including all SFF-8472 functionality. The device supports all LOS functions for two receivers, and continually monitors for LOS of either channel. Four ADC channels monitor V_{CC}, temperature, and two differential external monitor inputs that can be used to meet all monitoring requirements. Two digital-to-analog converter (DAC) outputs with temperature-indexed lookup tables (LUTs) are available for additional monitoring and control functionality.

Applications

SFF, SFP, and SFP+ Transceiver Modules

Dual Rx Video SFPs

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
DS1877T+	-40°C to +95°C	28 TQFN-EP*
DS1877T+T&R	-40°C to +95°C	28 TQFN-EP*

+Denotes a lead(Pb)-free/RoHS-compliant package.
T&R = Tape and reel.
**EP = Exposed pad.*

Features

- **Meets All SFF-8472 Control and Monitoring Requirements**
- **Four Analog Monitor Channels: Temperature, V_{CC}, RSSI1, RSSI2**
  - **RSSI1 and RSSI2 Support Internal and External Calibration**
  - **Differential Input**
  - **Common-Mode Range from GND to V_{CC}**
  - **Scalable Dynamic Range**
  - **Internal Direct-to-Digital Temperature Sensor**
  - **Alarm and Warning Flags for All Monitored Channels**
- **Two 10-Bit Delta-Sigma Outputs**
  - **Each Controlled by 72-Entry Temperature LUT**
- **Digital I/O Pins: Four Inputs, Four Outputs**
- **Comprehensive Loss-of-Signal (LOS) Detection System**
- **Flexible, Two-Level Password Scheme Provides Three Levels of Security**
- **120 Bytes of Password-1 Protected Memory**
- **128 Bytes of Password-2 Protected Memory in Main Device Address**
- **256 Additional Bytes Located at A0h Slave Address**
- **Receiver 1 is Accessed at A2h Slave Address**
- **Receiver 2 is Accessed at B2h Slave Address**
- **I^2C-Compatible Interface**
- **+2.85V to +3.9V Operating Voltage Range**
- **-40°C to +95°C Operating Temperature Range**
- **28-Pin TQFN (5mm x 5mm x 0.75mm) Package**

For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim Integrated's website at www.maximintegrated.com.

19-5188; Rev 1; 4/10

DS1877

SFP Controller for Dual Rx Interface

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Voltage Range on RSSI1_, RSSI2_, INX, LOS1, and LOS2 Pins Relative to Ground.....-0.5V to (V_{CC} + 0.5V)*
Voltage Range on V_{CC}, SDA, SCL, OUTX, FAULT, RSELOUT, and LOSOUT Pins Relative to Ground....-0.5V to +6V
Continuous Power Dissipation
28-Pin TQFN (derate 34.5mW/°C) above +70°C....2758.6mW

Operating Temperature Range.....-40°C to +95°C
Programming Temperature Range .....0°C to +95°C
Storage Temperature Range.....-55°C to +125°C
Lead Temperature (soldering, 10s) .....+300°C
Soldering Temperature (reflow) .....+260°C

**Subject to not exceeding +6V.*

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

(T_A = -40°C to +95°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Main Supply Voltage	V_{CC}	(Note 1)	+2.85		+3.9	V
High-Level Input Voltage (SDA, SCL)	$V_{IH:1}$		0.7 x V_{CC}		V_{CC} + 0.3	V
Low-Level Input Voltage (SDA, SCL)	$V_{IL:1}$		-0.3		0.3 x V_{CC}	V
High-Level Input Voltage (FAULT, RSEL, INX, LOS1, LOS2)	$V_{IH:2}$		2.0		V_{CC} + 0.3	V
Low-Level Input Voltage (FAULT, RSEL, INX, LOS1, LOS2)	$V_{IL:2}$		-0.3		+0.8	V

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = +2.85V to +3.9V, T_A = -40°C to +95°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current	I_{CC}	(Notes 1, 2)		2.5	10	mA
Output Leakage (SDA, OUTX, RSELOUT, LOSOUT, FAULT)	I_{LO}				1	µA
Low-Level Output Voltage (SDA, OUTX, RSELOUT, LOSOUT, DAC1, DAC2, FAULT)	V_{OL}	I_{OL} = 4mA			0.4	V
		I_{OL} = 6mA			0.6	
High-Level Output Voltage (DAC1, DAC2)	V_{OH}	I_{OH} = 4mA	V_{CC} - 0.4			V
DAC1 and DAC2 Before LUT Recall				10	100	nA
Input Leakage Current (SCL, RSEL, INX, LOS1, LOS2)	I_{LI}				1	µA
Digital Power-On Reset	POD		1.0		2.2	V
Analog Power-On Reset	POA		2.0		2.75	V

DAC1, DAC2 ELECTRICAL CHARACTERISTICS

(V_{CC} = +2.85V to +3.9V, T_A = -40°C to +95°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Main Oscillator Frequency	f_{OSC}			5		MHz
Delta-Sigma Input-Clock Frequency	f_{DS}			$f_{OSC}/2$		MHz
Reference Voltage Input (REFIN)	V_{REFIN}	Minimum 0.1µF to GND	2		V_{CC}	V
Output Range			0		V_{REFIN}	V
Output Resolution		See the *Delta-Sigma Outputs* section for details			10	Bits
Output Impedance	R_{DS}			35	100	Ω

ANALOG VOLTAGE MONITORING CHARACTERISTICS

(V_{CC} = +2.85V to +3.9V, T_A = -40°C to +95°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ADC Resolution				13		Bits
Input/Supply Accuracy (RSSI1_, RSSI2_, V_{CC})	ACC	At factory setting		0.25	0.5	%FS
Update Rate for Temperature, RSSI1_, RSSI2_, V_{CC}	t_{RR}			45	75	ms
Input/Supply Offset (RSSI1_, RSSI2_, V_{CC})	V_{OS}	(Note 3)		0	5	LSB
Factory Setting (Note 4)		RSSI1/RSSI2 coarse		2.5		V
		V_{CC}		6.5536		V
		RSSI1/RSSI2 fine		312.5		µV

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = +2.85V to +3.9V, T_A = -40°C to +95°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Fault Reset Time (to FAULT = 0)	t_{INITR}	From ↑ V_{CC} > VCC LO alarm (Note 5)		161		ms
LOSOUT Assert Time	t_{LOSS_ON}	LOS_ LO (Note 6)		25.6		µs
LOSOUT Deassert Time	t_{LOSS_OFF}	LOS_ HI (Note 7)		25.6		µs

ANALOG QUICK-TRIP CHARACTERISTICS

(V_{CC} = +2.85V to +3.9V, T_A = -40°C to +95°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
RSSI Full-Scale Voltage				1.25		V
Input Resistance			35	50	65	kΩ
Resolution				8		Bits
Error		T_A = +25°C		±2		%FS
Integral Nonlinearity			-1		+1	LSB
Differential Nonlinearity			-1		+1	LSB
Temperature Drift			-2		+2	%FS
Offset			-5		+10	mV

QUICK-TRIP TIMING CHARACTERISTICS

(V_{CC} = +2.85V to +3.9V, T_A = -40°C to +95°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output-Enable Time Following POA	t_{INIT}	(Note 5)		20		ms
Sample Time per Quick-Trip Comparison	t_{REP}			12.8		µs

DIGITAL THERMOMETER CHARACTERISTICS

(V_{CC} = +2.85V to +3.9V, T_A = -40°C to +95°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Thermometer Error	T_{ERR}	-40°C to +95°C	-3		+3	°C

I²C AC ELECTRICAL CHARACTERISTICS

(V_{CC} = +2.85V to +3.9V, T_A = -40°C to +95°C, unless otherwise noted. Timing is referenced to $V_{IL(MAX)}$ and $V_{IH(MIN)}$.) (Figure 12)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SCL Clock Frequency	f_{SCL}	(Note 8)	0		400	kHz
Clock Pulse-Width Low	t_{LOW}		1.3			µs
Clock Pulse-Width High	t_{HIGH}		0.6			µs
Bus Free Time Between STOP and START Condition	t_{BUF}		1.3			µs
START Hold Time	$t_{HD:STA}$		0.6			µs
START Setup Time	$t_{SU:STA}$		0.6			µs
Data Out Hold Time	$t_{HD:DAT}$		0		0.9	µs
Data In Setup Time	$t_{SU:DAT}$		100			ns
Rise Time of Both SDA and SCL Signals	t_R	(Note 9)	$20 + 0.1C_B$		300	ns
Fall Time of Both SDA and SCL Signals	t_F	(Note 9)	$20 + 0.1C_B$		300	ns
STOP Setup Time	$t_{SU:STO}$		0.6			µs
Capacitive Load for Each Bus Line	C_B				400	pF
EEPROM Write Time	t_{WR}	(Note 10)			20	ms

NONVOLATILE MEMORY CHARACTERISTICS

(V_{CC} = +2.85V to +3.9V, unless otherwise noted.)

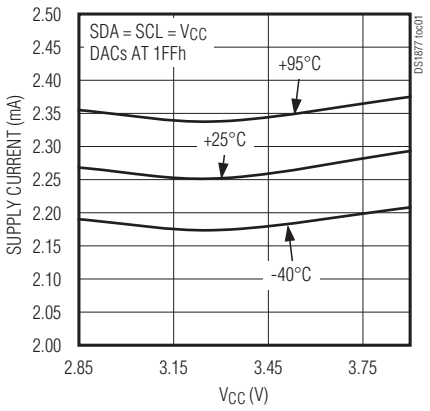
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
EEPROM Write Cycles		At +25°C	200,000			—
		At +85°C	50,000			

Note 1: All voltages are referenced to ground. Current into the IC is positive, and current out of the IC is negative.
Note 2: Inputs are at supply rail. Outputs are not loaded.
Note 3: This parameter is guaranteed by design.
Note 4: Full-scale is user programmable.
Note 5: A temperature conversion is completed and the DAC values are recalled from the LUTs and V_{CC} has been measured to be above the VCC LO alarm, if the VCC LO alarm is enabled.
Note 6: This specification is the time it takes from RSSI1_ and RSSI2_ voltage falling below the LLOS_ trip threshold to LOSOUT asserted high.
Note 7: This specification is the time it takes from RSSI1_ and RSSI2_ voltage rising above the HLOS_ trip threshold to LOSOUT asserted high.
Note 8: I^2C interface timing shown is for fast-mode (400kHz) operation. This device is also backward compatible with I^2C standard mode.
Note 9: C_B—Total capacitance of one bus line in pF.
Note 10: EEPROM write begins after a STOP condition occurs.

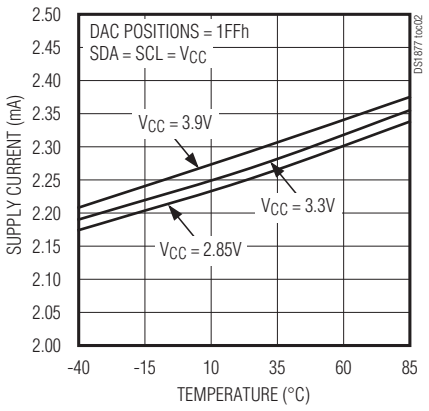
Typical Operating Characteristics

(V_{CC} = +3.3V, T_A = +25°C, unless otherwise noted.)

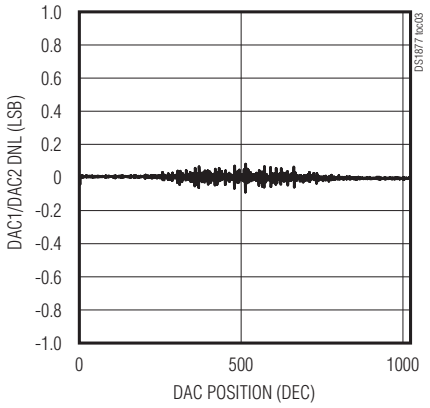
SUPPLY CURRENT vs. SUPPLY VOLTAGE



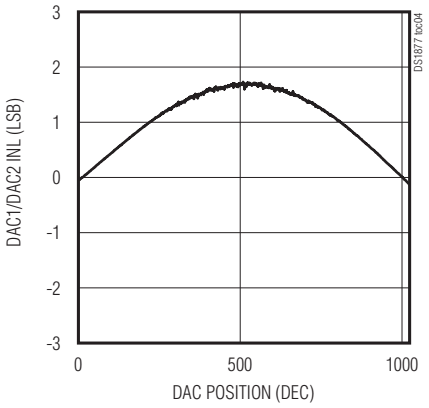
SUPPLY CURRENT vs. TEMPERATURE



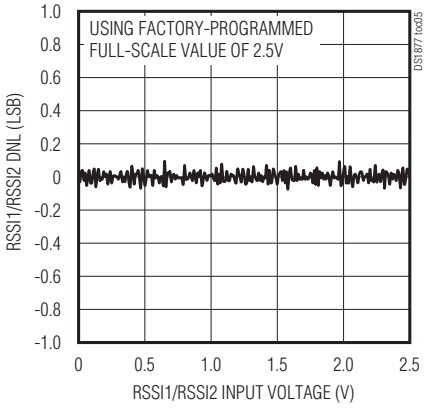
DAC1/DAC2 DNL



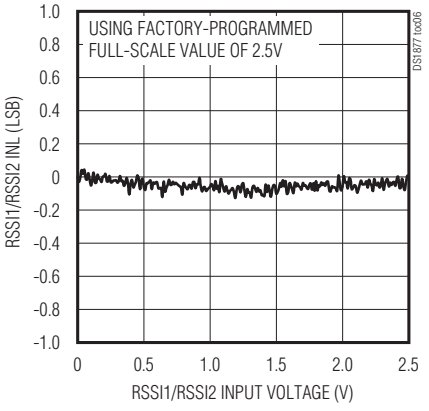
DAC1/DAC2 INL



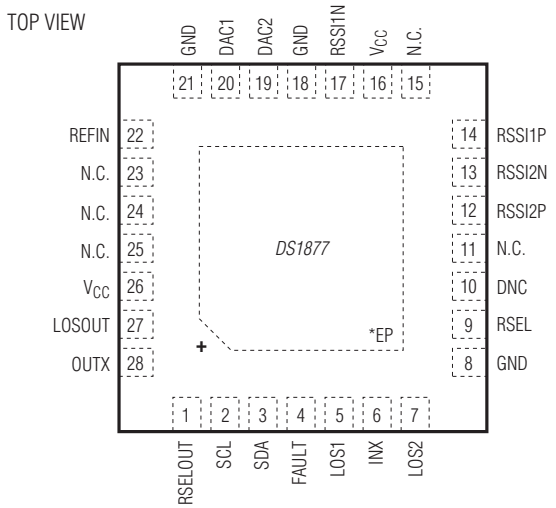
RSSI1/RSSI2 DNL



RSSI1/RSSI2 INL



Pin Configuration



THIN QFN
(5mm × 5mm × 0.8mm)

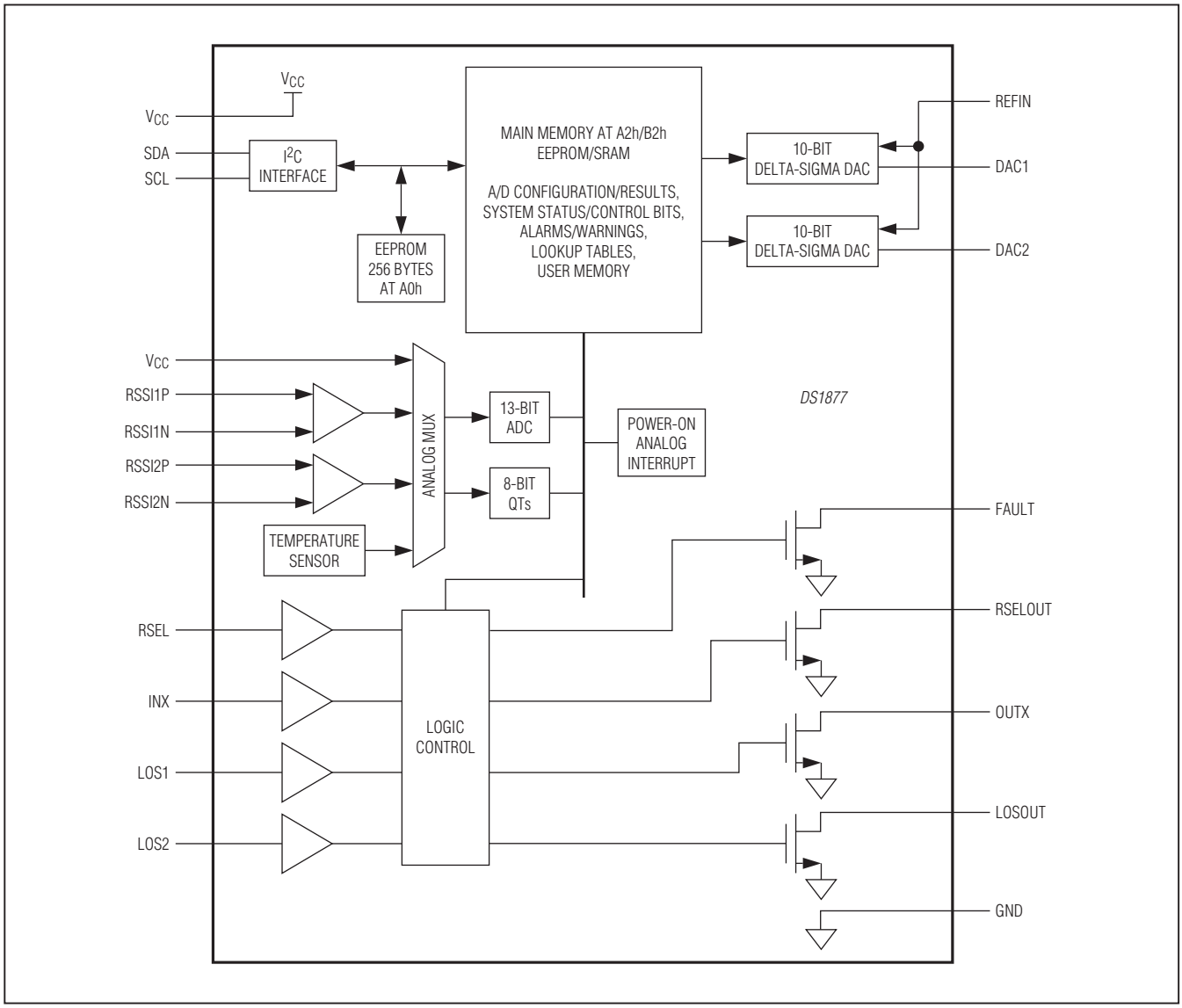
*EXPOSED PAD.

Pin Description

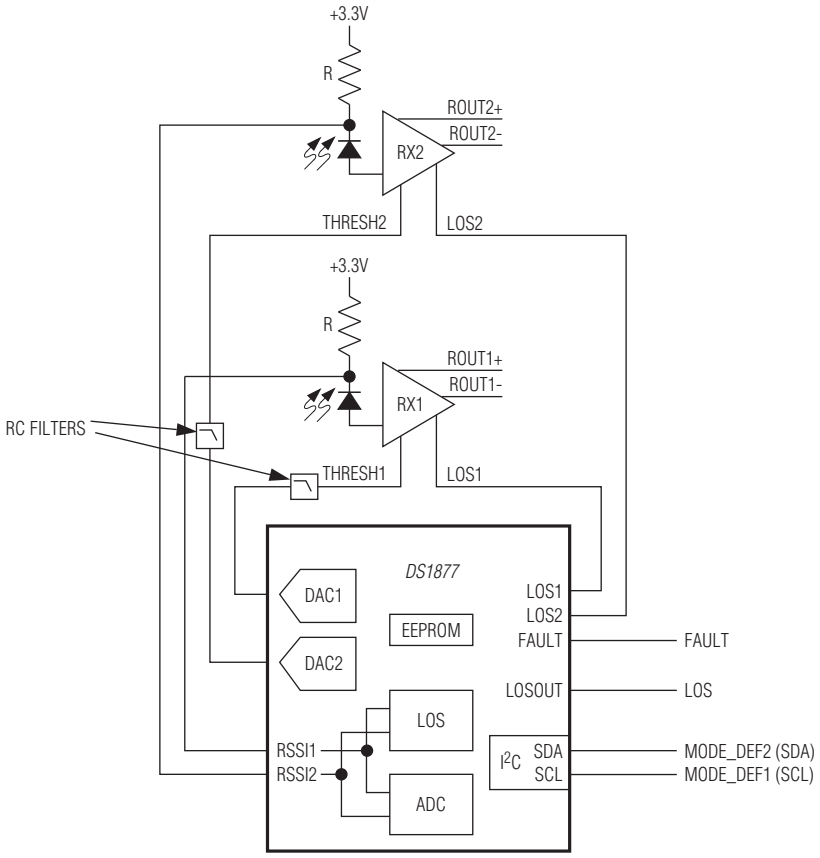
PIN	NAME	FUNCTION
1	RSELOUT	Rate-Select Output
2	SCL	I²C Serial-Clock Input
3	SDA	I²C Serial-Data Input/Output
4	FAULT	Transmit Fault Input and Output, Open Drain
5	LOS1	Loss-of-Signal Input 1
6	INX	Digital Input. General-purpose input, AS1 in SFF-8079, or RS1 in SFF-8431.
7	LOS2	Loss-of-Signal Input 2
8, 18, 21	GND	Ground Connection
9	RSEL	Rate-Select Input
10	DNC	Do Not Connect
11, 15, 23, 24, 25	N.C.	No Connection. Not internally connected.

PIN	NAME	FUNCTION
12, 13	RSSI2P, RSSI2N	Differential External Monitor Input 2 and LOS2 LO Quick Trip
14, 17	RSSI1P, RSSI1N	Differential External Monitor Input 1 and LOS1 LO Quick Trip
16, 26	VCC	Power-Supply Input
19	DAC2	DAC2, Delta-Sigma Output
20	DAC1	DAC1, Delta-Sigma Output
22	REFIN	Reference Input for DAC1 and DAC2
27	LOSOUT	Receive Loss-of-Signal Output
28	OUTX	Digital Output. General-purpose output, AS1 output in SFF-8079, or RS1 output in SFF-8431.
—	EP	Exposed Pad (Connect to GND)

Block Diagram



Typical Operating Circuit



Detailed Description

The DS1877 integrates the control and monitoring functionality required in an SFP or SFP+ system. The device is specifically designed for a dual-receiver SFP module. Key components of the device are shown in the *Block Diagram* and described in subsequent sections.

DACs During Power-Up

On power-up, the device sets the DACs to high impedance. After time t_{INIT}, the DACs are set to an initial condition set in EEPROM. After a temperature conversion is completed and if the VCC LO alarm is enabled, an additional V_{CC} conversion above the customer-defined VCC LO alarm level is required before the DACs are updated with the value determined by the temperature conversion and the DAC LUT. See Figure 1.

Quick-Trip Timing

As shown in Figure 2, the device's input comparator is shared between two LOS comparisons. The comparator polls the alarms in a multiplexed sequence. The comparator checks the LOS (RSSI1_ and RSSI2_) signals against the internal reference. Depending on the results of the comparison, the corresponding alarms and warnings are asserted or deasserted. Any QT alarm that is detected by default remains active until a subsequent comparator sample shows that the condition no longer exists.

Table 1. Acronyms

ACRONYM	DESCRIPTION
ADC	Analog-to-Digital Converter
AGC	Automatic Gain Control
APC	Automatic Power Control
APD	Avalanche Photodiode
ATB	Alarm Trap Bytes
DAC	Digital-to-Analog Converter
LOS	Loss of Signal
LUT	Lookup Table
NV	Nonvolatile
QT	Quick Trip
TIA	Transimpedance Amplifier
ROSA	Receiver Optical Subassembly
SEE	Shadowed EEPROM
SFF	Small Form Factor
SFF-8472	Document Defining Register Map of SFPs and SFFs
SFP	Small Form Factor Pluggable
SFP+	Enhanced SFP

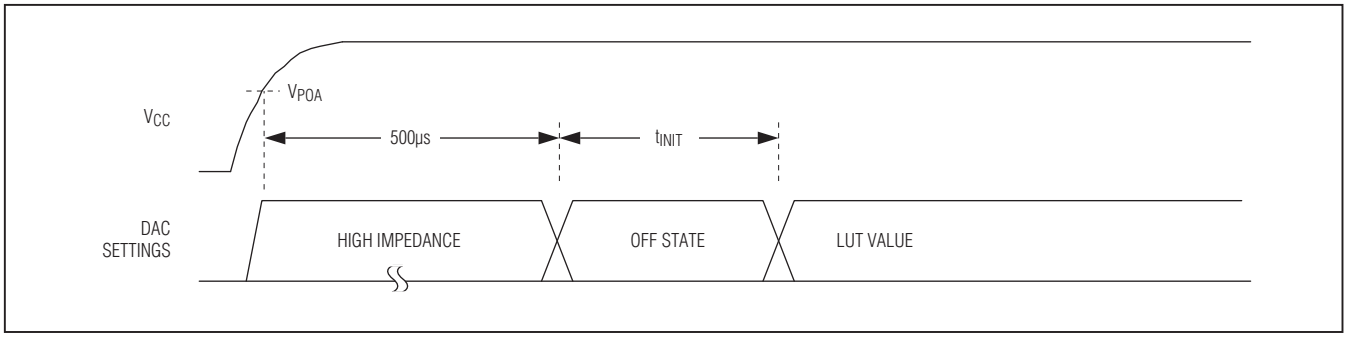


Figure 1. Power-Up Timing

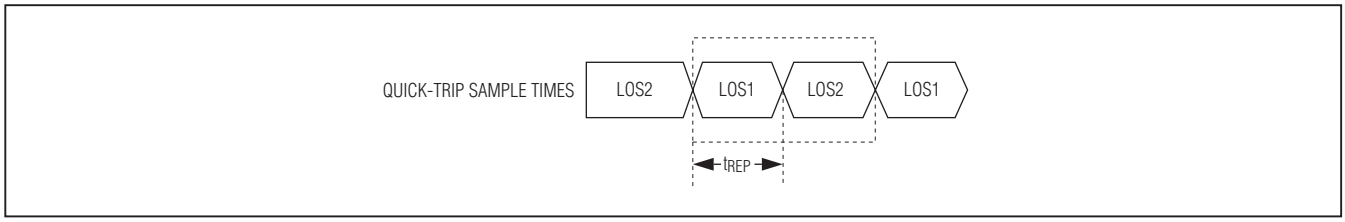


Figure 2. Quick-Trip Sample Timing

Monitors and Fault Detection

Monitors

Monitoring functions on the device include two QT comparators and four ADC channels. This monitoring combined with the alarm enables (Table 01h/05h) determines when/if the device triggers the FAULT and/or LOSOUT outputs. All the monitoring levels and interrupt masks are user programmable.

Two Quick-Trip Monitors and Alarms

Two quick-trip monitors are provided that monitor the following:

1) Loss of signal 1 (LOS1 LO)
2) Loss of signal 2 (LOS2 LO)

The LOS_ LO QTs compare the RSSI_ input against its threshold setting to determine if the present received power is below the specification. The LOS_ LO QT can be used to set the LOSOUT pin.

Four ADC Monitors and Alarms

The ADC monitors 4 channels that measure temperature (internal temp sensor), V_{CC}, RSSI1, and RSSI2 using an analog multiplexer to measure them round-robin with a single ADC (see the *ADC Timing* section). The 3V channels have a customer-programmable full-scale range, and all channels have a customer-programmable offset value that is factory programmed to a default value (see Table 2). Additionally, RSSI1 and RSSI2 can right-shift results by up to 7 bits before the results are compared to alarm thresholds or read over the I^2C bus. This allows customers with specified ADC ranges to calibrate the ADC full scale to a factor of $1/2^n$ of their specified range to measure small signals. The device can then right-shift the results by n bits to maintain the bit weight of their specification (see the *Right-Shifting ADC Result* section).

The ADC results (after right-shifting, if used) are compared to the alarm and warning thresholds after each conversion, and the corresponding alarms are set that can be used to trigger the FAULT output. These ADC thresholds are user programmable, as are the masking registers that can be used to prevent the alarms from triggering the FAULT output.

ADC Timing

There are four analog channels that are digitized in a round-robin fashion in the order as shown in Figure 3. The total time required to convert all 4 channels is t_{RR} (see the *Analog Voltage Monitoring Characteristics* for details).

Right-Shifting ADC Result

If the weighting of the ADC digital reading must conform to a predetermined full-scale (PFS) value defined by a standard's specification (e.g., SFF-8472), then right-shifting can be used to adjust the PFS analog measurement range while maintaining the weighting of the ADC results. The device's range is wide enough to cover all requirements; when the maximum input value is $\leq$ 1/2 the FS value, right-shifting can be used to obtain greater accuracy. For instance, the maximum voltage might be 1/8 the specified PFS value, so only 1/8 of the converter's range is effective over this range. An alternative is to calibrate the ADC's full-scale range to 1/8 the readable PFS value and use a right-shift value of 3. With this implementation, the resolution of the measurement is increased by

Table 2. ADC Default Monitor Full-Scale Ranges

SIGNAL (UNITS)	+FS SIGNAL	+FS HEX	-FS SIGNAL	-FS HEX
Temperature (°C)	127.996	7FFF	-128	8000
V_{CC} (V)	6.5528	FFF8	0	0000
RSSI1, RSSI2 (V)	2.4997	FFF8	0	0000

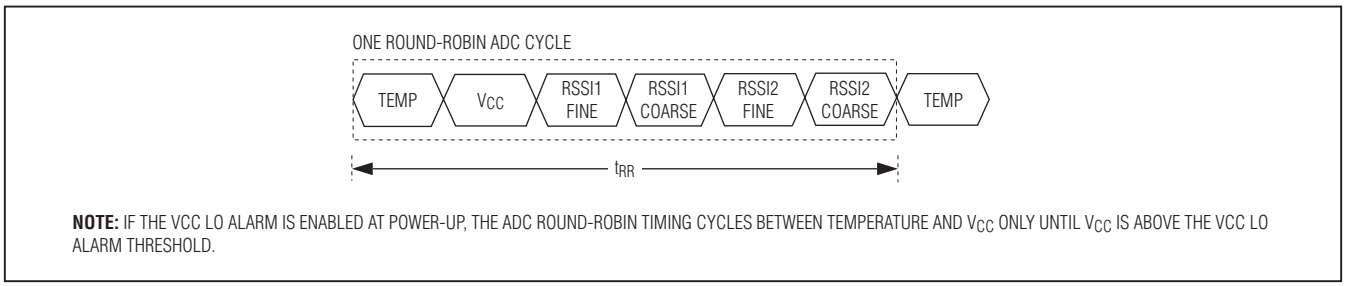


Figure 3. ADC Round-Robin Timing

a factor of 8, and because the result is digitally divided by 8 by right-shifting, the bit weight of the measurement still meets the standard's specification (i.e., SFF-8472).

The right-shift operation on the ADC result is carried out based on the contents of right-shift control registers (Table 02h, Registers 8Eh–8Fh) in EEPROM. Two analog channels—RSSI1 and RSSI2—each have 3 bits allocated to set the number of right-shifts. Up to seven right-shift operations are allowed and are executed as a part of every conversion before the results are compared to the high and low alarm levels, or loaded into their corresponding measurement registers (Lower Memory, Registers 64h to 6Bh). This is true during the setup of internal calibration as well as during subsequent data conversions.

Differential RSSI1/RSSI2 Inputs

The device offers fully differential inputs for RSSI1 and RSSI2. This enables high-side monitoring of RSSI, as shown in Figure 4. It also reduces board complexity by eliminating the need for a high-side differential amplifier or a current mirror.

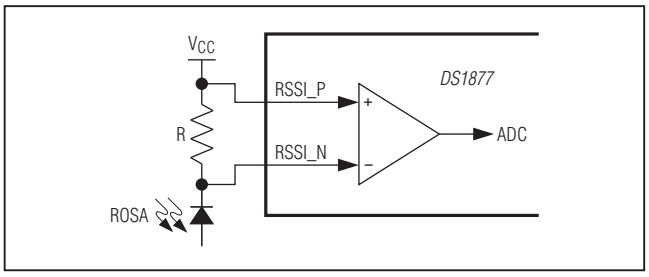


Figure 4. RSSI1/RSSI2 Differential Input for High-Side RSSI

Enhanced RSSI Monitoring (Dual-Range Functionality)

The device offers a feature to improve the accuracy and range of RSSI1/RSSI2, which is most commonly used for monitoring RSSI. Using a traditional input, the RSSI measurement accuracy can be increased at the cost of reduced input signal swing. The device eliminates this trade-off by offering "dual-range" calibration on the RSSI1/RSSI2 channels. The dual-range calibration can operate in two modes: crossover enabled and crossover disabled. Dual-range operation is enabled by default (factory programmed in EEPROM). However, it can easily be disabled by the RSSIn_FC and RSSIn_FF bits (where n can be 1 or 2) in 8Dh, Table 02h.

Dual-range functionality consists of two ADC modes of operation: fine mode and coarse mode. Each mode is calibrated for a unique transfer function, hence the term, dual range. Table 3 highlights the registers related to RSSI1/RSSI2. Fine mode is calibrated using the gain, offset, and right-shifting registers at locations shown in Table 3, and is ideal for relatively small analog-input voltages. Coarse mode is automatically switched to when the input exceeds a threshold. Coarse mode is calibrated using different gain and offset registers from fine mode. The gain and offset registers for coarse mode are also shown in Table 3. Additional information for each of the registers can be found in the memory map (Figure 14).

Table 3. RSSI1/RSSI2 Configuration Registers

REGISTER	FINE MODE	COARSE MODE
RSSI1/RSSI2 Gain (RSSI1/2 FINE/COARSE SCALE)	9Eh–9Fh/9Ah–9Bh, Table 02h	9Ch–9Dh/98h–99h, Table 02h
RSSI1/RSSI2 Offset (RSSI1/2 FINE/COARSE OFFSET)	AEh–AFh/AAh–ABh, Table 02h	ACh–ADh/A8h–A9h, Table 02h
Right-Shift ($RSHIFT_1$, $RSHIFT_2$)	8Eh–8Fh, Table 02h	8Eh–8Fh, Table 02h
Crossover (XOVER1/XOVER2 FINE/COARSE)	A6h–A7h/96h–97h, Table 02h	A4h–A5h/94h–95Fh, Table 02h
FORCE RSSI (RSSIn_FC and RSSIn_FF Bits)	8Dh, Table 02h	
UPDATE (RSSIR Bit)	6Fh, Lower Memory	
RSSI VALUE (RSSI1/RSSI2 Measurement)	68h–69h, Lower Memory	

Dual-range operation is transparent to the end user. The results of RSSI1/RSSI2 ADCs are still stored/reported in the same memory locations (68h–69h, Lower Memory) regardless of whether the conversion was performed in fine mode or coarse mode. The RSSIR bit indicates whether a fine or coarse conversion generated the digital result.

When the device is powered up, ADCs begin in a round-robin fashion. Every RSSI1/RSSI2 time slice begins with a fine mode ADC (using fine mode's gain, offset, and right-shifting settings). If the value is too large for a fine conversion, a coarse conversion is performed and the result is reported. The coarse-mode conversion is performed using the coarse gain and offset settings. The intersection between coarse and fine depends on the crossover mode used.

The RSSIn_FC and RSSIn_FF bits are used to force fine-mode or coarse-mode conversions or to disable the dual-range functionality. Dual-range functionality is enabled by default (both RSSIn_FC and RSSIn_FF are factory programmed to 0 in EEPROM). Dual-range functionality can be disabled by setting RSSIn_FC to 0 and RSSIn_FF to 1. These bits are also useful when calibrating RSSI1/RSSI2. See the register descriptions and memory map for additional information.

Crossover Enabled

For systems with a nonlinear relationship between the ADC input and desired ADC result, the mode should be set to crossover enabled (Figure 5). The RSSI measurement of an APD receiver is one such application. Using the crossover-enabled mode allows a piecewise linear approximation of the nonlinear response of the APD's gain factor. The crossover point is the value where the fine and coarse ranges intersect. The ADC result transitions between the fine and coarse ranges as defined by the XOVER registers. Right-shifting, slope adjustment, and offset are configurable for both the fine and coarse ranges. The XOVER1/XOVER2 FINE registers determine the maximum results returned by the fine ADC conversions before right-shifting. The XOVER1/XOVER2 COARSE registers determine the minimum results returned by coarse ADC conversions before right-shifting.

Crossover Disabled

The crossover-disabled mode is intended for systems with a linear relationship between the RSSI1/RSSI2 input and the desired ADC result. The ADC result transitions between the fine and coarse ranges with hysteresis, as shown in Figure 6.

In crossover-disabled mode, the thresholds between coarse and fine mode are a function of the number of right-shifts being used. With the use of right-shifting, the fine-mode full scale is programmed to ($1/2^n$) of the coarse-mode full scale. The device now automatically ranges to choose the range that gives the best resolution for the measurement. Table 4 shows the threshold values for each possible number of right-shifts.

Low-Voltage Operation

The device contains two power-on reset (POR) levels. The lower level is a digital POR (POD) and the higher level is an analog POR (POA). At startup, before the supply voltage rises above POA, the outputs are disabled, all SRAM locations are set to their defaults, shadowed EEPROM (SEE) locations are zero, and all analog circuitry is disabled. When V_{CC} reaches POA, the SEE is recalled, and the analog circuitry is enabled. While V_{CC} remains above POA, the device is in its normal operating state, and it responds based on its nonvolatile configuration. If during operation V_{CC} falls below POA, but is still above POD, the SRAM retains the SEE settings from the first SEE recall, but the device analog is shut down and the outputs disabled. If the supply voltage recovers back above POA, the device immediately resumes normal operation. If the supply voltage falls below POD, the device SRAM is placed in its default state and another SEE recall is required to reload the nonvolatile settings. The EEPROM recall occurs the next time V_{CC} next exceeds POA. Figure 7 shows the sequence of events as the voltage varies.

Table 4. RSSI1/RSSI2 Hysteresis Threshold Values

NO. OF RIGHT-SHIFTS	FINE MODE MAX (HEX)	COARSE MODE MIN* (HEX)
0	FFF8	F000
1	7FFC	7800
2	3FFE	3C00
3	1FFF	1E00
4	0FFF	0F00
5	07FF	0780
6	03FF	03C0
7	01FF	01E0

**This is the minimum reported coarse-mode conversion.*

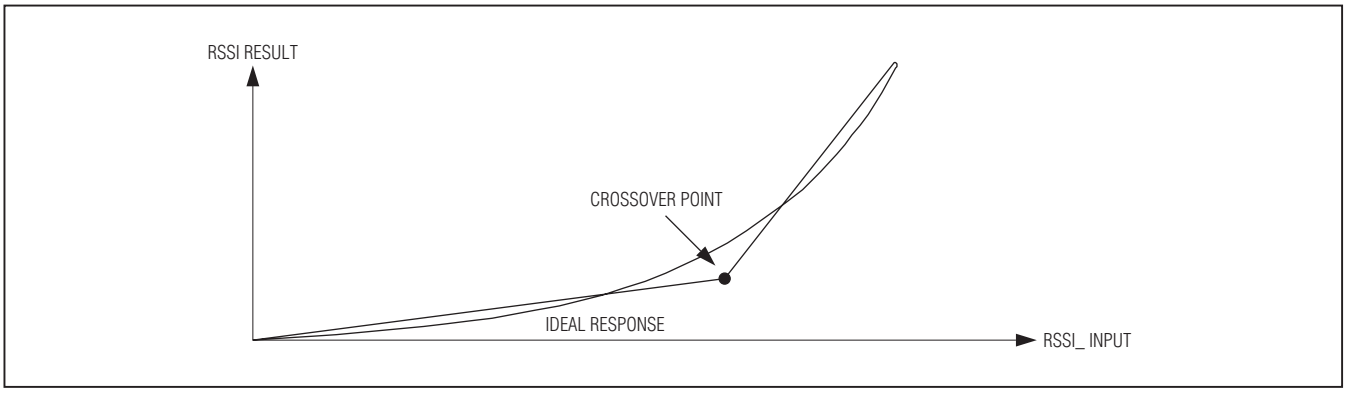


Figure 5. Crossover Enabled

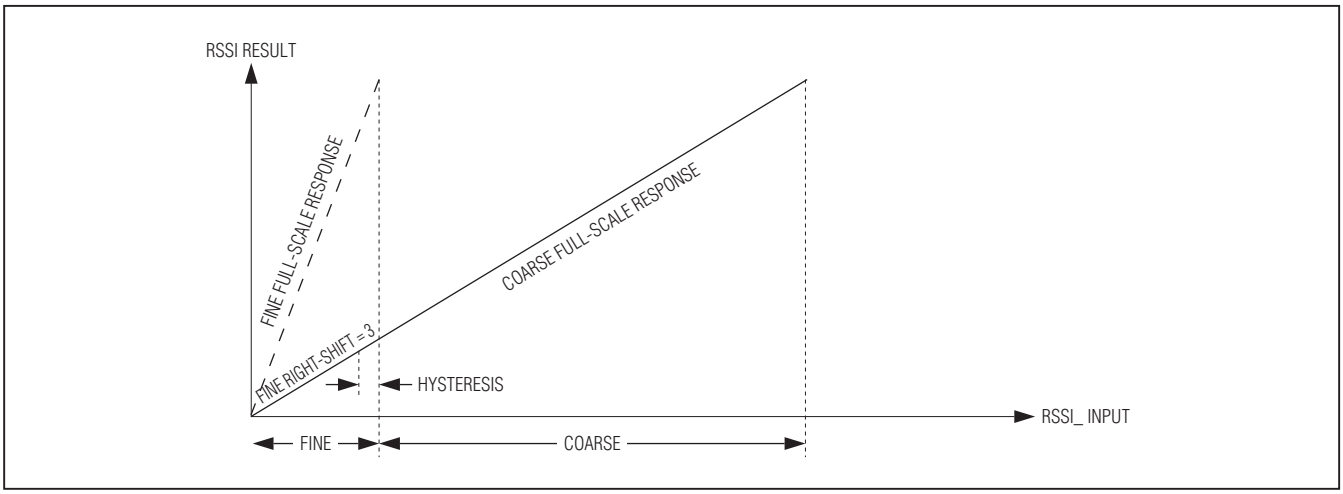


Figure 6. Crossover Disabled

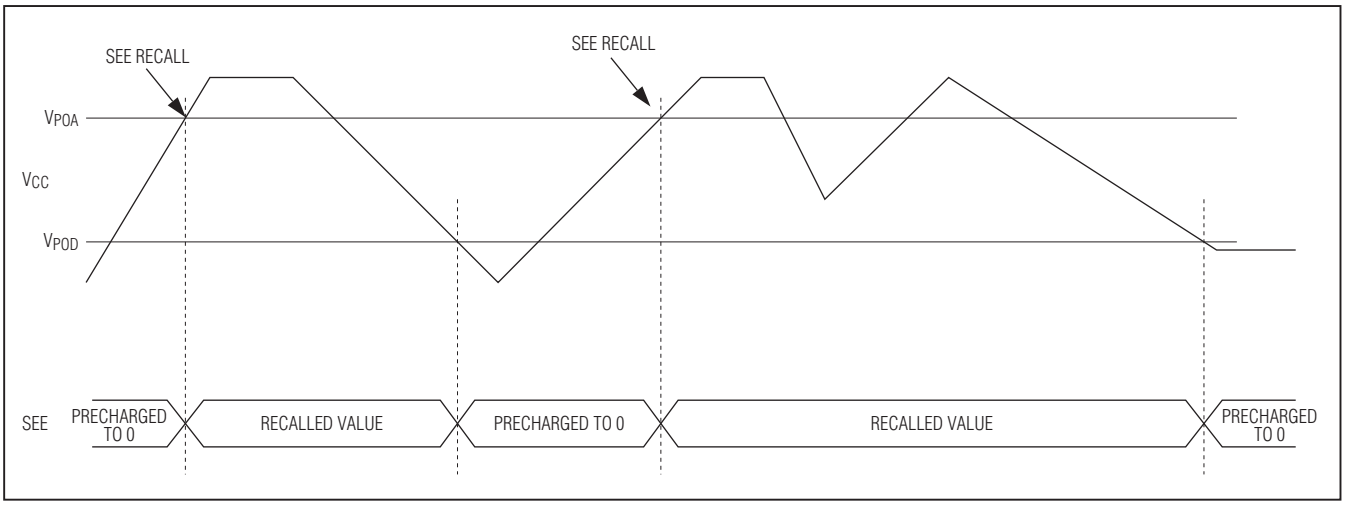


Figure 7. Low-Voltage Operation

Any time V_{CC} is above POD, the I^2C interface can be used to determine if V_{CC} is below the POA level. This is accomplished by checking the RDYB bit in the STATUS byte (Lower Memory, Register 6Eh). RDYB is set when V_{CC} is below POA; when V_{CC} rises above POA, RDYB is timed (within 500µs) to go to 0, at which point the part is fully functional.

For all device addresses sourced from EEPROM (Table 02h, Register 8Bh), the default device address is A2h until V_{CC} exceeds POA, allowing the device address to be recalled from the EEPROM.

Delta-Sigma Outputs

The device's delta-sigma outputs are 10 bits. For illustrative purposes, a 3-bit example is provided in Figure 8.

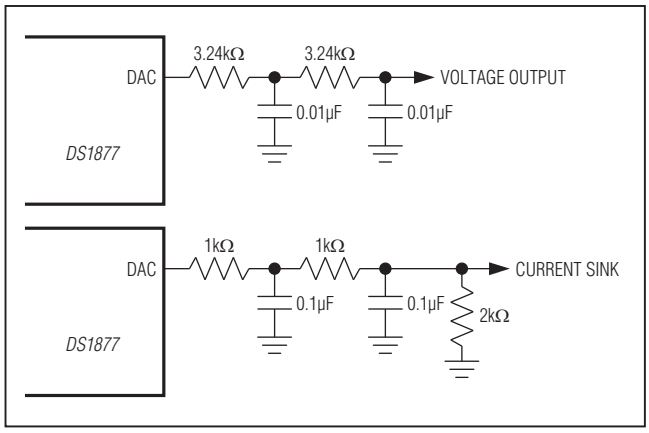


Figure 8. Recommended RC Filter for DAC Outputs

Each possible output of this 3-bit delta-sigma DAC is provided in Figure 9.

In LUT mode the DACs are each controlled by an LUT with high-temperature resolution and an OFFSET LUT with lower temperature resolution. The high-resolution LUTs each have 2°C resolutions. The OFFSET LUTs are located in the upper eight registers (F8h–FFh, Table 04h) of the table containing each high-resolution LUT. The DAC values are determined as follows:

DAC value = DAC LUT + 4 x (DAC OFFSET LUT)

An example calculation for DAC1 is as follows:

Assumptions:

1) Temperature is +43°C
2) Table 04h (DAC OFFSET LUT), Register FCh = 2Ah
3) Table 04h (DAC LUT), Register AAh = 7Bh

Because the temperature is +43°C, the DAC LUT index is AAh and the DAC1 OFFSET LUT index is FCh.

DAC1 = 7Bh + 4 x 2Ah = 123h = 291

When temperature controlled, the DACs are updated after each temperature conversion. See Figure 10.

The reference input, REFIN, is the supply voltage for the output buffer of all the DACs. The voltage connected to REFIN must be able to support the edge rate requirements of the delta-sigma outputs. In a typical application, a 0.1µF capacitor should be connected between REFIN and ground.

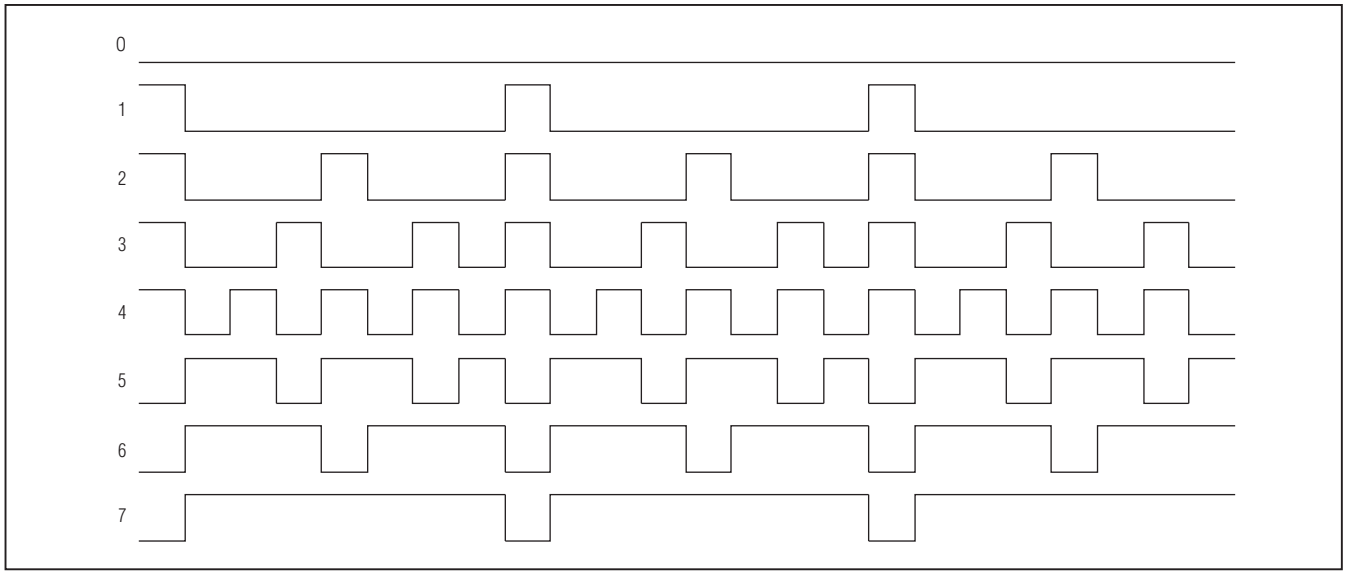


Figure 9. 3-Bit (8-Position) Delta-Sigma Example

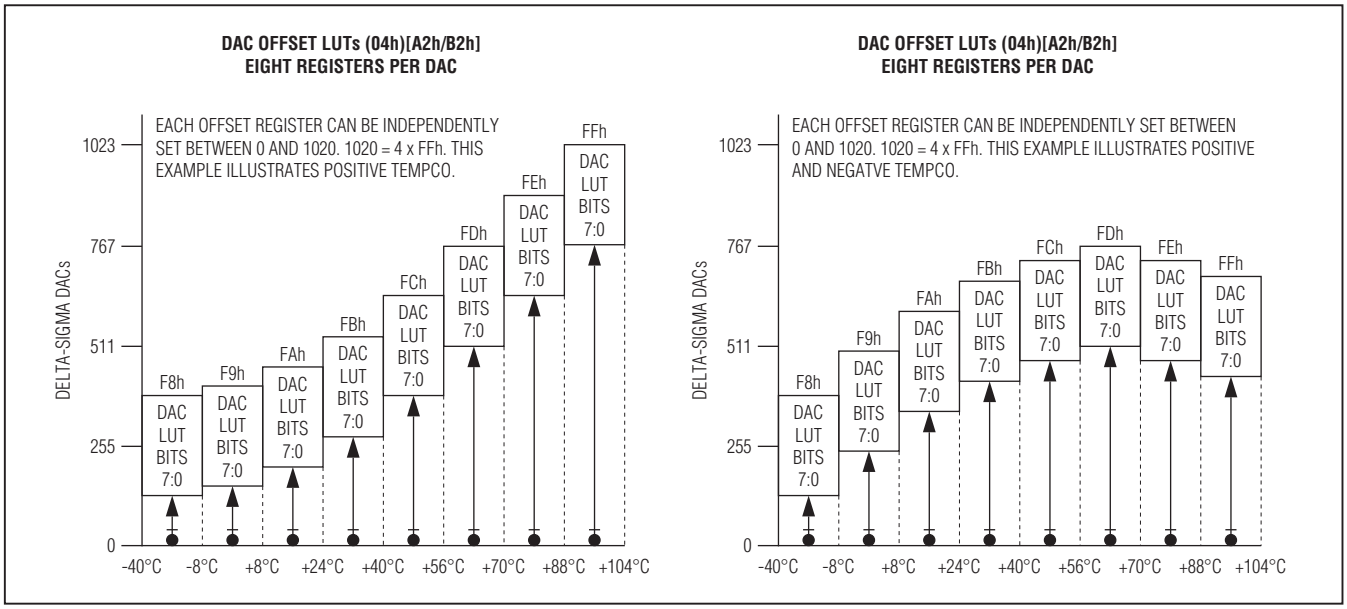


Figure 10. DAC Offset LUTs

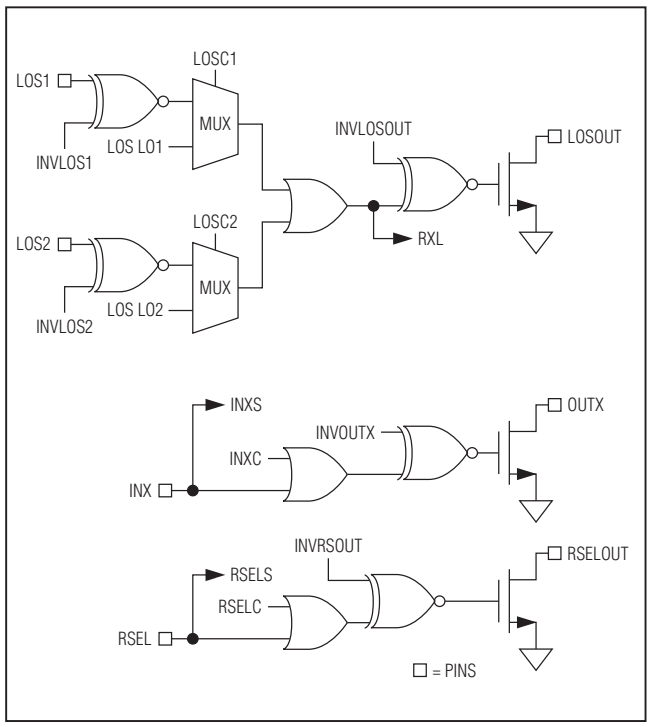


Figure 11. Logic Diagram

Digital I/O Pins

Four digital input pins and four digital output pins are provided for monitoring and control.

LOS1, LOS2, and LOSOUT

When LOSC_ = 0 (Table 02h, Register 8Ah), the LOS_ pin is used to convert a standard comparator output for LOS to an open-collector output. The output of the mux can be read in the STATUS register (Lower Memory, Register 6Eh) as the RXL bit. The RXL signal can be inverted (INVLOS_ = 1) before driving the open-drain output transistor using the XOR gate provided. Setting LOSC_ = 1 configures the mux to be controlled by the LOS LO QT alarm. The mux setting (stored in EEPROM) does not take effect until V_{CC} > POA, allowing the EEPROM to recall.

INX, RSEL, OUTX, RSELOUT

Digital input pins INX and RSEL primarily serve to meet the rate-select requirements of SFP and SFP+. They can also serve as general-purpose inputs. OUTX and RSELOUT are driven by a combination of the INX, RSEL, and logic dictated by control registers in the EEPROM (see Figure 11). The levels of INX and RSEL can be read from the STATUS register (Lower Memory, Register 6Eh). The open-drain output OUTX can be controlled and/or inverted using the CNFGB register (Table 02h, Register 89h). The open-drain RSELOUT output is software controlled and/or inverted through the STATUS register and

CNFGA register (Table 02h, Register 88h). External pullup resistors must be provided on OUTX and RSELOUT to realize high logic levels.

FAULT Output

FAULT can be triggered by all alarms, warnings, and QTs. The six ADC alarms, warnings, and LOS QTs require enabling (Table 01h/05h, Registers F8h and FCh). Latching of the alarms is controlled by the CNFGB and CNFGC registers (Table 02h, Registers 89h–8Ah).

Die Identification

The device has an ID hardcoded in its die. Two registers (Table 02h, Registers 86h–87h) are assigned for this feature. Register 86h reads 77h to identify the part as the DS1877; Register 87h reads the present device version.

I²C Communication

I²C Definitions

The following terminology is commonly used to describe I²C data transfers.

Master Device: The master device controls the slave devices on the bus. The master device generates SCL clock pulses and START and STOP conditions.

Slave Devices: Slave devices send and receive data at the master's request.

Bus Idle or Not Busy: Time between STOP and START conditions when both SDA and SCL are inactive and in their logic-high states.

START Condition: A START condition is generated by the master to initiate a new data transfer with a slave. Transitioning SDA from high to low while SCL remains high generates a START condition. See Figure 12 for applicable timing.

STOP Condition: A STOP condition is generated by the master to end a data transfer with a slave. Transitioning SDA from low to high while SCL remains high generates a STOP condition. See Figure 12 for applicable timing.

Repeated START Condition: The master can use a repeated START condition at the end of one data transfer to indicate that it will immediately initiate a new data transfer following the current one. Repeated STARTs are commonly used during read operations to identify a specific memory address to begin a data transfer. A repeated START condition is issued identically to a normal START condition. See Figure 12 for applicable timing.

Bit Write: Transitions of SDA must occur during the low state of SCL. The data on SDA must remain valid and unchanged during the entire high pulse

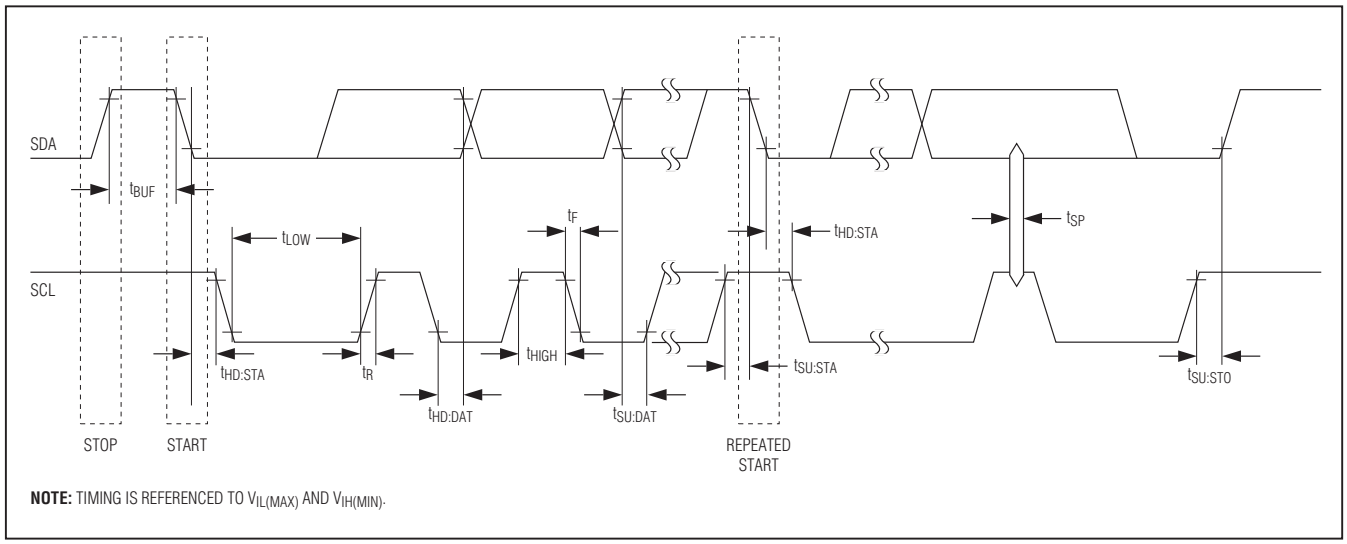


Figure 12. I²C Timing

of SCL plus the setup and hold time requirements (Figure 12). Data is shifted into the device during the rising edge of the SCL.

Bit Read: At the end of a write operation, the master must release the SDA bus line for the proper amount of setup time (Figure 12) before the next rising edge of SCL during a bit read. The device shifts out each bit of data on SDA at the falling edge of the previous SCL pulse and the data bit is valid at the rising edge of the current SCL pulse. Remember that the master generates all SCL clock pulses, including when it is reading bits from the slave.

Acknowledgement (ACK and NACK): An acknowledgement (ACK) or not-acknowledge (NACK) is always the 9th bit transmitted during a byte transfer. The device receiving data (the master during a read or the slave during a write operation) performs an ACK by transmitting a zero during the 9th bit. A device performs a NACK by transmitting a one during the 9th bit. Timing (Figure 12) for the ACK and NACK is identical to all other bit writes. An ACK is the acknowledgment that the device is properly receiving data. A NACK is used to terminate a read sequence or as an indication that the device is not receiving data.

Byte Write: A byte write consists of 8 bits of information transferred from the master to the slave (most significant bit first) plus a 1-bit acknowledgement from the slave to the master. The 8 bits transmitted by the master are done according to the bit write definition and the acknowledgement is read using the bit read definition.

Byte Read: A byte read is an 8-bit information transfer from the slave to the master plus a 1-bit ACK or NACK from the master to the slave. The 8 bits of information that are transferred (most significant bit first) from the slave to the master are read by the master using the bit read definition, and the master transmits an ACK using the bit write definition to receive additional data bytes. The master must NACK the last byte read to terminate communication so the slave returns control of SDA to the master.

Slave Address Byte: Each slave on the I²C bus responds to a slave address byte sent immediately following a START condition. The slave address byte contains the slave address in the most significant 7 bits and the R/$\overline{W}$ bit in the least significant bit.

The device responds to three slave addresses. The auxiliary memory always responds to a fixed I²C slave address, A0h. (If the main device's slave address is programmed to be A0h/B0h, access to the auxiliary memory is disabled.) The Lower Memory and Tables 00h–05h respond to I²C slave addresses whose lower 3 bits are configurable (A0h–AEh, B0h–BEh) using the DEVICE ADDRESS byte (Table 02h, Register 8Bh). The user also must set the ASEL bit (Table 02h, Register 88h) for this address to be active. By writing the correct slave address with R/$\overline{W}$ = 0, the master indicates it writes data to the slave. If R/$\overline{W}$ = 1, the master reads data from the slave. If an incorrect slave address is written, the device assumes the master is communicating with another I²C device and ignores the communications until the next START condition is sent.

Memory Address: During an I²C write operation to the device, the master must transmit a memory address to identify the memory location where the slave is to store the data. The memory address is always the second byte transmitted during a write operation following the slave address byte.

I²C Protocol

See Figure 13 for an example of I²C timing.

Writing a Single Byte to a Slave: The master must generate a START condition, write the slave address byte (R/$\overline{W}$ = 0), write the memory address, write the byte of data, and generate a STOP condition. Remember that the master must read the slave's acknowledgement during all byte write operations.

Writing Multiple Bytes to a Slave: To write multiple bytes to a slave, the master generates a START condition, writes the slave address byte (R/$\overline{W}$ = 0), writes the memory address, writes up to 8 data bytes, and generates a STOP condition. The device writes 1 to 8 bytes (one page or row) with a single write transaction. This is internally controlled by an address counter that allows data to be written to consecutive addresses without transmitting a memory address before each data byte is sent. The address counter limits the write to one 8-byte page (one row of the memory map). Attempts to write to additional pages of memory without sending a STOP condition between pages result in the address counter wrapping around to the beginning of the present row.

For example: A 3-byte write starts at address 06h and writes three data bytes (11h, 22h, and 33h) to three "consecutive" addresses. The result is that addresses 06h and 07h would contain 11h and 22h, respectively, and the third data byte, 33h, would be written to address 00h.

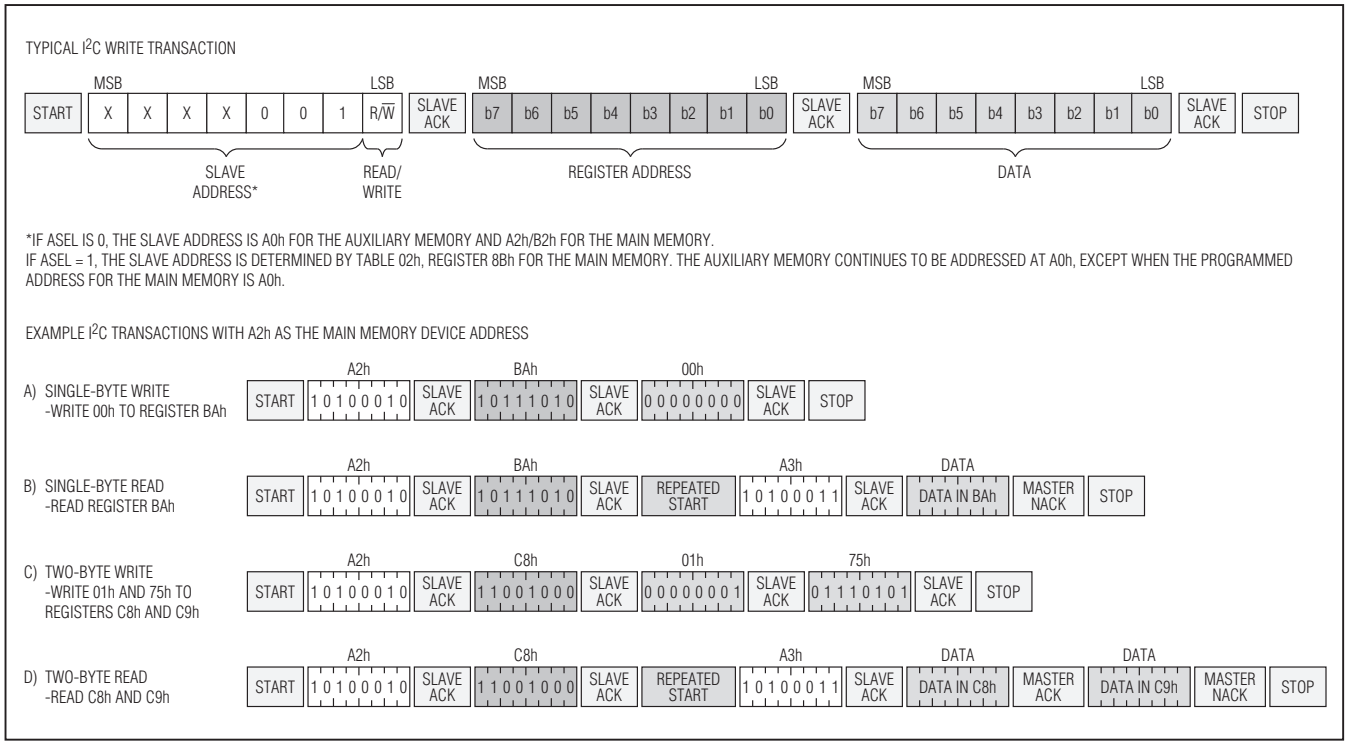


Figure 13. Example I²C Timing

To prevent address wrapping from occurring, the master must send a STOP condition at the end of the page, then wait for the bus-free or EEPROM write time to elapse. Then the master can generate a new START condition and write the slave address byte ($R/\overline{W}$ = 0) and the first memory address of the next memory row before continuing to write data.

Acknowledge Polling: Any time a EEPROM page is written, the device requires the EEPROM write time (t_{WR}) after the STOP condition to write the contents of the page to EEPROM. During the EEPROM write time, the device does not acknowledge its slave address because it is busy. It is possible to take advantage of that phenomenon by repeatedly addressing the device, which allows the next page to be written as soon as the device is ready to receive the data. The alternative to acknowledge polling is to wait for maximum period of t_{WR} to elapse before attempting to write again to the device.

EEPROM Write Cycles: When EEPROM writes occur, the device writes the whole EEPROM memory page, even if only a single byte on the page was modified. Writes that do not modify all 8 bytes on the page are allowed and do not corrupt the remaining bytes of memory on the same page. Because the whole page is written, bytes on the page that were not modified during the transaction are still subject to a write cycle. This can result in a whole page being worn out over time by writing a single byte repeatedly. Writing a page 1 byte at a time wears the EEPROM out 8x faster than writing the entire page at once. The device's EEPROM write cycles are specified in the *Nonvolatile Memory Characteristics* table. The specification shown is at the worst-case temperature. It can handle approximately 10x that many writes at room temperature. Writing to SRAM-shadowed EEPROM memory with SEEB = 1 does not count as a EEPROM write cycle when evaluating the EEPROM's estimated lifetime.

Reading a Single Byte from a Slave: Unlike the write operation that uses the memory address byte to define where the data is to be written, the read operation occurs at the present value of the memory address counter. To read a single byte from the slave, the master generates a START condition, writes the slave address byte with R/$\overline{W}$ = 1, reads the data byte with a NACK to indicate the end of the transfer, and generates a STOP condition.

Manipulating the Address Counter for Reads: A dummy write cycle can be used to force the address pointer to a particular value. To do this, the master generates a START condition, writes the slave address byte (R/$\overline{W}$ = 0), writes the memory address where it desires to read, generates a repeated START condition, writes the slave address byte (R/$\overline{W}$ = 1), reads data with ACK or NACK as applicable, and generates a STOP condition.

Memory Organization

The device features memory tables that are internally organized into 8-byte rows. The main device located at A2h is used for overall device configuration and receiver 1 control, calibration, alarms, warnings, and monitoring.

Lower Memory, A2h is addressed from 00h–7Fh and contains alarm and warning thresholds, flags, masks, several control registers, password entry area (PWE), and the table-select byte.

Table 01h, A2h primarily contains user EEPROM (with PW1 level access) as well as alarm and warning enable bytes.

Table 02h, A2h is a multifunction space that contains configuration registers, scaling and offset values, passwords, and interrupt registers as well as other miscellaneous control bytes.

Table 04h, A2h contains a temperature-indexed LUT for control of the DAC1 voltage. The DAC1 LUT can be programmed in 2°C increments over the -40°C to +102°C range. It also contains an LUT for temperature-controlled offsets for DAC1.

Table 05h, A2h is empty by default. It can be configured to contain the alarm and warning enable bytes from Table 01h, Registers F8h–FFh with the MASK bit enabled (Table 02h, Register 88h). In this case Table 01h is empty.

The main device located at B2h is used for receiver 2 control, calibration, alarms, warnings, and monitoring.

Lower Memory, B2h is addressed from 00h–7Fh and contains alarm and warning thresholds, flags, masks, several control registers, PWE, and the table-select byte.

Table 01h, B2h contains alarm and warning enable bytes.

Table 02h, B2h is a multifunction space that contains configuration registers, scaling and offset values, passwords, interrupt registers as well as other miscellaneous control bytes. Table 02h, B2h only contains functions related to receiver 2. All other functions are controlled by Table 02h, A2h.

Table 04h, B2h contains a temperature-indexed LUT for control of the DAC2 voltage. The DAC2 LUT can be programmed in 2°C increments over the -40°C to +102°C range. It also contains an LUT for temperature-controlled offsets for DAC2.

Table 05h, B2h is empty by default. It can be configured to contain the alarm and warning-enable bytes from Table 01h, Registers F8h–FFh with the MASK bit enabled (Table 02h, Register 88h). In this case Table 01h is empty.

Auxiliary Memory (Device A0h) contains 256 bytes of EE memory accessible from address 00h–FFh. It is selected with the device address of A0h.

See the *Register Descriptions* section for a more complete detail of each byte's function, as well as for read/write permissions for each byte.

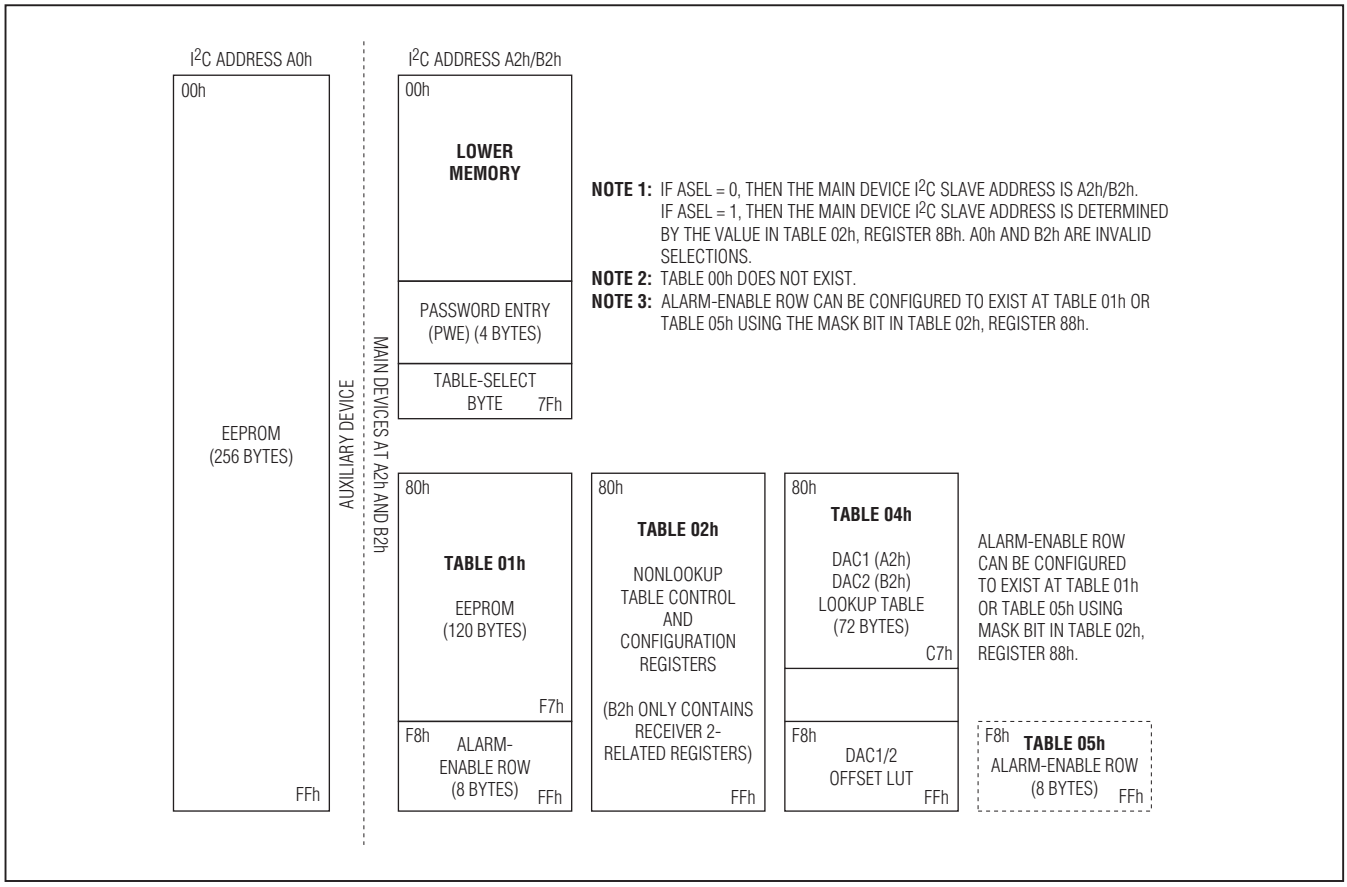


Figure 14. Memory Map

Shadowed EEPROM

Many nonvolatile memory locations (listed within the *Register Descriptions* section) are actually shadowed EEPROM and are controlled by the SEEB bit in Table 02h, Register 80h.

The device incorporates shadowed EEPROM memory locations for key memory addresses that can be written many times. By default the shadowed EEPROM bit, SEEB, is not set and these locations act as ordinary EEPROM. By setting SEEB, these locations function like SRAM cells, which allow an infinite number of write cycles without concern of wearing out the EEPROM. This also eliminates the requirement for the EEPROM write time, t_{WR}. Because changes made with SEEB enabled do not affect the EEPROM, these changes are not retained through power cycles. The power-on value is the last value written with SEEB disabled. This function can be used to limit the number of EEPROM writes during calibration or to change the monitor thresholds periodically during normal operation helping to reduce the number of times EEPROM is written. Figure 14 shows the memory map and indicates which locations are shadowed EEPROM.

Register Descriptions

The register maps show each byte/word (2 bytes) in terms of its row in the memory. The first byte in the row is located in memory at the row address (hexadecimal) in the leftmost column. Each subsequent byte on the row is one/two memory locations beyond the previous byte/word's address. A total of 8 bytes are present on each row. For more information about each of these bytes, see the corresponding register description.

Memory Map Access Codes

The following section provides the device's register definitions. Each register or row of registers has an access descriptor that determines the password level required to read or write the memory. Level 2 password is intended for the module manufacture access only. Level 1 password allows another level of protection for items the end consumer wishes to protect. Many registers are always readable, but require password access to write. There are a few registers that cannot be read without password access. The following access codes describe each mode the device uses with factory settings for the PW_ENA and PW_ENB (Table 02h, Registers C0h–C1h) registers.

ACCESS CODE	READ ACCESS	WRITE ACCESS
<0/_>	At least 1 byte/bit in the row/byte is different than the rest of the row/byte, so look at each byte/bit separately for permissions.	
<1/_>	Read all	Write PW2
<2/_>	Read all	Write not applicable
<3/_>	Read all	Write all, but the device hardware also writes to these bytes/bits
<4/_>	Read PW2	Write PW2 + mode_bit
<5/_>	Read all	Write all
<6/_>	Read not applicable	Write all
<7/_>	Read PW1	Write PW1
<8/_>	Read PW2	Write PW2
<9/_>	Read not applicable	Write PW2
<10/_>	Read PW2	Write not applicable
<11/_>	Read all	Write PW1

Memory Addresses A0h, A2h, and B2h

There are three separate I²C addresses in the device: A0h, A2h, and B2h. A2h and B2h are used to configure and monitor two receivers. Receiver 1 is accessed using A2h. Receiver 2 is accessed using B2h. Many of the registers in A2h and B2h are shared registers. These registers can be read and written from both A2h and B2h.

MEMORY CODE	A2h AND B2h REGISTERS
<C> or <_/C>	A common memory location is used for A2h and B2h device addresses. Reading or writing to these locations is identical, regardless of using A2h or B2h addresses.
<D> or <_/D>	Different memory locations are used for A2h and B2h device addresses.
<M> or <_/M>	Mixture of common and different memory locations for A2h and B2h device addresses. See the individual bytes within the row for clarification. If "M" is used on an individual byte, see the expanded bit descriptions to determine which bits are common vs. different.