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19-5537; Rev 1; 8/11

SFP+ Controller with Digital LDD Interface

DS1878

General Description

The DS1878 controls and monitors all functions for SFF, SFP, and SFP+ modules including all SFF-8472 functionality. The combination of the DS1878 with Maxim laser driver/limiting amplifier solutions supports VCSEL, DFB, and EML-based solutions. The device provides APC loop, modulation current control, and eye safety functionality. It continuously monitors for high output current, high bias current, and low and high transmit power to ensure that laser shutdown for eye safety requirements are met without adding external components. Six ADC channels monitor V_{CC}, temperature, and four external monitor inputs (MON1–MON4) that can be used to meet all monitoring requirements. MON3 is differential with support for common mode to V_{CC}. Two digital-to-analog (DAC) outputs with temperature-indexed lookup tables (LUTs) are available for additional control functionality.

Applications

SFF, SFP, and SFP+ Transceiver Modules

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
DS1878T+	-40°C to +95°C	28 TQFN-EP*
DS1878T+T&R	-40°C to +95°C	28 TQFN-EP*

+Denotes a lead(Pb)-free/RoHS-compliant package.
T&R = Tape and reel.
**EP = Exposed pad.*

Features

- **Meets All SFF-8472 Control and Monitoring Requirements**
- **Laser Bias Controlled by APC Loop and Temperature LUT to Compensate for Tracking Error**
- **Laser Modulation Controlled by Temperature LUT**
- **Six Analog Monitor Channels: Temperature, V_{CC}, MON1–MON4**
  - **MON1–MON4 Support Internal and External Calibration**
  - **Scalable Dynamic Range**
  - **Internal Direct-to-Digital Temperature Sensor**
  - **Alarm and Warning Flags for All Monitored Channels**
- **Two 9-Bit Delta-Sigma Outputs with 36 Entry Temperature LUTs**
- **Digital I/O Pins: Five Inputs, Four Outputs**
- **Comprehensive Fault-Measurement System with Maskable Laser Shutdown Capability**
- **Flexible, Two-Level Password Scheme Provides Three Levels of Security**
- **256 Additional Bytes Located at A0h Slave Address**
- **I^2C-Compatible Interface**
- **3-Wire Master to Communicate with a Maxim Laser Driver/Limiting Amplifier**
- **+2.85V to +5.5V Operating Voltage Range**
- **-40°C to +95°C Operating Temperature Range**
- **28-Pin TQFN (5mm x 5mm x 0.75mm) Package**

SFP+ Controller with Digital LDD Interface

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ABSOLUTE MAXIMUM RATINGS

Voltage Range on MON1–MON4, RSEL, CSEL1OUT, CSEL2OUT, SCLOUT, SDAOUT, TXDOUT, IN1, LOS, TXF, TXFOUT, and TXD Pins Relative to Ground .....-0.5V to (V_{CC} + 0.5V)*
Voltage Range on V_{CC}, SDA, SCL, RSELOUT, and LOSOUT Pins Relative to Ground .....-0.5V to +6V

**Subject to not exceeding +6V.*

Continuous Power Dissipation (T_A = +70°C)
28 Pin TQFN (derate 34.5mW/°C above +70°C) 2758.6mW
Operating Temperature Range .....-40°C to +95°C
Programming Temperature Range .....0°C to +95°C
Storage Temperature Range .....-55°C to +125°C
Lead Temperature (soldering, 10s) .....+300°C
Soldering Temperature (reflow) .....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

(T_A = -40°C to +95°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Main Supply Voltage	V_{CC}	(Note 1)	2.85		5.5	V
High-Level Input Voltage (SDA, SCL, SDAOUT)	$V_{IH:1}$		0.7 x V_{CC}		V_{CC} + 0.3	V
Low-Level Input Voltage (SDA, SCL, SDAOUT)	$V_{IL:1}$		-0.3		0.3 x V_{CC}	V
High-Level Input Voltage (TXD, TXF, RSEL, IN1, LOS)	$V_{IH:2}$		2.0		V_{CC} + 0.3	V
Low-Level Input Voltage (TXD, TXF, RSEL, IN1, LOS)	$V_{IL:2}$		-0.3		+0.8	V

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = +2.85V to +5.5V, T_A = -40°C to +95°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current	I_{CC}	(Notes 1, 2)		2.5	4	mA
Output Leakage (SDA, SDAOUT, RSELOUT, LOSOUT, TXFOUT)	I_{LO}				1	µA
Low-Level Output Voltage (SDA, SDAOUT, SCLOUT, CSEL1OUT, CSEL2OUT, RSELOUT, LOSOUT, TXDOUT, DAC1, DAC2, TXFOUT)	V_{OL}	I_{OL} = 4mA			0.4	V
		I_{OL} = 6mA			0.6	
High-Level Output Voltage (DAC1, DAC2, SCLOUT, SDAOUT, CSEL1OUT, CSEL2OUT, TXDOUT)	V_{OH}	I_{OH} = 4mA	V_{CC} - 0.4			V
TXDOUT Before EEPROM Recall		High impedance before recall	55	550	100	MΩ
DAC1 and DAC2 Before Recall						
Input Leakage Current (IN1, LOS, RSEL, SCL, TXD, TXF)	I_{LI}				1	µA
Digital Power-On Reset	POD		1.0		2.2	V
Analog Power-On Reset	POA		2.0		2.75	V

DAC1, DAC2 ELECTRICAL CHARACTERISTICS

(V_{CC} = +2.85V to +5.5V, T_A = -40°C to +95°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Main Oscillator Frequency	f_{OSC}			5		MHz
Delta-Sigma Input-Clock Frequency	f_{DS}			1.25		MHz
Reference Voltage Input (REFIN)	V_{REFIN}	Minimum 0.1µF to GND	2		V_{CC}	V
Output Range			0		V_{REFIN}	V
Output Resolution		See the *Delta-Sigma Outputs (DAC1 and DAC2)* section for details			9	Bits
Output Impedance	R_{DS}			35	100	Ω

ANALOG INPUT CHARACTERISTICS (MON2, TXP HI, TXP LO, HBIAS, LOS)

(V_{CC} = +2.85V to +5.5V, T_A = -40°C to +95°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
MON2, TXP HI, TXP LO, HBIAS, LOS Full-Scale Voltage		(Note 3)		1.25		V
MON2 Input Resistance			35	50	65	kΩ
Resolution		(Note 3)		8		Bits
Error		T_A = +25°C (Note 4)		±2		%FS
Integral Nonlinearity			-1		+1	LSB
Differential Nonlinearity			-1		+1	LSB
Temperature Drift			-2.5		+2.5	%FS

ANALOG VOLTAGE MONITORING CHARACTERISTICS

(V_{CC} = +2.85V to +5.5V, T_A = -40°C to +95°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ADC Resolution				13		Bits
Input/Supply Accuracy (MON1–MON4, V_{CC})	ACC	At factory setting		0.25	0.5	%FS
Sample Rate for Temperature, MON1–MON4, and V_{CC}	t_{RR}			64	75	ms
Input/Supply Offset (MON1–MON4, V_{CC})	V_{OS}	(Note 5)		0	5	LSB
Factory Setting Full-Scale (Note 6)		MON1–MON4		2.5		V
		V_{CC}		6.5536		
		MON3 Fine		312.5		µV

DIGITAL THERMOMETER CHARACTERISTICS

(V_{CC} = +2.85V to +5.5V, T_A = -40°C to +95°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Thermometer Error	T_{ERR}	-40°C to +95°C	-3		+3	°C

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = +2.85V to +5.5V, T_A = -40°C to +95°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
TXD Enable	t_{OFF}	From rising TXD to rising TXDOUT			5	µs
Recovery from TXD Disable	t_{ON}	From falling TXD to falling TXDOUT			5	µs
Fault Reset Time (to TXFOUT = 0)	t_{INITR1}	From falling TXD		131		ms
	t_{INITR2}	On power-up or falling TXD, when VCC LO alarm is detected (Note 7)		161		
Fault Assert Time (to TXFOUT = 1)	t_{FAULT}	After HTXP, LTXP, HBATH, IBIASMAX (Note 8)	6.4		55	µs
LOSOUT Assert Time	t_{LOSS_ON}	LLOS (Notes 8, 9)	6.4		55	µs
LOSOUT Deassert Time	t_{LOSS_OFF}	HLOS (Notes 8, 10)	6.4		55	µs

CONTROL LOOP AND QUICK-TRIP TIMING CHARACTERISTICS

(V_{CC} = +2.85V to +5.5V, T_A = -40°C to +95°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output-Enable Time Following POA	t_{INIT}	(Note 7)		20		ms
Binary Search Time	t_{SEARCH}	(Note 11)	8		10	BIAS Samples

3-WIRE DIGITAL INTERFACE SPECIFICATION

(V_{CC} = +2.85V to +5.5V, T_A = -40°C to +95°C, timing referenced to $V_{IL(MAX)}$ and $V_{IH(MIN)}$, unless otherwise noted.) (Figure 17)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SCLOUT Clock Frequency	f_{SCLOUT}			833		kHz
SCLOUT Duty Cycle	t_{3WDC}			50		%
SDAOUT Setup Time	t_{DS}		100			ns
SDAOUT Hold Time	t_{DH}		100			ns
CSEL1OUT, CSEL2OUT Pulse-Width Low	t_{CSW}		500			ns
CSEL1OUT, CSEL2OUT Leading Time Before the First SCLOUT Edge	t_L		500			ns
CSEL1OUT, CSEL2OUT Trailing Time After the Last SCLOUT Edge	t_T		500			ns
SDAOUT, SCLOUT Load	C_{B3W}	Total bus capacitance on one line			10	pF

I²C AC ELECTRICAL CHARACTERISTICS

(V_{CC} = +2.85V to +5.5V, T_A = -40°C to +95°C, timing referenced to $V_{IL(MAX)}$ and $V_{IH(MIN)}$, unless otherwise noted.) (Figure 19)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SCL Clock Frequency	f_{SCL}	(Note 12)	0		400	kHz
Clock Pulse-Width Low	t_{LOW}		1.3			µs
Clock Pulse-Width High	t_{HIGH}		0.6			µs
Bus-Free Time Between STOP and START Condition	t_{BUF}		1.3			µs
START Hold Time	$t_{HD:STA}$		0.6			µs
START Setup Time	$t_{SU:STA}$		0.6			µs
Data In Hold Time	$t_{HD:DAT}$		0		0.9	µs
Data In Setup Time	$t_{SU:DAT}$		100			ns
Rise Time of Both SDA and SCL Signals	t_R	(Note 13)	20 + 0.1C_B		300	ns
Fall Time of Both SDA and SCL Signals	t_F	(Note 13)	20 + 0.1C_B		300	ns
STOP Setup Time	$t_{SU:STO}$		0.6			µs
Capacitive Load for Each Bus Line	C_B				400	pF
EEPROM Write Time	t_{WR}	(Note 14)			20	ms

NONVOLATILE MEMORY CHARACTERISTICS

(V_{CC} = +2.85V to +5.5V, unless otherwise noted.)

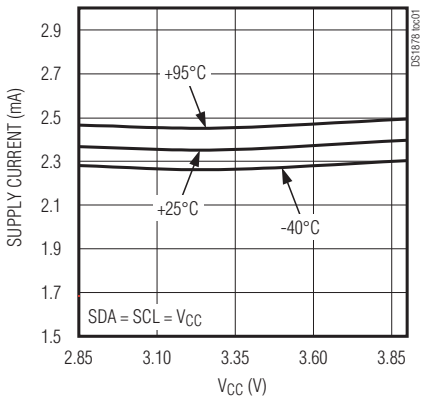
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
EEPROM Write Cycles		At +25°C	200,000			
		At +85°C	50,000			

Note 1: All voltages are referenced to ground. Current into the IC is positive, and current out of the IC is negative.
Note 2: Inputs are at supply rail. Outputs are not loaded.
Note 3: Eight ranges allow the full-scale range to change from 312mV to 1.25V.
Note 4: The output impedance of the device is proportional to its scale setting. For instance, if using the 1/2 scale, the output impedance is 1.5kΩ.
Note 5: This parameter is guaranteed by design.
Note 6: Full-scale is programmable.
Note 7: A temperature conversion is completed and the MODULATION register value is recalled from the LUT and V_{CC} has been measured to be above the VCC LO alarm.
Note 8: The timing is determined by the choice of the SAMPLE RATE setting (see Table 02h, Register 88h).
Note 9: This specification is the time it takes from MON3 voltage falling below the LLOS trip threshold to LOSOUT asserted high.
Note 10: This specification is the time it takes from MON3 voltage rising above the HLOS trip threshold to LOSOUT asserted low.
Note 11: Assuming an appropriate initial step is programmed that would cause the power to exceed the APC set point within four steps, the bias current will be within 3% within the time specified by the binary search time. See the *BIAS and MODULATION Control During Power-Up* section.
Note 12: I²C interface timing shown is for fast-mode (400kHz) operation. This device is also backward compatible with I²C standard-mode timing.
Note 13: C_B—the total capacitance of one bus line in pF.
Note 14: EEPROM write begins after a STOP condition occurs.

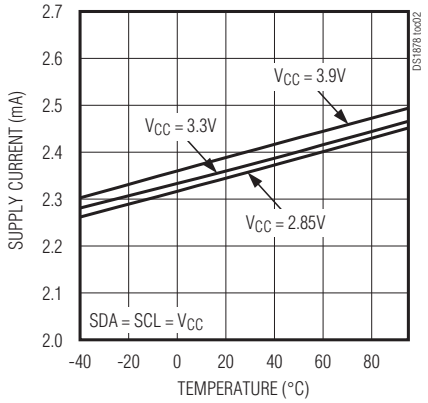
Typical Operating Characteristics

(V_{CC} = +2.85V to +3.9V, T_A = +25°C, unless otherwise noted.)

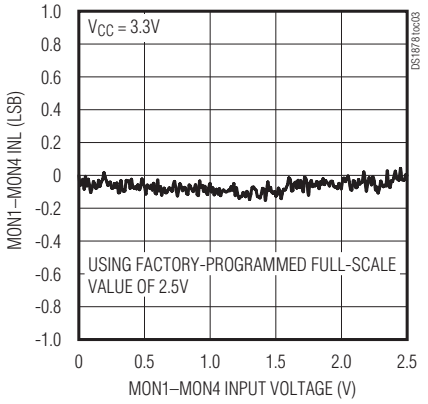
SUPPLY CURRENT vs. SUPPLY VOLTAGE



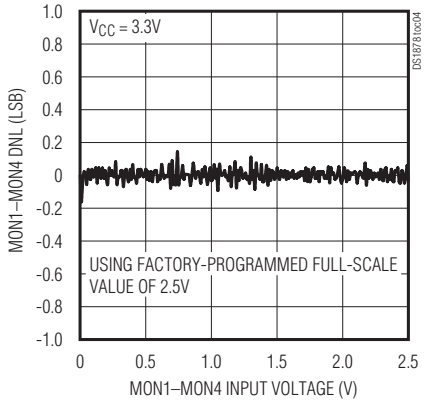
SUPPLY CURRENT vs. TEMPERATURE



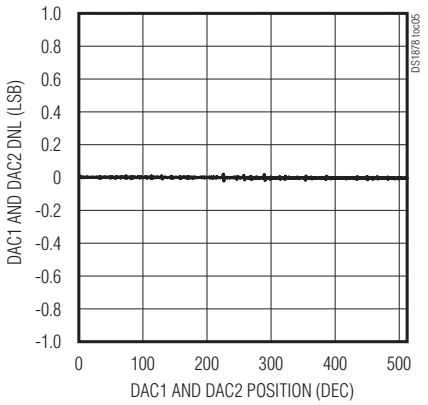
MON1–MON4 INL



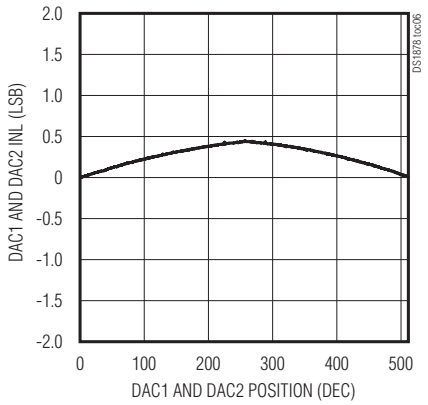
MON1–MON4 DNL



DAC1 AND DAC2 DNL

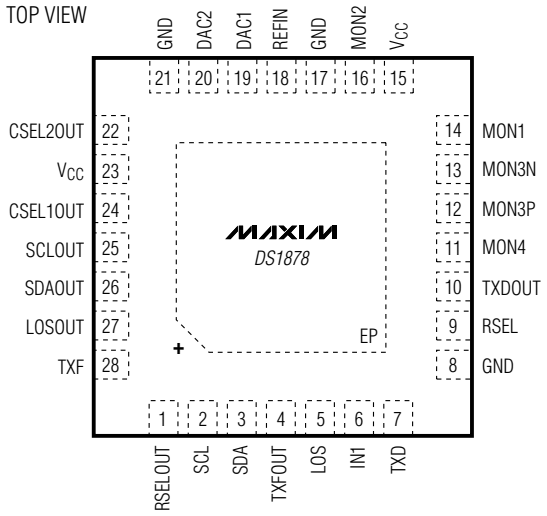


DAC1 AND DAC2 INL



SFP+ Controller with Digital LDD Interface

Pin Configuration

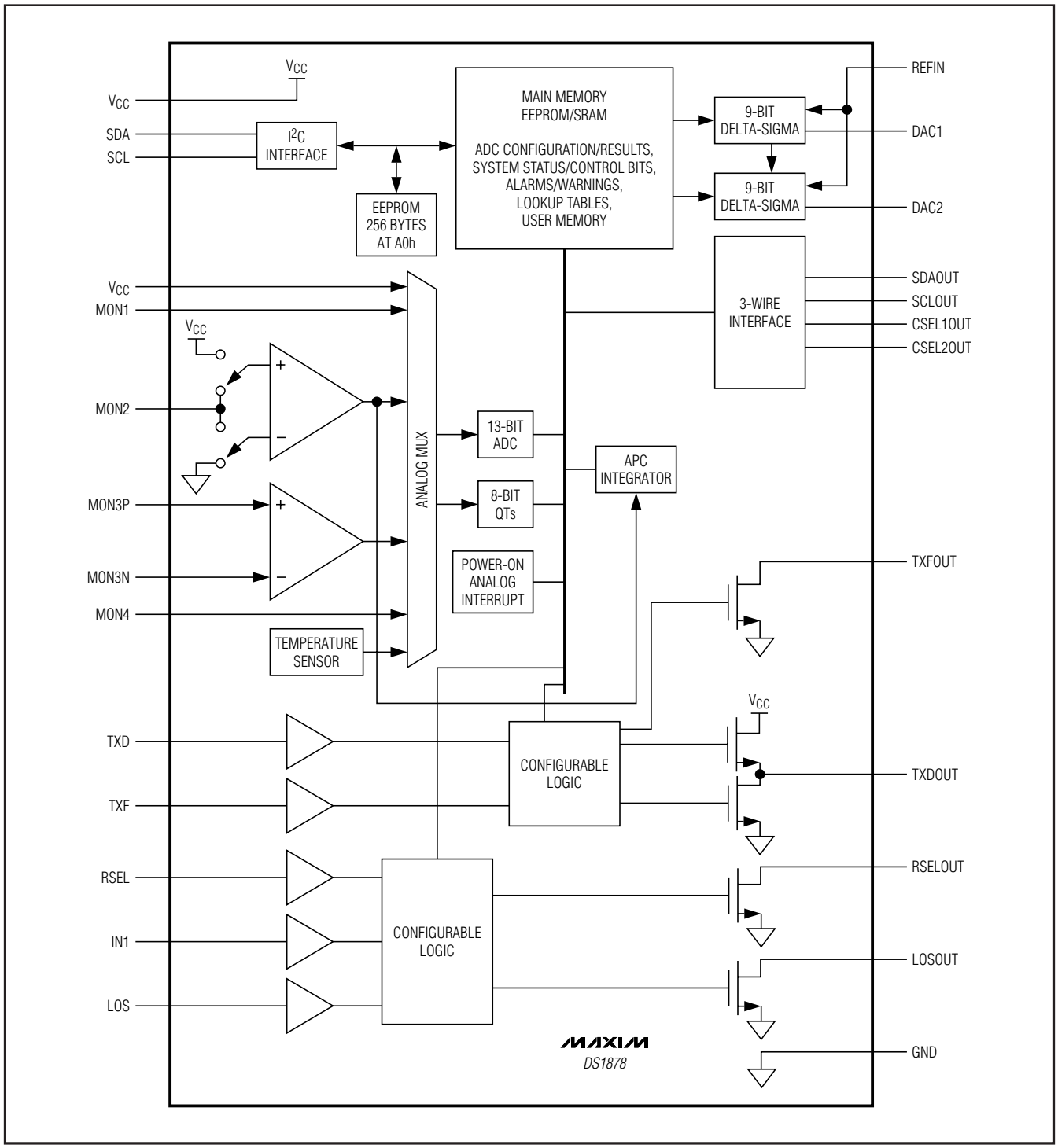


THIN QFN
(5mm × 5mm × 0.75mm)

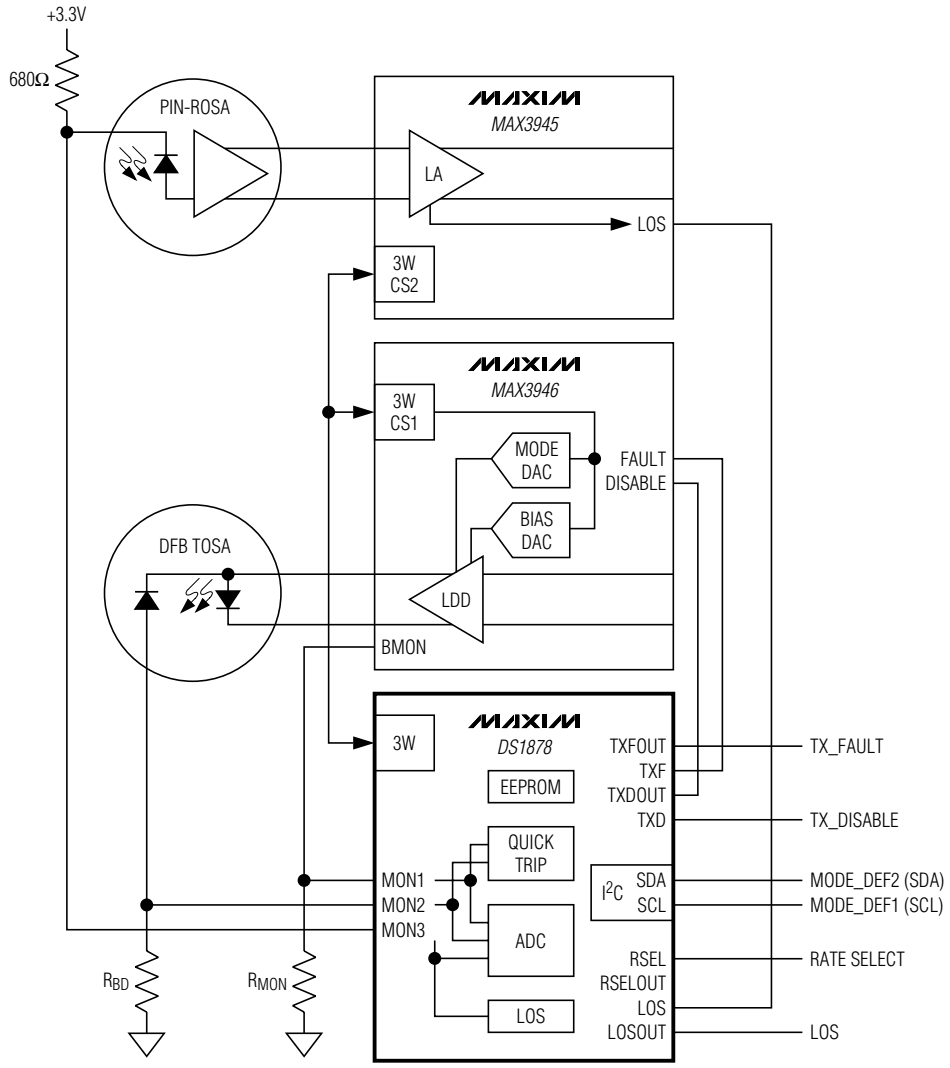
Pin Description

PIN	NAME	FUNCTION
1	RSELOUT	Rate-Select Output
2	SCL	I^2C Serial-Clock Input
3	SDA	I^2C Serial-Data Input/Output
4	TXFOUT	Transmit Fault Output, Open Drain
5	LOS	Loss of Signal Input
6	IN1	Digital Input. General-purpose input, AS1 in SFF-8079, or RS1 in SFF-8431.
7	TXD	Transmit Disable Input
8, 17, 21	GND	Ground Connection
9	RSEL	Rate-Select Input
10	TXDOUT	Transmit Disable Output
11	MON4	External Monitor Input 4
12, 13	MON3P, MON3N	Differential External Monitor Input 3 and LOS Quick Trip
14	MON1	External Monitor Input 1 and HBATH Quick Trip
15, 23	VCC	Power-Supply Input
16	MON2	External Monitor Input 2, Feedback Voltage for APC Loop, and TXP HI/TXP LO Quick Trip
18	REFIN	Reference Input for DAC1 and
19	DAC1	Delta-Sigma Output 1
20	DAC2	Delta-Sigma Output 2
22	CSEL2OUT	Chip-Select Output 2. Part of 3-wire interface to a laser driver/limiting amplifier.
24	CSEL1OUT	Chip-Select Output 1. Part of 3-wire interface to a laser driver/limiting amplifier.
25	SCLOUT	Serial-Clock Output. Part of 3-wire interface to a laser driver/limiting amplifier.
26	SDAOUT	Serial-Data Input/Output. Part of 3-wire interface to a laser driver/limiting amplifier.
27	LOSOUT	Receive Loss-of-Signal Output
28	TXF	Transmit Fault Input
—	EP	Exposed Pad. Connect to ground.

Block Diagram



Typical Operating Circuit



Detailed Description

The DS1878 integrates the control and monitoring functionality required to implement a VCSEL-based or DFB-based SFP or SFP+ system using Maxim's limiting amplifiers and laser drivers. Key components of the device are shown in the *Block Diagram* and described in subsequent sections.

3-Wire DAC Control

The device controls two 9-bit DACs inside the Maxim laser drivers. One DAC is used for laser bias control, while the other is used for modulation amplitude control. The device communicates with the laser driver over a 3-wire digital interface (see the *3-Wire Master for Controlling the Maxim Laser Driver* section). The communication between the device and Maxim laser driver and/or limiting amplifier is transparent to the end user.

Table 1. Acronyms

ACRONYM	DEFINITION
ADC	Analog-to-Digital Converter
AGC	Automatic Gain Control
APC	Automatic Power Control
APD	Avalanche Photodiode
ATB	Alarm Trap Bytes
BM	Burst Mode
DAC	Digital-to-Analog Converter
DFB	Distributed Feedback Laser
LDD	Laser Diode Driver
LOS	Loss of Signal
LUT	Lookup Table
NV	Nonvolatile
QT	Quick Trip
TE	Tracking Error
TIA	Transimpedance Amplifier
ROSA	Receiver Optical Subassembly
SEE	Shadowed EEPROM
SFF	Small Form Factor
SFF-8472	Document Defining Register Map of SFPs and SFFs
SFP	Small Form Factor Pluggable
SFP+	Enhanced SFP
TOSA	Transmit Optical Subassembly
TXP	Transmit Power
VCSEL	Vertical Cavity Self-Emitting Laser

BIAS Register/APC Control, 3-Wire Mode

A Maxim laser driver controls its laser bias current DAC using the APC loop within the device. The APC loop's feedback to the device is the monitor diode (MON2) current, which is converted to a voltage using an external resistor. The feedback is sampled by a comparator and compared to a digital set-point value. The output of the comparator has three states: up, down, or no-operation. The no-operation state prevents the output from excessive toggling once steady state is reached. As long as the comparator output is in either the up or down states, the bias is adjusted by writing increment and decrement values to the Maxim laser driver through the BIASINC register.

The device has an LUT to allow the APC set point to change as a function of temperature to compensate for tracking error (TE). The APC LUT has 36 entries that determine the APC setting in 4°C windows between -40°C and +100°C.

MODULATION Control

A Maxim laser driver controls the laser modulation using the internal temperature-indexed LUT within the device. The modulation LUT is programmed in 2°C increments over the -40°C to +102°C range to provide temperature compensation for the laser's modulation. The modulation is updated after each temperature conversion using the 3-wire interface that connects to the Maxim laser driver. A Maxim laser driver include a 9-bit DAC. The modulation LUT is 8 bits.

Figure 1 demonstrates how the 8-bit LUT controls the 9-bit DAC with the use of a temperature control bit

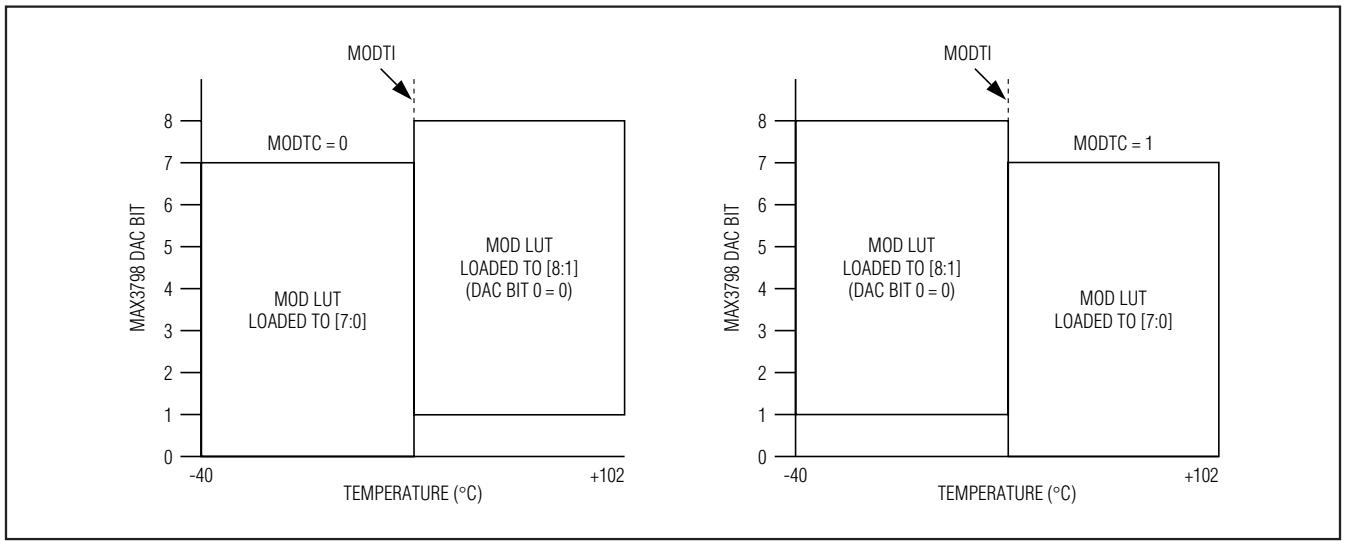


Figure 1. Modulation LUT Loading to a Maxim Laser Driver MOD DAC

(MODTC, Table 02h, Register C6h) and a temperature index register (MODTI, Table 02h, Register C2h).

BIAS and MODULATION Control During Power-Up

The device has two internal registers, MODULATION and BIAS, that represent the values written to the Maxim laser driver's modulation DAC and bias DAC through the 3-wire interface. On power-up, the device sets the MODULATION and BIAS registers to 0. When V_{CC} is above POA, the device initializes the Maxim laser driver. After a temperature conversion is completed and if the VCC LO alarm is enabled, an additional V_{CC} conversion above the customer-defined VCC LO alarm level is required before a Maxim laser driver MODULATION register is updated with the value determined by the temperature conversion and the modulation LUT.

When the MODULATION register is set, the BIAS register is set to a value equal to ISTEP (see Figure 2). The startup algorithm verifies whether this bias current causes a feedback voltage above the APC set point, and if not, it continues increasing the BIAS register by ISTEP until the APC set point is exceeded. When the APC set point is exceeded, the device begins a binary search to quickly reach the bias current corresponding to the proper power level. After the binary search is completed, the APC integrator is enabled and single LSB steps are used to tightly control the average power.

The TXP HI, TXP LO, and BIAS MAX QT alarms are masked until the binary search is completed. However, the BIAS MAX alarm is monitored during this time to prevent the BIAS register from exceeding IBIASMAX. During the bias current initialization, the BIAS register is not allowed to exceed IBIASMAX. If this occurs during the ISTEP sequence, then the binary search routine is enabled. If IBIASMAX is exceeded during the binary search, the next smaller step is activated. ISTEP or binary increments that would cause the BIAS register to exceed IBIASMAX are not taken. Masking the alarms until the completion of the binary search prevents false positive alarms during startup.

ISTEP is a value controlled by registers ISTEPH, ISTEPL, and ISTEPTI (Table 02h, Registers BAh, BBh, and C5h, respectively). See the register descriptions for more information. During the first steps, a Maxim laser driver's bias DAC is directly written using SET_IBIAS. ISTEP should be programmed to the maximum safe increase that is allowable during startup. If this value is programmed too low, the device still operates, but it could take significantly longer for the algorithm to converge and hence to control the average power.

If a fault is detected, and TXD is toggled to reenable the outputs, the device powers up following a similar sequence to an initial power-up. The only difference is that the device already has determined the present

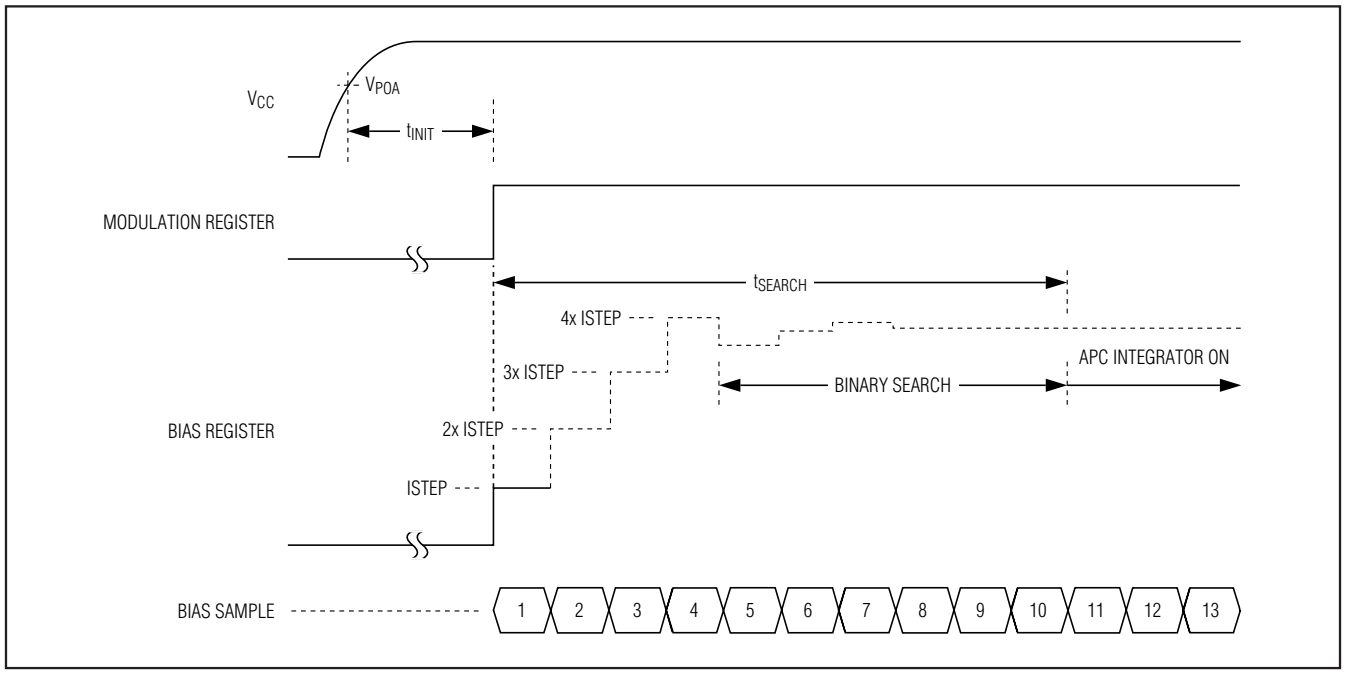


Figure 2. Power-Up Timing

temperature, so the t_{INIT} time is not required for the device to recall the APC and MOD set points from EEPROM.

BIAS and MODULATION Registers as a Function of Transmit Disable (TXD)

If TXD is asserted (logic 1) during normal operation, the 3-wire master writes the laser driver bias and MODULATION DACs to 0. When TXD is deasserted (logic 0), the device sets the MODULATION register with the value associated with the present temperature, and initializes the BIAS register using the same search algorithm as done at startup. When asserted, soft TXD (TXDC) (Lower Memory, Register 6Eh) would allow a software control identical to the TXD pin (see Figure 3).

APC and Quick-Trip Timing

As shown in Figure 4, the device's input comparator is shared between the APC control loop and the quick-trip alarms (TXP HI, TXP LO, LOS, BIAS HI, and IBIAS MAX). The comparator polls the alarms in a multiplexed sequence. Five of every eight comparator readings are used for APC loop bias-current control. The other three updates are used to check the HTXP/LTXP (monitor diode voltage), the HBATH (MON1), and LOS (MON3) signals against the internal APC, BIAS, and MON3 reference, respectively. If the last APC comparison was higher than the APC set point, it makes an HTXP comparison, and if it is lower, it makes an LTXP comparison. Depending on the results of the comparison, the corresponding alarms and warnings (TXP HI, TXP LO) are asserted or deasserted.

The device has a programmable comparator sample time based on an internally generated clock to facilitate a wide variety of external filtering options and time delays resulting from writing values to the laser driver's bias DAC. The SAMPLE RATE register (Table 02h, Register 88h) determines the sampling time. Samples occur at a regular interval, t_{REP}. Table 2 shows the sample rate options available. Any quick-trip alarm that is detected by default remains active until a subsequent comparator sample shows the condition no longer exists. A second bias current monitor (BIAS MAX) compares a Maxim laser driver's BIAS DAC's code to a digital value stored in the IBIASMAX register. This comparison is made at every bias current update to ensure that a high-bias current is quickly detected.

Table 2. Update Rate Timing

APC_SR[2:0]	SAMPLE PERIOD (t_{REP}) (ns)
000b	800
001b	1200
010b	1600
011b	2000
100b	2800
101b	3200
110b	4400
111b	6400

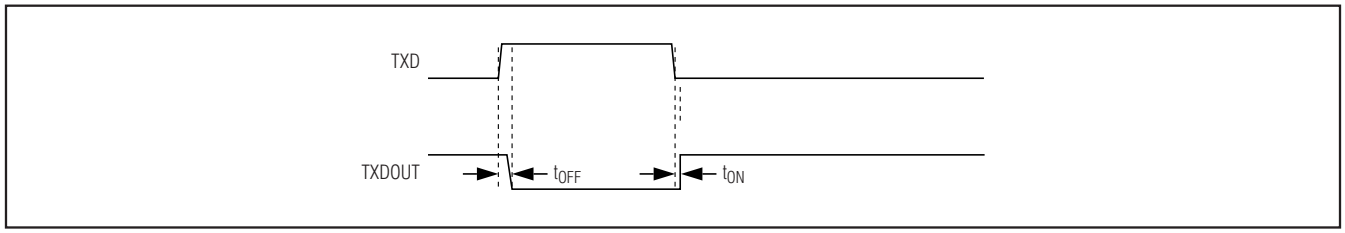


Figure 3. TXD Timing

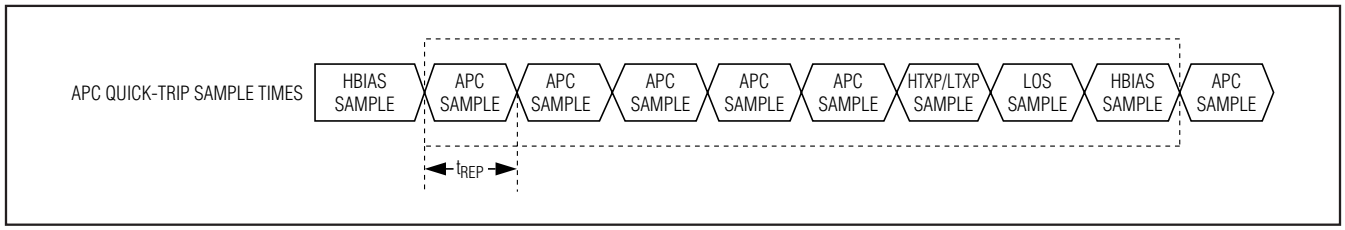


Figure 4. APC Loop and Quick-Trip Sample Timing

SFP+ Controller with Digital LDD Interface

An APC sample that requires an update of the BIAS register causes subsequent APC samples to be ignored until the end of the 3-wire communication that updates the laser driver's BIAS DAC, plus an additional 16 sample periods (t_{REP}).

Monitors and Fault Detection

Monitors

Monitoring functions on the device include five quick-trip comparators and six ADC channels. This monitoring combined with the alarm enables (Table 01h/05h) determines when/if the device turns off the Maxim laser driver's DACs and triggers the TXFOUT and TXDOUT outputs. All the monitoring levels and interrupt masks are user programmable.

Five Quick-Trip Monitors and Alarms

Five quick trip monitors are provided to detect potential laser safety issues and LOS status. These monitor the following:

1) High Bias Current (HBATH), causing QT BIAS HI
2) Low Transmit Power (LTXP), causing QT TXP LO
3) High Transmit Power (HTXP), causing QT TXP HI
4) Max Output Current (IBIASMAX), causing QT BIAS MAX
5) Loss of Signal (LLOS), causing QT LOS LO

The high and low transmit power quick-trip registers (HTXP and LTXP) set the thresholds used to compare against the MON2 voltage to determine if the transmit power is within specification. The HBATH quick trip compares the MON1 input (generally from a Maxim laser driver bias monitor output) against its threshold setting to determine if the present bias current is above specification. The user can program up to eight different temperature-indexed threshold levels for HBATH (Table 02h, Registers D0h–D7h).

The BIAS MAX quick trip compares the BIAS register with the MON2 voltage and determines if the BIAS register is above specification. The BIAS register is not allowed to exceed the value set in the IBIASMAX register. When the device detects the bias is at the limit, it sets the BIAS MAX status bit and holds the BIAS register setting at the IBIASMAX level.

The LOS LO quick trip compares the MON3 input against its threshold setting (LLOS) to determine if the present received power is below the specification. The LOS RANGING register allows the LOS threshold value to scale. The LOS LO quick trip can be used to set the LOSOUT pin. LOS HI does not set LOSOUT. See the description of the LOS LO and LOS HI bits (Table 01h, Register FBh) for further details of operation.

The quick trips are routed to create TXFOUT through interrupt masks to allow combinations of these alarms to be used to trigger the outputs.

Six ADC Monitors and Alarms

The ADC monitors six channels that measure temperature (internal temp sensor), V_{CC}, and MON1–MON4 using an analog multiplexer to measure them round robin with a single ADC (see the *ADC Timing* section). The five voltage channels have a customer-programmable full-scale range and all channels have a customer-programmable offset value that is factory programmed to default value (see Table 3). Additionally, MON1–MON4 can right-shift results by up to 7 bits before the results are compared to alarm thresholds or read over the I^2C bus. This allows customers with specified ADC ranges to calibrate the ADC full scale to a factor of $1/2^n$ of their specified range to measure small signals. The device can then right-shift the results by n bits to maintain the bit weight of their specification (see the *Right-Shifting ADC Result* and *Enhanced RSSI Monitoring (Dual-Range Functionality)* sections).

The ADC results (after right-shifting, if used) are compared to the alarm and warning thresholds after each conversion, and the corresponding alarms are set, which can be used to trigger the TXFOUT output. These ADC thresholds are user programmable, as are the masking registers that can be used to prevent the alarms from triggering the TXFOUT output.

ADC Timing

There are six analog channels that are digitized in a round-robin fashion in the order shown in Figure 5. The total time required to convert all six channels is t_{RR} (see the *Analog Voltage Monitoring Characteristics* for details).

Table 3. ADC Default Monitor Full-Scale Ranges

SIGNAL (UNITS)	+FS SIGNAL	+FS HEX	-FS SIGNAL	-FS HEX
Temperature (°C)	127.996	7FFF	-128	8000
V_{CC} (V)	6.5528	FFF8	0	0000
MON1–MON4 (V)	2.4997	FFF8	0	0000

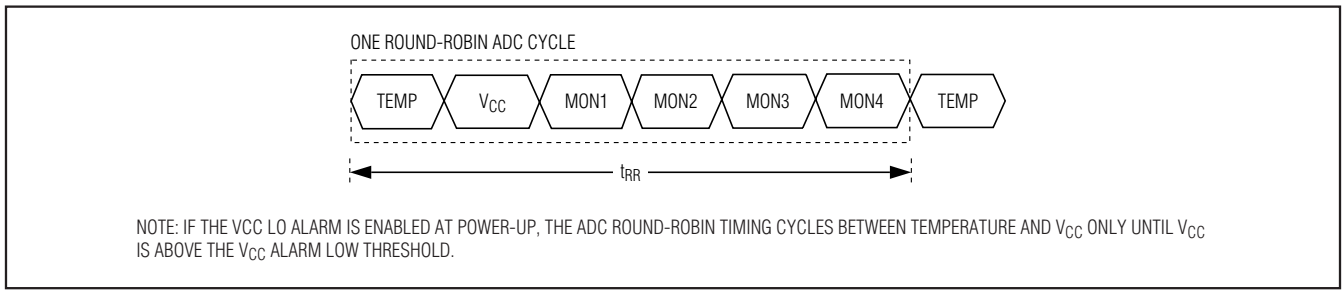


Figure 5. ADC Round-Robin Timing

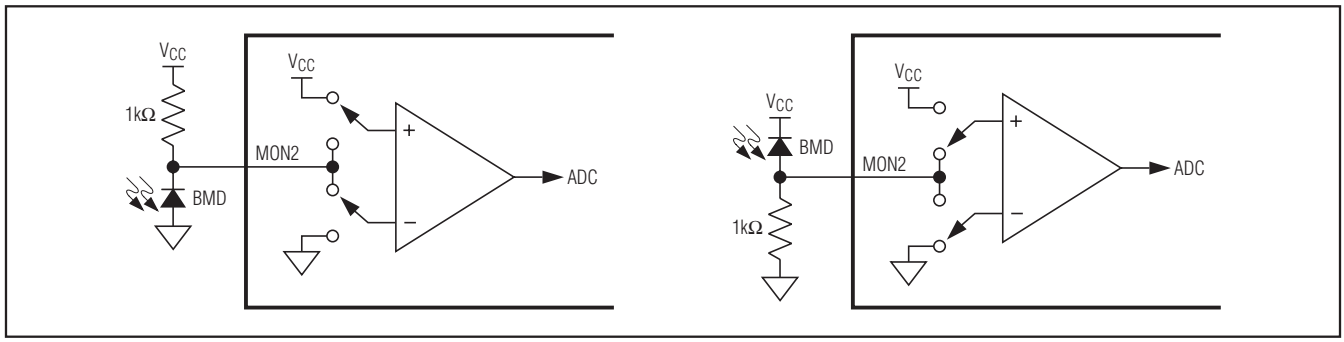


Figure 6. MON2 V_{CC} or GND Reference

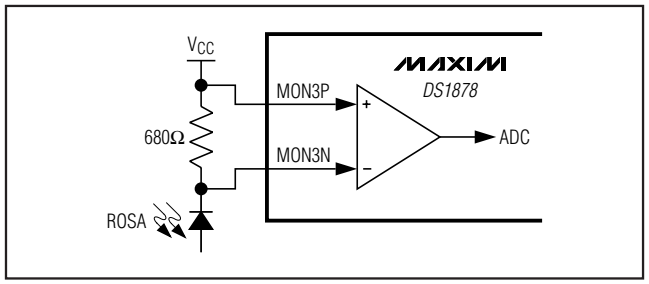


Figure 7. MON3 Differential Input for High-Side RSSI

Right-Shifting ADC Result

If the weighting of the ADC digital reading must conform to a predetermined full-scale (PFS) value defined by a standard's specification (e.g., SFF-8472), then right-shifting can be used to adjust the PFS analog measurement range while maintaining the weighting of the ADC results. The device's range is wide enough to cover all requirements; when the maximum input value is ≤ 1/2 of the FS value, right-shifting can be used to obtain greater accuracy. For instance, the maximum voltage might be 1/8 the specified PFS value, so only 1/8 the converter's range is effective over this range. An alternative is to calibrate the ADC's full-scale range to 1/8 the readable PFS value and use a right-shift value of 3. With this implementation, the resolution of the measurement is increased by a factor of 8, and because the result is digitally divided by 8 by right-shifting, the bit weight of the measurement still meets the standard's specification (i.e., SFF-8472).

The right-shift operation on the ADC result is carried out based on the contents of right-shift control registers (Table 02h, Registers 8Eh–8Fh) in EEPROM. Three analog channels, MON1–MON3, each have 3 bits allocated to set the number of right-shifts. Up to seven right-shift operations are allowed and are executed as a part of every conversion before the results are compared to the high-alarm and low-alarm levels, or loaded into their corresponding measurement registers (Lower Memory, Registers 64h–6Bh). This is true during the setup of internal calibration as well as during subsequent data conversions.

V_{CC} or GND Referenced MON2 Input

The device offers a configurable input for MON2. MON2 can either be referenced to V_{CC} or GND, as shown in Figure 6. This enables compatibility with different TOSA monitor diode configurations.

Differential MON3 Input

The device offers a fully differential input for MON3. This enables high-side monitoring of RSSI, as shown in Figure 7. This reduces board complexity by eliminating the need for a high-side differential amplifier or a current mirror.

Enhanced RSSI Monitoring (Dual-Range Functionality)

The device offers a feature to improve the accuracy and range of MON3, which is most commonly used for monitoring RSSI. Using a traditional input, the accuracy of the RSSI measurements is increased at the cost of reduced input signal swing. The device eliminates this trade-off by offering "dual range" calibration on the MON3 channel.

The dual-range calibration can operate in two modes: crossover enabled and crossover disabled.

- **Crossover Enabled:** For systems with a nonlinear relationship between the ADC input and desired ADC result, the mode should be set to crossover enabled (Figure 8). The RSSI measurement of an APD receiver is one such application. Using the crossover enabled mode allows a piecewise linear approximation of the nonlinear response of the APD's gain factor. The crossover point is the point between fine and coarse points. The ADC result transitions between the fine and coarse ranges with no hysteresis. Right-shifting, slope adjustment, and offset are configurable for both the fine and coarse ranges. The XOVER FINE register determines the maximum results returned by fine ADC conversions, before right-shifting. The XOVER COARSE register determines the minimum results returned by coarse ADC conversions, before right-shifting.
- **Crossover Disabled:** The crossover disabled mode is intended for systems with a linear relationship between the MON3 input and desired ADC result. The ADC result transitions between the fine and coarse ranges with hysteresis (Figure 9). In crossover disabled mode, the thresholds between coarse and fine mode are a function of the number of right-shifts being used. With the use of right-shifting, the fine-mode full scale is programmed to ($1/2^{nth}$) of the coarse-mode full scale. The device now auto ranges to choose the range that gives the best resolution for the measurement. Table 4 shows the threshold values for each possible number of right-shifts.

Table 4. MON3 Hysteresis Threshold Values

NUMBER OF RIGHT-SHIFTS	FINE MODE MAX (HEX)	COARSE MODE MIN* (HEX)
0	FFF8	F000
1	7FFC	7800
2	3FFE	3C00
3	1FFF	1E00
4	0FFF	0F00
5	07FF	0780
6	03FF	03C0
7	01FF	01E0

**This is the minimum reported coarse-mode conversion.*

Table 5. MON3 Configuration Registers

REGISTER	FINE MODE	COARSE MODE
GAIN	98h–99h, Table 02h	9Ch–9Dh, Table 02h
OFFSET	A8h–A9h, Table 02h	ACh–ADh, Table 02h
RIGHT-SHIFT$_0$	8Fh, Table 02h	8Fh, Table 02h
CNFGC (RSSI_FC and RSSI_FF Bits)	8Bh, Table 02h	
UPDATE (RSSIR Bit)	6Fh, Lower Memory	
MON3 VALUE	68h–69h, Lower Memory	

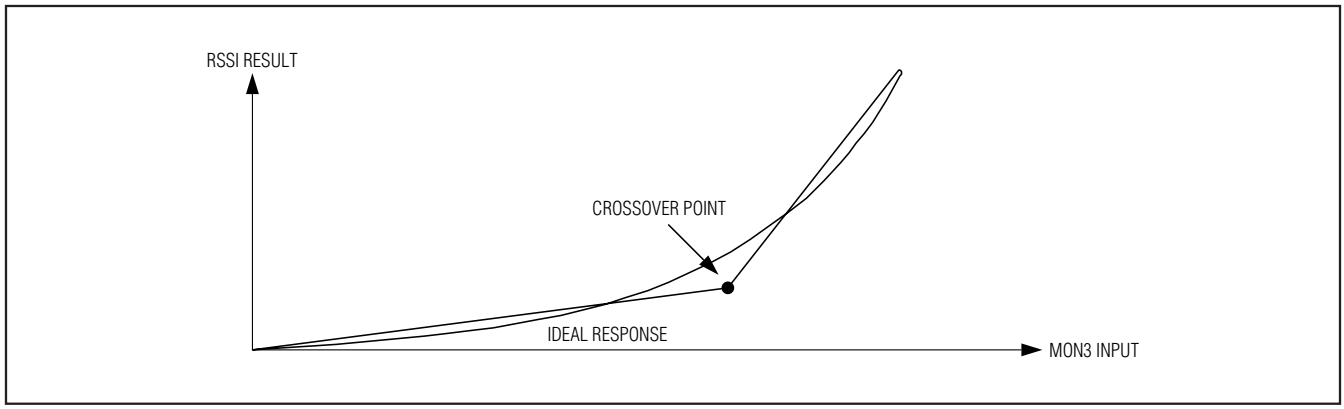


Figure 8. RSSI with Crossover Enabled

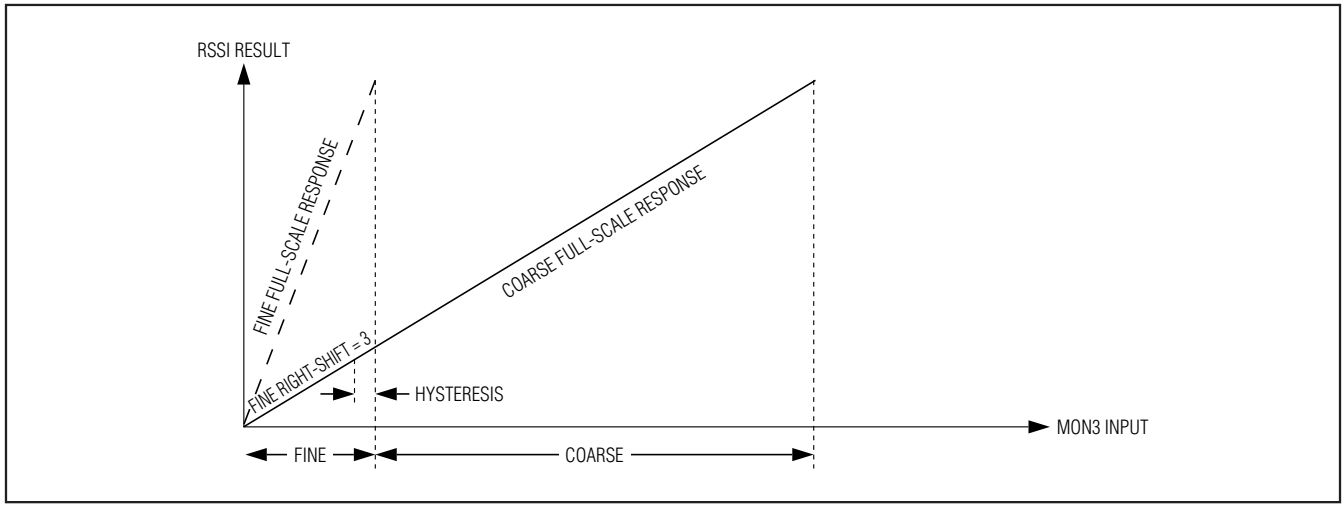


Figure 9. RSSI with Crossover Disabled

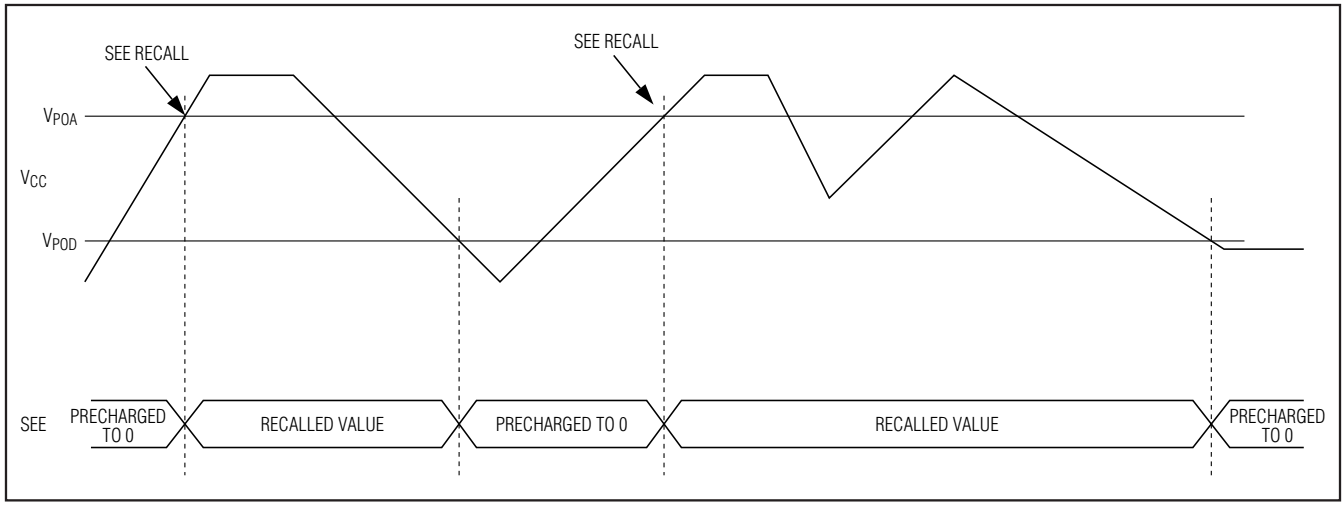


Figure 10. Low-Voltage Hysteresis Example

Low-Voltage Operation

The device contains two power-on reset (POR) levels. The lower level is a digital POR (POD) and the higher level is an analog POR (POA). At startup, before the supply voltage rises above POA, the outputs are disabled, all SRAM locations are set to their defaults, shadowed EEPROM (SEE) locations are zero, and all analog circuitry is disabled. When V_{CC} reaches POA, the SEE is recalled, and the analog circuitry is enabled. While V_{CC} remains above POA, the device is in its normal operating state, and it responds based on its nonvolatile configuration. If during operation V_{CC} falls below POA, but is still above POD, then the SRAM retains the SEE settings from the first SEE recall, but the device analog is shut down and the outputs disabled. If the supply voltage recovers back above POA, then the device immediately resumes normal operation. If the supply voltage falls below POD, then the device SRAM is placed in its default state and another SEE recall is required to reload the nonvolatile settings. The EEPROM recall occurs the next time V_{CC} exceeds POA. Figure 10 shows the sequence of events as the voltage varies.

Any time V_{CC} is above POD, the I^2C interface can be used to determine if V_{CC} is below the POA level. This is accomplished by checking the RDYB bit in the STATUS (Lower Memory, Register 6Eh) byte. RDYB is set when V_{CC} is below POA; when V_{CC} rises above POA, RDYB

is timed (within 500µs) to go to 0, at which point the part is fully functional.

For all device addresses sourced from EEPROM (Table 02h, Register 8Ch), the default device address is A2h until V_{CC} exceeds POA, allowing the device address to be recalled from the EEPROM.

Power-On Analog (POA)

POA holds the device in reset until V_{CC} is at a suitable level (V_{CC} > POA) for the device to accurately measure with its ADC and compare analog signals with its quick-trip monitors. Because V_{CC} cannot be measured by the ADC when V_{CC} is less than POA, POA also asserts the VCC LO alarm, which is cleared by a V_{CC} ADC conversion greater than the customer-programmable VCC LO ADC limit. This allows a programmable limit to ensure that the headroom requirements of the transceiver are satisfied during a slow power-up. The TXFOUT output does not latch until there is a conversion above the VCC LO limit. The POA alarm is nonmaskable. The TXF output is asserted when V_{CC} is below POA. See the *Low-Voltage Operation* section for more information.

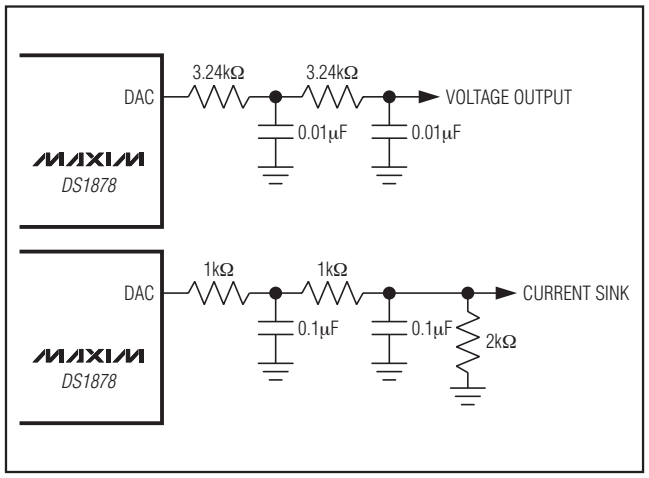


Figure 11. Recommended RC Filter for DAC1/DAC2

Delta-Sigma Outputs (DAC1 and DAC2)

Two delta-sigma outputs are provided, DAC1 and DAC2. With the addition of an external RC filter, these outputs provide two 9-bit resolution analog outputs with the full-scale range set by the input REFIN. Each output is either manually controlled or controlled using a temperature-indexed LUT. A delta-sigma is a digital output using pulse-density modulation. It provides much lower output ripple than a standard digital PWM output given the same clock rate and filter components. Before t_{INIT}, the DAC1 and DAC2 outputs are high impedance.

The external RC filter components are chosen based on ripple requirements, output load, delta-sigma frequency, and desired response time. A recommended filter is shown in Figure 11.

The device's delta-sigma outputs are 9 bits. For illustrative purposes, a 3-bit example is provided in Figure 12.

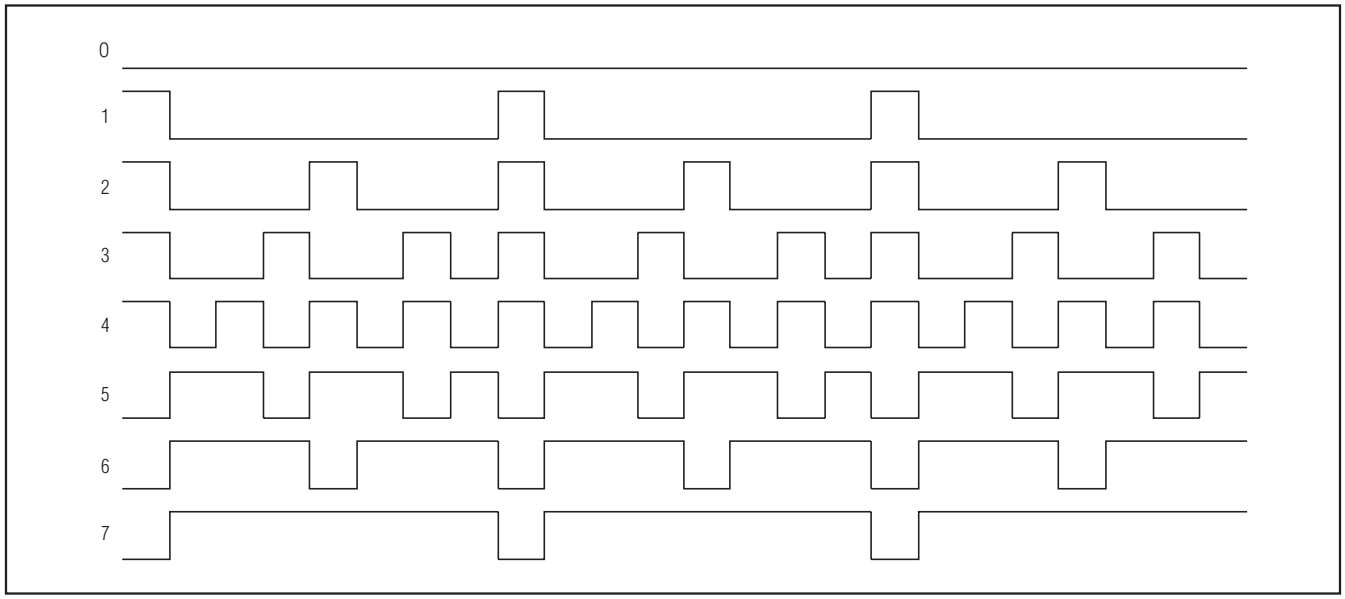


Figure 12. Delta-Sigma Outputs

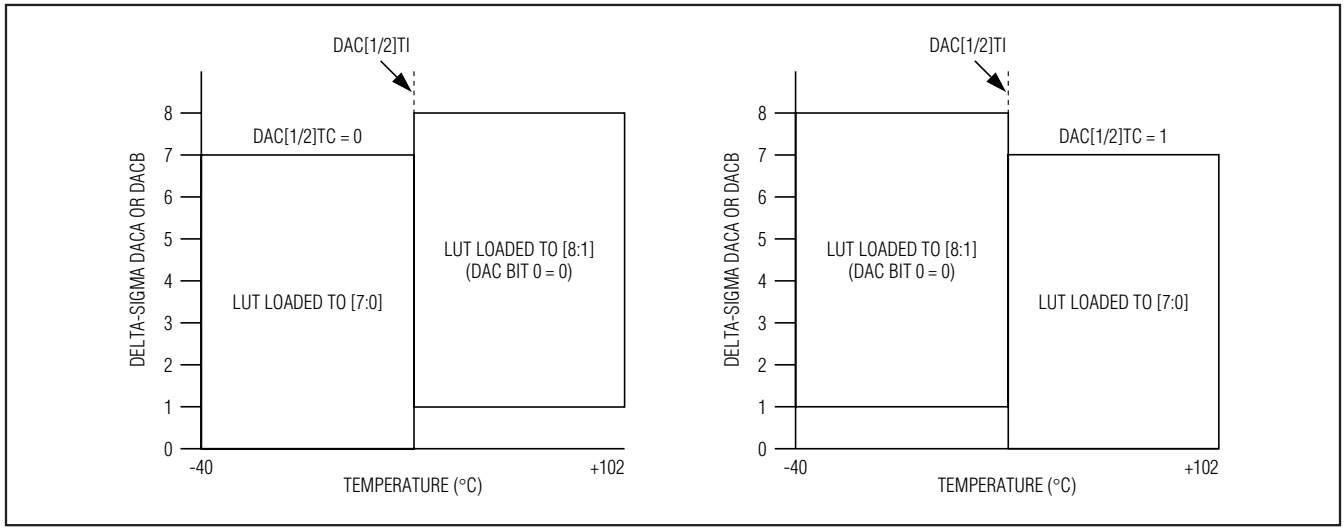


Figure 13. DAC1/DAC2 LUT Assignments

In LUT mode, DAC1 and DAC2 are each controlled by a separate 8-bit, 4°C-resolution, temperature-addressed LUT. The delta-sigma outputs use a 10-bit structure. The 8-bit LUTs are either loaded directly into the MSBs (8:1) or the LSBs (7:0). This is determined by DAC1TI (Table 02h, Register C3h), DAC2TI (Table 02h, Register C4h), DAC1TC (Table 02h, Register C6h, bit 6), and DAC2TC (Table 02h, Register C6h, bit 5). See Figure 13 for more details. The DAC1 LUT (Table 07h) and DAC2 LUT (Table 08h) registers are nonvolatile and password-2 protected.

The reference input, REFIN, is the supply voltage for the output buffer of DAC1 and DAC2. The voltage connected to REFIN must be able to support the edge rate requirements of the delta-sigma outputs. In a typical application, a 0.1µF capacitor should be connected between REFIN and ground.

Digital I/O Pins

Five digital input and four digital output pins are provided for monitoring and control.

LOS, LOSOUT

By default (LOSC = 1, Table 02h, Register 89h), the LOS pin is used to convert a standard comparator output for loss of signal (LOS) to an open-collector output. This means the mux shown in the *Block Diagram* by default selects the LOS pin as the source for the LOSOUT output transistor. The output of the mux can be read in the STATUS byte (Lower Memory, Register 6Eh) as the RXL bit. The RXL signal can be inverted (INV LOS = 1) before driving the open-drain output transistor using the XOR gate provided. Setting LOSC = 0 configures the mux to be controlled by LOS LO, which is driven by the output of the LOS quick trip (Table 02h, Registers BEh and BFh). The mux setting (stored in EEPROM) does not take effect until V_{CC} > POA, allowing the EEPROM to recall.

SFP+ Controller with Digital LDD Interface

IN1, RSEL, RSELOUT

The digital input IN1 and RSEL pins primarily serve to meet the rate-select requirements of SFP and SFP+. They also serve as general-purpose inputs. RSELOUT is driven by a combination of the RSEL and logic dictated by control registers in the EEPROM (Figure 16). The levels of IN1 and RSEL can be read using the STATUS register (Lower Memory, Register 6Eh). The open-drain RSELOUT output is software-controlled and/or inverted through the STATUS register and CNFGA register (Table 02h, Register 89h). External pullup resistors must be provided on RSELOUT to realize a high logic level. The RSEL pin determines the value sent by the 3-wire master to the limiting amplifier's SETLOS register. When RSEL is high, SETLOSH is used. When RSEL is low, SETLOSL is used. The DS1878 can transmit a bit on the 3-wire bus to Register 0x00 (bit 1) of the MAX3945, MAX3798, MAX3799, or RXCTRL1 (Table 02h, Register E8h) within 80ms of a transition (rising or falling) on the RSELOUT. This bit indicates the status of RSELOUT.

This feature is user programmable. A bit (RSELPIN, Table 02h, Register 89h) is provided to determine whether the I^2C register RXCTRL1 or the status of the RSELOUT pin is transmitted. When RSELPIN is set to 1, the status of RSELOUT is sent out. RSELOUT is determined by RSEL pin, RSELC control bit, and INVRSOUT control bit as shown in Figure 14.

The INVRSOUT bit inverts the RSELOUT bit, and this inversion is reflected when this bit is sent out on the 3-wire bus. Figure 14 illustrates the timing for the 3-wire communication when RSELPIN is set to 1.

TXD, TXDOUT

TXDOUT is generated from a combination of TXFOUT, TXD, and the internal signal FETG. A software control identical to TXD is available (TXDC, Lower Memory, Register 6Eh). A TXD pulse is internally extended (t_{INITR1}) to inhibit the latching of low alarms and warnings related to the APC loop to allow for the loop to stabilize. The nonlatching alarms and warnings are TXP

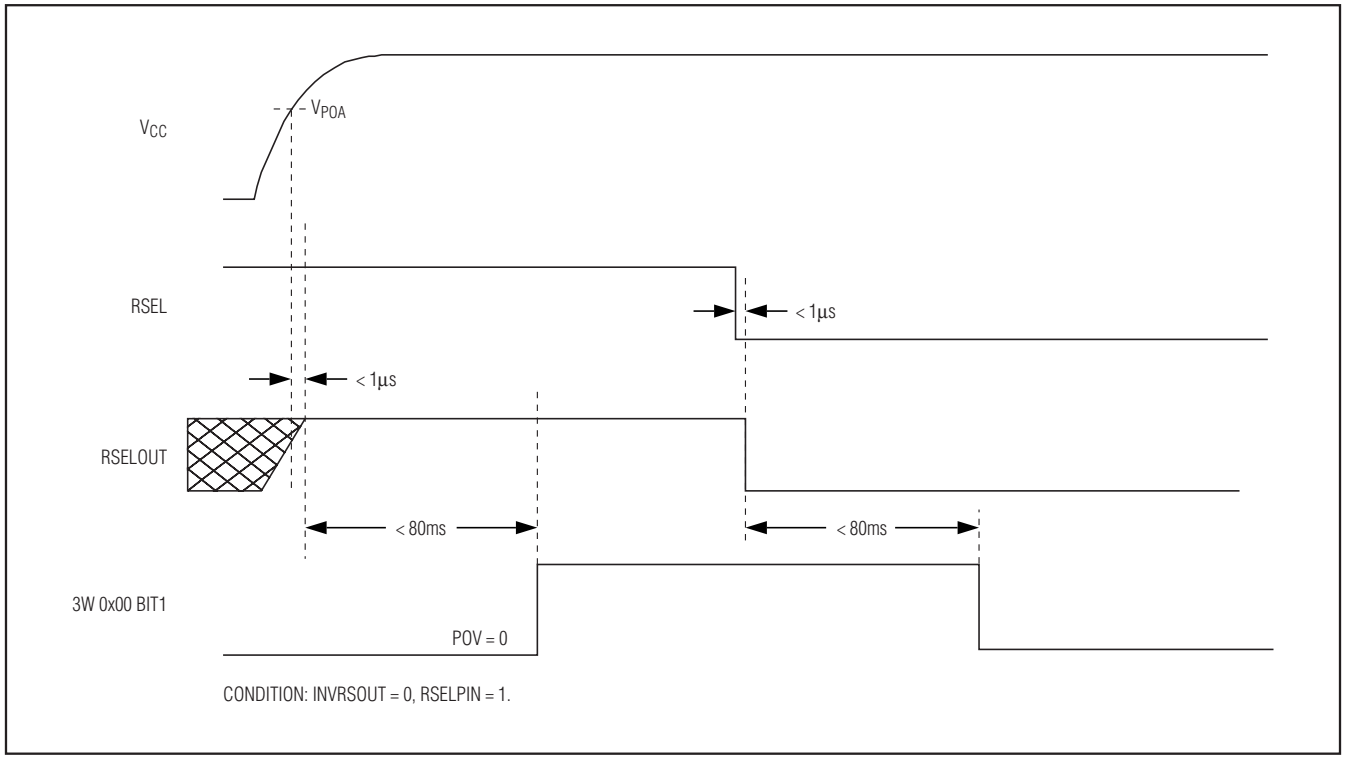


Figure 14. 3-Wire Communication on RSELOUT Transition

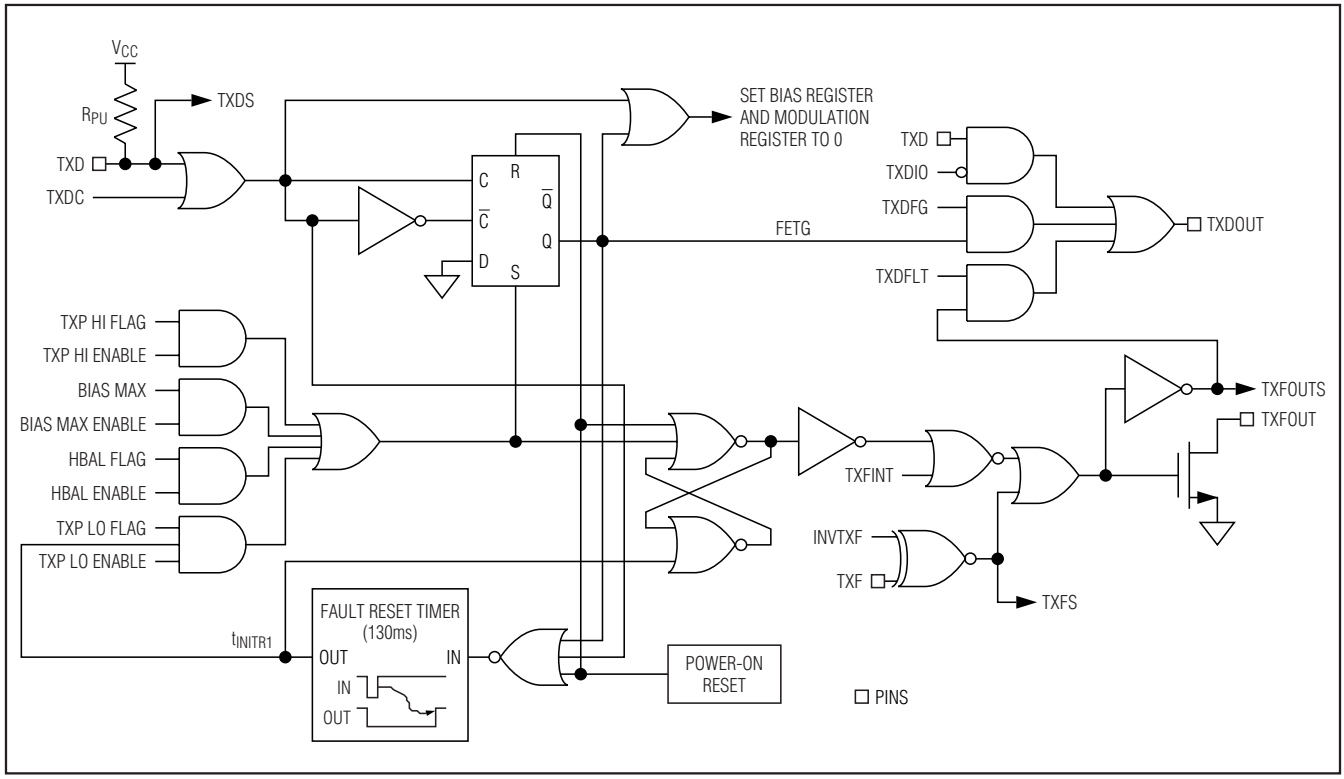


Figure 15. Logic Diagram 1

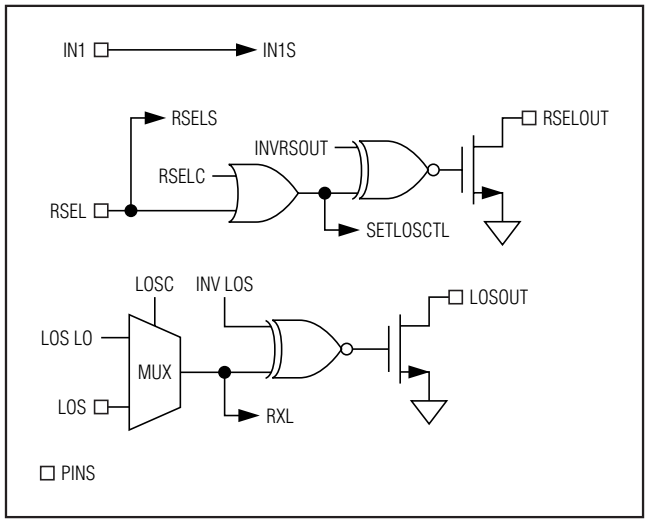


Figure 16. Logic Diagram 2

LO, LOS LO, and MON1–MON4 LO alarms and warnings. In addition, TXP LO is disabled from creating FETG. See the *Transmit Fault (TXFOUT) Output* section for a detailed explanation of TXFOUT. Figure 15 shows that the same signals and faults can also be used to generate the internal signal FETG (Table 01h/05h, Registers FAh–FBh). FETG is used to send a fast "turn-off" command to the laser driver. The status of FTEG can be read (Lower Memory, Register 71h). The intended use is a direct connection to the Maxim laser driver's TXD input if this is desired. When V_{CC} < POA, TXDOUT is high impedance.

Transmit Fault (TXFOUT) Output

TXFOUT can be triggered by TXF input and all alarms, warnings, and quick trips (Figure 16). The six ADC alarms, warnings, and the LOS quick trips require enabling (Table 01h/05h, Registers F8h, FCh–FDh). See Figures 17a and 17b for nonlatched and latched operation. Latching of the alarms is controlled by the CNFGB and CNFGC registers (Table 02h, Registers 8Ah–8Bh).

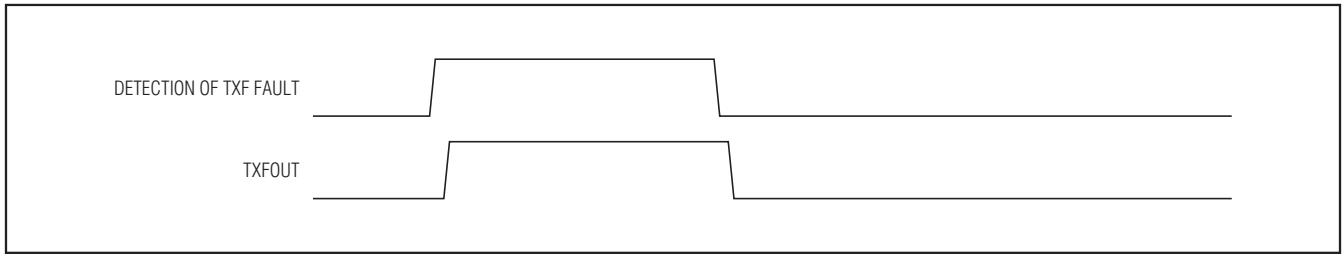


Figure 17a. TXFOUT Nonlatched Operation

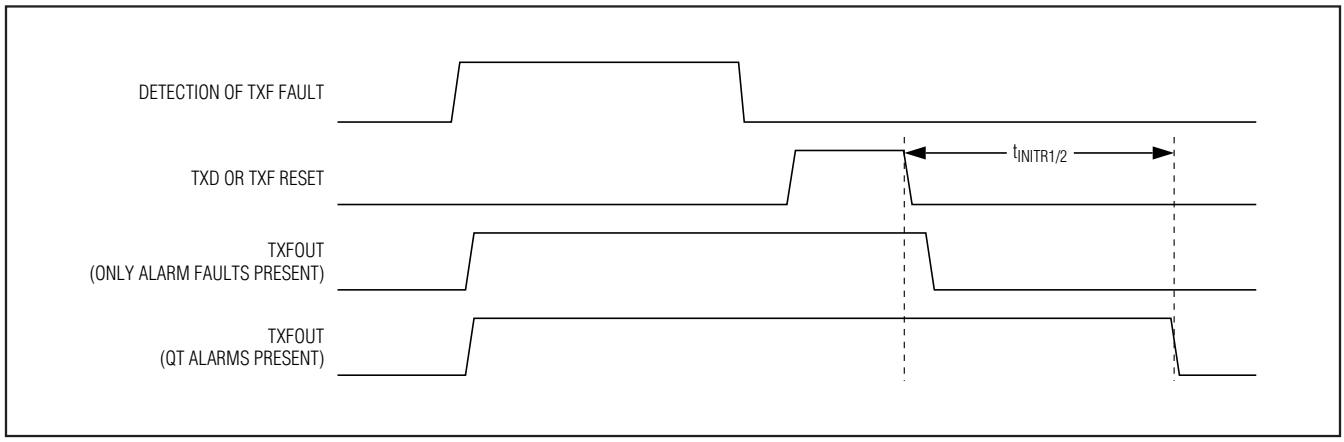


Figure 17b. TXFOUT Latched Operation and TXD_TXFEN = 1

By default, TXD does not impact TXFOUT (TXD_TXFEN = 0). This is shown in the Figure 17c. When TXD_TXFEN = 1, TXD affects TXFOUT. The particular behavior is described in Figure 17a and 17b.

VCCTXF is a new control bit is required to enable/disable VCC LO alarm/warning before the first V_{CC} conversion is complete. If VCCTXF = 1, VCC LO alarm/warning does not generate TXFOUT before the first V_{CC} conversion (which takes approximately 13ms to complete). When VCCTXF = 0, VCC LO alarm/warning generates TXFOUT before the first V_{CC} conversion, which is illustrated in Figure 17c and Figure 17d.

Two conditions are shown. In the first instance, V_{CC} powers on quickly and goes above the VCC LO threshold before the first conversion is complete (approximately 13ms).

In the other instance, V_{CC} would power up and go above the VCC LO threshold after the first conversion is complete. In this case TXFOUT behaves as in Figure 17d.

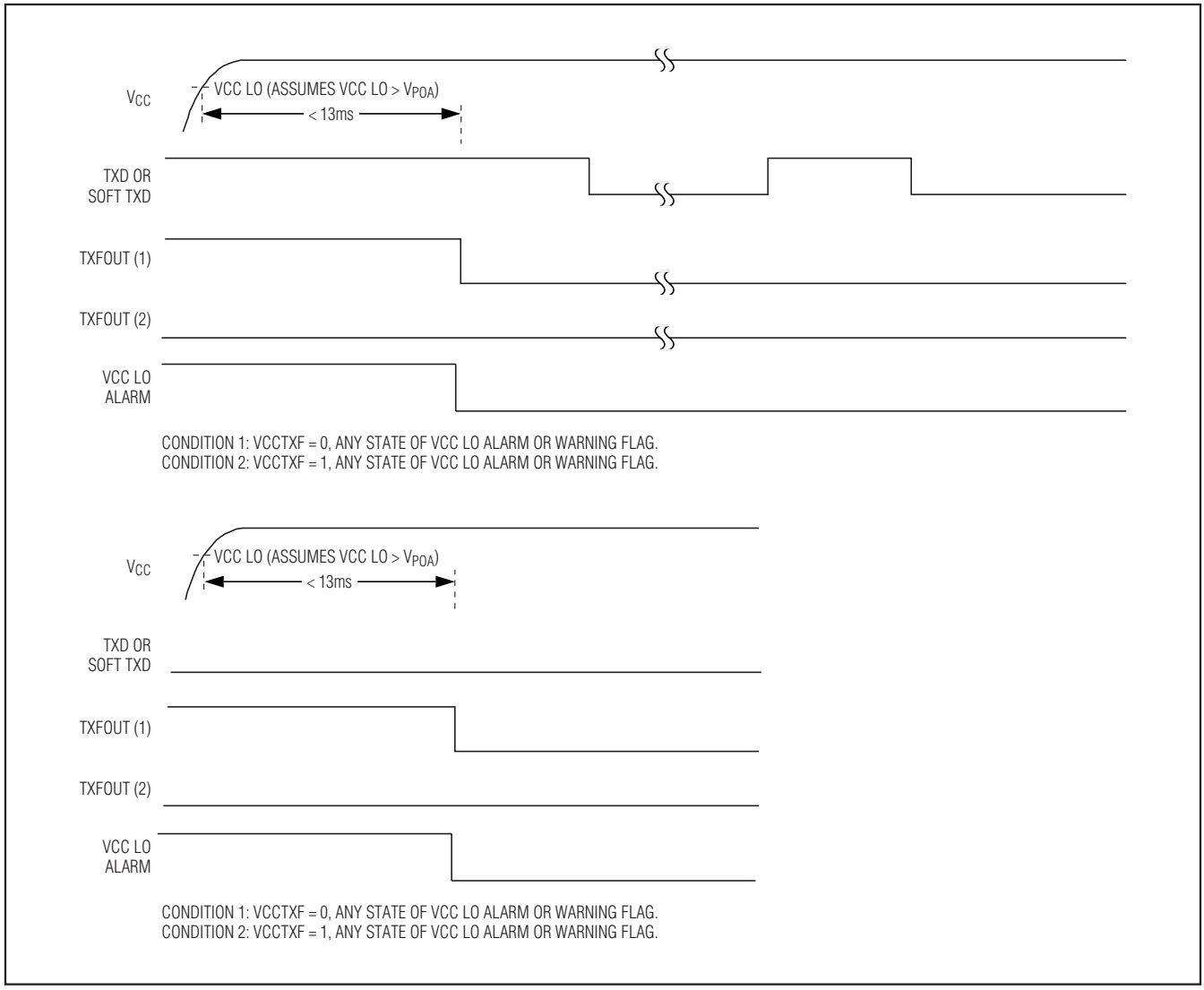


Figure 17c. TXFOUT When TXD_TXFEN = 0 on Fast Power-On