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DS1884

SFP and PON ONU Controller with Digital LDD Interface

General Description

The DS1884 controls and monitors all functions for SFF, SFP, and SFP+ modules including all SFF-8472 functionality. The combination of the DS1884 with the MAX3710 supports all transmitter and receiver functionality. The DS1884 includes modulation current control and APC set-point control with tracking error adjustment. It continually monitors RSSI for LOS generation. A 13-bit analog-to-digital converter (ADC) monitors V_{CC}, temperature, laser bias, laser modulation, and receive power to meet all monitoring requirements. Receive power measurement is differential with support for common mode to V_{CC}. A 9-bit digital-to-analog converter (DAC) is included with temperature compensation for APD bias control.

Applications

SFF, SFP, and PON ONU Modules

Ordering Information appears at end of data sheet.

For related parts and recommended products to use with this part, refer to www.maximintegrated.com/DS1884.related.

Features

- **Meets All SFF-8472 Control and Monitoring Requirements**
- **Companion Controller for the MAX3710 Laser Driver/Limiting Amplifier and MAX3945 Limiting Amplifier**
- **MAX3710/DS1884 Combination Supports Broad Spectrum of Continuous Mode and PON Applications Up to 2.5GHz**
- **Temperature Lookup Table (LUT) to Compensate for APC Tracking Error and Dual Closed-Loop Variables**
- **Three Laser Control Modes**
  - **Dual Closed Loop: Laser Bias and Laser Modulation Are Automatically Controlled with Multiple LUTs to Compensate Dual Closed-Loop Calibration Points**
  - **APC Loop: Laser Bias Automatically Controlled, Laser Modulation Controlled by Temperature LUT**
  - **Open Loop: Laser Bias and Laser Modulation Are Controlled by Temperature LUTs**
- **13-Bit ADC**
  - **Laser Bias, Laser Power, and Receive Power Support Internal and External Calibration**
  - **Differential Receive Power Input**
  - **Scalable Dynamic Range**
  - **Internal Direct-to-Digital Temperature Sensor**
  - **Alarm and Warning Flags for All Monitored Channels**
- **9-Bit DAC with Temperature Compensation for APD Bias**
- **Digital I/O Pins: Transmit Disable Input/Output, Rate Select Input/Output, LOS Input/Output, Transmit Fault Input/Output, and IN1 Status Monitor and Fault input**
- **Comprehensive Fault Measurement System with Maskable Alarm/Warnings**
- **Flexible Password Scheme Provides Three Levels of Security**
- **256-Byte A0h and 128-Byte Upper A2h EEPROM**
- **I^2C-Compatible Interface**
- **3-Wire Master to Communicate with the MAX3710 Laser Driver/Limiting Amplifier and MAX3945 Limiting Amplifier**

For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim Integrated's website at www.maximintegrated.com.

19-5928; Rev 1; 7/11

DS1884

SFP and PON ONU Controller with Digital LDD Interface

TABLE OF CONTENTS

General Description 1
Applications 1
Features 1
Absolute Maximum Ratings 10
Recommended Operating Conditions 10
DC Electrical Characteristics 10
DAC Electrical Characteristics 11
Analog Voltage Monitoring Characteristics 11
Digital Thermometer Characteristics 11
AC Electrical Characteristics 12
Startup Timing Characteristics 12
3-Wire Digital Interface Specification 12
I2C AC Electrical Characteristics 13
Nonvolatile Memory Characteristics 13
Typical Operating Characteristics 14
Pin Configuration 15
Pin Description 15
Block Diagram 16
Typical Operating Circuit—GPON ONU 17
Typical Operating Circuit—10G PON ONU 18
Detailed Description 19
- Monitors and Fault Detection 19
  - Monitors 19
  - ADC Monitors and Alarms 19
  - Alarms and Warnings 20
  - ADC Timing 20
  - Right-Shifting ADC Result 20
  - Differential RSSI Input 21
  - Laser Bias and Laser Power Through TXMON 21
  - Enhanced RSSI Monitoring (Dual Range Functionality) 21
    - APD Mode 21
    - PIN Mode 22
- Low-Voltage Operation 23
- Power-On Analog (POA) 23
- Delta-Sigma Output and Reference 24
- Digital I/O Pins 26

TABLE OF CONTENTS (continued)

LOS, LOSOUT . . . 26
RSEL . . . 26
TXD, TXDOUT . . . 26
IN1, TXF, Transmit Fault (TXFOUT) Output . . . 27
Die Identification . . . 27
DS1884 Master Communication Interface . . . 28
3-Wire Master Interface . . . 28
Protocol . . . 28
3-Wire Slave Register Map and DS1884 Corresponding Location . . . 29
3-Wire Master Flowchart . . . 29
DS1884 with MAX3710 Operating Modes . . . 31
Open Loop Mode, DPC_EN = 0, APC_EN = 0 . . . 31
APC Loop Mode, DPC_EN = 0, APC_EN = 1 . . . 31
Dual Closed-Loop Mode, DPC_EN = 1, APC_EN = 1 . . . 31
BIAS, MODULATION, SET_2XAPC, TXCTRL5 LUTs . . . 31
MODULATION Value . . . 33
BIAS Value . . . 33
Power Leveling . . . 34
Manual MAX3710 Operations . . . 34
I2C Communication . . . 34
I2C Definition . . . 34
I2C Protocol . . . 36
Memory Organization . . . 37
Register Descriptions . . . 39
A2h Lower Memory Register Map . . . 39
A2h Table 01h Register Map . . . 39
A2h Table 02h Register Map . . . 40
A2h Table 04h Register Map . . . 41
A2h Table 05h Register Map . . . 41
A2h Table 06h Register Map . . . 41
A2h Table 08h Register Map . . . 42
A2h Table 09h Register Map . . . 42
Auxiliary A0h Memory Register Map . . . 42
A2h Lower Memory Register Descriptions . . . 43
A2h Lower Memory, Register 00h–01h: TEMP ALARM HI . . . 43
A2h Lower Memory, Register 04h–05h: TEMP WARN HI . . . 43

TABLE OF CONTENTS (continued)

A2h Lower Memory, Register 02h–03h: TEMP ALARM LO . . . 43
A2h Lower Memory, Register 06h–07h: TEMP WARN LO . . . 43
A2h Lower Memory, Register 08h–09h: V_{CC} ALARM HI . . . 44
A2h Lower Memory, Register 0Ch–0Dh: V_{CC} WARN HI . . . 44
A2h Lower Memory, Register 10h–11h: TXB ALARM HI . . . 44
A2h Lower Memory, Register 14h–15h: TXB WARN HI . . . 44
A2h Lower Memory, Register 18h–19h: TXP ALARM HI . . . 44
A2h Lower Memory, Register 1Ch–1Dh: TXP WARN HI . . . 44
A2h Lower Memory, Register 20h–21h: RSSI ALARM HI . . . 44
A2h Lower Memory, Register 24h–25h: RSSI WARN HI . . . 44
A2h Lower Memory, Register 0Ah–0Bh: V_{CC} ALARM LO . . . 45
A2h Lower Memory, Register 0Eh–0Fh: V_{CC} WARN LO . . . 45
A2h Lower Memory, Register 12h–13h: TXB ALARM LO . . . 45
A2h Lower Memory, Register 16h–17h: TXB WARN LO . . . 45
A2h Lower Memory, Register 1Ah–1Bh: TXP ALARM LO . . . 45
A2h Lower Memory, Register 1Eh–1Fh: TXP WARN LO . . . 45
A2h Lower Memory, Register 22h–23h: RSSI ALARM LO . . . 45
A2h Lower Memory, Register 26h–27h: RSSI WARN LO . . . 45
A2h Lower Memory, Register 28h–37h: EMPTY . . . 46
A2h Lower Memory, Register 38h–5Fh: EE . . . 46
A2h Lower Memory, Register 60h–61h: TEMP VALUE . . . 46
A2h Lower Memory, Register 62h–63h: V_{CC} VALUE . . . 47
A2h Lower Memory, Register 64h–65h: TXB VALUE . . . 47
A2h Lower Memory, Register 66h–67h: TXP VALUE . . . 47
A2h Lower Memory, Register 68h–69h: RSSI VALUE . . . 47
A2h Lower Memory, Register 6Ah–6Dh: RESERVED . . . 47
A2h Lower Memory, Register 6Eh: STATUS . . . 48
A2h Lower Memory, Register 6Fh: UPDATE . . . 49
A2h Lower Memory, Register 70h: $ALARM_3$ . . . 50
A2h Lower Memory, Register 71h: $ALARM_2$ . . . 51
A2h Lower Memory, Register 72h–73h: RESERVED . . . 51
A2h Lower Memory, Register 74h: $WARN_3$ . . . 52
A2h Lower Memory, Register 75h: $WARN_2$ . . . 53
A2h Lower Memory, Register 76h–7Ah: RESERVED . . . 53
A2h Lower Memory, Register 7Bh–7Eh: PASSWORD ENTRY (PWE) . . . 54

TABLE OF CONTENTS (continued)

A2h Lower Memory, Register 7Fh: TBL SEL 54
A2h Table 01h Register Descriptions 55
A2h Table 01h, Register 80h–BFh: EEPROM. 55
A2h Table 01h, Register C0h–F7h: EEPROM 55
A2h Table 01h, Register F8h: ALARM EN_3 OR EE 56
A2h Table 01h, Register F9h: ALARM EN_2 OR EE 57
A2h Table 01h, Register FAh–FBh: RESERVED OR EE. 57
A2h Table 01h, Register FCh: WARN EN_3 OR EE 58
A2h Table 01h, Register FDh: WARN EN_2 OR EE 59
A2h Table 01h, Register FEh–FFh: RESERVED OR EE 59
A2h Table 02h Register Descriptions 60
A2h Table 02h, Register 80h: MODE. 60
A2h Table 02h, Register 81h: Temperature Index (TINDEX) 61
A2h Table 02h, Register 82h–83h: MODULATION VALUE 61
A2h Table 02h, Register 84h: RESERVED 61
A2h Table 02h, Register 85h: APC VALUE 62
A2h Table 02h, Register 86h–87h: SET_IBIAS VALUE 62
A2h Table 02h, Register 88h: DACFS 62
A2h Table 02h, Register 89h: CNFGA 63
A2h Table 02h, Register 8Ah: CNFGB. 64
A2h Table 02h, Register 8Bh: CNFGC. 65
A2h Table 02h, Register 8Ch: DEVICE ADDRESS 66
A2h Table 02h, Register 8Dh: CNFGD 66
A2h Table 02h, Register 8Eh: RIGHT-$SHIFT_1$ ($RSHIFT_1$) 66
A2h Table 02h, Register 8Fh: RIGHT-$SHIFT_0$ ($RSHIFT_0$). 67
A2h Table 02h, Register 90h–91h: XOVER COARSE 67
A2h Table 02h, Register 92h–93h: V_{CC} SCALE 68
A2h Table 02h, Register 94h–95h: TXB SCALE 68
A2h Table 02h, Register 96h–97h: TXP SCALE. 68
A2h Table 02h, Register 98h–99h: RSSI FINE SCALE 68
A2h Table 02h, Register 9Ah–9Bh: RESERVED 68
A2h Table 02h, Register 9Ch–9Dh: RSSI COARSE SCALE 68
A2h Table 02h, Register 9Eh–9Fh: RESERVED. 68
A2h Table 02h, Register A0h–A1h: XOVER FINE. 69
A2h Table 02h, Register A2h–A3h: V_{CC} OFFSET 69
A2h Table 02h, Register A4h–A5h: TXB OFFSET 69

TABLE OF CONTENTS (continued)

A2h Table 02h, Register A6h–A7h: TXP OFFSET 69
A2h Table 02h, Register A8h–A9h: RSSI FINE OFFSET 69
A2h Table 02h, Register AAh–ABh: RESERVED 69
A2h Table 02h, Register ACh–ADh: RSSI COARSE OFFSET 69
A2h Table 02h, Register AEh–AFh: INTERNAL TEMP OFFSET 70
A2h Table 02h, Register B0h–B3h: PW1 70
A2h Table 02h, Register B4h–B7h: PW2 71
A2h Table 02h, Register B8h–BFh: EMPTY 71
A2h Table 02h, Register C0h: PW_ENA 72
A2h Table 02h, Register C1h: PW_ENB 73
A2h Table 02h, Register C2h–C6h: RESERVED 74
A2h Table 02h, Register C7h: TBLSELPON 74
A2h Table 02h, Register C8h–C9h: DAC VALUE 74
A2h Table 02h, Register CAh: INCBYTE 75
A2h Table 02h, Register CBh: TXCTRL5 DPC 75
A2h Table 02h, Register CCh: IMODMAX 75
A2h Table 02h, Register CDh: IBIASMAX 76
A2h Table 02h, Register CEh: DEVICE ID 76
A2h Table 02h, Register CFh: DEVICE VER 76
A2h Table 02h, Register D0h–DFh: EMPTY 77
A2h Table 02h, Register E0h: RXCTRL1 77
A2h Table 02h, Register E1h: RXCTRL2 77
A2h Table 02h, Register E2h: SETCML 78
A2h Table 02h, Register E3h: SETLOSH 78
A2h Table 02h, Register E4h: TXCTRL1 78
A2h Table 02h, Register E5h: TXCTRL2 79
A2h Table 02h, Register E6h: TXCTRL3 79
A2h Table 02h, Register E7h: TXCTRL4 79
A2h Table 02h, Register E8h: TXCTRL5 APC OL 80
A2h Table 02h, Register E9h: TXCTRL6 80
A2h Table 02h, Register EAh: TXCTRL7 80
A2h Table 02h, Register EBh: RESERVED 81
A2h Table 02h, Register ECh: SETLOSH_3945 81
A2h Table 02h, Register EDh: SETLOSL_3945 81
A2h Table 02h, Register EEh: SETLOSTIMER_3945 82
A2h Table 02h, Register EFh: 3WSET 82

TABLE OF CONTENTS (continued)

A2h Table 02h, Register F0h: 3WCTRL . . . 83
A2h Table 02h, Register F1h: ADDRESS . . . 83
A2h Table 02h, Register F2h: WRITE . . . 84
A2h Table 02h, Register F3h: READ . . . 84
A2h Table 02h, Register F4h: TXSTAT2 . . . 84
A2h Table 02h, Register F5h: TXSTAT1 . . . 85
A2h Table 02h, Register F6h: DPCSTAT . . . 85
A2h Table 02h, Register F7h: RXSTAT . . . 85
A2h Table 02h, Register F8h–FFh: RESERVED . . . 85
A2h Table 04h Register Descriptions . . . 86
A2h Table 04h, Register 80h–A7h or 80h–9Fh: MODULATION or TXCTRL5 LUT . . . 86
A2h Table 04h, Register A8h–EFh: EMPTY . . . 86
A2h Table 04h, Register F0h–F7h: MOD MAX LUT . . . 86
A2h Table 04h, Register F8h–FFh: MOD OFFSET or SET_IMOD LUT . . . 87
A2h Table 06h Register Descriptions . . . 87
A2h Table 06h, Register 80h–A7h: BIAS or APC LUT . . . 87
A2h Table 06h, Register A8h–EFh: EMPTY . . . 88
A2h Table 06h, Register F0h–F7h: BIAS MAX LUT . . . 88
A2h Table 06h, Register F8h–FFh: BIAS OFFSET or SET_IBIAS LUT . . . 88
A2h Table 08h Register Descriptions . . . 89
A2h Table 08h, Register 80h–F7h: EMPTY . . . 89
A2h Table 08h, Register F8h–FBh: BIASINC LUT . . . 89
A2h Table 08h, Register FCh–FFh: MODINC LUT . . . 89
A2h Table 09h Register Descriptions . . . 90
A2h Table 09h, Register 80h–F7h: EMPTY . . . 90
A2h Table 09h, Register F8h–FFh: DAC OFFSET LUT . . . 90
Auxiliary Memory A0h Register Description . . . 90
Auxiliary Memory A0h, Register 00h–FFh: EEPROM . . . 90
Applications Information . . . 91
Power-Supply Decoupling . . . 91
Layout Considerations . . . 91
SDA and SCL Pullup Resistors . . . 91
Ordering Information . . . 91
Package Information . . . 91
Revision History . . . 92

LIST OF FIGURES

Figure 1. ADC Channel 19
Figure 2. ADC Round-Robin Timing. 20
Figure 3. RSSI Differential Input for High-Side RSSI 21
Figure 4. Laser Bias (TXB) and Laser Power (TXP) Monitoring Through TXMON 21
Figure 5. RSSI in APD Mode 22
Figure 6. RSSI in PIN Mode 22
Figure 7. Low-Voltage Hysteresis Example 24
Figure 8. Recommended Shunt Reference and RC Filter for DAC Output 24
Figure 9. Delta-Sigma Output 25
Figure 10. Logic Diagram 1 26
Figure 11. Logic Diagram 2 26
Figure 12a. TXFOUT Nonlatched Operation 27
Figure 12b. TXFOUT Latched 27
Figure 12c. TXFOUT During Power-On 27
Figure 13. 3-Wire Interface Timing Diagram 28
Figure 14. 3-Wire Flowchart 30
Figure 15. Offset LUT 33
Figure 16. MODULATION LUT (Open Loop and APC Mode) 33
Figure 17. BIAS LUT (Open Loop) 33
Figure 18. I2C Timing Diagram 35
Figure 19. Example I2C Timing 36
Figure 20. Memory Organization 38

LIST OF TABLES

Table 1. Acronyms 19
Table 2. ADC Default Monitor Full-Scale Ranges 19
Table 3. RSSI Hysteresis Threshold Values 23
Table 4. RSSI Configuration Registers 23
Table 5. 3-Wire Transaction Detail 28
Table 6. 3-Wire Register Map and DS1884 Corresponding Location 29
Table 7. DS1884 LUT Functions in Open Loop, APC Loop, and Dual Closed-Loop Modes 31
Table 8. DS1884 LUT Memory Map for 4-Row Table (Temperature Values Indicated in °C) 32
Table 9. DS1884 LUT Memory Map for 4-Row Table (TINDEX Values Indicated in Hex) 32
Table 10. DS1884 LUT Memory Map for 5-Row Table (Temperature Values Indicated in °C) 32
Table 11. DS1884 LUT Memory Map for 5-Row Table (TINDEX Values Indicated in Hex) 32
Table 12. Temperature Resolution for Offsets 33
Table 13. Power Leveling Details 34

ABSOLUTE MAXIMUM RATINGS

Voltage Range on IN1, DAC, LOS, RSSIP, RSSIN, REFIN, RSEL, TXF, TXMON and TXD Pins Relative to Ground ..... -0.5V to (V_{CC} + 0.5V) (subject to not exceeding +6V)

Voltage Range on V_{CC}, SDA, SCL, TXFOUT and LOSOUT Pins Relative to Ground .....-0.5V to +6V

Continuous Power Dissipation (T_A = +70°C)
TQFN (derate 28.6mW/°C above +70°C).....2285.7mW

Operating Temperature Range ..... -40°C to +95°C

Programming Temperature Range ..... 0°C to +95°C

Storage Temperature Range..... -55°C to +125°C

Lead Temperature (soldering, 10s) .....+300°C

Soldering Temperature (reflow) .....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

(T_A = -40°C to +95°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Main Supply Voltage	V_{CC}	(Note 1)	2.85		3.6	V
High-Level Input Voltage (SDA, SCL, SDAOUT)	$V_{IH:1}$		0.7 x V_{CC}		V_{CC} + 0.3	V
Low-Level Input Voltage (SDA, SCL, SDAOUT)	$V_{IL:1}$		-0.3		+0.3 x V_{CC}	V
High-Level Input Voltage (IN1, LOS, RSEL, TXD, TXF)	$V_{IH:2}$		2.0		V_{CC} + 0.3	V
Low-Level Input Voltage (IN1, LOS, RSEL, TXD, TXF)	$V_{IL:2}$		-0.3		+0.8	V

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = +2.85V to +3.6V, T_A = -40°C to +95°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current	I_{CC}	(Notes 1, 2)		1	2	mA
Output Leakage (LOSOUT, SDA, SDAOUT, TXFOUT)	I_{LO}				1	µA
Low-Level Output Voltage (CSEL1OUT, CSEL2OUT, LOSOUT, SDA, SDAOUT, SCLOUT, TXDOUT, TXFOUT)	V_{OL}	I_{OL} = 4mA			0.4	V
		I_{OL} = 6mA			0.6	
High-Level Output Voltage (CSEL1OUT, CSEL2OUT, SCLOUT, SDAOUT, TXDOUT)	V_{OH}	I_{OH} = 4mA	V_{CC} - 0.4			V
Input Leakage Current (IN1, LOS, RSEL, SCL, TXD, TXF)	I_{LI}				1	µA
Digital Power-On Reset	POD		2.1		2.6	V
Analog Power-On Reset	POA		2.2		2.8	V

DAC ELECTRICAL CHARACTERISTICS

(V_{CC} = +2.85V to +3.6V, T_A = -40°C to +95°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Delta-Sigma Input Clock Frequency	f_{DS}			2		MHz
Reference Voltage Input (REFIN)	V_{REFIN}	Minimum 0.1µF to GND	2		V_{CC}	V
Output Range			0		V_{REFIN}	V
Output Resolution		See the *Delta-Sigma Output and Reference* section for details (DAC FS[9:2] = FFh)			10	Bits
Output Impedance	R_{DS}	V_{REFIN} = 2.5V		45	100	Ω
Recovery After Power-Up	t_{INIT_DAC}	From V_{CC} > VCC LO alarm or warning	See the *Startup Timing Characteristics* table			ms

ANALOG VOLTAGE MONITORING CHARACTERISTICS

(V_{CC} = +2.85V to +3.6V, T_A = -40°C to +95°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ADC Resolution		(Note 3)		13		Bits
INL		T_A = +25°C	-3		+3	LSB
DNL			-1		+1	LSB
Update Rate for Temperature, TXMON (TXB/TXP), RSSIP-RSSIN, V_{CC}	t_{RR}	RSSIP-RSSIN requires only a coarse conversion (Note 4)		30		ms
Update Rate for RSSIP-RSSIN	$t_{R/R2}$	RSSIP-RSSIN requires a fine conversion		36		ms
Input/Supply Offset (TXMON, RSSIP, RSSIN, V_{CC})	V_{OS}	(Notes 4, 5)	-1	0	+1	LSB
Factory Setting Full Scale		TXMON and RSSIP-RSSIN coarse (Notes 5, 6)		2.5		V
		V_{CC} (Note 6)		6.5536		
		RSSIP-RSSIN fine (Note 6)		312.5		µV
Temperature LSB Weighting				1/256		°C

DIGITAL THERMOMETER CHARACTERISTICS

(V_{CC} = +2.85V to +3.6V, T_A = -40°C to +95°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Thermometer Error	T_{ERR}	-40°C to +95°C	-2		+2	°C

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = +2.85V to +3.6V, T_A = -40°C to +95°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
TXD Rising Edge to Fault Clear	t_{OFF}	From ↑ TXD (Notes 7, 8)			5	µs
TXD Falling Edge to TXDOUT Falling	t_{ON}	From ↓ TXD (Note 9)			5	µs
Recovery After Power-Up: MAX3710	t_{INIT_3710}	From ↑ V_{CC} > POA (Note 10)		1		ms
Recovery After Power-Up: MAX3710 and MAX3945	t_{INIT_3945}	From ↑ V_{CC} > VCC LO alarm or warning (Note 11)		1		ms
Fault Assert Time (to TXFOUT = 1)	t_{INITR1}	From ↓ TXD		30		ms
Fault Reset Time at Power-On (to TXFOUT = 0)	t_{INITR2}	From ↑ V_{CC} > POA, Figure 12c (Note 12)		12.5		ms

STARTUP TIMING CHARACTERISTICS

(V_{CC}= +2.85V to +3.6V, T_A = -40°C to +95°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Enable Time Following POA	t_{INIT}	(Notes 12, 13)		13		ms

3-WIRE DIGITAL INTERFACE SPECIFICATION

(V_{CC} = +2.85V to +3.6V, T_A = -40°C to +95°C, unless otherwise noted. Timing is referenced to $V_{IL(MAX)}$ and $V_{IH(MIN)}$.) (See Figure 13.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SCLOUT Clock Frequency	f_{SCLOUT}			1		MHz
SCLOUT Duty Cycle	t_{3WDC}			50		%
SDAOUT Setup Time	t_{DS}			500		ns
SDAOUT Hold Time	t_{DH}		100			ns
CSEL1OUT, CSEL2OUT Pulse-Width Low	t_{CSW}		1			µs
CSEL1OUT, CSEL2OUT Leading Time Before the First SCLOUT Edge	t_L			1		µs
CSEL1OUT, CSEL2OUT Trailing Time After the Last SCLOUT Edge	t_T			1		µs
SDAOUT, SCLOUT Load	C_{B3W}	Total bus capacitance on one line			10	pF

I²C AC ELECTRICAL CHARACTERISTICS

(V_{CC} = +2.85V to +3.6V, T_A = -40°C to +95°C, unless otherwise noted. Timing is referenced to $V_{IL(MAX)}$ and $V_{IH(MIN)}$.) (See Figure 18.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SCL Clock Frequency	f_{SCL}	(Note 14)	0		400	kHz
Clock Pulse-Width Low	t_{LOW}		1.3			µs
Clock Pulse-Width High	t_{HIGH}		0.6			µs
Bus Free Time Between STOP and START Condition	t_{BUF}		1.3			µs
START Hold Time	$t_{HD:STA}$		0.6			µs
START Setup Time	$t_{SU:STA}$		0.6			µs
Data in Hold Time	$t_{HD:DAT}$		0		0.9	µs
Data in Setup Time	$t_{SU:DAT}$		100			ns
Rise Time of Both SDA and SCL Signals	t_R	(Note 15)	20 + 0.1C_B		300	ns
Fall Time of Both SDA and SCL Signals	t_F	(Note 15)	20 + 0.1C_B		300	ns
STOP Setup Time	$t_{SU:STO}$		0.6			µs
Capacitive Load for Each Bus Line	C_B				400	pF
EEPROM Write Time	t_W	(Note 16)			20	ms

NONVOLATILE MEMORY CHARACTERISTICS

(V_{CC} = +2.85V to +3.6V, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
EEPROM Write Cycles		At T_A = +25°C	50,000			—
		At T_A = +85°C	10,000			

Note 1: All voltages are referenced to ground. Current entering the IC is considered positive, and current exiting the IC is considered negative.

Note 2: Inputs are at supply rail. Outputs are not loaded. Does not include REFIN current. Measured using the *Typical Operating Circuit—GPON ONU*.

Note 3: The ADC output is available internally as a 16-bit value. The 16 bits are derived by left-shifting the 13-bit ADC output by 3.

Note 4: Guaranteed by design.

Note 5: TXB (transmit bias) and TXP (transmit power) are separate ADC conversions that are performed on the same input pin, TXMON.

Note 6: Full scale is user-programmable.

Note 7: Time until faults are cleared (falling edge of TXFOUT).

Note 8: Time until rising edge of TXDOUT.

Note 9: Time until falling edge of TXDOUT.

Note 10: Time until completion of initial MAX3710 control registers configuration.

Note 11: Time until completion of initial MAX3945 and MAX3710 control registers configuration.

Note 12: VCC LO alarm or warning is enabled, a V_{CC} conversion is completed, and V_{CC} is above VCC LO alarm or warning. See Figure 12c.

Note 13: DAC output valid, 3-wire writes from LUTs complete, and digital outputs valid.

Note 14: I²C interface timing shown is for fast-mode (400kHz) operation. This device is also backward compatible with I²C standard mode.

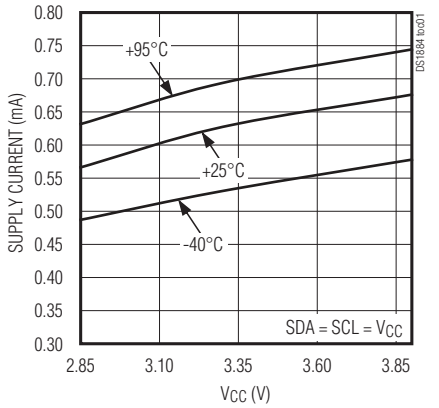
Note 15: C_B = Total capacitance of one bus line in pF.

Note 16: EEPROM write begins after a STOP condition occurs.

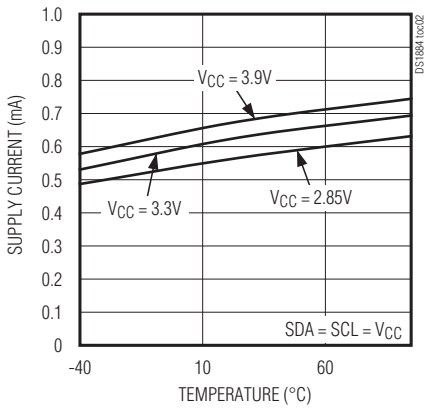
Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)

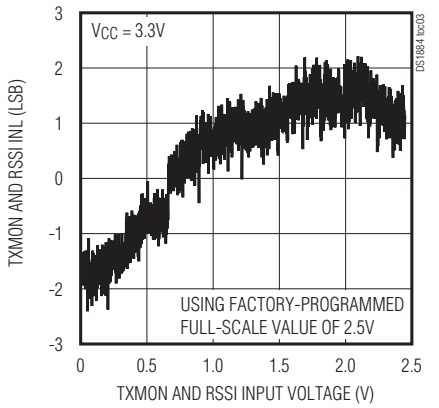
SUPPLY CURRENT vs. SUPPLY VOLTAGE



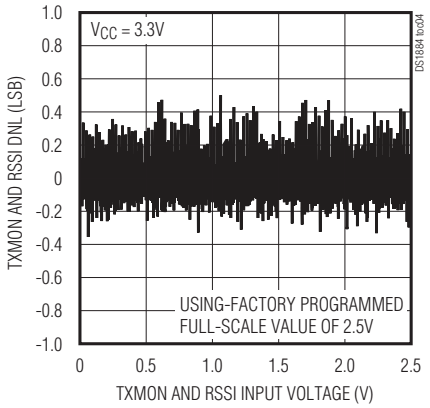
SUPPLY CURRENT vs. TEMPERATURE



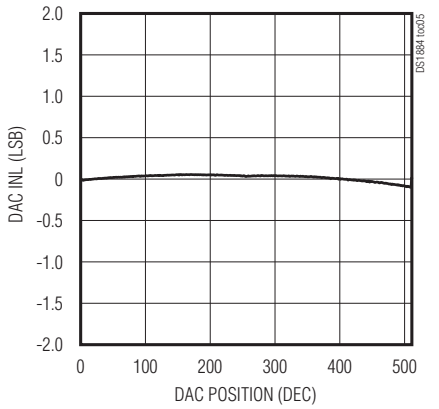
TXMON AND RSSI INL



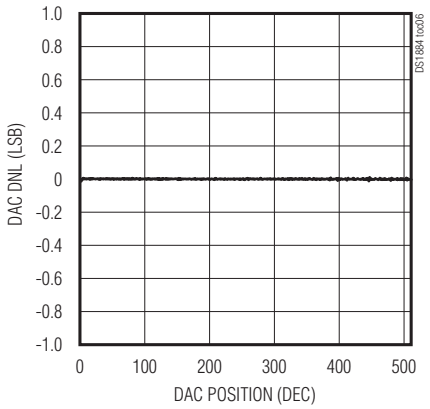
TXMON AND RSSI DNL



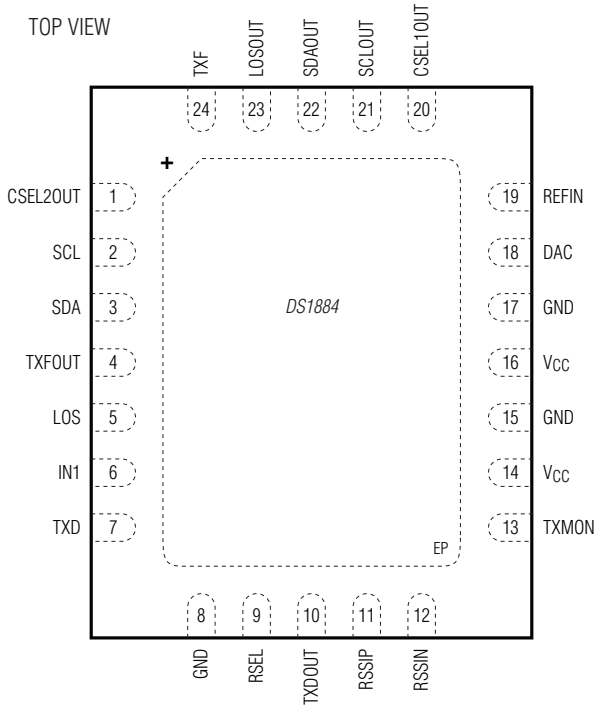
DAC INL



DAC DNL



Pin Configuration

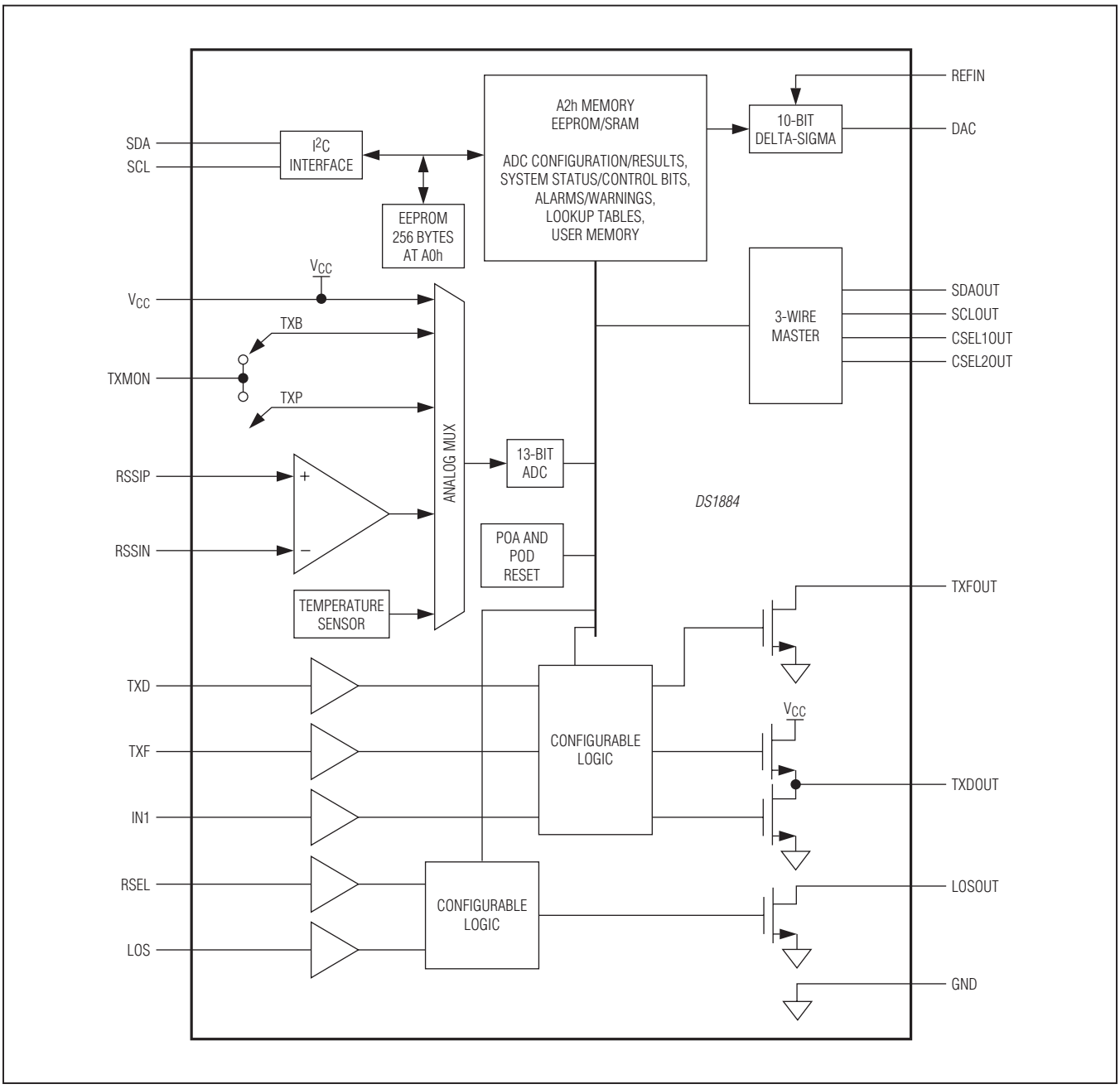


TQFN
(4mm × 5mm × 0.75mm)

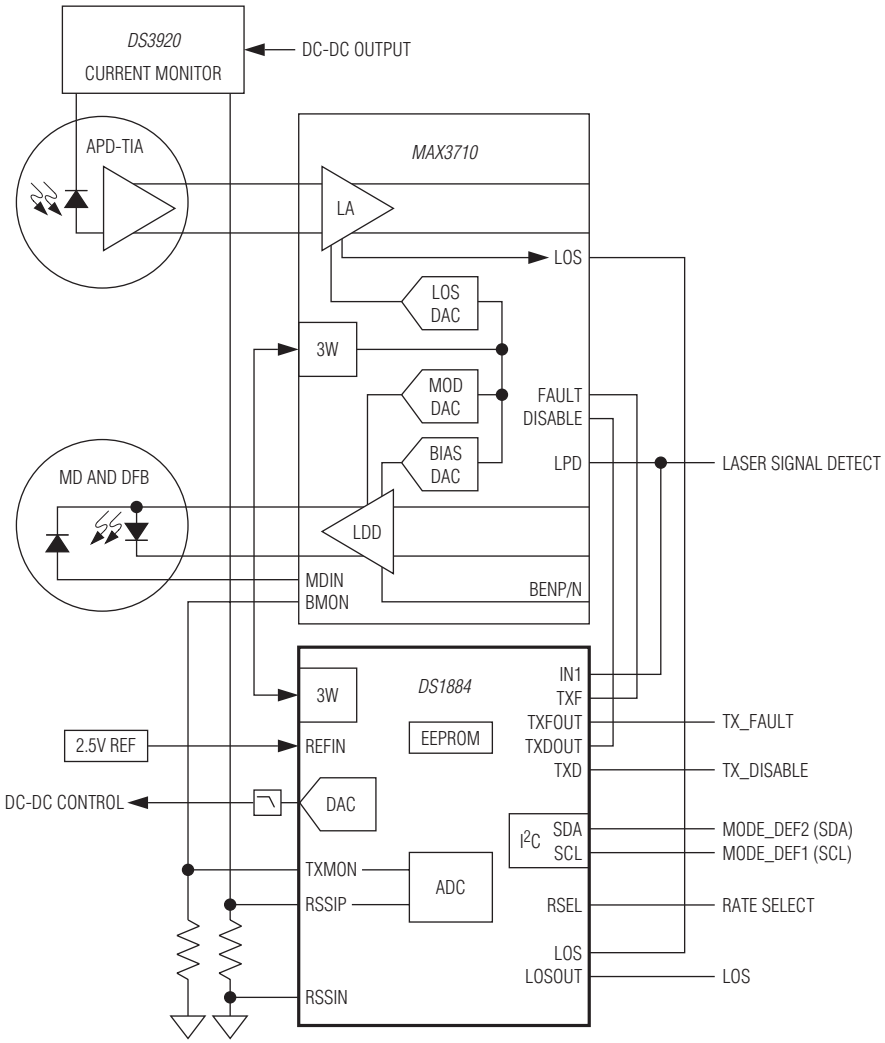
Pin Description

PIN	NAME	FUNCTION
1	CSEL2OUT	Chip-Select Output. Part of the 3-wire interface to the MAX3945.
2	SCL	I^2C Serial-Clock Input
3	SDA	Open-Drain I^2C Serial-Data Input/ Output
4	TXFOUT	Open-Drain Transmit Fault Output
5	LOS	Loss-of-Signal Input
6	IN1	Digital Maskable Fault Input
7	TXD	Transmit Disable Input
8, 15, 17	GND	Ground
9	RSEL	Rate Select Input
10	TXDOUT	Transmit Disable Output
11, 12	RSSIP, RSSIN	Differential External Monitor Input
13	TXMON	External Monitor Input for Both Transmit Power (TXP) and Transmit Bias (TXB)
14, 16	V_{CC}	Power-Supply Input
18	DAC	DAC Output
19	REFIN	Reference Input for DAC Full Scale
20	CSEL1OUT	Chip-Select Output. Part of the 3-wire interface to the MAX3710.
21	SCLOUT	Serial-Clock Output. Part of the 3-wire interface to the MAX3710.
22	SDAOUT	Serial-Data Input/Output. Part of the 3-wire interface to the MAX3710.
23	LOSOUT	Open-Drain Receive Loss-of-Signal Output
24	TXF	Transmit Fault Input
—	EP	Exposed Pad. Connect to ground.

Block Diagram



Typical Operating Circuit—GPON ONU



Typical Operating Circuit—10G PON ONU

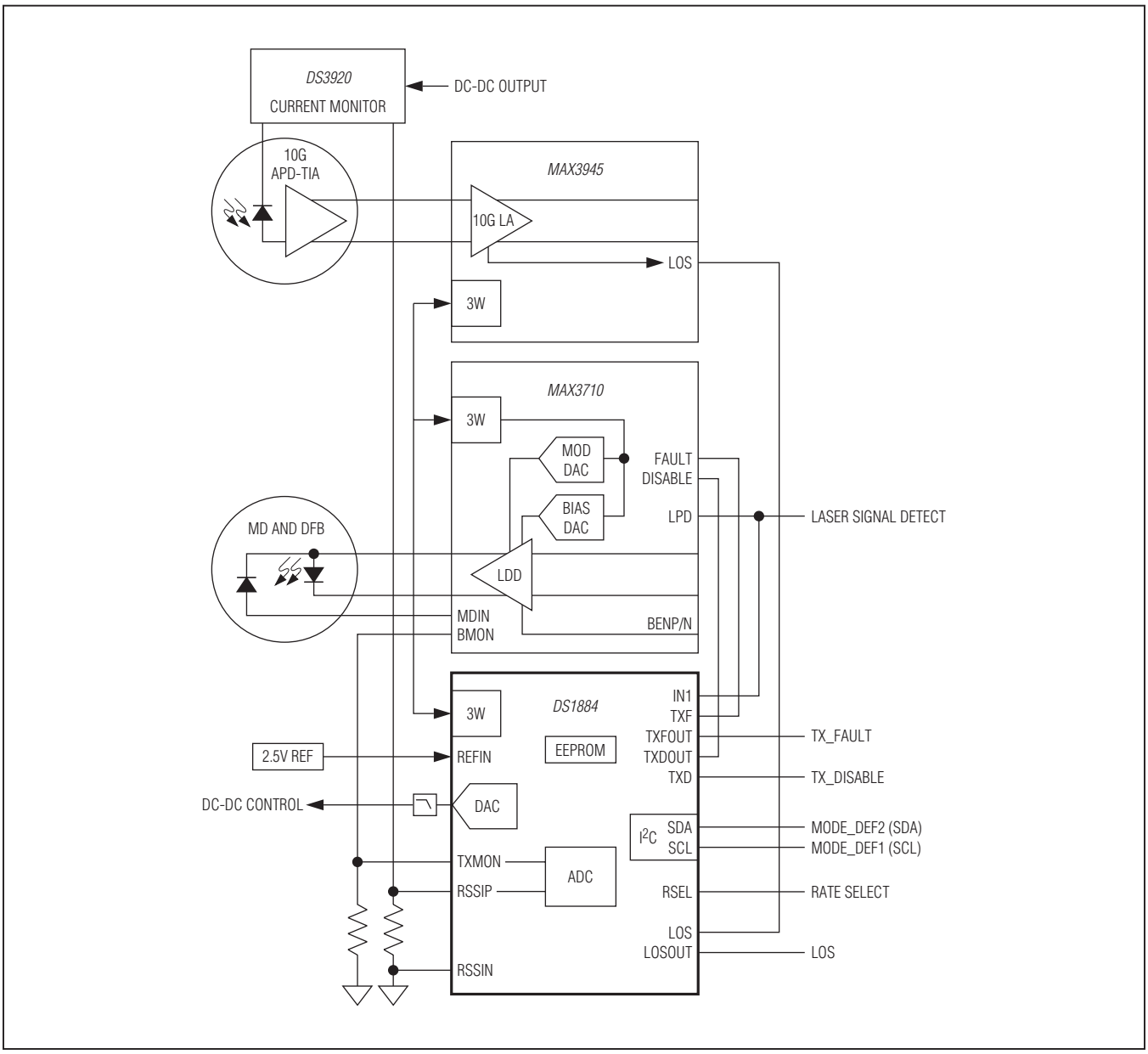


Table 1. Acronyms

ACRONYM	DESCRIPTION
ADC	Analog-to-Digital Converter
APC	Automatic Power Control
APD	Avalanche Photodiode
DAC	Digital-to-Analog Converter
LOS	Loss of Signal
LUT	LUT
NV	Nonvolatile
QT	Quick Trip
ROSA	Receiver Optical Subassembly
SEE	Shadowed EEPROM
SFF	Small Form Factor
SFF-8472	Document Defining Register Map of SFPs and SFFs
SFP	Small Form-Factor Pluggable
SFP+	Enhanced SFP
TE	Tracking Error. Deviation from linear of the relationship between transmitted power and monitor diode current.
TIA	Transimpedance Amplifier
TOSA	Transmit Optical Subassembly
TXP	Transmit Power

Detailed Description

The DS1884 integrates the control and monitoring functionality required to implement an SFP or PON ONU system using the Maxim MAX3710 or other compatible laser driver and limiting amplifier. Key components of the DS1884 are shown in the *Block Diagram* and described in subsequent sections.

Monitors and Fault Detection

Monitors

The DS1884 monitors five ADC channels. This monitoring combined with the alarm enables (A2h Table 01h/05h) determines when/if the DS1884 turns off the MAX3710 DACs and triggers the TXFOUT and TXDOUT outputs. All the monitoring levels and interrupt masks are user-programmable. See Figure 1.

ADC Monitors and Alarms

The ADC monitors temperature (internal temp sensor), V_{CC}, laser bias (TXB), laser power (TXP), and receive power (RSSIC for coarse, RSSIF for fine) using an analog multiplexer to measure them round-robin with a single ADC (see the *ADC Timing* section). The voltage channels have a customer-programmable full-scale range and all channels have a customer-programmable offset value that is factory programmed to a default value (Table 2).

Table 2. ADC Default Monitor Full-Scale Ranges

SIGNAL (UNITS)	+FS SIGNAL	+FS HEX	-FS SIGNAL	-FS HEX
Temperature (°C)	127.996	7FFFh	-128	8000h
V_{CC} (V)	6.5528	FFF8h	0	0000h
TXB, TXP, RSSIC, RSSIF (V)	2.4997	FFF8h	0	0000h

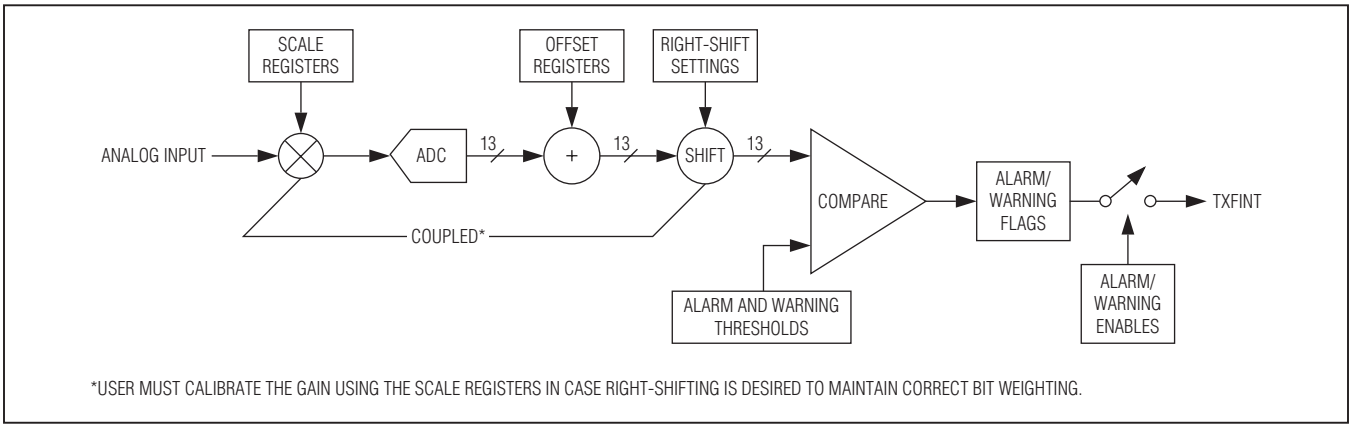


Figure 1. ADC Channel

Additionally, TXB, TXP, RSSIC, and RSSIF can right-shift results as described in the *Right-Shifting ADC Result* section. This allows customers with specified ADC ranges to calibrate the ADC input gain by a factor of 2^n to measure small signals (thereby reducing the full scale by a factor of 2^n). The DS1884 can then right-shift the results by n bits (effectively multiplying by a factor of $1/2^n$) to maintain the bit weight of their specification. See the *Right-Shifting ADC Result* and *Enhanced RSSI Monitoring (Dual Range Functionality)* sections for more information.

Alarms and Warnings

The ADC results (after right-shifting, if used) are compared to the alarm and warning thresholds after each conversion, and the corresponding alarms and/or warnings are set, which can be programmed to create the internal signal TXFINT. The status of TXFINT can be read in A2h Lower Memory, Register 71h. TXFINT is one of the signals used to trigger TXFOUT. TXFOUT can be programmed to cause TXDOUT outputs. These ADC thresholds are user-programmable, as are the masking registers that can be used to prevent the alarms from triggering the TXFOUT and TXDOUT outputs.

ADC Timing

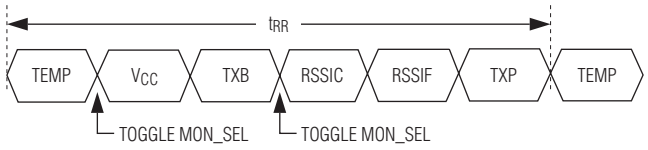
Five analog channels are digitized in a round-robin fashion in the order as shown in Figure 2. RSSI is measured twice to obtain coarse and fine measurements (RSSIC and RSSIF, respectively). The total time required to convert all channels is t_{RR} (see the *Analog Voltage Monitoring Characteristics* table for details). After each TXMON conversion, a 3-wire communication is initiated to toggle the MON_SEL bit (bit 6 in the MAX3710's TXCTRL2 register, programmed through A2h Table 02h, Register E5h, bit 6). This causes the laser driver to alternate sending laser bias (TXB) and laser power (TXP) signals to the DS1884's TXMON input.

Right-Shifting ADC Result

If the weighting of the ADC digital reading must conform to a predetermined full-scale (PFS) value defined by a standard's specification (e.g., SFF-8472), then right-shifting can be used to adjust the PFS analog measurement range while maintaining the weighting of the ADC results. The DS1884's range is wide enough to cover all requirements; when the maximum input value is ≤ 1/2 of the full-scale value, right-shifting can be used to obtain greater accuracy.

For instance, the maximum voltage might be 1/8 the specified PFS value, so only 1/8 the converter's range is effective over this range. An alternative is to calibrate the ADC's full-scale range to 1/8 the readable PFS value (by calibrating an input gain of about 8 using the scale registers) and use a right-shift value of 3. With this implementation, the resolution of the measurement is increased by a factor of 8, and because the result is digitally divided by 8 by right-shifting, the bit weight of the measurement still meets the standard's specification (i.e., SFF-8472).

The right-shift operation on the ADC result is carried out based on the contents of right-shift control registers (A2h Table 02h, Register 8Eh and A2h Table 02h, Register 8Fh) in EEPROM. TXB, TXP, RSSIC, and RSSIF have 3 bits allocated to set the number of right-shifts. Up to seven right-shift operations are allowed and are executed as a part of every conversion before the results are compared to the high and low alarm levels, or loaded into their corresponding measurement registers (Lower Memory, Registers 64h–69h). This is true during the setup of internal calibration as well as during subsequent data conversions.



NOTE: IF VCC LO ALARM OR WARNING IS ENABLED AT POWER-UP, THE ADC ROUND-ROBIN TIMING CYCLES BETWEEN TEMPERATURE AND V_{CC} ONLY UNTIL V_{CC} IS ABOVE THE VCC LO ALARM THRESHOLD.

Figure 2. ADC Round-Robin Timing

Differential RSSI Input

The DS1884 offers a fully differential input for RSSI that enables high-side monitoring of RSSI, as shown in Figure 3. This reduces board complexity by eliminating the need for a high-side differential amplifier or a current mirror.

Laser Bias and Laser Power Through TXMON

The DS1884 measures both laser bias (TXB) and laser power (TXP) through the same input pin, TXMON. The DS1884 commands the MAX3710 laser driver to output the correct monitor signal before each ADC conversions takes place. Figure 4 shows the two conversion paths. Each path has independent gain and offset calibration registers.

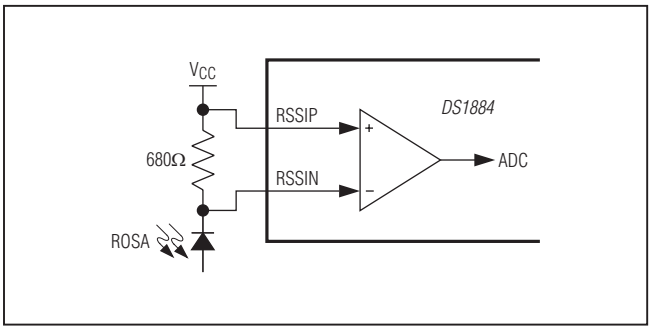


Figure 3. RSSI Differential Input for High-Side RSSI

Enhanced RSSI Monitoring (Dual Range Functionality)

The DS1884 offers a feature to improve the accuracy and range of RSSI, which is most commonly used for monitoring RSSI. To achieve the SFF-8472 requirement of 0.1µW/LSB over -40 to 8.2dBm, the DS1884 makes two measurements to effectively achieve a 16-bit conversion with a 13-bit physical ADC. This “dual range” calibration can operate in two modes: APD mode and PIN mode.

APD Mode

For systems with a nonlinear relationship between the ADC input and desired ADC result, the mode should be set to APD mode (Figure 5). The RSSI measurement of an APD receiver is one such application. Using the APD mode allows a piece-wise linear approximation of the nonlinear response of the APD’s gain factor. The crossover point is the point between fine and coarse points. The ADC result transitions between the fine and coarse ranges with no hysteresis. Right-shifting, slope adjustment, and offset are configurable for both the fine and coarse ranges. Two registers, XOVER FINE and XOVER COARSE, determine the crossover point. The XOVER FINE register (A2h Table 02h, Register A0h–A1h) determines the maximum results returned by fine ADC conversions, before right-shifting. The XOVER COARSE register (A2h Table 02h, Register 90h–91h) determines the minimum results returned by coarse ADC conversions, before right-shifting.

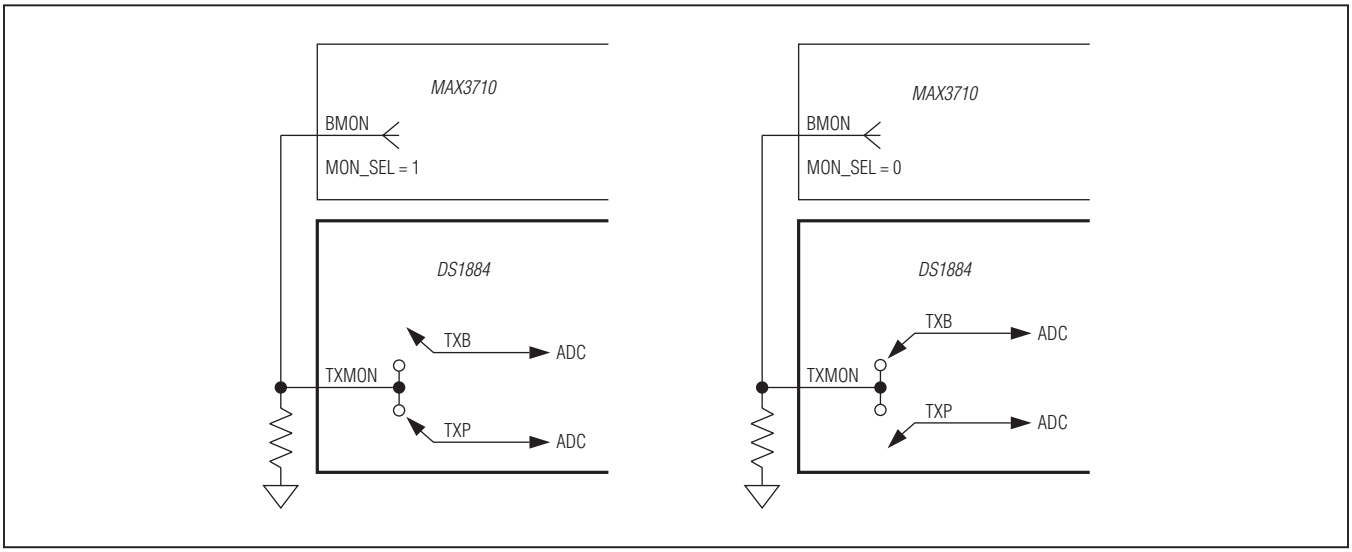


Figure 4. Laser Bias (TXB) and Laser Power (TXP) Monitoring Through TXMON

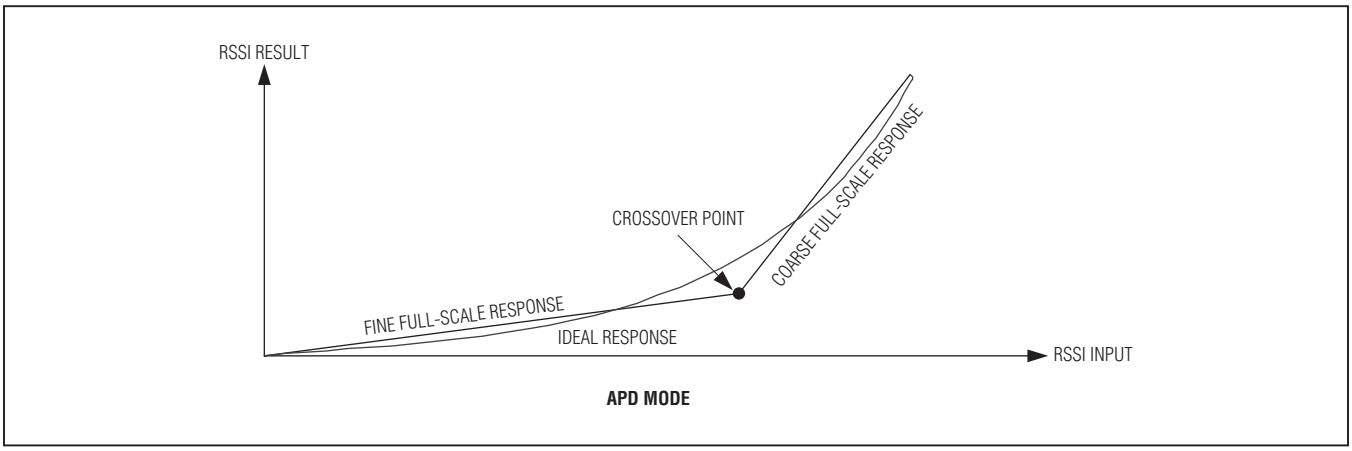


Figure 5. RSSI in APD Mode

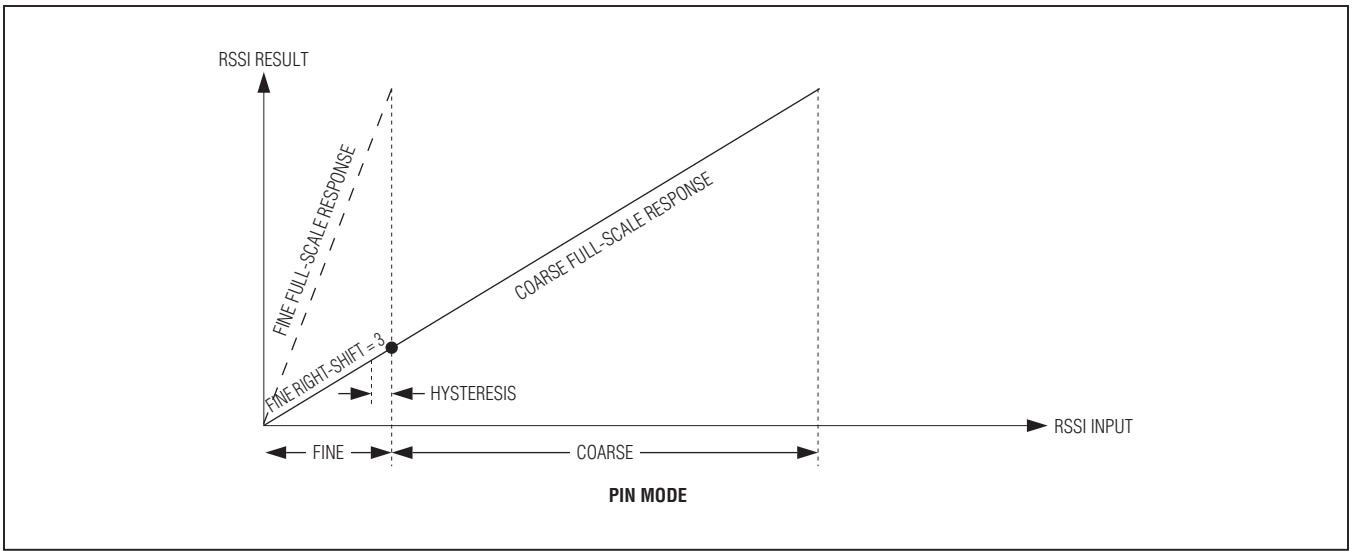


Figure 6. RSSI in PIN Mode

PIN Mode

The PIN mode is intended for systems with a linear relationship between the RSSI input and desired ADC result. The ADC result transitions between the fine and coarse ranges with hysteresis, as shown in Figure 6.

In PIN mode, the thresholds between coarse and fine mode are a function of the number of right-shifts being used. With the use of right-shifting, the fine mode full scale is programmed to ($1/2^{nth}$) of the coarse mode full scale. The DS1884 now auto ranges to choose the range that gives the best resolution for the measurement. Table 3 shows the threshold values for each possible number of right-shifts.

Low-Voltage Operation

The DS1884 contains two power-on reset (POR) levels. The lower level is a digital POR (POD) and the higher level is an analog POR (POA). At startup, before the supply voltage rises above POA, the outputs are disabled, all SRAM locations are set to their defaults, shadowed EEPROM locations are zero, and all analog circuitry is disabled. When V_{CC} reaches POA, the SEE is recalled, and the analog circuitry is enabled. While V_{CC} remains above POA, the device is in its normal operating state, and it responds based on its nonvolatile configuration. If during operation V_{CC} falls below POA, but is still above POD, the SRAM retains the SEE settings from the first SEE recall, but the device analog is shut down and the outputs are disabled. If the supply voltage recovers back above POA, the device immediately resumes normal operation. If the supply voltage falls below POD, the device SRAM is placed in its default state and another SEE recall is required to reload the nonvolatile settings. The EEPROM recall occurs the next time V_{CC} next exceeds POA. Figure 7 shows the sequence of events as the voltage varies.

Any time V_{CC} is above POD, the I^2C interface can be used to determine if V_{CC} is below the POA level. This is accomplished by checking the RDYB bit in the STATUS byte (A2h Lower Memory, Register 6Eh). RDYB is set when V_{CC} is below POA; when V_{CC} rises above POA, RDYB is timed (within 500µs) to go to 0, at which point the part is fully functional.

For all device addresses sourced from EEPROM (A2h Table 02h, Register 8Ch), the default DEVICE ADDRESS is A2h until V_{CC} exceeds POA, allowing the device address to be recalled from the EEPROM.

Power-On Analog (POA)

POA holds the DS1884 in reset until V_{CC} is at a suitable level (V_{CC} > POA) for the device to accurately measure with its ADC and compare analog signals with its quick-trip monitors. Because V_{CC} cannot be measured by the ADC when V_{CC} is less than POA, POA also asserts the VCC LO alarm, which is cleared by a V_{CC} ADC conversion greater than the customer-programmable V_{CC} low ADC limit. This allows a programmable limit to ensure that the head room requirements of the transceiver are satisfied during a slow power-up. The TXFOUT output does not latch until there is a conversion above the V_{CC} low limit. The POA alarm is nonmaskable. See the *Low-Voltage Operation* section for more information.

Table 3. RSSI Hysteresis Threshold Values

# OF RIGHT-SHIFTS	FINE MODE MAX (HEX)	COARSE MODE MIN* (HEX)
0	FFF8h	F000h
1	7FFCh	7800h
2	3FFEh	3C00h
3	1FFFh	1E00h
4	0FFFh	0F00h
5	07FFh	0780h
6	03FFh	03C0h
7	01FFh	01E0h

**This is the minimum reported coarse mode conversion.*

Table 4. RSSI Configuration Registers

REGISTER	FINE MODE	COARSE MODE
Gain Register (RSSI FINE/COARSE SCALE)	98h–99h, A2h Table 02h	9Ch–9Dh, A2h Table 02h
Offset Register (RSSI FINE/COARSE OFFEST)	A8h–A9h, A2h Table 02h	ACh–ADh, A2h Table 02h
RIGHT-SHIFT$_1$ Register	8Eh, A2h Table 02h	N/A
RSSIC and RSSIF Bits (RIGHT-SHIFT$_0$)	8Fh, A2h Table 02h	
RSSIR Bit (UPDATE)	6Fh, A2h Lower Memory	
RSSI Measurement (RSSI VALUE)	68h–69h, A2h Lower Memory	

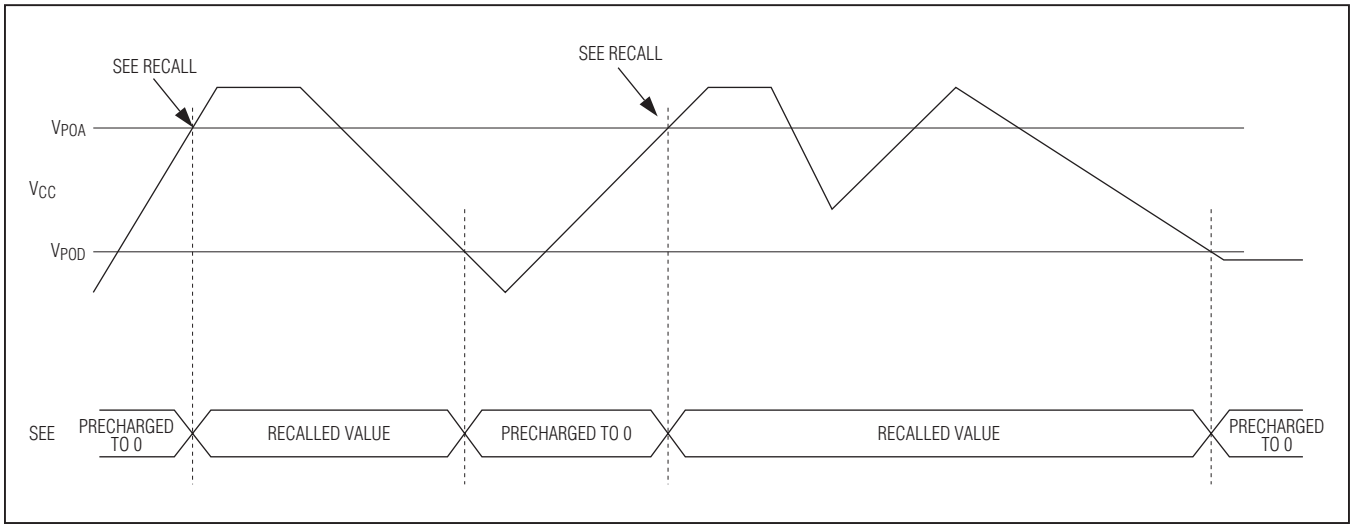


Figure 7. Low-Voltage Hysteresis Example

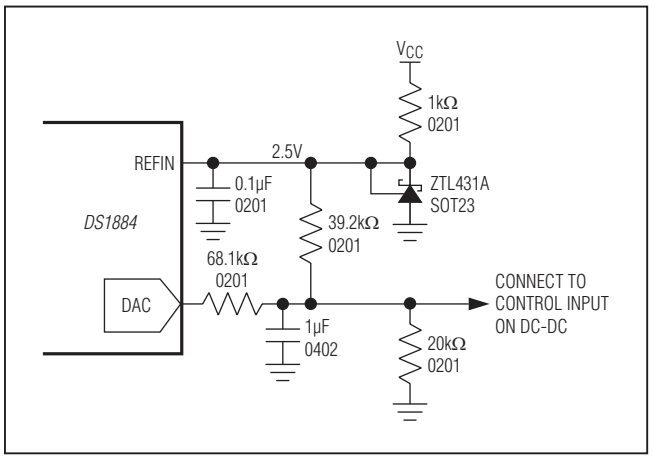


Figure 8. Recommended Shunt Reference and RC Filter for DAC Output

Delta-Sigma Output and Reference

One delta-sigma output (DAC) is provided. This provides a 9-bit resolution output. The maximum voltage output is set by the input REFIN. An inexpensive shunt reference is recommended to generate the voltage applied to REFIN, as shown in Figure 8. The output includes the ability to compensate the APD bias for temperature as given by the following formula:

DAC_INT = TINDEX[6:0] + DAC OFFSET

If INV_DAC = 0, then DAC[9:0] = DAC_INT/DACFS x V_{REFIN}.

If INV_DAC = 1, then DAC[9:0] = [3FF - (DAC_INT/DACFS)] x V_{REFIN}.

where:

1) INV_DAC is at A2h Table 02h, Register 8Dh, bit 7.
2) TINDEX is at A2h Table 02h, Register 81h.
3) DAC OFFSET is an 8-bit value, representing the 8 MSBs of a 10-bit value. The two LSBs are 0.
4) DACFS (A2h Table 02h, Register 88h) is an 8-bit value, representing the 8 MSBs of a 10-bit value. The two LSBs are 0.
5) DAC is a 10-bit value.
6) The DAC[9:0] is clamped at DACFS.
7) DAC_INT is an internal signal.

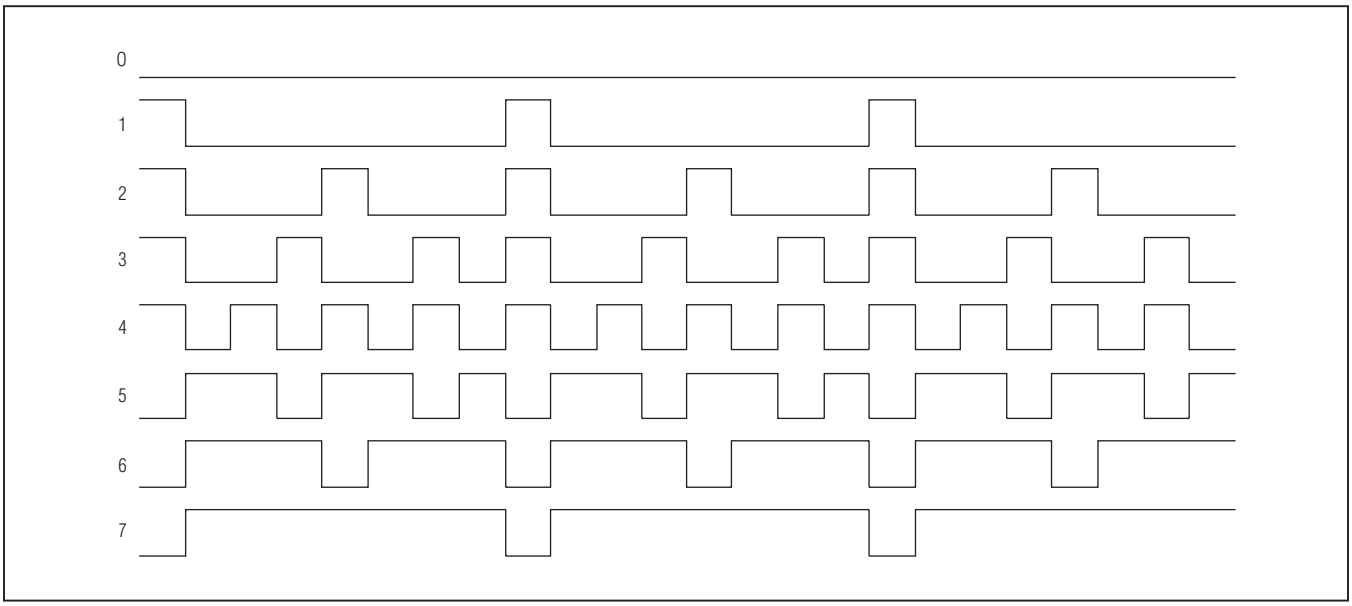


Figure 9. Delta-Sigma Output

The delta-sigma output uses pulse-density modulation. It provides much lower output ripple than a standard digital PWM output given the same clock rate and filter components. An RC filter is required on the DAC output as suggested in Figure 8. The external RC filter components are chosen based on ripple requirements, output load, delta sigma frequency, and desired response time. Before t_{INIT}, the DAC output is high impedance.

The reference input, REFIN, is the supply voltage for the DAC's output buffer. The voltage source connected to REFIN must be able to support the edge rate requirements of the delta sigma outputs. In a typical application, a 0.1uF capacitor should be connected between REFIN and ground.

The DS1884's delta-sigma output is 9 bits. For illustrative purposes, a 3-bit example is provided in Figure 9.