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## Thermochron <u>i</u>Button

### **General Description**

The DS1921G Thermochron® iButton® is a rugged, selfsufficient system that measures temperature and records the result in a protected memory section. The recording is done at a user-defined rate, both as a direct storage of temperature values as well as in the form of a histogram. Up to 2048 temperature values taken at equidistant intervals ranging from 1 to 255min can be stored. The histogram provides 63 data bins with a resolution of 2.0°C. If the temperature leaves a user-programmable range, the DS1921G also records when this happened, for how long the temperature staved outside the permitted range. and if the temperature was too high or too low. An additional 512 bytes of battery-backed SRAM allow storing information pertaining to the object to which the DS1921G is associated. Data is transferred serially through the 1-Wire® protocol, which requires only a single data lead and a ground return. Every DS1921G is factory lasered with a guaranteed unique, electrically readable, 64-bit registration number that allows for absolute traceability. The durable stainless steel package is highly resistant to environmental hazards such as dirt, moisture, and shock. Accessories permit the DS1921G to be mounted on almost any object including containers. pallets. and bags.

### **Applications**

Temperature Logging in Cold Chain, Food Safety, Pharmaceutical, and Medical Products

## \_MpbcpgleGldmpk\_rgml

PART	TEMP RANGE	PIN-PACKAGE
DS1921G-F5#	-40°C to +85°C	F5 <u>i</u> Button
DS1921G-F5N#	-40°C to +85°C	F5 <u>i</u> Button

#Denotes a RoHS-compliant device that may include lead(Pb) that is exempt under the RoHS requirements.

A NIST traceability certificate is available for the DS1921G-F5N. See Application Note 4629 for details.

### **Examples of Accessories**

PART	ACCESSORY				
DS9096P	Self-Stick Adhesive Pad				
DS9101	Multipurpose Clip				
DS9093RA	Mounting Lock Ring				
DS9093A	Snap-In Fob				
DS9092	<u>i</u> Button Probe				

#### Pin Configuration appears at end of data sheet.

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### **Features**

- ◆ Digital Thermometer Measures Temperature in 0.5°C Increments
- ◆ Accuracy ±1°C from -30°C to +70°C (See the Electrical Characteristics for Accuracy Specification)
- ♦ Built-In Real-Time Clock (RTC) and Timer Has Accuracy of ±2 Minutes per Month from 0°C to +45°C
- Water Resistant or Waterproof if Placed Inside DS9107 iButton Capsule (Exceeds Water Resistant 3 ATM Requirements)
- Automatically Wakes Up and Measures Temperature at User-Programmable Intervals from 1 Minute to 255 Minutes
- ◆ Logs Consecutive Temperature Measurements in 2KB of Data-Log Memory
- ♦ Records a Long-Term Temperature Histogram with 2.0°C Resolution
- ♦ Programmable Temperature High and Temperature Low Alarm Trip Points
- ♦ Records Up to 24 Timestamps and Durations When Temperature Leaves the Range Specified by the Trip Points
- ♦ 512 Bytes of General-Purpose Battery-Backed SRAM
- ♦ Communicates to Host with a Single Digital Signal at 15.4kbps or 125kbps Using 1-Wire Protocol

### **Common iButton Features**

- Digital Identification and Information by Momentary Contact
- ♦ Unique, Factory-Lasered, and Tested 64-Bit Registration Number (8-Bit Family Code + 48-Bit Serial Number + 8-Bit CRC Tester) Assures Absolute Traceability Because No Two Parts are Alike
- ♦ Multidrop Controller for 1-Wire Net
- ♦ Chip-Based Data Carrier Compactly Stores Information
- ♦ Data Can Be Accessed While Affixed to Object
- Button Shape is Self-Aligning with Cup-Shaped Probes
- ♦ Durable Stainless-Steel Case Engraved with Registration Number Withstands Harsh Environments
- Easily Affixed with Self-Stick Adhesive Backing, Latched by Its Flange, or Locked with a Ring Pressed Onto Its Rim
- Presence Detector Acknowledges When Reader First Applies Voltage
- Meets UL 913, 5th Ed., Rev. 1997-02-24; Intrinsically Safe Apparatus: Approved Under Entity Concept for Use in Class I, Division 1, Group A, B, C, and D Locations

For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim's website at www.maximintegrated.com.

# Thermochron iButton

### **ABSOLUTE MAXIMUM RATINGS**

IO Voltage Range Relative to GND0.5V to +6V	Operating Temperature Range40°C to +85°C*
IO Sink Current20mA	Storage Temperature Range40°C to +50°C*

<sup>\*</sup>Storage or operation above +50°C significantly reduces battery life.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

### **ELECTRICAL CHARACTERISTICS**

 $(V_{PUP} = +2.8V \text{ to } +5.25V, T_A = -40^{\circ}\text{C to } +85^{\circ}\text{C.})$ 

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS		
IO PIN: GENERAL DATA			•			•		
1-Wire Pullup Resistance	Rpup	(Notes 1, 2)			2.2	kΩ		
Input Capacitance	CIO	(Notes 3, 4)		100	800	pF		
Input Load Current	ΙL	IO pin at V <sub>PUP</sub> (Note 5)			10	μΑ		
High-to-Low Switching Threshold	VTL	V <sub>PUP</sub> > 4.5V	1.14		2.70	V		
(Notes 4, 6, 7, 8)	V I L		0.71		2.70	V		
Input Low Voltage	VIL	(Notes 1, 6, 9)			0.30	V		
Low-to-High Switching Threshold	VTH	V <sub>PUP</sub> > 4.5V	1.00		2.70	V		
(Notes 4, 6, 7, 10)	VIH		0.66		2.70	\ \ \		
Output Low Voltage at 4mA	V <sub>OL</sub>	(Notes 6, 11)			0.4	V		
		Standard speed, $R_{PUP} = 2.2k\Omega$	5					
Recovery Time (Notes 1, 4)	tREC	Overdrive speed, R <sub>PUP</sub> = $2.2k\Omega$	2			– μs		
		Overdrive speed, directly prior to reset pulse; $R_{PUP} = 2.2k\Omega$	5					
Time Clet Demotion (Nets - 1, 10)	4	Standard speed	65					
Time-Slot Duration (Notes 1, 12)	tslot	Overdrive speed	8		μs			
IO PIN: 1-Wire RESET, PRESEN	CE-DETECT	CYCLE						
		Standard speed, V <sub>PUP</sub> > 4.5V	480	480				
Depart Law Times (Nates 1 10)	+	Standard speed	540	640		]		
Reset Low Time (Notes 1,12)	trstl	Overdrive speed, V <sub>PUP</sub> > 4.5V	48		80	μs		
		Overdrive speed	58		80			
Presence-Detect High	topu	Standard speed	15		60	0		
Time (Note 12)	tPDH	Overdrive speed	1.1		6	μs		
		Standard speed	60		270			
Presence-Detect Low Time (Note 12)	tpDL	Overdrive speed, V <sub>PUP</sub> > 4.5V	<b>7.5</b> 24		μs			
11110 (14010-12)		Overdrive speed	7.5		32	]		
Presence-Detect	tmsp	Standard speed	60		75	116		
Sample Time (Notes 1, 4)	44125	Overdrive speed	6		8.6	μs		

### **ELECTRICAL CHARACTERISTICS (continued)**

 $(V_{PUP} = +2.8V \text{ to } +5.25V, T_A = -40^{\circ}\text{C to } +85^{\circ}\text{C.})$ 

PARAMETER	SYMBOL	CONDITIONS	MIN TY	P MAX	UNITS	
IO PIN: 1-Wire WRITE	<b>'</b>		- '			
		Standard speed		120		
Write-Zero Low Time (Notes 1, 12, 13)	twoL	Overdrive speed, V <sub>PUP</sub> > 4.5V	6	15	μs	
(Notes 1, 12, 13)		Overdrive speed	8.5	15		
Write-One Low Time	<b>*</b>	Standard speed	5	15		
(Notes 1, 13)	t <sub>W1</sub> L	Overdrive speed	1	2	μs	
IO PIN: 1-Wire READ	•					
Daniel and Time (Nichaeld 14)		Standard speed	5	15 - δ		
Read Low Time (Notes 1, 14)	t <sub>RL</sub>	Overdrive speed	1	2 - δ	μs	
Read Sample Time		Standard speed	t <sub>RL</sub> + δ	15		
(Notes 1, 14)	tmsr	Overdrive speed	t <sub>RL</sub> + δ	2	μs	
REAL-TIME CLOCK	•					
Frequency Deviation	ΔF	-5°C to +46°C	-48	+46	ppm	
TEMPERATURE CONVERTER	•					
Tempcore Operating Range	T <sub>TC</sub>		-40	+85	°C	
Conversion Time	tconv		19	90	ms	
Thermal Response Time Constant	τRESP	(Note 15)	13	0	S	
		-40°C to < -30°C	-1.3	+1.3		
Conversion Error (Notes 16, 17)	$\Delta \vartheta$	-30°C to +70°C	-1.0	+1.0	°C	
(110163 10, 17)		> +70°C to +85°C	-1.3	+1.3		
Number of Conversions	Nconv	(Notes 4, 18) (See the lifetime graphs.)				

- Note 1: System requirement.
- **Note 2:** Maximum allowable pullup resistance is a function of the number of 1-Wire devices in the system and 1-Wire recovery times. The specified value here applies to systems with only one device and with the minimum 1-Wire recovery times. For more heavily loaded systems, an active pullup such as that found in the DS2480B may be required.
- **Note 3:** Capacitance on IO could be 800pF when power is first applied. If a 2.2kΩ resistor is used to pull up the data line, 2.5μs after V<sub>PUP</sub> has been applied, the parasite capacitor does not affect normal communication.
- Note 4: These values are derived from simulation across process, voltage, and temperature and are not production tested.
- **Note 5:** Input load is to ground.
- Note 6: All voltages are referenced to ground.
- **Note 7:** V<sub>TL</sub> and V<sub>TH</sub> are functions of the internal supply voltage, which is a function of V<sub>PUP</sub> and the 1-Wire recovery times. The V<sub>TH</sub> and V<sub>TL</sub> maximum specifications are valid at V<sub>PUP</sub> = 5.25V. In any case, V<sub>TL</sub> < V<sub>TH</sub> < V<sub>PUP</sub>.
- Note 8: Voltage below which, during a falling edge of IO, a logic 0 is detected.
- Note 9: The voltage on IO must be less than or equal to V<sub>ILMAX</sub> whenever the master drives the line low.
- Note 10: Voltage above which, during a rising edge on IO, a logic 1 is detected.
- Note 11: The I-V characteristic is linear for voltages less than 1V.
- Note 12: Numbers in **bold** are **not** in compliance with the published <u>i</u>Button standards. See the *Comparison Table*.
- **Note 13:**  $\epsilon$  in Figure 15 represents the time required for the pullup circuitry to pull the voltage on the IO pin up from V<sub>IL</sub> to V<sub>TH</sub>. The actual maximum duration for the master to pull the line low is  $tw_{1LMAX} + tF \epsilon$  and  $tw_{0LMAX} + tF \epsilon$ , respectively.
- **Note 14:**  $\delta$  in Figure 15 represents the time required for the pullup circuitry to pull the voltage on the IO pin up from  $V_{IL}$  to the input high threshold of the bus master. The actual maximum duration for the master to pull the line low is  $t_{RLMAX} + t_{F}$ .
- Note 15: This number was derived from a test conducted by Cemagref in Antony, France, in July 2000. http://www.cemagref.fr/English/index.htm Test Report No. E42
- Note 16: Total accuracy is  $\Delta\vartheta$  plus 0.25°C quantization due to the 0.5°C digital resolution of the device.

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### **ELECTRICAL CHARACTERISTICS (continued)**

 $(V_{PUP} = +2.8V \text{ to } +5.25V, T_A = -40^{\circ}\text{C to } +85^{\circ}\text{C.})$ 

Note 17: WARNING: Not for use as the sole method of measuring or tracking temperature in products and articles that could affect the health or safety of persons, plants, animals, or other living organisms, including but not limited to foods, beverages, pharmaceuticals, medications, blood and blood products, organs, flammable, and combustible products. User shall assure that redundant (or other primary) methods of testing and determining the handling methods, quality, and fitness of the articles and products should be implemented. Temperature tracking with this product, where the health or safety of the aforementioned persons or things could be adversely affected, is only recommended when supplemental or redundant information sources are used. Data-logger products are 100% tested and calibrated at time of manufacture by Maxim to ensure that they meet all data sheet parameters, including temperature accuracy. User shall be responsible for proper use and storage of this product. As with any sensor-based product, user shall also be responsible for occasionally rechecking the temperature accuracy of the product to ensure it is still operating properly.

**Note 18:** The number of temperature conversions (= samples) possible with the built-in energy source depends on the operating and storage temperature of the device. When not in use for a mission, the RTC oscillator should be turned off and the device should be stored at a temperature not exceeding +25°C. Under this condition the shelf life time is 10 years minimum.

#### **COMPARISON TABLE**

		LEGACY	VALUES		DS1921G VALUES				
PARAMETER	STANDARD	SPEED (µs)	OVERDRIVE	SPEED (µs)	STANDARD	SPEED (µs)	OVERDRIVE SPEED (µs		
	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t <sub>SLOT</sub> (including t <sub>REC</sub> )	61	(undefined)	7	(undefined)	65*	(undefined)	8*	(undefined)	
trstl	480	(undefined)	48	80	540	640	58	80	
tpDH	15	60	2	6	15	60	1.1	6	
tpDL	60	240	8	24	60	270	7.5	32	
t <sub>WOL</sub>	60	120	6	16	60	120	8.5	15	

<sup>\*</sup>Intentional change; longer recovery time between time slots.

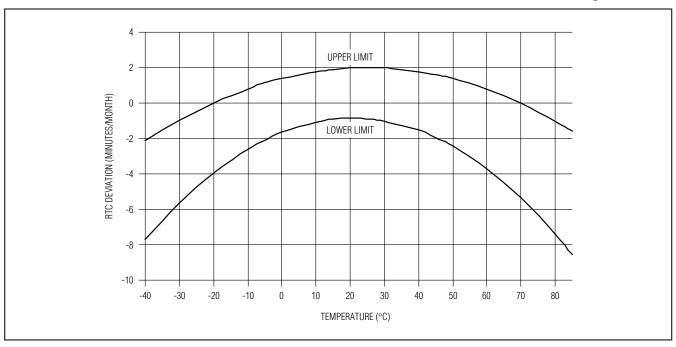
Note: Numbers in bold are not in compliance with the published iButton standards.

#### iButton CAN PHYSICAL SPECIFICATION

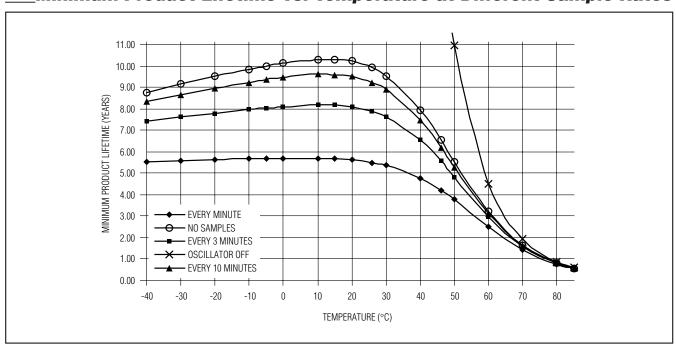
SIZE	See the Package Information section.						
WEIGHT	Ca. 3.3g						
SAFETY	Meets UL 913, 5th Ed., Rev. 1997-02-24; Intrinsically Safe Apparatus, approval under Entity Concept for use in Class I, Division 1, Group A, B, C, and D Locations.						

# Thermochron iButton

### RTC Deviation vs. Temperature

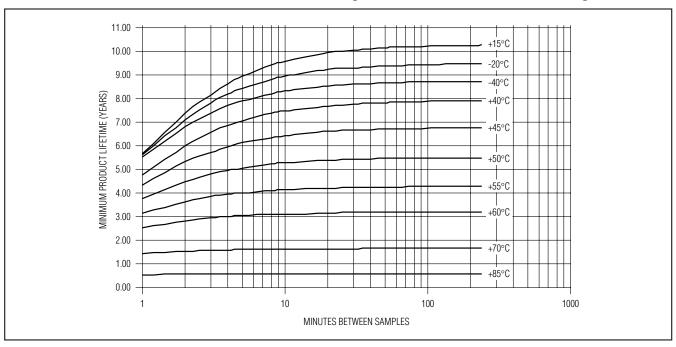


### Minimum Product Lifetime vs. Temperature at Different Sample Rates

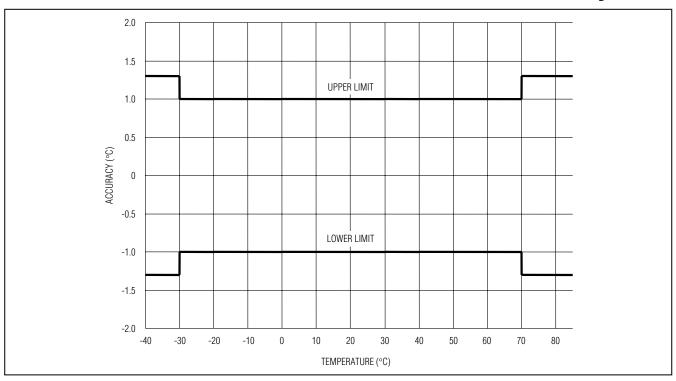


# Thermochron <u>i</u>Button

### Minimum Product Lifetime vs. Sample Rate at Different Temperatures



### **Accuracy Limits**



### **Detailed Description**

The DS1921G Thermochron iButton is an ideal device to monitor the temperature of any object it is attached to or shipped with, such as perishable goods or containers of temperature-sensitive chemicals. The general-purpose battery-backed SRAM can store an electronic copy of shipping information, date of manufacture and other important data written as clear as well as encrypted files. Note that the initial sealing level of the DS1921G achieves IP56. Aging and use conditions can degrade the integrity of the seal over time, therefore, for applications with significant exposure to liquids, sprays, or other similar environments, it is recommended to place the Thermochron in the DS9107

<u>iButton</u> capsule. The DS9107 provides a watertight enclosure that has been rated to IP68 (refer to Application Note 4126: *Understanding the IP (Ingress Protection) Ratings of <u>iButton Data Loggers and Capsule)</u>.* 

#### **Overview**

Figure 1 shows the relationships between the major control and memory sections of the DS1921G. The device has seven main data components: 64-bit lasered ROM; 256-bit scratchpad; 4096-bit general-purpose SRAM; 256-bit register page of timekeeping, control, and counter registers; 96 bytes of alarm timestamp and duration logging memory; 126 bytes of

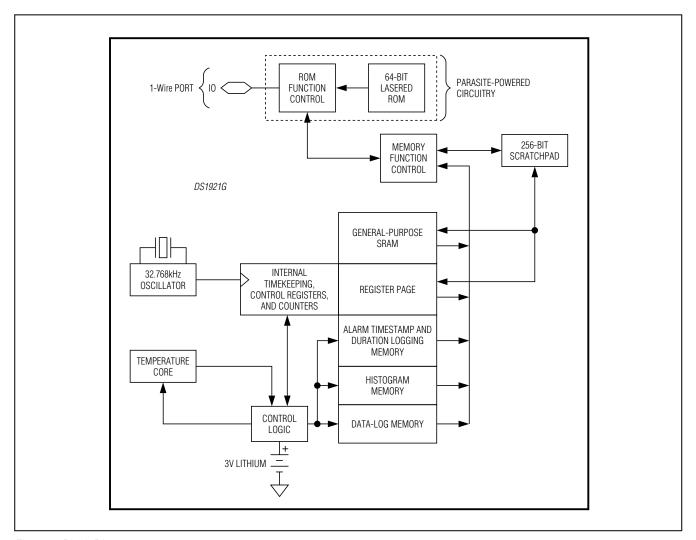


Figure 1. Block Diagram

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histogram memory; and 2048 bytes of data-log memory. Except for the ROM and the scratchpad, all other memory is arranged in a single linear address space. All memory reserved for logging purposes, including counter registers and several other registers, is readonly for the user. The timekeeping and control registers are write protected while the device is programmed for a mission.

The hierarchical structure of the 1-Wire protocol is shown in Figure 2. The bus master must first provide one of the seven ROM function commands: Read ROM, Match ROM, Search ROM, Conditional Search ROM, Skip ROM, Overdrive-Skip ROM, or Overdrive-Match ROM. Upon completion of an Overdrive ROM command byte executed at standard speed, the device enters overdrive mode, where all subsequent communication occurs at a higher speed. The protocol required for these ROM function commands is described in Figure 13. After a ROM function command is successfully executed, the memory functions become accessi-

ble and the master can provide any one of the seven available commands. The protocol for these memory function commands is described in Figure 10. All data is read and written least significant bit first.

#### **Parasite Power**

Figure 1 shows the parasite-powered circuitry. This circuitry "steals" power whenever the IO input is high. IO provides sufficient power as long as the specified timing and voltage requirements are met. The advantages of parasite power are two-fold: 1) By parasiting off this input, battery power is not consumed for 1-Wire ROM function commands, and 2) if the battery is exhausted for any reason, the ROM may still be read normally. The remaining circuitry of the DS1921G is solely operated by battery energy. As a consequence, if the battery is exhausted, all memory data is lost including the data of the last mission, and no new mission can be started. Refer to Application Note 5057: *OneWireViewer Tips and Tricks* for how to check the battery status.

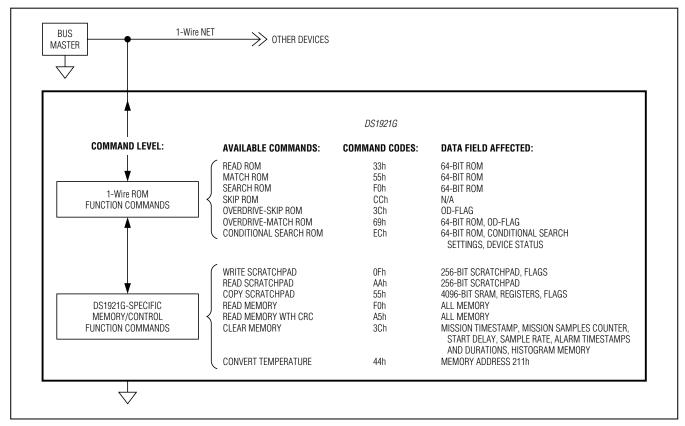


Figure 2. Hierarchical Structure for 1-Wire Protocol

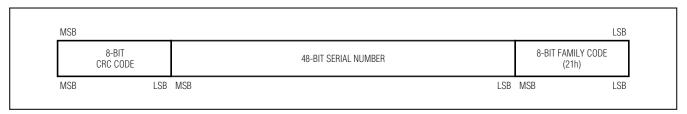


Figure 3. 64-Bit Lasered ROM

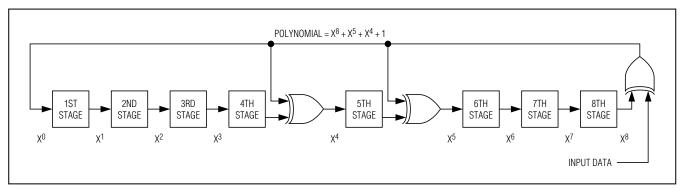


Figure 4. 1-Wire CRC Generator

#### 64-Bit Lasered ROM

Each DS1921G contains a unique ROM code that is 64 bits long. The first 8 bits are a 1-Wire family code. The next 48 bits are a unique serial number. The last 8 bits are a cyclic redundancy check (CRC) of the first 56 bits (see Figure 3 for details). The 1-Wire CRC is generated using a polynomial generator consisting of a shift register and XOR gates as shown in Figure 4. The polynomial is  $X^8 + X^5 + X^4 + 1$ . Additional information about the 1-Wire CRC is available in Application Note 27: Understanding and Using Cyclic Redundancy Checks with Maxim <u>i</u>Button Products.

The Shift register bits are initialized to 0. Then, starting with the least significant bit of the family code, one bit at a time is shifted in. After the 8th bit of the family code has been entered, the serial number is then entered. After the 48th bit of the serial number has been entered, the Shift register contains the CRC value.

Shifting in the 8 bits of CRC returns the Shift register to all zeros.

### Memory

Figure 5 shows the DS1921G memory map. The 4096-bit general-purpose SRAM makes up pages 0 to 15. The timekeeping, control, and counter registers fill page 16, called register page (see Figure 6). Pages 17, 18, and 19 are assigned to storing the alarm timestamps and durations. The temperature histogram bins begin at page 64 and use up to four pages. The data-log memory covers pages 128 to 191. Memory pages 20 to 63, 68 to 127, and 192 to 255 are reserved for future extensions. The scratchpad is an additional page that acts as a buffer when writing to the SRAM or the register page. The memory pages 17 and higher are read only for the user. They are written to or erased solely under the supervision of the on-chip control logic.

# Thermochron <u>i</u>Button

	32-BYTE INTERMEDIATE STORAGE SCRATCHPAD	
ADDRESS		
0000h to 01FFh	GENERAL-PURPOSE SRAM (16 PAGES)	PAGES 0 to 15
0200h to 021Fh	32-BYTE REGISTER PAGE	PAGE 16
0220h to 027Fh	ALARM TIMESTAMPS AND DURATIONS	PAGES 17 to 19
0280h to 07FFh	(RESERVED FOR FUTURE EXTENSIONS)	PAGES 20 to 63
0800h to 087Fh	TEMPERATURE HISTOGRAM MEMORY	PAGES 64 to 67
0880h to 0FFFh	(RESERVED FOR FUTURE EXTENSIONS)	PAGES 68 to 127
1000h to 17FFh	DATA-LOG MEMORY (64 PAGES)	PAGES128 to 191
1800h to 1FFFh	(RESERVED FOR FUTURE EXTENSIONS)	PAGES 192 to 255

Figure 5. Memory Map

ADDRESS	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3 BIT 2 BIT 1 BIT 0				FUNCTION	ACC	ESS*	
0200h	0	10 Seconds				Single S	Seconds					
0201h	0	10 Minutes				Single I	Minutes		]			
0202h	0	12/24	20 Hour AM/PM	10 Hour		Single Hours			DTO			
0203h	0	0	0	0	0	D	ay of Wee	k	RTC Registers	R/W	R/W**	
0204h	0	0	10 [	Date		Single	e Date		riegisters			
0205h	CENT	0	0	10 Months		Single Months						
0206h		10 Years			10 Years Single Years					]		
0207h	MS	10 Seconds Alarm			5	Single Sec	onds Alarr	n				
0208h	MM	10 Minutes Alarm				Single Min	utes Alarr	n				
0209h	МН	12/24	20 Hour AM/PM Alarm	10 Hour Alarm		Single Ho	urs Alarm		RTC Alarm Registers	R/W	R/W**	
020Ah	MD	0	0	0	0	Day	of Week A	larm	]			
020Bh			Tempe	rature Low	Alarm Th	reshold			Temperature	DAM	R/W**	
020Ch		Temperature High Alarm Threshold							Alarms	R/W	H/VV	
020Dh		Numbe	r of Minute	s Betwee	n Tempera	ature Conv	ersions	Sample Rate	R/W	R**		
020Eh	EOSC	EMCLR	0	ĒM	RO	TLS	THS	TAS	Control	R/W	R/W**	
020Fh			7)	lo function	, reads 00	)h)			_	R	R**	

<sup>\*</sup>The left entry in the ACCESS column is valid between missions. The right entry shows the applicable access mode while a mission is in progress.

Figure 6. Register Pages Map

<sup>\*\*</sup>While a mission is in progress, these addresses can be read. The first attempt to write to these registers (even read-only ones), however, ends the mission and overwrites selected writable registers.

## Thermochron <u>i</u>Button

ADDRESS	BIT 7	BIT 6	BIT 0	FUNCTION	ACC	ESS*					
0210h				_	R	R**					
0211h		Τe	emperatur	e Read-Ou	ıt (Forced (	Conversio	n)		Temperature	R	R**
0212h				Low	Byte				Mission Start	R/W	R/W**
0213h				High	Byte				Delay	□/VV	H/VV
0214h	TCB	MEMCLR	MIP	SIP	0	TLF	THF	TAF	Status	R/W	R/W
0215h				Min	utes						
0216h				Но	urs				1		
0217h				Da	ate				Mission Timestamp	R	R
0218h				Мо	nth				- Timestamp		
0219h				Υe	ear						
021Ah				Low	Byte				Mission		
021Bh				Cente	r Byte				Samples	R	R
021Ch				High	Byte				Counter		
021Dh		Low Byte									
021Eh		Center Byte								R	R
021Fh				High	Byte				Counter		

<sup>\*</sup>The left entry in the ACCESS column is valid between missions. The right entry shows the applicable access mode while a mission is in progress.

Figure 6. Register Pages Map (continued)

### **Detailed Register Descriptions**

#### **Timekeeping**

The RTC/alarm and calendar information is accessed by reading/writing the appropriate bytes in the register page, address 0200h to 0206h. Note that some bits are set to 0. These bits always read 0 regardless of how they are written. The contents of the time, calendar, and alarm registers are in the binary-coded decimal (BCD) format.

#### RTC/Calendar

The RTC of the DS1921G can run in either 12hr or 24hr mode. Bit 6 of the Hours register (address 0202h) is defined as the 12hr or 24hr mode select bit. When high, the 12hr mode is selected. In the 12hr mode, bit 5 is the AM/PM bit with logic 1 being PM. In the 24hr mode, bit 5 is the 20hr bit (20hr to 23hr).

To distinguish between the days of the week, the DS1921G includes a counter with a range from 1 to 7. The assignment of a counter value to the day of week is arbitrary. Typically, the number 1 is assigned to a Sunday (U.S. standard) or to a Monday (European standard).

The calendar logic is designed to automatically compensate for leap years. For every year value that is either 00 or a multiple of four, the device adds a 29th of February. This works correctly up to (but not including) the year 2100.

The DS1921G is Y2K compliant. Bit 7 (CENT) of the Months register at address 0205h serves as a century flag. When the Year register rolls over from 99 to 00, the century flag toggles. It is recommended to write the century bit to a 1 when setting the RTC to a time/date between the years 2000 and 2099.

<sup>\*\*</sup>While a mission is in progress, these addresses can be read. The first attempt to write to these registers (even read-only ones), however, ends the mission and overwrites selected writable registers.

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### **RTC and RTC Alarm Registers Map**

ADDRESS	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
0200h	0		10 Seconds			Single	Seconds	
0201h	0		10 Minutes			Single	Minutes	
0202h	0	12/24	12/24 20 Hour AM/PM 10 Hour			Single	Hours	
0203h	0	0	0	0	0 Day of Week			
0204h	0	0	10 [	Date		Singl	e Date	
0205h	CENT	0	0	10 Months		Single	Months	
0206h		10 Y	'ears			Single	e Years	
0207h	MS	10	) Seconds Alar	m		Single Sec	onds Alarm	
0208h	MM	1	0 Minutes Alar	m		Single Mir	nutes Alarm	
0209h	МН	12/24	20 Hour AM/PM Alarm	10 Hour Alarm	Single Hours Alarm			
020Ah	MD	0	0	0	0	D	ay of Week Aları	m

#### **RTC Alarm Control**

A	LARM REGIST (BIT 7 OF 020	_	_	FUNCTION
MS	ММ	МН	MD	
1	1	1	1	Alarm once per second.
0	1	1	1	Alarm when seconds match (once per minute).
0	0	1	1	Alarm when minutes and seconds match (once every hour).
0	0	0	1	Alarm when hours, minutes, and seconds match (once every day).
0	0	0	0	Alarm when day, hours, minutes, and seconds match (once every week).

#### **RTC Alarms**

The DS1921G also contains an RTC alarm function. The RTC Alarm registers are located in registers 0207h to 020Ah. The most significant bit of each of the alarm registers is a mask bit. When all the mask bits are logic 0, an alarm occurs once per week when the values stored in timekeeping registers 0200h to 0203h match

the values stored in the RTC Alarm registers. Any alarm sets the timer alarm flag (TAF) in the device's Status register (address 214h). The bus master can set the search conditions in the Control register (address 20Eh) to identify devices with timer alarms by means of the conditional search function (see the *ROM Function Commands* section).

### **Temperature Alarm Register Map**

ADDRESS	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
020Bh			Te	mperature Low	Alarm Thresho	old		
020Ch			Ter	mperature High	Alarm Thresh	old		

### Sample Rate Register Map

ADDRRESS	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
020Dh				Sampl	e Rate			

### **Temperature Conversion**

The DS1921G measures temperatures with a resolution of 0.5°C. Temperature values are represented in a single byte as an unsigned binary number, which translates into a theoretical range of 128°C. The range, however, has been limited to values from 0000 0000 (00h) through 1111 1010 (FAh). The codes 01h to F9h are considered valid temperature readings.

If a temperature conversion yields a temperature that is out of range, it is recorded as 00h (if too low) or FAh (if too high). Since out-of-range results are accumulated in histogram bins 0 and 62 (see the *Temperature Logging and Histogram* section), the data in these bins is of limited value. For this reason the specified temperature range of the DS1921G is considered to begin at code 04h and end at code F7h, which corresponds to histogram bins 1 to 61.

With T[7...0] representing the decimal equivalent of a temperature reading, the temperature value is calculated as

$$\vartheta(^{\circ}C) = T[7...0]/2 - 40.0$$

This equation is valid for converting temperature readings stored in the data-log memory as well as for data read from the Forced Temperature Conversion Readout register (address 0211h).

To specify the temperature alarm thresholds, this equation needs to be resolved to

$$T[7...0] = 2 \times \vartheta(^{\circ}C) + 80.0$$

A value of 23°C, for example, thus translates into 126 decimal or 7Eh. This corresponds to the binary patterns 0111 1110, which could be written to a Temperature Alarm register (address 020Bh and 020Ch, respectively).

### **Sample Rate**

The content of the Sample Rate register (address 020Dh) determines how many minutes the temperature conversions are apart from each other during a mission. The sample rate can be any value from 1 to 255, coded as an unsigned 8-bit binary number. If the memory has been cleared (Status register bit MEMCLR = 1) and a mission is enabled (Control register bit  $\overline{\rm EM}$  = 0), writing a nonzero value to the Sample Rate register starts a mission. For a full description of the correct sequence of steps to start a temperature-logging mission, see the Missioning or Mission Example: Prepare and Start a New Mission sections.

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### **Control Register Map**

ADDRESS	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
020Eh	EOSC	EMCLR	0	ĒM	RO	TLS	THS	TAS

#### **Control Register**

The DS1921G is set up for its operation by writing appropriate data to its special function registers that are located in the register page. Several functions that are controlled by a single bit only are combined into a single byte called the Control register (address 020Eh). This register can be read and written. If the device is programmed for a mission, writing to the Control register ends the mission and changes the register contents.

The functional assignments of the individual bits are explained below. Bit 5 has no function. It always reads 0 and cannot be written to 1.

Bit 7: Enable Oscillator (EOSC). This bit controls the crystal oscillator of the RTC. When set to logic 0, the oscillator starts operation. When written to logic 1, the oscillator stops and the device is in a low-power data-retention mode. This bit must be 0 for normal operation. The RTC must have advanced at least 1 second before a Mission Start is accepted.

Bit 6: Memory Clear Enable (EMCLR). This bit needs to be set to logic 1 to enable the Clear Memory function, which is invoked as a memory function command. The timestamp, histogram memory as well as the Mission Timestamp, Mission Samples Counter, Mission Start Delay, and Sample Rate are cleared only if the Clear Memory command is issued with the next access to the device. The EMCLR bit returns to 0 as the next memory function command is executed.

**Bit 4: Enable Mission (EM).** This bit controls whether the DS1921G begins a mission as soon as the sample rate is written. To enable the device for a mission, this bit must be 0.

**Bit 3: Rollover Enable/Disable (RO).** This bit controls whether the data-log memory is overwritten with new data or whether data logging is stopped once the memory is filled with data during a mission. Setting this bit to a 1 enables the rollover and data logging continues at the beginning, overwriting previously collected data. Clearing this bit to 0 disables the rollover and no further

temperature values are stored in the data-log memory once it is filled with data. This does not stop the mission. The device continues measuring temperatures and updating the histogram and alarm timestamps and durations.

**Bit 2: Temperature Low Alarm Search (TLS).** If this bit is 1, the device responds to a Conditional Search ROM command if, during a mission, the temperature has reached or is lower than the Low Temperature Threshold stored at address 020Bh.

**Bit 1: Temperature High Alarm Search (THS).** If this bit is 1, the device responds to a Conditional Search ROM command if, during a mission, the temperature has reached or is higher than the High Temperature Threshold stored at address 020Ch.

**Bit 0: Timer Alarm Search (TAS).** If this bit is 1, the device responds to a Conditional Search ROM command if, during a mission, a timer alarm has occurred. Since a timer alarm cannot be disabled, the TAF flag usually reads 1 during a mission. Therefore, it is advisable to set the TAS bit to a 0, in most cases.

### **Mission Start Delay Counter**

The content of the Mission Start Delay Counter register determines how many minutes the device waits before starting the logging process. The Mission Start Delay value is stored as an unsigned 16-bit integer number at addresses 0212h (low byte) and 0213h (high byte). The maximum delay is 65,535 minutes, equivalent to 45 days, 12 hours, and 15 minutes.

For a typical mission, the Mission Start Delay is 0. If a mission is too long for a single DS1921G to store all temperature readings at the selected sample rate, one can use several devices, staggering the Mission Start Delay to record the full period. In this case, the rollover enable (RO) bit in the Control register (address 020Eh) must be set to 0 to prevent overwriting of the recorded temperature log after the data-log memory is full. See the *Mission Start and Logging Process* section and Figure 11 for details.

### Status Register Map

ADDRESS	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
0214h	TCB	MEMCLR	MIP	SIP	0	TLF	THF	TAF

#### **Status Register**

The Status register holds device status information and alarm flags. The register is located at address 0214h. Writing to this register does not necessarily end a mission.

The functional assignments of the individual bits are explained below. The bits MIP, TLF, THF, and TAF can only be written to 0. All other bits are read-only. Bit 3 has no function.

**Bit 7: Temperature Core Busy (TCB).** If this bit reads 0, the DS1921G is currently performing a temperature conversion. This temperature conversion is either self-initiated because of a mission being in progress or initiated by a command when a mission is not in progress. The TCB bit goes low just before a conversion starts and returns to high just after the result is latched into the Read-Out register at address 0211h.

**Bit 6: Memory Cleared (MEMCLR).** If this bit reads 1, the memory pages 17 and higher (alarm timestamps/durations, temperature histogram, excluding data-log memory), as well as the Mission Timestamp, Mission Samples Counter, Mission Start Delay, and Sample Rate have been cleared to 0 from executing a Clear Memory function command. The MEMCLR bit returns to 0 as soon as writing a nonzero value to the Sample Rate register starts a new mission, provided that the EM bit is also 0. **The memory has to be cleared in order for a mission to start.** 

Bit 5: Mission in Progress (MIP). If this bit reads 1, the DS1921G has been set up for a mission and this mission is still in progress. A mission is started if the EM bit of the Control register (address 20Eh) is 0 and a nonzero value is written to the Sample Rate register, address 20Dh. The MIP bit returns from logic 1 to logic 0 when a mission is ended. A mission ends with the first write attempt (Copy Scratchpad command) to any register in

the address range of 200h to 213h. Alternatively, a mission can be ended by directly writing to the Status register and setting the MIP bit to 0. The MIP bit cannot be set to 1 by writing to the Status register.

BIT 4: Sample in Progress (SIP). If this bit reads 1, the DS1921G is currently performing a temperature conversion as part of a mission in progress. The mission samples occur on the seconds rollover from 59 to 00. The SIP bit changes from 0 to 1 approximately 250ms before the actual temperature conversion begins allowing the circuitry of the chip to wake up. A temperature conversion including a wake-up phase takes maximum 875ms. During this time, read accesses to the memory pages 17 and higher are permissible but can reveal invalid data.

**Bit 2: Temperature Low Flag (TLF).** Logic 1 in the temperature low flag bit indicates that a temperature measurement during a mission revealed a temperature equal to or lower than the value in the Temperature Low Threshold register. The temperature low flag can be cleared at any time by writing this bit to 0. This flag must be cleared before starting a new mission.

**Bit 1: Temperature High Flag (THF).** Logic 1 in the temperature high flag bit indicates that a temperature measurement during a mission revealed a temperature equal to or higher than the value in the Temperature High Threshold register. The temperature high flag can be cleared at any time by writing this bit to 0. This flag must be cleared before starting a new mission.

**Bit 0: Timer Alarm Flag (TAF).** If this bit reads 1, a RTC alarm has occurred (see the *Timekeeping* section for details). The timer alarm flag can be cleared at any time by writing this bit to logic 0. Since the timer alarm cannot be disabled, the TAF flag usually reads 1 during a mission. This flag should be cleared before starting a new mission.

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### **Mission Timestamp Register Map**

ADDRESS	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
0215h	0		10 Minutes			Single	Minutes	
0216h	0	12/24	20 Hour AM/PM	10 Hour		Single	Hours	
0217h	0	0	10 [	Date		Single	e Date	
0218h	0	0	0	10 Months		Single	Months	
0219h		10 Y	'ears			Single	Years	

### **Mission Samples Counter Register Map**

ADDRESS	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
021Ah				Low	Byte			
021Bh				Cente	r Byte			
021Ch				High	Byte			

#### **Device Samples Counter Register Map**

ADDRESS	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
021Dh				Low	Byte			
021Eh				Cente	r Byte			
021Fh				High	Byte			

#### **Mission Timestamp**

The Mission Timestamp register indicates the time and date of the first temperature conversion of a mission. Subsequent temperature conversions take place as many minutes apart from each other as specified by the value in the Sample Rate register. Mission samples occur on minute boundaries.

#### **Mission Samples Counter**

The Mission Samples Counter register indicates how many temperature measurements have taken place during the current mission in progress (if MIP = 1) or during the latest mission (if MIP = 0). The value is stored as an unsigned 24-bit integer number. This counter is reset through the Clear Memory command.

#### **Device Samples Counter**

The Device Samples Counter register indicates how many temperature measurements have taken place since the device was assembled at the factory. The value is stored as an unsigned, 24-bit integer number. The maximum number that can be represented in this format is 16,777,215, which is higher than the expected lifetime of the DS1921G <u>iButton</u>. This counter cannot be reset under software control.

#### **Temperature Logging and Histogram**

Once set up for a mission, the DS1921G logs the temperature measurements simultaneously byte after byte in the data-log memory as well as in histogram form in the histogram memory. The data-log memory is able to store 2,048 temperature values measured at equidistant time points. The first temperature value of a mission is written to address location 1000h of the data-log memory, the second value to address location 1001h and so on. Knowing the starting time point (Mission Timestamp register), the interval between temperature measurements, the Mission Samples Counter register, and the rollover setting, one can reconstruct the time and date of each measurement stored in the data log.

There are two alternatives to the way the DS1921G behaves after the 2048 bytes of data-log memory is filled with data. With rollover disabled (RO = 0), the device fills the data-log memory with the first 2048 mission samples. Additional mission samples are not logged in the data-log, but the histogram and temperature alarm RAM continue to update. With rollover enabled (RO = 1), the data log wraps around and overwrites previous data starting at 1000h for the every 2049th mission sample. In this mode, the device stores the last 2048 mission samples.

TEMPERATURE READING	TEMPERATURE EQUIVALENT IN °C	HISTOGRAM BIN NUMBER	HISTOGRAM BIN ADDRESS
00h	-40.0 or lower	0	800h to 801h
01h	-39.5	0	800h to 801h
02h	-39.0	0	800h to 801h
03h	-38.5	0	800h to 801h
04h	-38.0	1	802h to 803h
05h	-37.5	1	802h to 803h
06h	-37.0	1	802h to 803h
07h	-36.5	1	802h to 803h
08h	-36.0	2	804h to 805h
F3h	+81.5	60	878h to 879h
F4h	+82.0	61	87Ah to 87Bh
F5h	+82.5	61	87Ah to 87Bh
F6h	+83.0	61	87Ah to 87Bh
F7h	+83.5	61	87Ah to 87Bh
F8h	+84.0	62	87Ch to 87Dh
F9h	+84.5	62	87Ch to 87Dh
FAh	+85.0 or higher	62	87Ch to 87Dh

Figure 7. Histogram Bin and Temperature Cross-Reference

For the temperature histogram, the DS1921G provides 63 bins that begin at memory address 0800h. Each bin consists of a 16-bit, nonrolling-over binary counter that is incremented each time a temperature value acquired during a mission falls into the range of the bin. The least significant byte of each bin is stored at the lower address. Bin 0 begins at memory address 0800h, bin 1 at 0802h, and so on up to 087Ch for bin 62, as shown in Figure 7. The number of the bin to be updated after a temperature conversion is determined by cutting off the two least significant bits of the binary temperature value. Out-of-range values are range locked and counted as 00h or FAh.

Since each data bin is 2 bytes, it can increment up to 65,535 times. Additional measurements for a bin that has already reached its maximum value are not counted; the bin counter remains at its maximum value. With the fastest sample rate of one sample every minute, a 2-byte bin is sufficient for up to 45 days if all temperature readings fall into the same bin.

### **Temperature Alarm Logging**

For some applications it is essential to not only record temperature over time and the temperature histogram, but also record when exactly the temperature exceeded a predefined tolerance band and for how long the temperature stayed outside the desirable range. The DS1921G can log high and low durations. The tolerance band is specified by means of the Temperature Alarm Threshold registers, addresses 20Bh and 20Ch in the register page. One can set a high temperature and low temperature threshold. See the Temperature Conversion section for the data format the temperature has to be written in. As long as the temperature values stay within the tolerance band (i.e., are higher than the low threshold and lower than the high threshold), the DS1921G does not record any temperature alarm. If the temperature during a mission reaches or exceeds either threshold, the DS1921G generates an alarm and sets either the temperature high flag (THF) or the temperature low flag (TLF) in the Status register (address

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ALARM EVENT	DESCRIPTION	ADDRESS	
	Mission Samples Counter, Low Byte	0220h	
I ow Alarm 1	Mission Samples Counter, Center Byte	0221h	
Low Alarm 1	Mission Samples Counter, High Byte	0222h	
	Alarm Duration Counter	0223h	
Low Alarm 2	Alarm Timestamp and Duration	0224h to 0227h	
Low Alarms 3 to 1	Alarm Timestamp and Durations	0228h to 024Fh	
	Mission Samples Counter, Low Byte	0250h	
Llieb Alexand	Mission Samples Counter, Center Byte	0251h	
High Alarm 1	Mission Samples Counter, High Byte	0252h	
	Alarm Duration Counter	0253h	
High Alarm 2	Alarm Timestamp and Duration	0254h to 0257h	
High Alarms 3 to 1	Alarm Timestamp and Durations	0258h to 027Fh	

Figure 8. Alarm Timestamps and Durations Address Map

214h). This way, if the search conditions (address 20Eh) are set accordingly, the master can quickly identify devices with temperature alarms by means of the conditional search function (see the *ROM Function Commands* section). The device also generates a timestamp of when the alarm occurred and begins recording the duration of the alarming temperature.

Timestamps and durations where the temperature leaves the tolerance band are stored in the address range 0220h to 027Fh, as shown in Figure 8. This allocation allows recording 24 individual alarm events and periods (12 periods for too hot and 12 for too cold). The date and time of each of these periods can be determined from the Mission Timestamp register and the time distance between each temperature reading.

The alarm timestamp is a copy of the Mission Samples Counter register when the alarm first occurred. The least significant byte is stored at the lower address. One address higher than the timestamp, the DS1921G maintains a 1-byte duration counter that stores the number of samples the temperature was found to be beyond the threshold. If this counter has reached its limit after 255 consecutive temperature readings and the temperature has not yet returned to within the tolerance band, the device issues another timestamp at the next higher alarm location and opens another counter to record the duration. If the temperature returns to normal before the counter has reached its limit, the dura-

tion counter of the particular timestamp does not increment any further. Should the temperature again cross this threshold, it is recorded at the next available alarm location. This algorithm is implemented for the low temperature thresholds as well as for the high temperature threshold.

### Missioning

The typical task of the DS1921G <u>i</u>Button is recording the temperature of a temperature-sensitive object. Before the device can perform this function, it needs to be configured. This procedure is called missioning.

First, the DS1921G must have its RTC set to a valid time and date. This reference time can be UTC (also called GMT, Greenwich Mean Time) or any other time standard that was chosen for the application. The clock must be running  $(\overline{EOSC} = 0)$  for at least one second. Setting an RTC alarm is optional. The memory assigned to store the alarm timestamps and durations, temperature histogram, Mission Timestamp, Mission Samples Counter, Mission Start Delay, and Sample Rate must be cleared using the Clear Memory command. In case there were temperature alarms in the previous mission, the TLF and THF flags need to be cleared manually. To enable the device for a mission, the EM flag must be set to 0. These are general settings that have to be made regardless of the type of object to be monitored and the duration of the mission.

Next, the low temperature and high temperature thresholds that specify the temperature tolerance band must be defined. The *Temperature Conversion* section describes how to convert a temperature value into the binary code to be written to the threshold registers.

The state of the search condition bits in the Control register does not affect the mission. If multiple devices are connected to form a 1-Wire net, the setting of the search condition enables these devices to participate in the conditional search if certain events, such as timer or temperature alarms, have occurred. Details on the search conditions are found in the *ROM Function Commands* section and in the Control register description.

The setting of the rollover-enable bit (RO) and sample rate depends on the duration of the mission and the monitoring requirements. If the most recent temperature history is important, the rollover should be enabled (RO = 1). Otherwise, one should estimate the duration of the mission in minutes and divide the number by 2048 to calculate the value of the sample rate (number of minutes between temperature conversions). For example, if the estimated duration of a mission is 10 days (14,400min), then the 2048-byte capacity of the data-log memory would be sufficient to store a new value every 7min. If the DS1921G's data-log memory is not large enough to store all temperature readings, one can use several devices and set the Mission Start Delay to values that make the second device start recording as soon as the memory of the first device is full and so on. The RO bit needs to be set to 0 to disable rollover that would otherwise overwrite the recorded tempera-

After the RO bit and the Mission Start Delay are set, the Sample Rate register is the last element of data that is written. The sample rate can be any value from 1 to 255, coded as an unsigned 8-bit binary number. As soon as the sample rate is written, the DS1921G sets the MIP flag and clears the MEMCLR flag. After as many minutes as specified by the Mission Start Delay are over, the device waits for the next minute boundary, then wakes up, copies the current time and date to the Mission Timestamp register, and makes the first temperature conversion of the mission. This increments both the Mission Samples Counter and Device Samples Counter. All subsequent temperature measurements are taken on minute boundaries specified by the value in the Sample Rate register. One can read the memory of the DS1921G to watch the mission as it progresses. Care should be taken to avoid memory access conflicts. See the Memory Access Conflicts section for details.

### \_Address Registers and Transfer Status

Because of the serial data transfer, the DS1921G employs three address registers, called TA1, TA2, and E/S (Figure 9). Registers TA1 and TA2 must be loaded with the target address to which the data is written or from which data is sent to the master upon a read command. Register E/S acts like a byte counter and transfer status register. It is used to verify data integrity with write commands. Therefore, the master has only read access to this register. The lower 5 bits of the E/S register indicate the address of the last byte that has been written to the scratchpad. This address is called Ending Offset. Bit 5 of the E/S register, called PF or partial byte flag, is set if the number of data bits sent by the master is not an integer multiple of 8. Bit 6 is always a 0. Note that the lowest 5 bits of the target address also determine the address within the scratchpad where intermediate storage of data begins. This address is called byte offset. If the target address for a write command is 13Ch, for example, then the scratchpad stores incoming data beginning at the byte offset 1Ch and is full after only 4 bytes. The corresponding ending offset in this example is 1Fh. For the best economy of speed and efficiency, the target address for writing should point to the beginning of a new page, i.e., the byte offset is 0. Thus, the full 32-byte capacity of the scratchpad is available, resulting also in the ending offset of 1Fh. However, it is possible to write one or several contiguous bytes somewhere within a page. The ending offset together with the partial and overflow flag are a means to support the master checking the data integrity after a write command. The highest valued bit of the E/S register, called authorization accepted (AA), indicates that a valid copy command for the scratchpad has been received and executed. Writing data to the scratchpad clears this flag.

### Writing with Verification

To write data to the DS1921G, the scratchpad must be used as intermediate storage. First, the master issues the Write Scratchpad command to specify the desired target address, followed by the data to be written to the scratchpad. In the next step, the master sends the Read Scratchpad command to read the scratchpad and to verify data integrity. As preamble to the scratchpad data, the DS1921G sends the requested target address TA1 and TA2 and the contents of the E/S register. If the PF flag is set, data did not arrive correctly in the scratchpad. The master does not need to continue reading; it can start a new trial to write data to the scratchpad. Similarly, a set AA flag indicates that the

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BIT NUMBER	7	6	5	4	3	2	1	0
TARGET ADDRESS (TA1)	Т7	T6	T5	T4	Т3	T2	T1	ТО
TARGET ADDRESS (TA2)	T15	T14	T13	T12	T11	T10	Т9	Т8
ENDING ADDRESS WITH DATA STATUS (E/S) (READ-ONLY)	AA	0	PF	E4	E3	E2	E1	E0

Figure 9. Address Registers

write command was not recognized by the device. If everything went correctly, both flags are cleared and the ending offset indicates the address of the last byte written to the scratchpad. Now the master can continue verifying every data bit. After the master has verified the data, it has to send the Copy Scratchpad command. This command must be followed exactly by the data of the three address registers TA1, TA2, and E/S as the master has read them verifying the scratchpad. As soon as the DS1921G has received these bytes, it copies the data to the requested location beginning at the target address.

### Memory/Control Function Commands

The Memory/Control Function Flowchart (Figure 10) describes the protocols necessary for accessing the memory and the special function registers of the DS1921G. An example on how to use these and other functions to set up the DS1921G for a mission is included in the Mission Example: Prepare and Start a New Mission section. The communication between master and DS1921G takes place either at standard speed (default, OD = 0) or at overdrive speed (OD = 1). If not explicitly set into the overdrive mode, the DS1921G assumes standard speed. Internal memory access during a mission has priority over external access through the 1-Wire interface. This affects the read memory commands described below. See the Memory Access Conflicts section for details.

### Write Scratchpad [0Fh]

After issuing the Write Scratchpad command, the master must first provide the 2-byte target address, followed by the data to be written to the scratchpad. The data is written to the scratchpad starting at the byte offset T[4:0]. The ending offset E[4:0] is the byte offset at which the master stops writing data. Only full data bytes are accepted. If the last data byte is incomplete, its content is ignored and the partial byte flag (PF) is set.

When executing the Write Scratchpad command, the CRC generator inside the DS1921G (see Figure 16) calculates a CRC of the entire data stream, starting at the command code and ending at the last data byte sent by the master. This CRC is generated using the CRC-16 polynomial by first clearing the CRC generator and then shifting in the command code (0Fh) of the Write Scratchpad command, the target addresses TA1 and TA2 as supplied by the master, and all the data bytes. The master can end the Write Scratchpad command at any time. However, if the ending offset is 11111b, the master can send 16 read time slots and receive an inverted CRC-16 generated by the DS1921G.

**Note:** The range 200h to 213h of the register page is protected during a mission. See Figure 6 for the access type of the individual registers between and during missions.

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#### Read Scratchpad [AAh]

This command is used to verify scratchpad data and target addresses. After issuing the Read Scratchpad command, the master begins reading. The first 2 bytes are the target address. The next byte is the ending off-set/data status byte (E/S) followed by the scratchpad data beginning at the byte offset T[4:0], as shown in Figure 9. Regardless of the actual ending offset, the master can read data until the end of the scratchpad after which it receives an inverted CRC-16 of the command code, target addresses TA1 and TA2, the E/S byte, and the scratchpad data starting at the target address. After the CRC is read, the bus master reads logical "1"s from the DS1921G until a reset pulse is issued.

### Copy Scratchpad [55h]

This command is used to copy data from the scratchpad to the writable memory sections. Applying a Copy Scratchpad command to the Sample Rate register can start a mission provided that several preconditions are met. See the Mission Start and Logging Process section and the flowchart in Figure 11 for details. After issuing the Copy Scratchpad command, the master must provide a 3-byte authorization pattern, which can be obtained by reading the scratchpad for verification. This pattern must exactly match the data contained in the three address registers (TA1, TA2, E/S, in that order). If the pattern matches, the AA flag is set and the copy begins. A pattern of alternating "1"s and "0"s is transmitted after the data has been copied until the master issues a reset pulse. While the copy is in progress, any attempt to reset the part is ignored. Copy typically takes 2µs per byte.

The data to be copied is determined by the three address registers. The scratchpad data from the beginning offset through the ending offset is copied, starting at the target address. Anywhere from 1 to 32 bytes can be copied to memory with this command. The AA flag remains at logic 1 until it is cleared by the next Write Scratchpad command. Note that the Copy Scratchpad command, when applied to the address range 200h to 213h during a mission, ends the mission.

### Read Memory [F0h]

The Read Memory command can be used to read the entire memory. After issuing the command, the master must provide the 2-byte target address. After the 2 bytes, the master reads data beginning from the target address and can continue until the end of memory, at which point logic "0"s are read. It is important to realize that the target address registers contain the address provided. The ending offset/data status byte is unaffected.

The hardware of the DS1921G provides a means to accomplish error-free writing to the memory section. To safeguard data in the 1-Wire environment when reading and to simultaneously speed up data transfers, it is recommended to packetize data into data packets of the size of one memory page each. Such a packet would typically store a 16-bit CRC with each page of data to ensure rapid, error-free data transfers that eliminate having to read a page multiple times to verify if the received data is correct (refer to Application Note 114: 1-Wire File Structure for the recommended file structure).

## Thermochron iButton

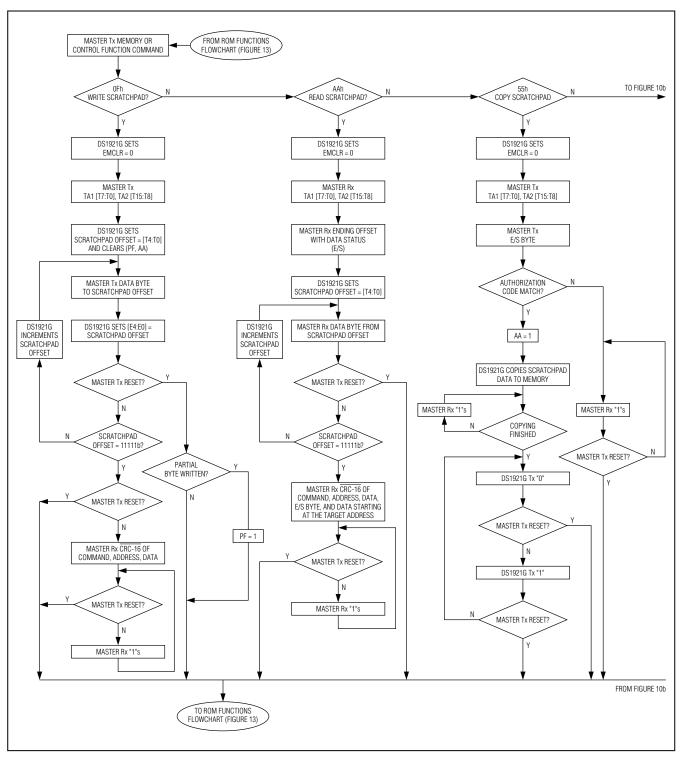


Figure 10a. Memory/Control Function Flowchart

# Thermochron iButton

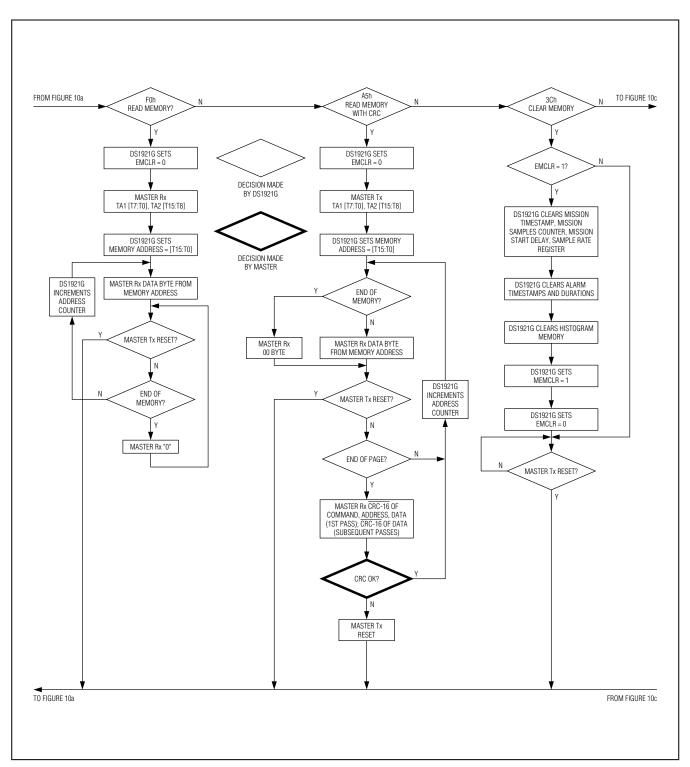


Figure 10b. Memory/Control Function Flowchart

# Thermochron <u>i</u>Button

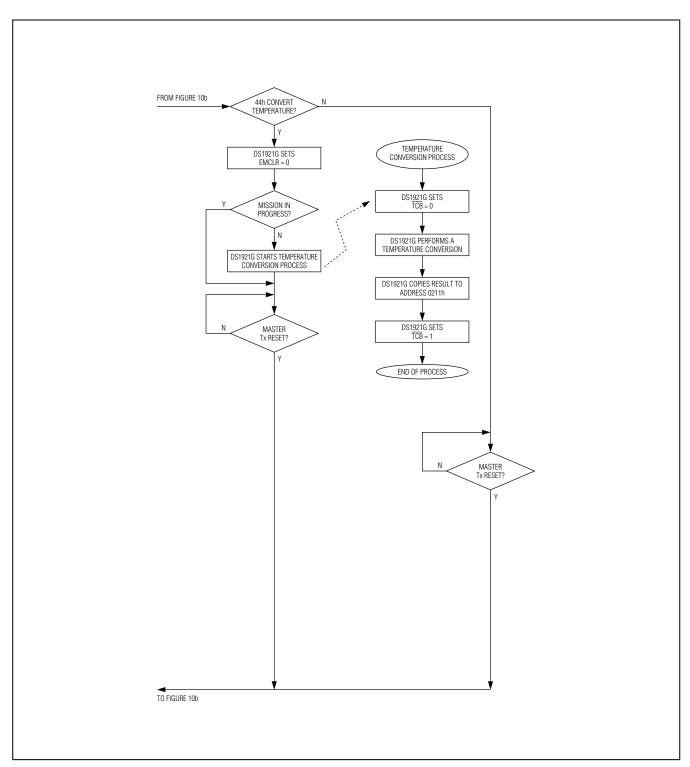


Figure 10c. Memory/Control Function Flowchart

### Read Memory with CRC [A5h]

The Read Memory with CRC command is used to read memory data that cannot be packetized, such as the register page and the data recorded by the device during a mission. The command works the same way as the simple Read Memory command, except for the 16-bit CRC that the DS1921G generates and transmits following the last data byte of a memory page.

After having sent the command code of the Read Memory with CRC command, the bus master sends a 2-byte address (TA1 = T[7:0], TA2 = T[15:8]) that indicates a starting byte location. With the subsequent read-data time slots, the master receives data from the DS1921G starting at the initial address and continues until the end of a 32-byte page is reached. At that point the bus master sends 16 additional read-data time slots and receives an inverted 16-bit CRC. With subsequent read-data time slots the master receives data starting at the beginning of the next page followed again by the inverted CRC for that page. This sequence continues until the bus master resets the device.

With the initial pass through the Read Memory with CRC command flow, the 16-bit CRC value is the result of shifting the command byte into the cleared CRC generator followed by the two address bytes and the contents of the data memory. Subsequent passes through the Read Memory with CRC command flow generate a 16-bit CRC that is the result of clearing the CRC generator and then shifting in the contents of the data memory page. After the 16-bit CRC of the last page is read, the bus master receives logical "0"s from the DS1921G and inverted CRC-16s at page boundaries until a reset pulse is issued. The Read Memory with CRC command sequence can be ended at any point by issuing a reset pulse.

#### Clear Memory [3Ch]

The Clear Memory command is used to clear the Sample Rate, Mission Start Delay, Mission Timestamp. and Mission Samples Counter in the register page and the temperature alarm memory and the temperature histogram memory. These memory areas must be cleared for the device to be set up for another mission. The Clear Memory command does not clear the datalog memory or the temperature and timer alarm flags in the Status register. The RTC oscillator must be on and have counted at least 1s before issuing the command. For the Clear Memory command to function, the EMCLR bit in the Control register must be set to 1, and the Clear Memory command must be issued with the very next access to the device's memory functions. Issuing any other memory function command resets the EMCLR bit. The Clear Memory process takes 500µs.

When the command is completed the MEMCLR bit in the Status register reads 1 and the EMCLR bit is 0.

### **Convert Temperature [44h]**

If a mission is not in progress (MIP = 0), the Convert Temperature command can be issued to measure the current temperature of the device. The result of the temperature conversion can be found at memory address 211h in the register page. This command takes maximum 90ms to complete. During this time the device remains fully accessible for memory/control and ROM function commands.

### **Mission Start and Logging Process**

The DS1921G does not use a special command to start a mission. Instead, a mission is started by writing a nonzero value to the Sample Rate register using the Copy Scratchpad command. As shown in Figure 11, a new mission can only be started if the previous mission has been stopped (MIP = 0), the memory is cleared (MEMCLR = 1), and the mission is enabled ( $\overline{EM} = 0$ ). If the new sample rate is different from zero, the value is copied to the Sample Rate register. At the same time the MIP bit is set and the MEMCLR bit is cleared to indicate that the device is on a mission. Next, the Mission Start Delay Counter starts decrementing every minute until it is down to 0. Now the DS1921G waits until the next minute boundary and starts the logging process, which as its first action copies the applicable RTC reqisters to the Mission Timestamp register.

#### **Stop Mission**

The DS1921G does not have a special command to stop a mission. A mission can be stopped at any time by writing to any address in the range of 0200h to 0213h or by writing the MIP bit of the Status register at address 0214h to 0. Either approach involves the use of the Copy Scratchpad command. There is no need for the Mission Start Delay to expire before a mission can be stopped (see Figure 11).

### Memory Access Conflicts

While a mission is in progress, a temperature sample is periodically taken and stored in the data-log, histogram, and potential alarm memory. This "internal activity" has priority over a Read Memory command's or Read Memory with CRC command's access to these pages. If a conflict occurs, the data read may be invalid, even if the CRC value matches the data. To ensure that the data read is valid, it is recommended to first read the SIP bit of the Status register. If the SIP bit is set, delay reading the data-log, histogram, and alarm memory until SIP is 0. The interference is more likely to be seen with a high sample rate (one sample every