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DS1925

iButton High-Capacity Temperature Logger with 122KB Data-Log Memory

General Description

The iButton® temperature logger (DS1925) is a rugged, self-sufficient system that measures temperature and records the result in a protected memory section. The recording is done at a user-defined rate. A total of 122K 8-bit readings or 61K 16-bit readings taken at equidistant intervals ranging from 5min to 273hrs can be stored. In addition, there are 512 bytes of nonvolatile memory for storing application-specific information. A mission to collect data can be programmed to begin immediately, after a user-defined delay, or after a temperature alarm. Access to the memory and control functions can be password protected. The DS1925 is configured and communicates with a host computing device through the serial 1-Wire® protocol, which requires only a single data lead and a ground return. Every DS1925 is factory-lasered with a guaranteed unique 64-bit registration number that allows for absolute traceability. The durable stainless-steel package is highly resistant to environmental hazards such as dirt, moisture, and shock. Accessories permit the DS1925 to be mounted on almost any object, including containers, pallets, and bags.

Applications

- Temperature Logging in Cold Chain
- Food Safety
- Bio Science
- Pharmaceutical and Medical Products High-Temperature Logging (Process Monitoring, Industrial Monitoring)

Examples of Accessories

PART	ACCESSORY
DS9093RA	Mounting Lock Ring
DS9093A	Snap-in FOB
DS9092	iButton Probe
DS1402D-DR8+	Blue Dot Receptor Cable

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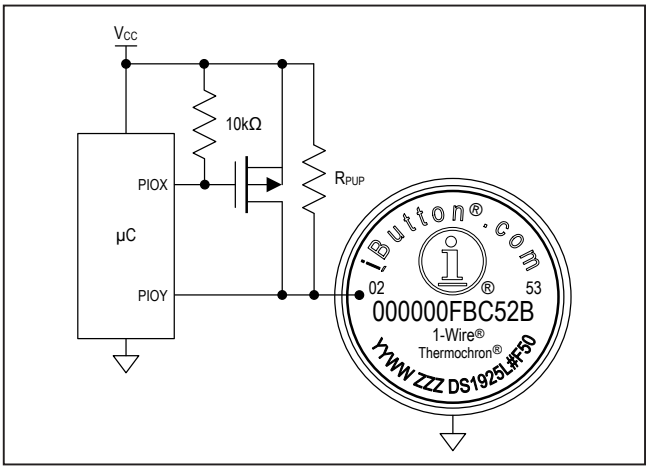
Benefits and Features

- Provides High-Quality Temperature Exposure Assessment of an End Product
  - Temperature Measurement Accuracy of ±0.5°C with Storage for Up to 125,440 Timestamped Values
  - Flexibility to Monitor and Data-Log Long Duration Exposures with Short-Duration Time Intervals
  - Unique Factory-Lasered 64-Bit Serial Number Ensures Absolute Traceability Because No Two Parts Are Alike
- Highly Configurable Options for Data Logging and Security
  - Programmable Sample Rates from 5min to 273hrs
  - Programmable Recording Start Delay After Elapsed Time or Upon a Temperature Alarm Trip Point
  - Two-Level Password Protection of All Memory and Configuration Registers
  - Measure and Report Internal Battery Level and Output-Logged Data if a Battery is Depleted
- Physically Robust, Operationally Efficient
  - Durable Stainless-Steel Enclosure Withstands Harsh Environments and Conditions
  - Communicates to a Host System with the Single-Contact 1-Wire Interface
  - -40°C to +85°C Operating Temperature Range

***Ordering Information* appears at end of data sheet.**

Typical Application Circuit



19-8480; Rev 2; 10/16

maxim integrated™

Absolute Maximum Ratings

IO Voltage to GND .....-0.3V to +6V
IO Sink Current.....20mA
Operating Temperature Range..... -40°C to +85°C
Junction Temperature.....+150°C
Storage Temperature Range.....-40°C to +85°C*

**Storage or operation above +50°C significantly reduces battery life.*

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Characteristics

(V_{PUP} = 3.0V to 5.25V, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Temperature	T_A	(Note 1)	-40		+85	°C
IO PIN: GENERAL DATA						
1-Wire Pullup Resistance	R_{PUP}	(Notes 2, 3)			2200	Ω
Input Capacitance	C_{IO}	(Note 4)		120		nF
Input Leakage Current	I_L	IO pin at V_{PUP}		6	60	µA
High-to-Low Switching Threshold	V_{TL}	(Notes 5, 6)		0.5 x V_{PUP}		V
Input Low Voltage	V_{IL}	(Notes 2, 7)			0.4	V
Low-to-High Switching Threshold	V_{TH}	(Notes 5, 8)		0.75 x V_{PUP}		V
Switching Hysteresis	V_{HY}	(Note 9)		0.2 x V_{PUP}		V
Output Low Voltage	V_{OL}	At 4mA (Note 10)			0.4	V
Recovery Time (Note 2)	t_{REC}	Standard speed, R_{PUP} = 2200Ω	5			µs
		Overdrive speed, R_{PUP} = 2200Ω	2			
		Overdrive speed, directly prior to reset pulse; R_{PUP} = 2200Ω	5			
Time Slot Duration (Note 2)	t_{SLOT}	Standard speed	65			µs
		Overdrive speed	8			
Rising-Edge Hold-Off Time	t_{REH}	(Note 11)		0.1		µs
IO PIN: 1-Wire RESET, PRESENSE-DETECT CYCLE						
Reset Low Time (Note 2)	t_{RSTL}	Standard speed, V_{PUP}	480		640	µs
		Overdrive speed	48		80	
Presence-Detect Sample Time (Note 2)	t_{MSP}	Standard speed	65		75	µs
		Overdrive speed	8		10	

Electrical Characteristics (continued)

(V_{PUP} = 3.0V to 5.25V, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
IO PIN: 1-Wire WRITE						
Write-Zero Low Time (Note 2)	t_{W0L}	Standard speed	60		120	µs
		Overdrive speed	6		16	
Write-One Low Time (Notes 2, 12)	t_{W1L}	Standard speed	5		15 - ε	µs
		Overdrive speed	0.25		2 - ε	
IO PIN: 1-Wire READ						
Read Low Time (Notes 2, 13)	t_{RL}	Standard speed	5		15 - δ	µs
		Overdrive speed	0.25		2 - δ	
Read Sample Time (Notes 2, 13)	t_{MSR}	Standard speed	t_{RL} + δ		15	µs
		Overdrive speed	t_{RL} + δ		2	
REAL-TIME CLOCK						
Accuracy	t_{ACC}	+25°C		1		Min/Month
Frequency Deviation	Δ_F	-40°C to +85°C	-300		+60	PPM
TEMPERATURE CONVERTER						
Conversion Time	t_{CONV}			10		ms
Thermal Response Time Constant	τ_{RESP}	iButton package (Note 14)		130		s
Conv. Error	$\Delta\vartheta$	(Note 15)	-0.5		+0.5	°C
COMMAND DELAYS AND CURRENT						
Standard Delay	t_{STD}				5	ms
Long Standard Delay	t_{LSTD}				15	ms
XPC Clear Memory (Log)	t_{CML}				1500	ms
RTC Start Delay from Clear Memory State	t_{SRTC}				500	ms
XPC Active Current	I_{XPCA}			5		mA

Note 1: Limits are 100% tested at T_A = +85°C (and/or T_A = +25°C). Limits over the operating temperature and relevant supply voltage range are guaranteed by design and characterization.
Note 2: System requirement.
Note 3: Maximum allowable pullup resistance is a function of the number of 1-Wire devices in the system and 1-Wire recovery times. The specified value here applies to systems with only one device and with the minimum 1-Wire recovery times. For more heavily loaded systems, an active pullup such as that found in the DS2480B may be required.
Note 4: Typical value represents the internal parasite capacitance when V_{PUP} is first applied. Once the parasite capacitance is charged, it does not affect normal communication.
Note 5: V_{TL}, V_{TH} are a function of the internal supply voltage.
Note 6: Voltage below which, during a falling edge on IO, a logic 0 is detected.
Note 7: The voltage on IO must be less than or equal to V_{ILMAX} whenever the master drives the line low.
Note 8: Voltage above which, during a rising edge on IO, a logic 1 is detected.
Note 9: After V_{TH} is crossed during a rising edge on IO, the voltage on IO must drop by V_{HY} to be detected as logic 0.

Electrical Characteristics (continued)

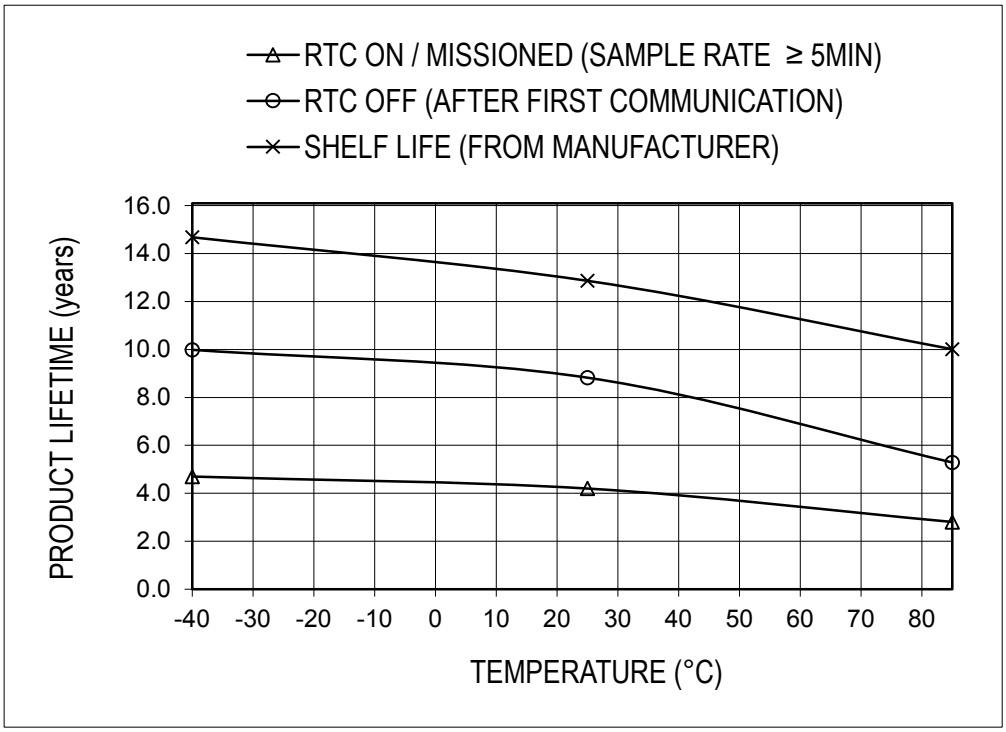
(V_{PUP} = 3.0V to 5.25V, unless otherwise noted.)

Note 10: The I-V characteristic is linear for voltages less than 1V.
Note 11: The earliest recognition of a negative edge is possible at t_{REH} after V_{TH} has been previously reached.
Note 12: ε in Figure 13 represents the time required for the pullup circuitry to pull the voltage on IO up from V_{IL} to V_{TH}.
Note 13: δ in Figure 13 represents the time required for the pullup circuitry to pull the voltage on IO up from V_{IL} to the input-high threshold of the bus master.
Note 14: This number was derived from a test conducted by Cemagref Antony, France, in July 2000 (Cemagref Test Report No. E42).
Note 15: Maxim data-logger products are 100% tested and calibrated at time of manufacture to ensure that they meet all data sheet parameters, including temperature accuracy. As with any sensor-based product, user shall be responsible for occasionally rechecking the temperature accuracy of the product to ensure it is still operating properly. Furthermore, as with all products of this type, when deployed in the field and subjected to handling, harsh environments, or other hazards/use conditions, there may be some extremely small but nonzero logger failure rate. In applications where the failure of any logger is a concern, user shall assure that redundant (or other primary) methods of testing and determining the handling methods, quality, and fitness of the articles and products are implemented to further mitigate any risk.

iButton Can Physical Specification

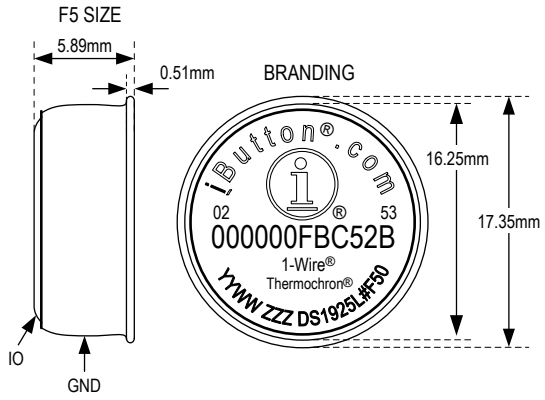
SIZE	See the *Package Information* section.
WEIGHT	Ca. 3.3 grams

Typical Product Lifetime*



*NOT CONNECTED TO 1-WIRE. TYPICAL LIFETIME WITH 1-WIRE IDLE HIGH IS 0.5YR. DISCONNECT 1-WIRE DURING MISSIONS.

Pin Configuration



Pin Description

NAME	FUNCTION
IO	Input/Output
GND	Ground

Detailed Description

The DS1925 is an ideal device to monitor for extended time periods the temperature of any object it is attached to or shipped with, such as fresh produce, medical drugs, and supplies, and for use in refrigerators and freezers. Note that the initial sealing level of the DS1925 achieves IP56. Aging and use conditions can degrade the integrity of the seal over time, so for applications with significant exposure to liquids, sprays, or other similar environments, it is recommended to place the DS1925 in the DS9107 iButton capsule. The DS9107 provides a watertight enclosure that has been rated to IP68 (refer to **Application Note 4126: Understanding the IP (Ingress Protection) Ratings of iButton Data Loggers and Capsule**). Software for setup and data retrieval through the 1-Wire interface is available for free download from the Maxim website at **www.maximintegrated.com/1-wiredrivers**. This software also includes drivers for the serial and USB port of a PC, and routines to access the general-purpose memory for storing application- or equipment-specific data files.

Overview

Figure 1 shows the relationships between the DS1925's major control and memory sections. The device has five main data components: 1) 64-bit lasered ROM, 2) 256-bit scratchpad, 3) 512-byte general-purpose memory, 4) two 256-bit register pages of timekeeping, control, status, and counter registers and passwords, and 5) 122KB of data-logging memory. Except for the ROM and the scratchpad, all other memory is arranged in a single linear address space. The data-logging memory, counter registers, and several other registers are read-only for the user. Both register pages are write-protected while the device is programmed for a mission. The password registers, one for a read password and another one for a read/write password, can only be written, never read.

Figure 2 shows the hierarchical structure of the 1-Wire protocol. The bus master must first provide one of the eight ROM function commands: 1) Read ROM, 2) Match ROM, 3) Search ROM, 4) Conditional Search ROM, 5) Skip ROM, 6) Overdrive-Skip ROM, 7) Overdrive-Match ROM, or 8) Resume. Upon completion of an Overdrive ROM command byte executed at standard speed, the device enters overdrive mode, where all subsequent communication occurs at a higher speed. Figure 12 describes the protocol required for these ROM function commands. After a ROM function command is successfully executed, the memory and control functions become accessible and the master can provide any one of the eight available commands. Figure 9 describes the protocol for these memory and control function commands. **All data is read and written least significant bit first**.

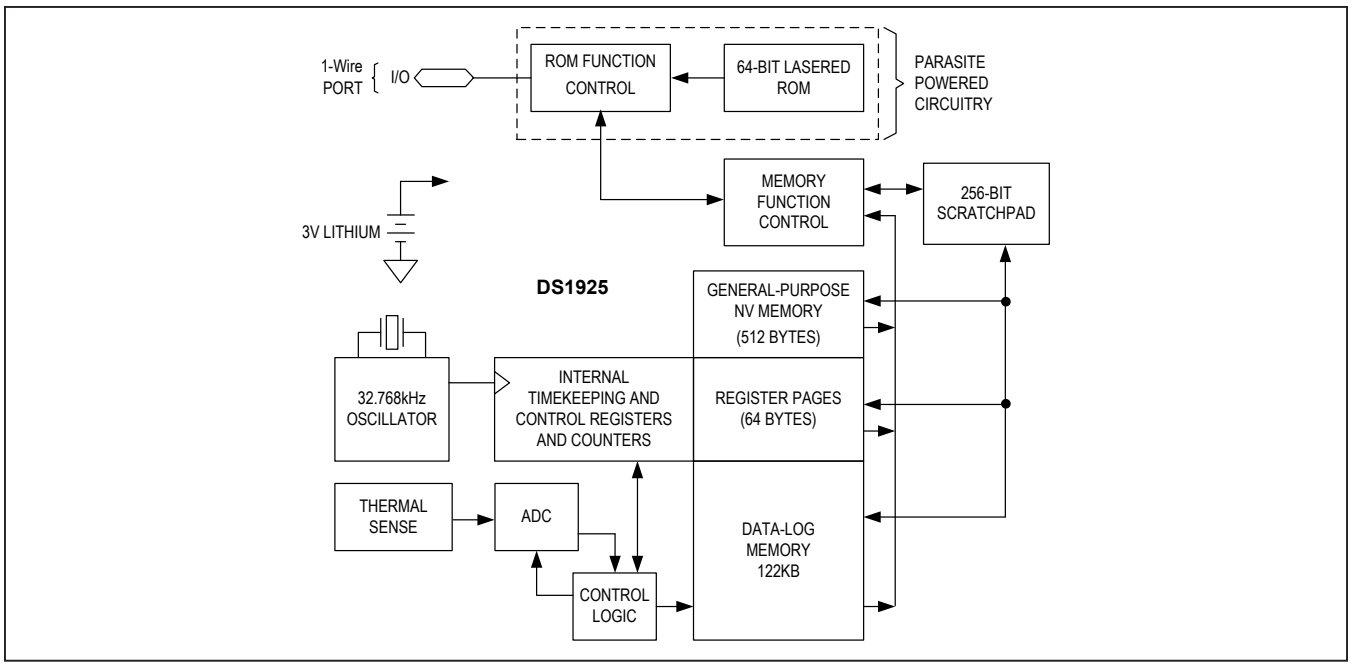


Figure 1. DS1925 Block Diagram

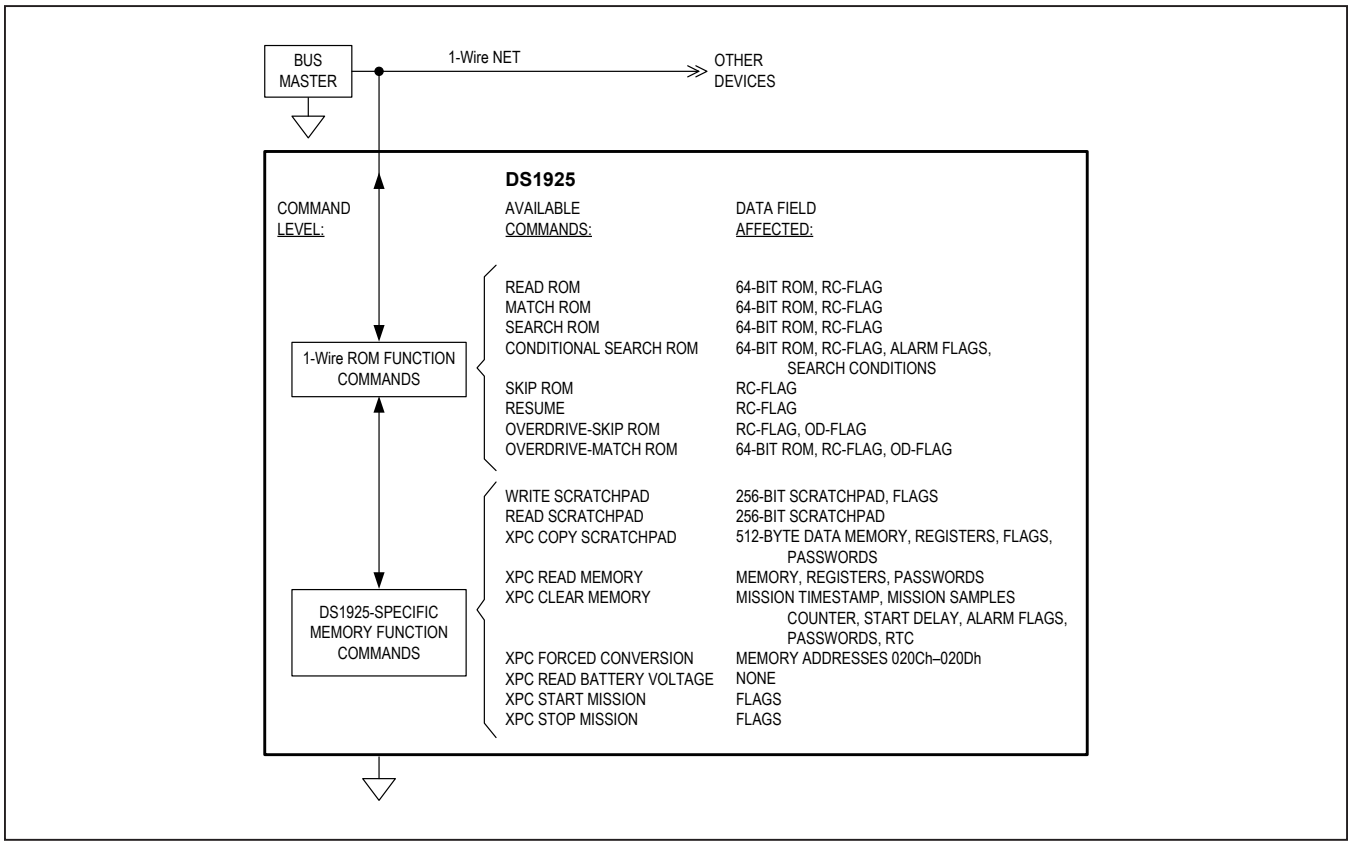


Figure 2. Hierarchical Structure for 1-Wire Protocol

Parasite Power

The block diagram (Figure 1) shows the parasite-powered circuitry. This circuitry “steals” power whenever the I/O input is high. I/O provides sufficient power as long as the specified timing and voltage requirements are met. The advantage of parasite power is that if the battery is exhausted for any reason, the ROM and data log may still be read.

64-Bit Unique ROM

Each DS1925 contains a unique ROM code that is 64 bits long. The first 8 bits are a 1-Wire family code. The next 48 bits are a unique serial number. The last 8 bits are a CRC of the first 56 bits. See Figure 3 for details. The 1-Wire CRC is generated using a polynomial generator consisting of a shift register and XOR gates as shown in Figure 4. The polynomial is $X^8 + X^5 + X^4 + 1$. Additional information about the Maxim Integrated 1-Wire Cyclic Redundancy Check (CRC) is available in Application Note 27: *Understanding and Using Cyclic Redundancy Checks with Maxim 1-Wire and iButton Products.*

The shift register bits are initialized to 0. Then starting with the least significant bit of the family code, one bit at a time is shifted in. After the 8th bit of the family code has been entered, then the serial number followed by the temperature range code is entered. After the range code has been entered, the shift register contains the CRC value. Shifting in the 8 bits of CRC returns the shift register to all 0s.

Clear Memory State

The DS1925 enters a clear memory state if it is new or if an XPC Clear Memory (log) sequence is done. In this state, some commands that enable the RTC takes an extra 500ms the first time they are called. The commands that could incur this additional delay (t_{SRTC}) are XPC Copy Scratchpad (99h), XPC Forced Conversion (4Bh), XPC Start Mission (DDh), and XPC Read Battery Voltage (33h). This is a one-time delay when coming out of the clear memory state.

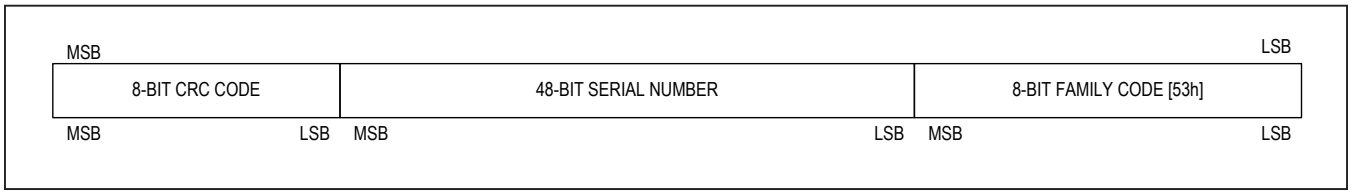


Figure 3. 64-Bit Unique ROM

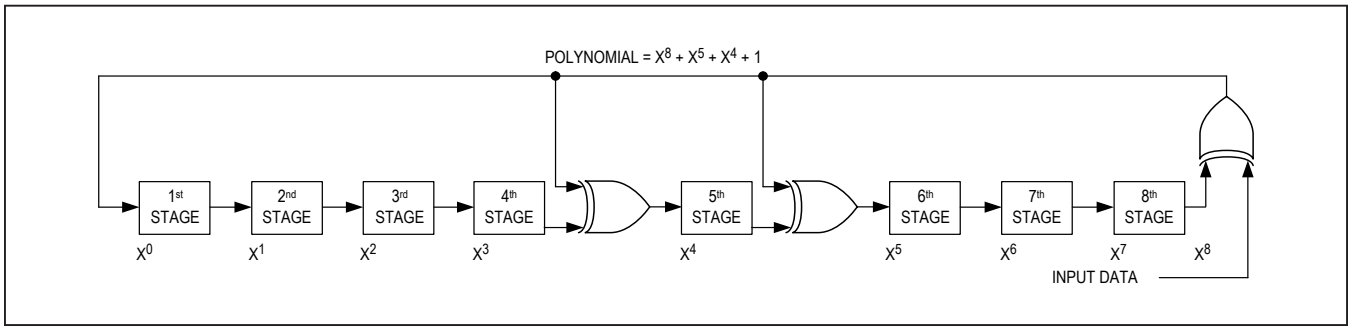


Figure 4. 1-Wire CRC Generator

Memory

Figure 5 shows the DS1925's memory map. The 512 bytes of general-purpose nonvolatile memory is located in pages 0 to 15. The various registers to set up and control the device fill pages 16 and 17, called register pages 1 and 2 (details in Figure 6). The data-log logging memory starts at address 1000h (page 122) and extends over 3920 pages. The memory pages 18 to 127 are reserved for future extensions. The scratchpad is an additional page that acts as a buffer when writing to the SRAM memory or the register page. The data memory can be written at any time. See the *Security by Password* section for ways to protect the memory. The access type for the register pages is register-specific and depends on whether the device is programmed for a mission. Figure 6 shows the details. The data-log memory is read-only for the user. It is written solely under supervision of the on-chip control logic. See the *Address Registers and Transfer Status* section for details.

Several commands provide a repeating result byte as described in Table 1.

Table 1. Repeating Byte Commands

REPEAT BYTE	DESCRIPTION
FFh	Operation not complete
AAh	(or 55h) Operation success
22h	Unable to complete the operation due to mission is in progress
44h	Error writing memory: Possibly writing memory that needs to be cleared
77h	Invalid parameter in operation
33h	Invalid authorization sequence: usually indicates TA1/TA2/ES is not correct in a copy operation
11h	Invalid password
00h	Unable to complete operation, requires XPC clear memory (log) sequence required

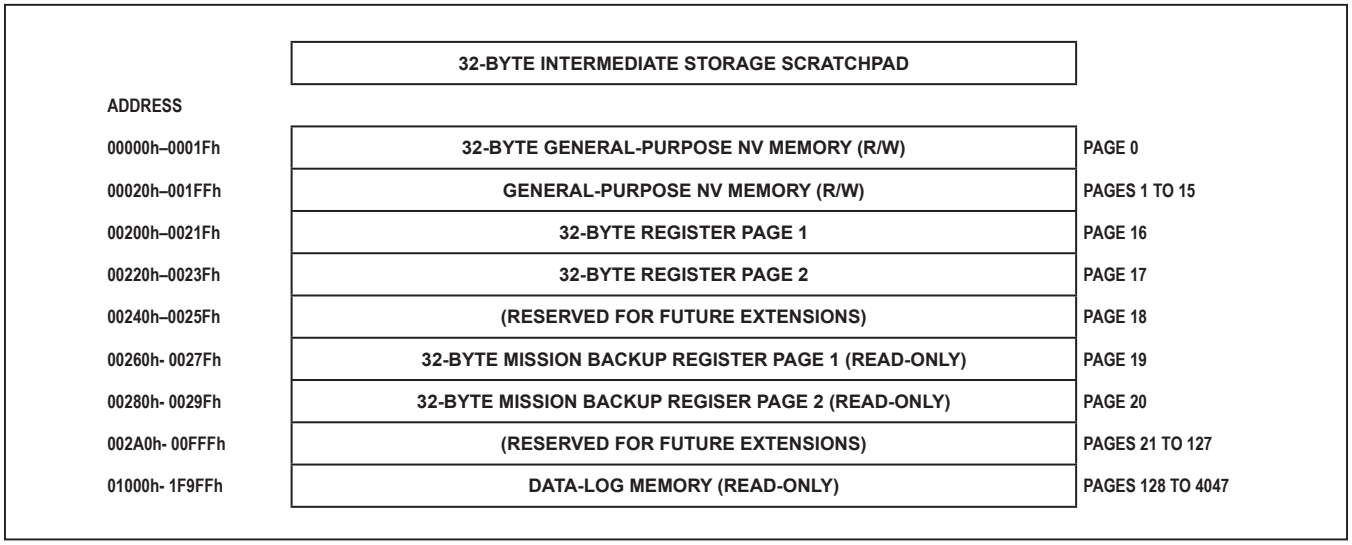


Figure 5. Memory Map

ADDR	b7	b6	b5	b4	b3	b2	b1	b0	FUNCTION	ACCESS*
0200h	LSByte Seconds								Real-Time Clock Registers	R/W; R
0201h	. . .									
0202h	. . .									
0203h	MSByte Seconds									
0204h	(not used)								(N/A)	R; R
0205h	(not used)								(N/A)	R; R
0206h	Low Byte								Sample Rate	R/W; R
0207h	0	0	High Byte							
0208h	Low Threshold								Temp Alarms	R/W; R
0209h	High Threshold									
020Ah	Reserved								(N/A)	R; R
020Bh	Reserved								(N/A)	R; R
020Ch	Low Byte			0	0	0	0	0	Latest Temp	R; R
020Dh	High Byte									
020Eh	Reserved								(N/A)	R; R
020Fh	Reserved									
0210h	0	0	0	0	0	0	ETHA	ETLA	Temperature Alarm Enable	R/W; R
0211h	1	1	1	1	1	1	0	0	(N/A)	R/W; R
0212h	0	0	0	0	0	0	EHSS	EOSC	RTC Control	R/W; R
0213h	1	1	SUTA	1	(X)	TLFS	0	ETL	Mission Control	R/W; R
0214h	BOR	1	1	1	0	0	THF	TLF	Alarm Status	R; R
0215h	1	1	0	WFTA	MEMCLR	0	MIP	0	General Status	R; R
0216h	Low Byte								Mission Start Delay Counter	R/W; R
0217h	Center Byte									
0218h	High Byte									
0219h	LSByte Seconds								Mission Timestamp	R/W; R
021Ah	. . .									
021Bh	. . .									
021Ch	MSByte Seconds									
021Dh	(not used)								(N/A)	R; R
021Eh	(not used)								(N/A)	R; R
021Fh	(No function; reads 00h)								(N/A)	R; R
0220h	Low Byte								Mission Samples Counter	R; R
0221h	Center Byte									
0222h	High Byte									
0223h	Low Byte								Device Samples Counter	R; R
0224h	Center Byte									
0225h	High Byte									
0226h	Configuration Code								Flavor	R; R
0227h	EPW								Password Control	R/W; R
0228h	First Byte								Read Access Password	W; ---
...	. . .									
022Fh	Eighth Byte									
0230h	First Byte								Full Access Password	W; —
...	. . .									
0237h	Eighth Byte									
0238h	(No function; all these bytes read 00h)								(N/A)	R; R
...										
023Fh										

***The first entry in the "ACCESS" column is valid between missions. The second entry shows the applicable access type while a mission is in progress.**

Figure 6. Register Pages Map

Detailed Register Descriptions

Timekeeping and Calendar

The real-time clock (RTC) is a second counter accessed by reading/writing the appropriate bytes in the register page, address 200h–203h. For readings to be valid, all RTC registers must be read sequentially starting at address 0200h. The number representation of the RTC registers is in seconds format. Typically, this is the number of seconds since January 1, 1970 12:00a.m. See Table 2 for the bitmap.

Sample Rate

The content of the Sample Rate register (addresses 0206h, 0207h) specifies the time elapse between temperature-logging events. The sample rate is coded as an unsigned 14-bit binary number with a maximum value of 16,383. If EHSS = 1, the sample rate is in seconds. If EHSS = 0, the sample rate is in minutes. The fatest recommended sample rate is 5 minutes. Setting a sample rate less than 3 minutes (180 seconds ESHSS = 1 or 3 minutes EHSS = 0) results in a failure on the XPC Start Mission command with repeat code 77h Invalid Parameter. The EHSS bit is located in the RTC Control register at address 0212h. It is important that the user sets the EHSS bit accordingly while setting the Sample Rate register. During a mission, there is only read access to these registers. Bits cells marked 0 always read 0 and cannot be written to 1. See Table 3 for the bitmap.

Temperature Conversion

The DS1925 measures temperatures in the -40°C to +85°C range. Temperature values are represented as an 8-bit or 16-bit unsigned binary number with a resolution of 0.5°C in the 8-bit mode and 0.0625°C in the 16-bit mode.

The higher temperature byte TRH is always valid. In 16-bit mode, only the three highest bits of the lower byte TRL are valid. The five lower bits all read 0. TRL is undefined if the device is in 8-bit temperature mode. An out-of-range temperature reading is indicated as 00h or 0000h when too cold and FFh or FFE0h when too hot. See Table 4 for the bitmap.

Table 2. Real-Time Clock and RTC Alarm Registers Bitmap

ADDR	b7	b6	b5	b4	b3	b2	b1	b0
0200h	LSByte Seconds							
0201h	. . .							
0202h	. . .							
0203h	MSByte Seconds							

Table 3. Sample Rate Register Bitmap

ADDR	b7	b6	b5	b4	b3	b2	b1	b0
0206h	Sample Rate Low							
0207h	0	0	Sample Rate High					

Table 4. Latest Temperature Conversion Result Register Bitmap

ADDR	b7	b6	b5	b4	b3	b2	b1	b0	
020Ch	T2	T1	T0	0	0	0	0	0	TRL
020Dh	T10	T9	T8	T7	T6	T5	T4	T3	TRH

Table 5. Temperature Conversion Examples

MODE	TRH		TRL		ϑ = (°C) DS1925
	HEX	DECIMAL	HEX	DECIMAL	
8-bit	54h	84	—	—	1.0
8-bit	17h	23	—	—	-29.5
16-bit	54h	84	00h	0	1.000
16-bit	17h	23	60h	96	-29.3125

With TRH and TRL representing the decimal equivalent of a temperature reading, calculate the temperature value as:

ϑ(°C) = TRH/2 - 41+ TRL/512 (16-bit mode, TLFS = 1, see address 0213h)

ϑ(°C) = TRH/2 - 41 (8-bit mode, TLFS = 0, see address 0213h)

This equation is valid for converting temperature readings stored in the data-log memory as well as for data read from the Latest Temperature Conversion Result register. The "- 41" applies to the DS1925.

To specify the temperature alarm thresholds, the previous equation needs to be resolved to:

$$TALM = 2 \times \vartheta\ (°C) + 82$$

where "+ 82" applies to the DS1925.

Because the temperature alarm threshold is only 1 byte, the resolution or temperature increment is limited to 0.5°C. The TALM value needs to be converted into hexadecimal format before it can be written to one of the temperature alarm threshold registers (**low alarm address 0208h; high alarm address 0209h**). Independent of the conversion mode (8-bit or 16-bit), only the most significant byte of a temperature conversion is used to determine whether an alarm is generated.

Temperature Sensor Alarm

The DS1925 has two Temperature Alarm Threshold registers (address 0208h, 0209h) to store values, which determine whether a critical temperature has been reached. A temperature alarm is generated if the device measures an alarming temperature **and** the alarm signaling is enabled. The ETLA and ETHA bits that enable the temperature alarm are located in the Temperature Sensor Control register. See Table 7 for the bitmap. During a mission, there is only read access to this register. Bits 7:2 have no function. They always read 0 and cannot be written to 1. The temperature alarm flags TLF and THF are found in the Alarm Status register at address 0214h.

Table 6. Temperature Alarm Threshold Examples

ϑ (°C)	TALM (DS1925)	
	HEX	DECIMAL
65.5	85h	133
30.0	3Eh	62

Table 7. Temperature Sensor Control Register Bitmap

ADDR	b7	b6	b5	b4	b3	b2	b1	b0
0210h	0	0	0	0	0	0	ETHA	ETLA

Table 8. Temperature Sensor Control Register Bit Descriptions

BIT	NAME	FUNCTION
b1	ETHA	Enable Temperature High Alarm. This bit controls whether during a mission the temperature high alarm flag (THF) may be set, if a temperature conversion results in a value equal to or higher than the value in the Temperature High Alarm Threshold Register. If ETHA is 1, temperature high alarms are enabled. If ETHA is 0, temperature high alarms are not generated.
b0	ETLA	Enable Temperature Low Alarm. This bit controls whether during a mission the temperature low alarm flag (TLF) may be set, if a temperature conversion results in a value equal to or lower than the value in the Temperature Low Alarm Threshold register. If ETLA is 1, temperature low alarms are enabled. If ETLA is 0, temperature low alarms are not generated.

RTC Control

To minimize the DS1925's power consumption, the RTC oscillator should be turned off when device is not in use. The oscillator on/off bit is located in the RTC Control register (0212h). Turning the oscillator on when the device is in clear memory state incurs an additional t_{SRTC} delay. This register also includes the EHSS bit, which determines whether the sample rate is specified in seconds or minutes. Table 9 shows the register bitmap. See Table 10 for register descriptions. During a mission, there is only read access to this register. Bits 7:2 have no function; they always read 0 and cannot be written to 1.

Mission Control

The DS1925 is set up for its operation by writing appropriate data to its special function registers, which are located in the two register pages. The settings in the Mission Control register determine which format (8 or 16 bits) is to be used and whether old data can be overwritten by new data, once the data-log memory is full. An additional control bit can be set to tell the DS1925 to wait with logging data until a temperature alarm is encountered. See Table 11 for the register bitmap. During a mission, there is only read access to this register. Bits 7:6 have no function; they always read 1 and cannot be written to 0. Bits 1 and 3 control functions that are not available with the DS1925. Bit 1 must be set to 0. Under this condition the setting of bit 3 becomes a "don't care."

Table 9. RTC Control Register Bitmap

ADDR	b7	b6	b5	b4	b3	b2	b1	b0
0212h	0	0	0	0	0	0	EHSS	EOSC

Table 10. RTC Control Register Bit Descriptions

BIT	NAME	FUNCTION
b1	EHSS	Enable High Speed Sample. This bit controls the speed of the sample rate counter. When set to logic 0, the sample rate is specified in minutes. When set to logic 1, the sample rate is specified in seconds.
b0	EOSC	Enable Oscillator. This bit controls the crystal oscillator of the RTC. When set to logic 1, the oscillator starts operation. When written to logic 0, the oscillator stops and the device is in a low-power data-retention mode. This bit must be 1 for normal operation. XPC Start Mission command automatically starts the RTC by changing the EOSC bit to logic 1.

Table 11. Mission Control Register Bitmap

ADDR	b7	b6	b5	b4	b3	b2	b1	b0
0213h	1	1	SUTA	1	(X)	TLFS	0	ETL

Table 12. Mission Control Register Bit Descriptions

BIT	NAME	FUNCTION
b5	SUTA	Start Mission Upon Temperature Alarm. This bit specifies whether a mission begins immediately (includes delayed start) or if a temperature alarm is required to start the mission. If this bit is 1, the device performs an 8-bit temperature conversion at the selected sample rate and begins with data logging only if an alarming temperature (high alarm or low alarm) was found. The first logged temperature is when the alarm occurred. However, the Mission Sample Counter does not increment. This functionality is guaranteed by design and not production tested.
b2	TLFS	Temperature Logging Format Selection. This bit specifies the format used to store temperature readings in the data-log memory. If this bit is 0, the data is stored in 8-bit format. If this bit is 1, the 16-bit format is used (higher resolution). With 16-bit format, the most significant byte is stored at the lower address.
b0	ETL	Enable Temperature Logging. To set up the device for a temperature-logging mission, this bit must be set to logic 1. The recorded temperature values start at address 1000h.

Alarm Status

The fastest way to determine whether a programmed temperature threshold was exceeded during a mission is through reading the Alarm Status register. In a networked environment that contains multiple DS1925 devices, the devices that encountered an alarm can quickly be identified by means of the Conditional Search ROM command (see the *1-Wire ROM Function Commands* section). The temperature alarm only occurs if enabled (see the Temperature Sensor Alarm). The BOR alarm is always enabled. See Table 13 for the bitmap and Table 14 for the bit descriptions. There is only read access to this register. Bits 6:4 have no function; they always read 1. Bits 3:2 have no function with the DS1925; they always read 0. The alarm status bits are cleared simultaneously when the XPC Clear Memory function is invoked. See the *Memory and Control Function Commands* for details.

General Status

The information in the General Status register tells the host computer whether a mission-related command was executed successfully. Individual status bits indicate whether the DS1925 is performing a mission, waiting for a temperature alarm to trigger the logging of data, or whether the data from the latest mission has been cleared. See Table 15 for the bitmap. There is only read access to this register. Bits 6 and 7 have no function. Bits 0, 2, and 5 are normally 0's for typical operation but change to 1's to indicate if the register pages are a backup copy and represent the last state recorded at the start of a mission.

Mission Start Delay Counter

The content of the Mission Start Delay Counter register tells how many minutes have to expire from the time a mission was started until the first measurement of the mission takes place (SUTA = 0), or until the device starts testing the temperature for a temperature alarm (SUTA = 1). The Mission Start Delay is stored as an unsigned 24-bit integer number. If the start delay is non-zero and the SUTA bit is set to 1, first the delay has to expire before the device starts testing for temperature alarms to begin logging data. See Table 17 for the register bitmap. During a mission, there is only read access to these registers.

For a typical mission, the Mission Start Delay Counter is 0. If a mission is too long for a single DS1925 to store all readings at the selected sample rate, one can use several devices and set the Mission Start Delay for the second device to start recording as soon as the memory of the first device is full, and so on.

Mission Timestamp

The Mission Timestamp register indicates the date and time of the first temperature sample of the mission. There is only read access to the Mission Timestamp register. See Table 18 for the register bitmap.

Table 13. Alarm Status Register Bitmap

ADDR	b7	b6	b5	b4	b3	b2	b1	b0
0214h	BOR	1	1	1	0	0	THF	TLF

Table 14. Alarm Status Register Bit Descriptions

BIT	NAME	FUNCTION
b7	BOR	Battery On Reset Alarm. If this bit reads 1, the device has performed a power-on-reset or battery-fail event.
b1	THF	Temperature High Alarm Flag. If this bit reads 1, there was at least one temperature conversion during a mission revealing a temperature equal to or higher than the value in the Temperature High Alarm register. A forced conversion can affect the THF bit. This bit can also be set with the initial alarm in the SUTA = 1 mode.
b0	TLF	Temperature Low Alarm Flag. If this bit reads 1, there was at least one temperature conversion during a mission revealing a temperature equal to or lower than the value in the Temperature Low Alarm Register. A forced conversion can affect the TLF bit. This bit can also be set with the initial alarm in the SUTA = 1 mode.

Table 15. General Status Register Bitmap

ADDR	b7	b6	b5	b4	b3	b2	b1	b0
0215h	1	1	0	WFTA	MEMCLR	0	MIP	0

Table 16. General Status Register Bit Descriptions

BIT	NAME	FUNCTION
b4	WFTA	Waiting for Temperature Alarm. If this bit reads 1, the Mission Start Upon Temperature Alarm was selected and the XPC Start Mission command was successfully executed, but the device has not yet experienced the temperature alarm. This bit is cleared after a temperature alarm event, but is not affected by the XPC Clear Memory command. Once set, WFTA remains set if a mission is stopped before a temperature alarm occurs. To clear WFTA manually before starting a new mission, set the high temperature alarm (address 0209h) to -40°C and perform a forced conversion.
b3	MEMCLR	Memory Cleared. If this bit reads 1, the Mission Timestamp, Mission Samples Counter, as well as all the alarm flags of the Alarm Status register have been cleared in preparation of a new mission. Executing the XPC Clear Memory command with parameter byte 01h clears these memory sections. The MEMCLR bit returns to 0 as soon as a new mission is started by using the XPC Start Mission command. The memory must be cleared for a mission to start.
b1	MIP	Mission In Progress. If this bit reads 1, the device has been set up for a mission and this mission is still in progress. The MIP bit returns from logic 1 to logic 0 when a mission has ended. See the XPC Start Mission and XPC Stop Mission function commands.

Table 17. Mission Start Delay Counter Register Bitmap

ADDR	b7	b6	b5	b4	b3	b2	b1	b0
0216h	Delay Low Byte							
0217h	Delay Center Byte							
0218h	Delay High Byte							

Table 18. Mission Timestamp Register Bitmap

ADDR	b7	b6	b5	b4	b3	b2	b1	b0
0219h	LSByte Seconds							
021Ah	. . .							
021Bh	. . .							
021Ch	MSByte Seconds							

Mission Progress Indicator

Depending on settings in the Mission Control register (address 0213h), the DS1925 logs temperature in 8-bit or 16-bit format. The Mission Samples Counter register together with the starting address and the logging format (8 or 16 bits) provides the information to identify valid blocks of data that have been gathered during the current (MIP = 1) or latest mission (MIP = 0). See the *Data-Log Memory Usage* section for an illustration. See Table 19 for the register bitmap. There is only read access to this register.

The number read from the Mission Samples Counter indicates how often the DS1925 woke up during a mission to measure temperature. The number format is 24-bit unsigned integer. The Mission Samples Counter is reset through the XPC Clear Memory command

Other Indicators

The Device Samples Counter is similar to the Mission Samples Counter. During a mission this counter increments whenever the DS1925 wakes up to measure and log data and when the device is testing for a temperature alarm in SUTA mode. This way the Device Samples Counter functions like a gas gauge for the battery that powers the iButton device. There is only read access to this register.

The Device Samples Counter is reset to zero when the iButton device is assembled. The counter increments a couple of times during final test. The number format is 24-bit unsigned integer. The maximum number that can be represented in this format is 16777215.

The Device Configuration byte is used to allow the master to distinguish between the different versions of the iButton logger devices. Table 21 shows the codes assigned to the various devices. There is only read access to this register.

Security by Password

The DS1925 is designed to use two passwords that control read access and full access. Reading from or writing to the scratchpad as well as the XPC Forced Conversion command do not require a password. The password needs to be transmitted right after the command code of the memory or control function. If password checking is enabled, the password transmitted is compared to the passwords stored in the device. The data pattern stored in the Password Control register determines whether password checking is enabled. See Table 22 for the register bitmap. During a mission, there is only read access to this register.

Table 19. Mission Samples Counter Register Bitmap

ADDR	b7	b6	b5	b4	b3	b2	b1	b0
0220h	Low Byte							
0221h	Center Byte							
0222h	High Byte							

Table 20. Device Samples Counter Register Bitmap

ADDR	b7	b6	b5	b4	b3	b2	b1	b0
0223h	Low Byte							
0224h	Center Byte							
0225h	High Byte							

Table 21. Device Configuration Byte (0226h)

ADDR	b7	b6	b5	b4	b3	b2	b1	b0	DEVICE
0226h	0	0	0	0	0	0	0	0	DS2422
0226h	0	0	1	0	0	0	0	0	DS1923
0226h	0	1	0	0	0	0	0	0	DS1922L
0226h	0	1	1	0	0	0	0	0	DS1922T
0226h	1	0	0	0	0	0	0	0	DS1922E
0226h	1	0	1	0	0	0	0	0	DS1925

To enable password checking, set EPW to (AAh). The default pattern of EPW, and any value other than AAh allows the 64-bit read and 64-bit full access passwords to be set. Once password checking is enabled, changing the passwords and disabling password checking requires the knowledge of the current full-access password.

Before enabling password checking, passwords for read-only access and for full access (read/write/control) need to be written to the password registers. Setting up a password or enabling/disabling the password checking is done in the same way as writing data to a memory location, only the address is different. Because they are located in the same memory page, both passwords can be redefined at the same time.

The Read Access Password needs to be transmitted exactly in the sequence RP0, RP1 . . . RP62, RP63. This password only applies to XPC Read Memory function. The DS1925 delivers the requested data only if the password transmitted by the master was correct or if password checking is not enabled. See Table 23 for the Read Access Password Register bitmap. There is only write access to this register. Attempting to read the password reports all zeros. The password cannot be changed while a mission is in progress.

The Full Access Password needs to be transmitted exactly in the sequence FP0, FP1 . . . FP62, FP63. It affects the functions XPC Read Memory, XPC Copy Scratchpad, XPC Clear Memory, XPC Start Mission, and XPC Stop Mission. The DS1925 executes the command only if the password transmitted by the master was correct, or if password checking is not enabled. See Table 24 for the Full Access Password Register bitmap. There is only write access to this register. Attempting to read the password reports all zeros. The password cannot be changed while a mission is in progress.

Due to the special behavior of the write access logic, the Password Control register and both passwords must be written at the same time. When setting up new passwords, always verify (read back) the scratchpad before sending the XPC Copy Scratchpad command. After a new password is successfully copied from the scratchpad to its memory location, erase the scratchpad by filling it with new data (write scratchpad command). Otherwise, a copy of the passwords remain in the scratchpad for public read access.

Table 22. Password Control Register Bitmap

ADDR	b7	b6	b5	b4	b3	b2	b1	b0
0227h	EPW							

Table 23. Read Access Password Register Bitmap

ADDR	b7	b6	b5	b4	b3	b2	b1	b0
0228h	RP7	RP6	RP5	RP4	RP3	RP2	RP1	RP0
0229h	RP15	RP14	RP13	RP12	RP11	RP10	RP9	RP8
. . .	. . .							
022Eh	RP55	RP54	RP53	RP52	RP51	RP50	RP49	RP48
022Fh	RP63	RP62	RP61	RP60	RP59	RP58	RP57	RP56

Table 24. Full Access Password Register Bitmap

ADDR	b7	b6	b5	b4	b3	b2	b1	b0
0230h	FP7	FP6	FP5	FP4	FP3	FP2	FP1	FP0
0231h	FP15	FP14	FP13	FP12	FP11	FP10	FP9	FP8
. . .	. . .							
0236h	FP55	FP54	FP53	FP52	FP51	FP50	FP49	FP48
0237h	FP63	FP62	FP61	FP60	FP59	FP58	FP57	FP56

Data-Log Memory Usage

Once set up for a mission, the DS1925 logs the temperature measurements at equidistant time points entry after entry in its data-log memory. The data-log memory is able to store 125,440 entries in 8-bit format or 62,720 entries in 16-bit format (Figure 7). In 16-bit format, the higher 8 bits of an entry are stored at the lower address. Knowing the starting time point (Mission Timestamp) and the interval between temperature measurements, one can reconstruct the time and date of each measurement.

The contents of the Mission Samples Counter in conjunction with the sample rate and the Mission Timestamp then allows reconstructing the time points of all values stored in the data-log memory. This gives the exact history over time for the most recent measurements taken.

Missioning

The DS1925's typical task is recording temperature. Before the device can perform this function, it needs to be set up properly. This procedure is called missioning.

First, the DS1925 needs to have its RTC set to valid time and date. This reference time can be the local time, or, when used inside of a mobile unit, UTC/GMT (Coordinated Universal Time or Greenwich Mean Time) or any other time standard that was agreed upon. The RTC oscillator must be running (EOSC = 1). The memory assigned to store the Mission Timestamp, Mission Samples Counter, and Alarm Flags must be cleared using the memory clear command. To enable the device for a mission, the ETL bit must be set to 1. These are general settings that have to be made in any case, regardless of the type of object to be monitored and the duration of the mission.

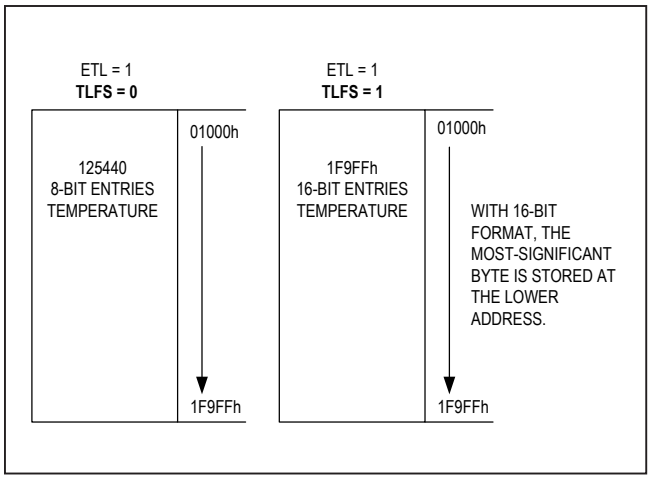


Figure 7. Temperature Logging

If alarm signaling is desired, the temperature alarm low and high thresholds must be defined. See the *Temperature Conversion* section on how to convert a temperature value into the binary code to be written to the threshold registers. In addition, the temperature alarm must be enabled for the low and/or high threshold. This makes the device respond to a Conditional Search ROM command (see the *1-Wire ROM Function Commands* section), provided that an alarming condition has been encountered.

The setting of the sample rate depends on the duration of the mission and the monitoring requirements. One should estimate the duration of the mission in minutes and divide the number by 125,440 (8-bit format) or 62,720 (16-bit format) to calculate the value of the sample rate (number of minutes between conversions). If the estimated duration of a mission is 300 days (= 432,000 minutes), for example, then the 122KB capacity of the data-log memory would be sufficient to store a new 11-bit value every 6.9 minutes (413 seconds). If the data-log memory of the DS1925 is not large enough to store all readings, one can use several devices and set the Mission Start Delay to values that make the second device start logging as soon as the memory of the first device is full, and so on.

After the Mission Start Delay is set, the sample rate needs to be written to the Sample Rate register. The sample rate may be any value from 1 to 16,383, coded as an unsigned 14-bit binary number. The fastest sample rate is one sample per 3 minutes (EHSS = 1, sample rate = 0B4h); however, the fasted recommended sample rate is 5 minutes and the slowest is one sample every 273.05 hours (EHSS = 0, Sample Rate = 3FFFh). To get one sample every 6 minutes, for example, the sample rate value needs to be set to 6 (EHSS = 0) or 360 decimal (equivalent to 0168h at EHSS = 1).

If there is a risk of unauthorized access to the DS1925 or manipulation of data, one should define passwords for read access and full access. Before the passwords become effective, their use needs to be enabled. See the *Security by Password* section for more details.

The last step to begin a mission is to issue the XPC Start Mission command. As soon as it has received this command, the DS1925 sets the MIP flag and clears the MEMCLR flag. With the immediate/delayed start mode (SUTA = 0), after as many minutes as specified by the Mission Start Delay are over, the device wakes up, copies the current date and time to the Mission Timestamp register, and logs the first entry of the mission. This increments both the Mission Samples Counter and Device Samples Counter. All subsequent log entries are made as specified by the value in the Sample Rate register and the EHSS bit.

If the Start Upon Temperature Alarm mode is chosen (SUTA = 1) and temperature logging is enabled (ETL = 1), the DS1925 first waits until the start delay is over. Then the device wakes up in intervals as specified by the sample rate and EHSS bit and measure the temperature. This increments the Device Samples Counter and Mission Samples Counter. The first sample of the mission is logged when the temperature alarm occurred. All subsequent log entries are made as specified by the value in the Sample Rate register and the EHSS bit.

The general-purpose memory operates independently of the other memory sections and is not write protected during a mission. All the DS1925's memory can be read at any time, i.e., to watch the progress of a mission. Attempts to read the passwords read FFh bytes instead of the data that is stored in the password registers.

Memory Access

Address Registers and Transfer Status

Because of the serial data transfer, the DS1925 employs three address registers: TA1, TA2, and E/S (Figure 8). Registers TA1 and TA2 must be loaded with the target address to which the data are written or from which data are sent to the master upon a Read command. Register E/S acts like a byte counter and transfer status register. It is used to verify data integrity with Write commands. Therefore, the master only has read access to this register. The lower 5 bits of the E/S register indicate the address of the last byte that has been written to the scratchpad. This address is called Ending Offset. Bit 5 of the E/S register, called PF or "partial byte flag," is set if the number of data bits sent by the master is not an integer multiple of 8. Bit 6 is always a 0. Note that the lowest 5 bits of the target address also determine the address within the scratchpad, where intermediate storage of data begins. This address is called byte offset. If the target address for a write command is 13Ch, for example, then the scratchpad stores incoming data beginning at the byte offset 1Ch and is full after only 4 bytes. The corresponding ending offset in this example is 1Fh. For best economy of speed and efficiency, the target address for writing should point to the beginning of a page, i.e., the byte offset is 0. Thus, the full 32-byte capacity of the scratchpad is available, resulting also in the ending offset of 1Fh. The ending offset together with the PF is mainly a means to support the master checking the data integrity after a write command. The highest valued bit of the E/S Register, called AA or "authorization accepted," indicates that a valid copy command for the scratchpad has been received and executed. Writing data to the scratchpad clears this flag.

Writing with Verification

To write data to the DS1925, the scratchpad has to be used as intermediate storage. First, the master issues the Write Scratchpad command to specify the desired target address, followed by the data to be written to the scratchpad. In the next step, the master sends the Read Scratchpad command to read the scratchpad and to verify data integrity. As preamble to the scratchpad data, the DS1925 sends the requested target address TA1 and TA2 and the contents of the E/S Register. If the PF flag is set, data did not arrive correctly in the scratchpad. The

BIT	7	6	5	4	3	2	1	0
TARGET ADDRESS (TA1)	T7	T6	T5	T4	T3	T2	T1	T0
TARGET ADDRESS (TA2)	T15	T14	T13	T12	T11	T10	T9	T8
ENDING ADDRESS WITH DATA STATUS (E/S) (READ ONLY)	AA	0	PF	E4	E3	E2	E1	E0

Figure 8. Address Registers

master does not need to continue reading; it can start a new trial to write data to the scratchpad. Similarly, a set AA flag indicates that the Write command was not recognized by the device. If everything went correctly, both flags are cleared and the ending offset indicates the address of the last byte written to the scratchpad. Now the master can continue verifying every data bit. After the master has verified the data, it has to use the XPC Copy Scratchpad command. This command sequence uses the three address registers TA1, TA2, and E/S as the master has read them verifying the scratchpad. As soon as the XPC Copy Scratchpad starts, it copies the data to the requested location beginning at the target address.

Memory and Control Function Commands

Figure 9 describes the protocols necessary for accessing the memory and the special function registers of the DS1925. See the *Mission Example: Prepare and Start a New Mission* section for how to use these and other functions to set up the DS1925 for a mission. The communication between master and DS1925 takes place either at standard speed (default, OD = 0) or at overdrive speed (OD = 1). If not explicitly set into the overdrive mode, the DS1925 assumes standard speed. Internal memory access during a mission has priority over external access through the 1-Wire interface. This affects several of the commands described below. See the *Memory Access Conflicts* section for details and remedies.

Write Scratchpad Command [0Fh]

After issuing the Write Scratchpad command, the master must first provide the 2-byte target address, followed by the data to be written to the scratchpad. The data is written to the scratchpad starting at the byte offset (T[4:0]).

When executing the Write Scratchpad command, the CRC generator inside the DS1925 (see Figure 15) calculates a CRC of the entire data stream, starting at the command code and ending at the last data byte sent by the master. This CRC is generated using the CRC-16 polynomial by first clearing the CRC generator and then shifting in the command code (0Fh) of the Write Scratchpad command, the target addresses TA1 and TA2 as supplied by the master and all the data bytes. If the ending offset is 11111b, the master may send 16 read time slots and receive the inverted CRC-16 generated by the DS1925.

Note that both register pages are write protected during a mission. Although the Write Scratchpad command works normally at any time, the subsequent XPC Copy Scratchpad to a register page fails during a mission.

Read Scratchpad Command [AAh]

This command is used to verify scratchpad data and target address. After issuing the Read Scratchpad command, the master begins reading. The first 2 bytes are the target address. The next byte is the ending offset/data status byte (E/S) followed by the scratchpad data beginning at the byte offset (T4:T0), as shown in Figure 8. The master may continue reading data until the end of the scratchpad after which it receives an inverted CRC-16 of the command code, target addresses TA1 and TA2, the E/S byte, and the scratchpad data starting at the target address. After the CRC is read, the bus master reads logical 1s from the DS1925 until a reset pulse is issued.

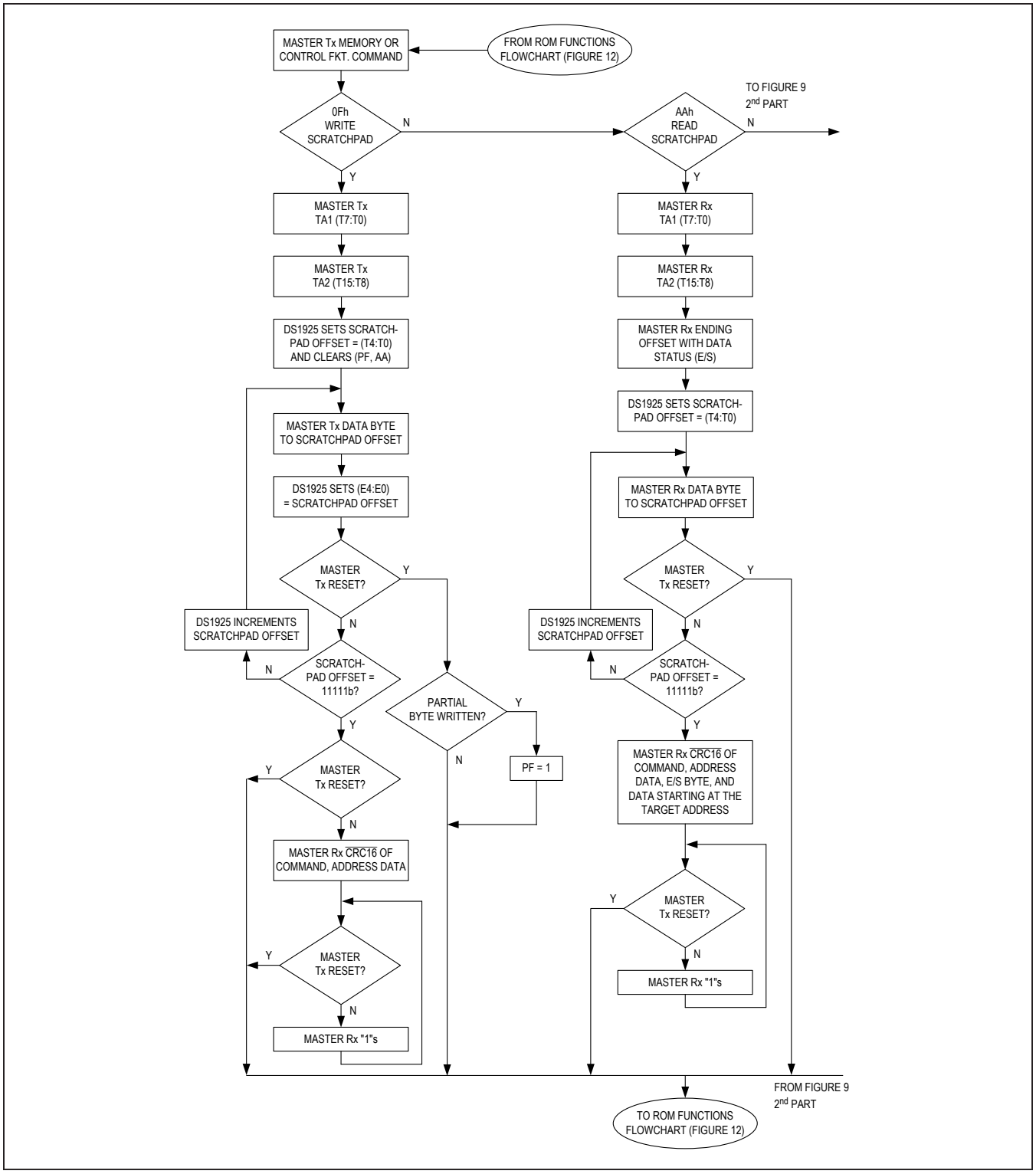


Figure 9a. Memory/Control Function Flowchart- XPC Sub-Commands Flowchart

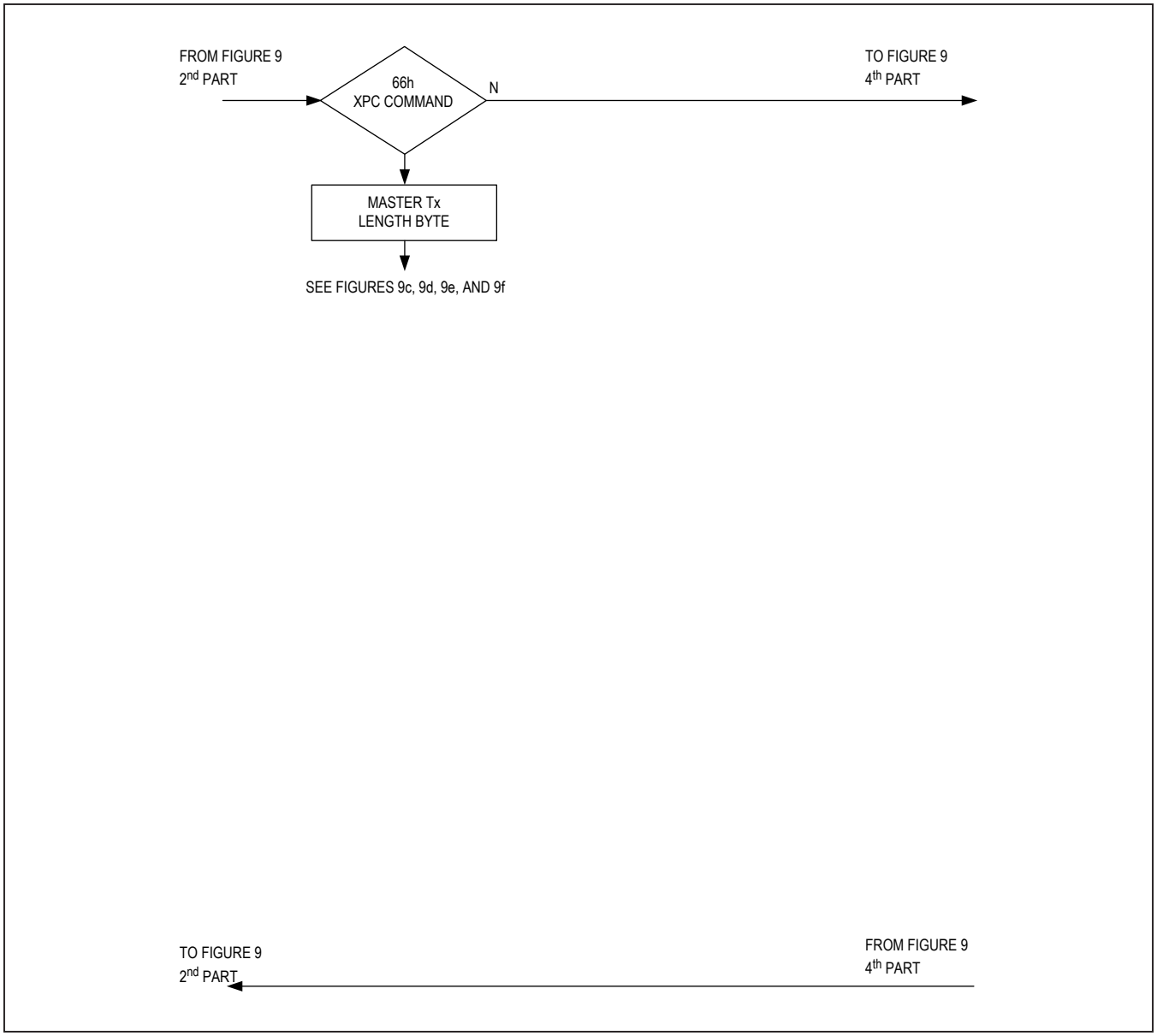


Figure 9b. Memory/Control Function Flowchart—XPC Subcommands Flowchart (continued)

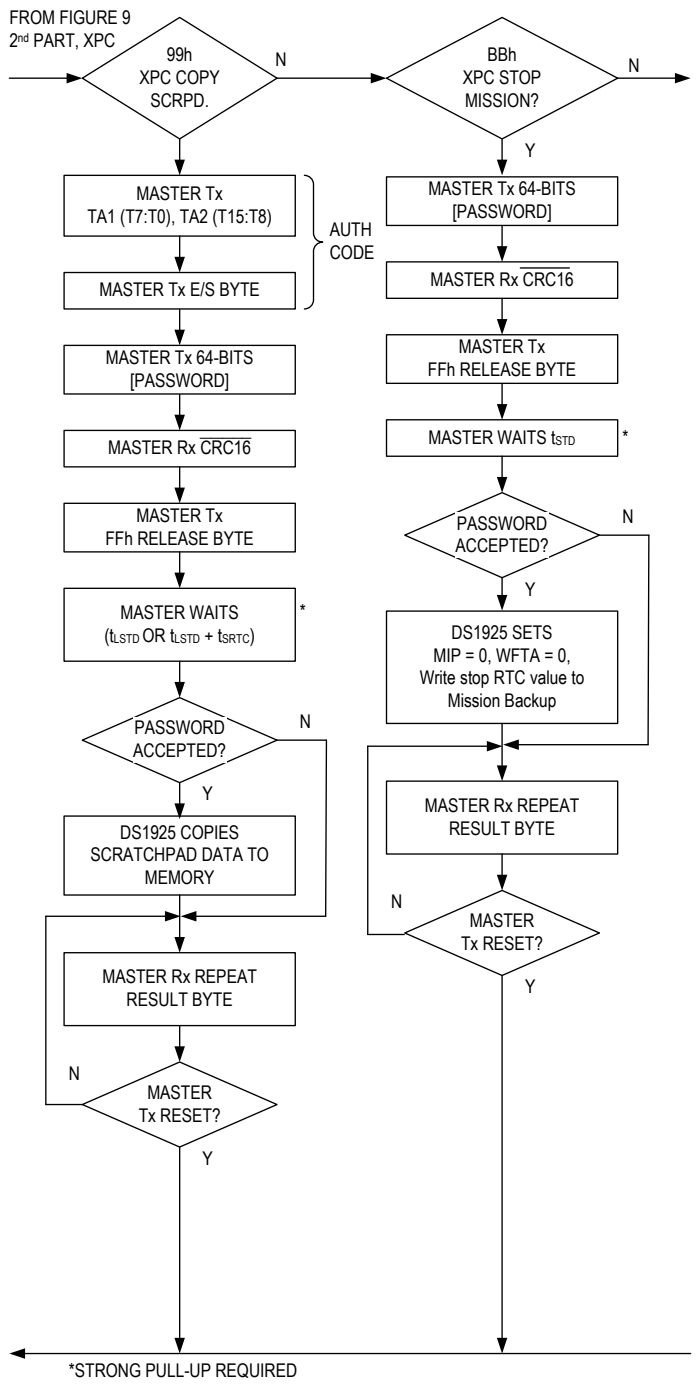


Figure 9c. Memory/Control Function Flowchart—XPC Subcommands Flowchart (continued)

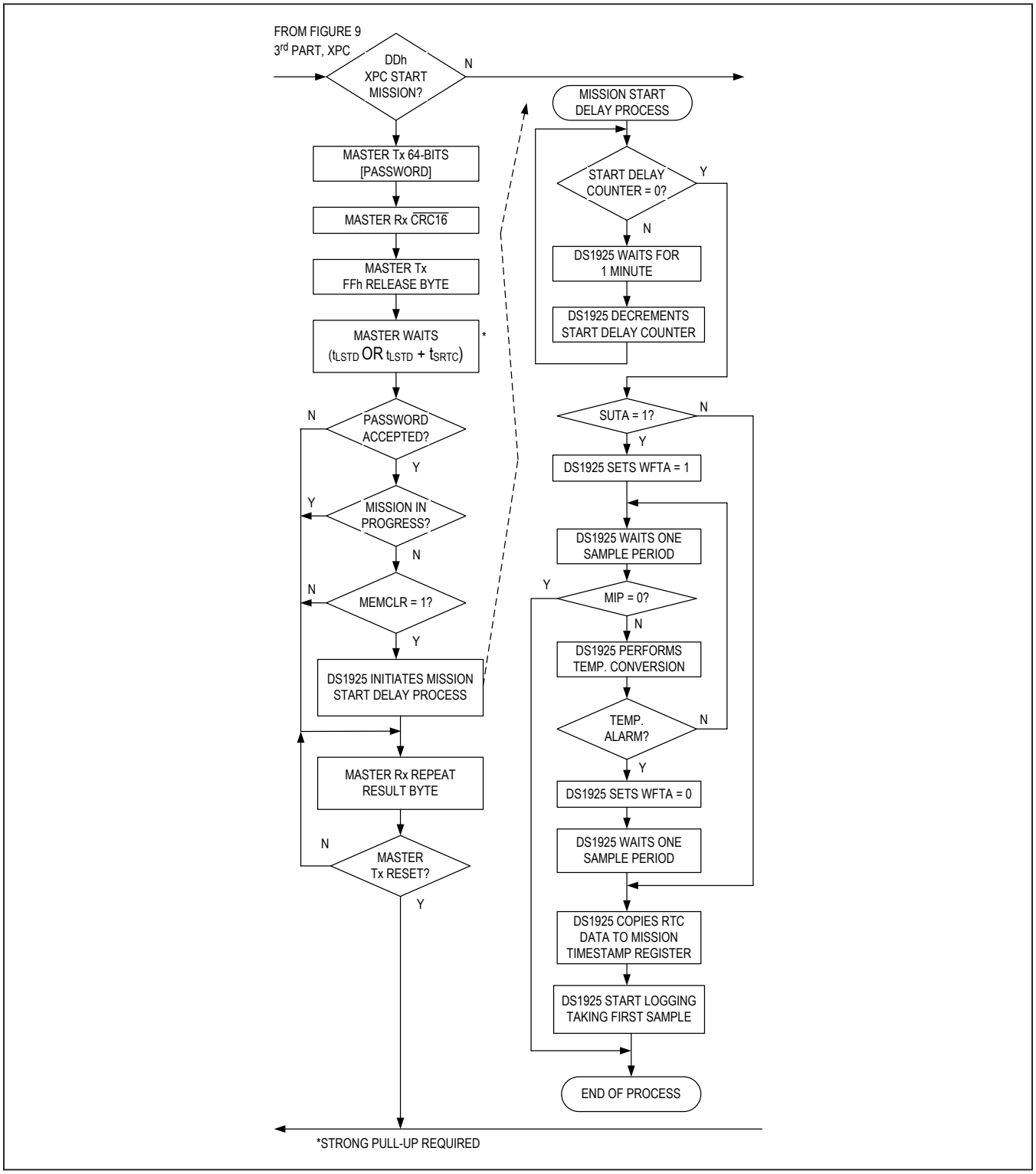


Figure 9d. Memory/Control Function Flowchart (continued)

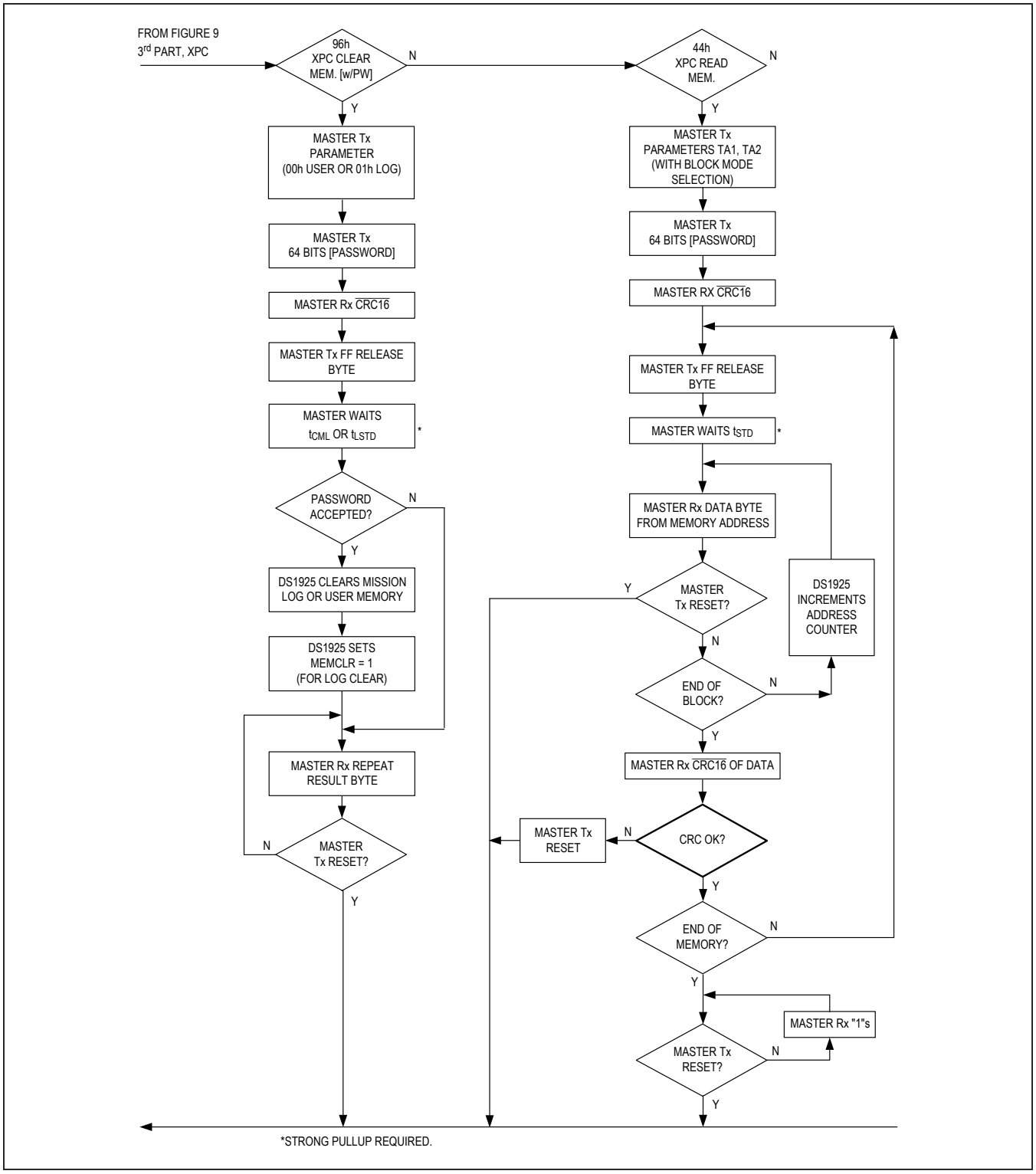


Figure 9e. Memory/Control Function Flowchart— XPC Sub-Commands Flowchart