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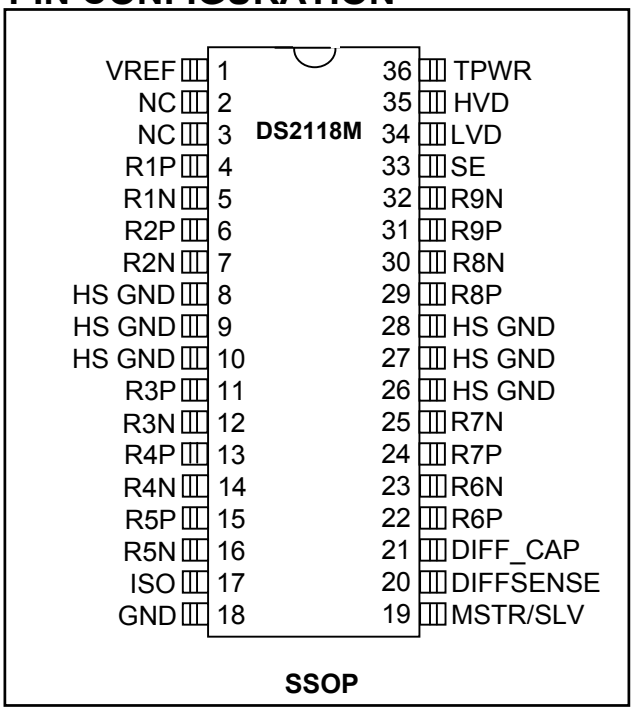
DS2118M
Ultra3 LVD/SE SCSI Terminator

www.maxim-ic.com

FEATURES

- Fully Compliant with SCSI SPI-2, SPI-3, SPI-4, Ultra160, and Ultra320
- Provides Multimode Low-Voltage Differential/Single-Ended (LVD/SE) Termination for Nine Signal Line Pairs
- Autoselection of LVD or SE Termination
- 5% Tolerance on SE and LVD Termination Resistance
- Low Power-Down Capacitance of 3pF
- On-Board Thermal Shutdown Circuitry
- SCSI Bus Hot-Plug Compatible
- Fully Supports Actively Negated SE SCSI Signals

PIN CONFIGURATION



SSOP

ORDERING INFORMATION

PART	VOLTAGE (V)	TEMP RANGE	PIN-PACKAGE	TOP MARK*
DS2118MB	5	0°C to +70°C	36 SSOP (0.300")	DS2118MB
DS2118MB+	5	0°C to +70°C	36 SSOP (0.300")	DS2118MB
DS2118MB/T&R	5	0°C to +70°C	36 SSOP (0.300")/Tape and Reel	DS2118MB
DS2118MB+T&R	5	0°C to +70°C	36 SSOP (0.300")/Tape and Reel	DS2118MB

+ Denotes a lead-free/RoHS-compliant package.
** The top mark includes a "+" on lead-free packages.*

DETAILED DESCRIPTION

The DS2118M Ultra3 LVD/SE SCSI terminator is both a low-voltage differential (LVD) and single-ended (SE) terminator. The multimode operation enables the designer to implement LVD in current products while allowing the end-user SE-backward compatibility with legacy devices. If the device is connected in an LVD-only bus, the DS2118M will use LVD termination. If any SE devices are connected to the bus, the DS2118M will use SE termination. This is accomplished automatically inside the part by sensing the voltage on the SCSI bus DIFFSENS line.

For the LVD termination, the DS2118M integrates two current sources with nine precision resistor strings. For the SE termination, one regulator and nine precision 110Ω resistors are used. Three DS2118M terminators are needed for a wide SCSI bus.

REFERENCE DOCUMENTS

Small Computer Systems Interface (SCSI-3)	SCSI Parallel Interface (SPI)	Project: 0855-M, 1995
Small Computer Systems Interface (SCSI-3)	SCSI Parallel Interface 2 (SPI-2)	Project: 1142-M, 1998
Small Computer Systems Interface (SCSI-3)	SCSI Parallel Interface 3 (SPI-3)	Project: 1302-D, 1999
Small Computer Systems Interface (SCSI-3)	SCSI Parallel Interface 4 (SPI-4)	Project: 1365-D, 200x

Available From:

American National Standards Institute (ANSI) Phone: (212) 642-4900

Global Engineering Documents 15 Inverness Way East; Englewood, CO 80112 Phone: (800) 854-7179

FUNCTIONAL DESCRIPTION

The DS2118 combines LVD and SE termination with DIFFSENSE sourcing and detection.

A bandgap reference is fed into two amplifiers, which creates a 1.25V reference voltage and a 2.85V reference voltage. The control logic determines which of these references will be applied to the termination resistors. If the SCSI bus is in LVD mode, then the 1.25V reference will be used. If the SCSI bus is in SE mode, then the 2.85V reference will be used. That same control logic will switch in/out parallel resistors to change the total termination resistance accordingly. Finally, in SE mode the Rp pins will be switched to ground.

The DIFFSENSE circuitry decodes trinary logic. There will be one of three voltages on the SCSI control line called DIFFSENS. Two comparators and a NAND gate determine if the voltage is below 0.6V, above 2.15V, or in between. That indicates the mode of the bus to be HVD, SE, or LVD, respectively.

The DS2118M's DIFF_CAP pin monitors the DIFFSENS line to determine the proper operating mode of the device; this mode is indicated by the SE/LVD/HVD outputs. The DIFFSENSE pin can also drive the SCSI DIFFSENS line (when MSTR/SLV = 1) to determine the SCSI bus operating mode. The DS2118M switches to the termination mode that is appropriate for the bus based on the value of the DIFFSENS voltage. These modes are:

- **LVD Mode:** LVD termination is provided by a precision laser-trimmed resistor string with two amplifiers. This configuration yields a 105Ω differential and 150Ω common-mode impedance. A fail-safe bias of 112mV is maintained when no drivers are connected to the SCSI bus.

- **SE Mode:** When the external driver for a given signal line turns off, the active terminator will pull that signal line to 2.85V (quiescent state). When used with an active negation driver, the power amp can sink 22mA per line while keeping the voltage reference in regulation. The terminating resistors maintain their 110Ω value.

- **HVD Isolation Mode:** The DS2118M identifies that there is an HVD (high-voltage differential) device on the SCSI bus and isolates the termination pins from the bus.

When ISO is pulled high, the termination pins are isolated from the SCSI bus, V_{REF} remains active, and the bus mode indicators (SE/LVD/HVD) remain active. During thermal shutdown, the termination pins are isolated from the SCSI bus, V_{REF} becomes high impedance, and the bus mode indicators (SE/LVD/HVD) remain active. The DIFFSENSE driver is shut down during either of these two events. An internal pulldown resistor assures that the DS2118M will be terminating the bus if the ISO pin is left floating.

To ensure proper operation, the TPWR pin should be connected to the SCSI bus TERMPWR line. As with all analog circuitry, the TERMPWR and V_{DD} lines should be bypassed locally. A 2.2µF capacitor and a 0.01µF high-frequency capacitor is recommended between TPWR and ground and placed as close as possible to the DS2118M. The DS2118M should be placed as close as possible to the SCSI connector to minimize signal and power-trace length, thereby resulting in less input capacitance and reflections, which can degrade the bus signals.

To maintain the specified regulation, a 4.7µF capacitor is required between the V_{REF} pin (VREF) and ground of each DS2118M. A high frequency cap (0.1µF ceramic recommended) can also be placed on the

V_{REF} pin in applications that use fast rise/fall time drivers. A typical SCSI bus configuration is shown in Figure 2.

NOTES:

1) DIFFSENS. Refers to the SCSI bus signal.
2) DIFFSENSE. Refers to the DS2118M pin name and internal circuitry capable of driving the DIFFSENS line.
3) DIFF_CAP. Refers to the DS2118M pin name and internal circuitry relating to monitoring the DIFFSENS line.

Figure 1. DS2118M Block Diagram

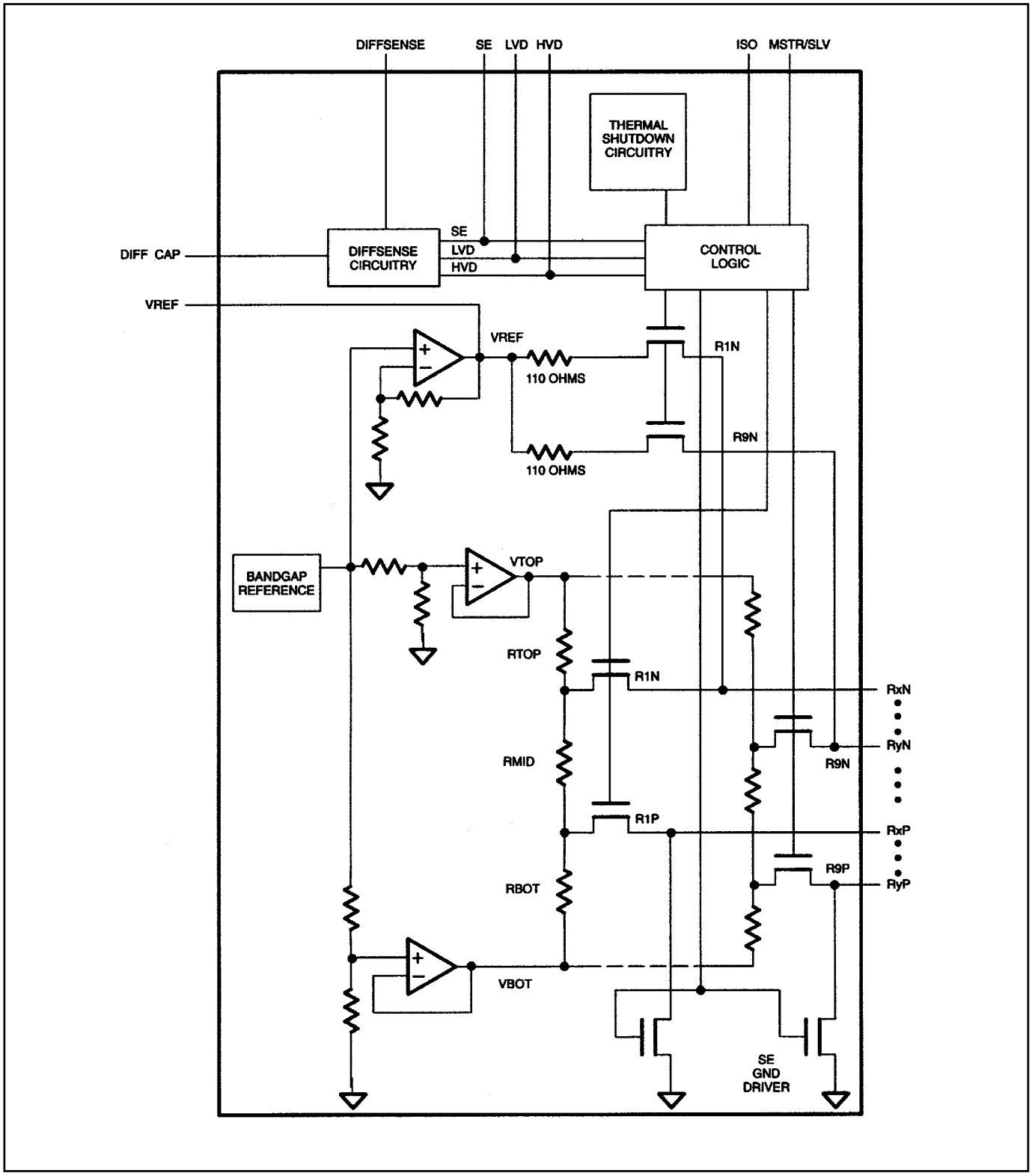
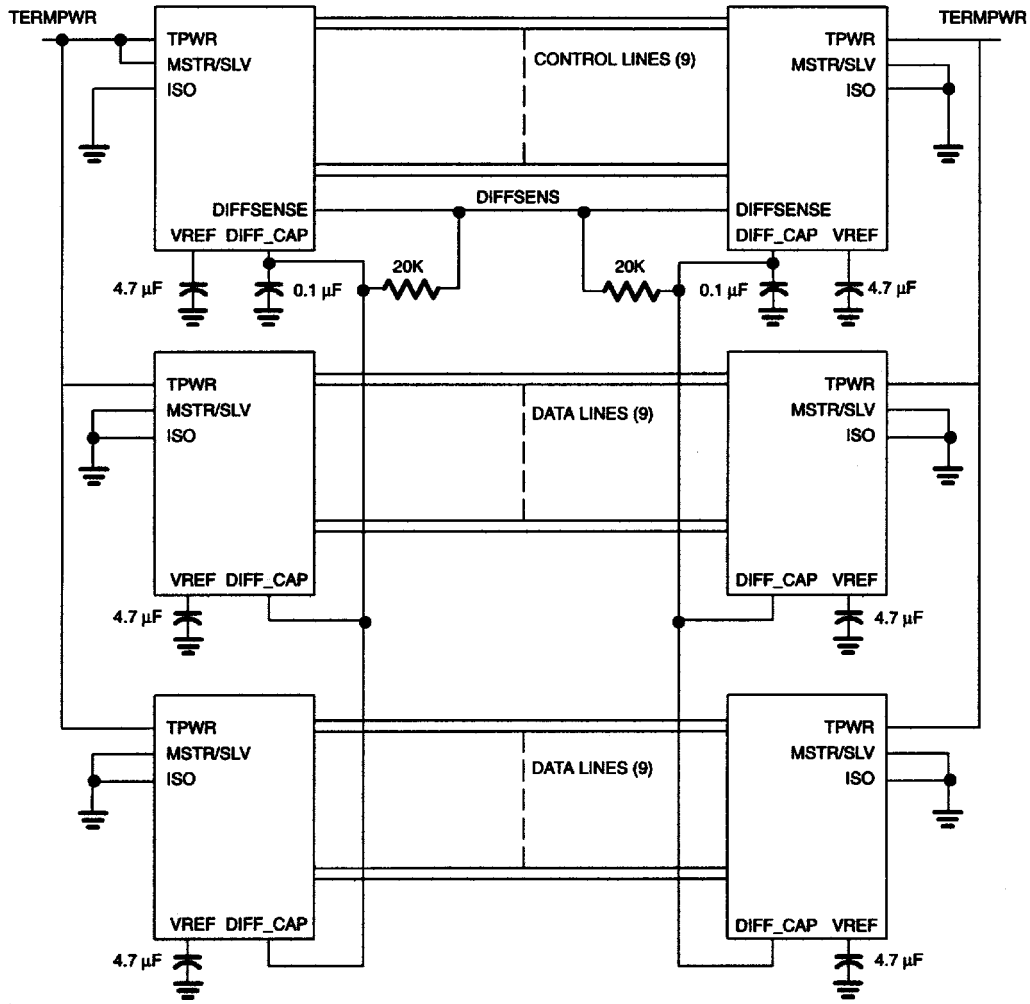


Figure 2. SCSI Bus Configuration



PIN DESCRIPTION

PIN	NAME	FUNCTION
1	VREF	**Reference Voltage.** 2.85V reference in SE mode and 1.25V reference in LVD mode; must be decoupled with a 4.7µF cap.
2, 3	NC	**No Connection.** Do not connect these pins.
4–7, 11–16, 22–25, 29–32	RxP, RxN	**Signal Termination.** Connect to SCSI bus signal lines.
8, 10, 26, 9, 28, 27	HS GND	**Heat Sink Ground.** Internally connected to the mounting pad. Should be grounded.
17	ISO	**Isolation.** When pulled high, the DS2118M isolates its bus pins (RxP, FxP) from the SCSI bus.
18	GND	**Ground.** Signal ground; 0V.
19	MSTR/SLV	**Master/Slave.** Mode-select for the noncontrolling terminator. When pulled high (MSTR), the DIFFSENSE driver is enabled.
20	DIFFSENSE	**DIFFSENSE.** Output to drive the SCSI bus DIFFSENS line.
21	DIFF_CAP	**DIFFSENSE Capacitor.** Connect 0.1µF capacitor for DIFFSENSE filter. Input to detect the type of device (differential or single-ended) on the SCSI bus.
33	SE	**Single-Ended.** SE output of DIFFSENSE receiver; indicates SE bus operation.
34	LVD	**Low-Voltage Differential.** LVD output of DIFFSENSE receiver; indicates LVD bus operation.
35	HVD	**High-Voltage Differential.** HVD output of DIFFSENSE receiver; indicates HVD bus operation or thermal shutdown.
36	TPWR	**Termination Power.** Connect to the SCSI TERMPWR line and decouple with 2.2µF capacitor.

RECOMMENDED OPERATING CONDITIONS

PARAMETER		SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Termpower Voltage	SE Mode	$V_{TPWR(SE)}$	4.0		5.5	V	
	LVD Mode	$V_{TPWR(LVD)}$	2.7		5.5	V	
Logic 0		V_{IL}	-0.3		+0.8	V	
Logic 1		V_{IH}	2.0		V_{TPWR} + 0.3	V	
Operating Temperature		V_{AMB}	0		70	°C	

SINGLE-ENDED CHARACTERISTICS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
SE Termination Resistance	R_{SE}	104.5	110	115.5	Ω	1
SE Voltage Reference	V_{REF}	2.7		3.0	V	
SE Output Current	I_{OSE}			25.4	mA	2
Output Capacitance	C_{OUT}			3	pF	3

LOW-VOLTAGE DIFFERENTIAL CHARACTERISTICS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Differential Mode Termination Resistance	R_{DM}	100		110	Ω	
Common Mode Termination Resistance	R_{CM}	110		190	Ω	
Differential Mode Bias	V_{DM}	100		125	mV	4
Common Mode Bias	V_{CM}	1.125		1.375	V	

DC CHARACTERISTICS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Termpower Current	I_{TPMR}		12		mA	4
Input Leakage High	I_{IH}	-1.0			µA	
Input Leakage Low	I_{IL}			1.0	µA	
Output Current High	I_{OH}	-1.0			mA	5, 7
Output Current Low	I_{OL}	4.0			mA	6, 7
DIFFSENS SE Operating Range	V_{SEOR}	-0.3		0.5	V	
DIFFSENS LVD Operating Range	V_{LVDOR}	0.7		1.9	V	
DIFFSENS HVD Operating Range	V_{HVDOR}	2.4		V_{TPWR} + 0.3	V	
DIFFSENSE Driver Output Voltage	V_{DSO}	1.2		1.4	V	8, 9
DIFFSENSE Driver Source Current	I_{DSH}	5		15	mA	8, 10, 12
DIFFSENSE Driver Sink Current	I_{DSL}	20		200	µA	8, 11
Thermal Shutdown			150		ºC	3

REGULATOR CHARACTERISTICS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Line Regulation	LI_{REG}		1.0	2.5	%	
Load Regulation	LO_{REG}		1.3	3.5	%	
Current Limit	I_{LIM}		550		mA	
Sink Current	I_{SINK}	200			mA	

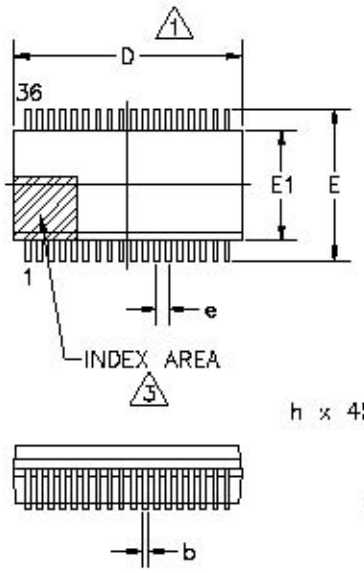
NOTES:

1) V_{LINE} = 0V to 3V.
2) V_{LINE} = 0.2V.
3) Guaranteed by design.
4) All lines open.
5) V_{OUT} = 2.4V.
6) V_{OUT} = 0.4V.
7) SE/LVD/HVD pins only.
8) MSTR/SLV = 1.
9) I_{DS} = 0mA to 5mA.
10) V_{DSO} = 0V.
11) V_{DSO} = 2.75V.
12) TPWR = 5.5V.

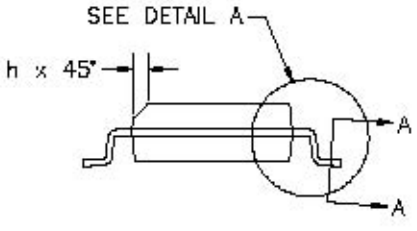
PACKAGE INFORMATION

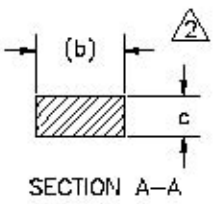
(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/DallasPackInfo**.)

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
A	NEW DRAWING	1/97	

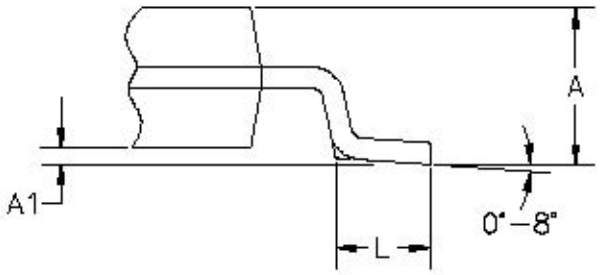


1. DIMENSIONS D AND E1 INCLUDE MOLD MISMATCH, BUT DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.254 MM PER SIDE.
2. SECTION A–A DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.13 TO 0.25 MM FROM THE LEAD TIP.
3. THE CHAMFER ON THE BODY IS OPTIONAL. IF IT IS NOT PRESENT, A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE CROSS–HATCHED AREA.





DIM	MIN	MAX
A	2.44	2.64
A1	0.12	–
b	0.29	0.43
c	0.23	0.32
D	15.20	15.54
E	10.11	10.52
E1	7.40	7.60
e	0.80 BSC	
h	0.25	0.71
L	0.51	1.02



DETAIL A

DIMENSIONS ARE IN MILLIMETERS

SIGNATURE	DATE
DOC. CONTROL:	
ENGR. MGR:	
MFG. ENGR:	
CHECKED BY:	
DRAWN BY: R.W.E.	1/97
DO NOT SCALE DWG.	

DALLAS SEMICONDUCTOR MAXIM

TITLE: MARKETING OUTLINE, 36 LEAD SSOP 7.5 MM BODY, .80 MM LEAD PITCH

SIZE	FSCM NO	PART NO.	REV
A		56–G2007–001	A

SCALE N/A SHEET 1 OF 1