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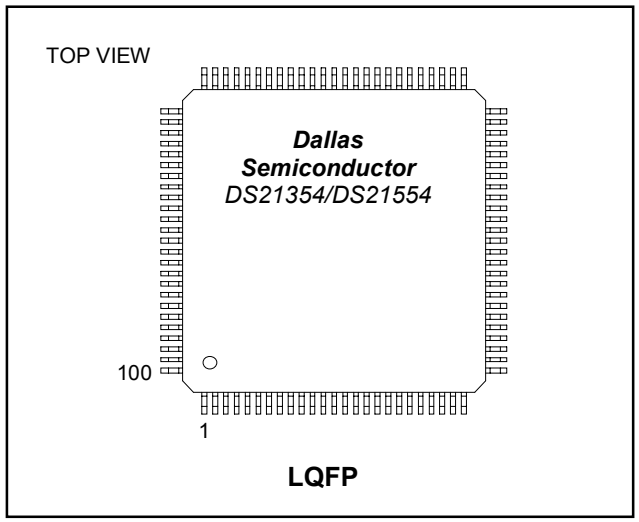
DS21354/DS21554
3.3V/5V E1 Single-Chip Transceivers

www.maxim-ic.com

GENERAL DESCRIPTION

The DS21354/DS213554 single-chip transceivers (SCTs) contain all the necessary functions to connect to E1 lines. The devices are upward-compatible versions of the DS2153 and DS2154 SCTs. The on-board clock/data recovery circuitry coverts the AMI/HDB3 E1 waveforms to an NRZ serial stream. Both devices automatically adjust to E1 22AWG (0.6mm) twisted-pair cables from 0 to over 2km in length. They can generate the necessary G.703 waveshapes for both 75Ω coax and 120Ω twisted cables. The on-board jitter attenuator (selectable to either 32 bits or 128 bits) can be placed in either the transmit or receive data paths. The framer locates the frame and multiframe boundaries and monitors the data stream for alarms. It is also used for extracting and inserting signaling data, Si, and Sa-bit information. The on-board HDLC controller can be used for Sa-bit links or DS0s. The devices contain a set of internal registers that the user can access to control the operation of the units. Quick access through the parallel control port allows a single controller to handle many E1 lines. The devices fully meet all the latest E1 specifications, including ITU-T G.703, G.704, G.706, G.823, G.732, and I.431, ETS 300 011, 300 233, and 300 166, as well as CTR12 and CTR4.

PIN CONFIGURATION



FEATURES

- Complete E1 (CEPT) PCM-30/ISDN-PRI Transceiver Functionality
- On-Board Long- and Short-Haul Line Interface for Clock/Data Recovery and Waveshaping
- 32-Bit or 128-Bit Crystal-Less Jitter Attenuator
- Frames to FAS, CAS, CCS, and CRC4 Formats
- Integral HDLC Controller with 64-Byte Buffers Configurable for Sa Bits, DS0, or Sub-DS0 Operation
- Dual Two-Frame Elastic Store Slip Buffers that can Connect to Asynchronous Backplanes up to 8.192MHz
- Interleaving PCM Bus Operation
- 8-Bit Parallel Control Port that can be used Directly on Either Multiplexed or Nonmultiplexed Buses (Intel or Motorola)
- Extracts and Inserts CAS Signaling
- Detects and Generates Remote and AIS Alarms
- Programmable Output Clocks for Fractional E1, H0, and H12 Applications
- Fully Independent Transmit and Receive Functionality
- Full Access to Si and Sa Bits Aligned with CRC-4 Multiframe
- Four Separate Loopback Functions for Testing Functions
- Large Counters for Bipolar and Code Violations, CRC4 Codeword Errors, FAS Word Errors, and E Bits
- IEEE 1149.1 JTAG-Boundary Scan Architecture
- Pin Compatible with DS2154/52/352/552 SCTs
- 3.3V (DS21354) or 5V (DS21554) Supply; Low-Power CMOS
- 100-pin LQFP package (14mm x 14mm)

ORDERING INFORMATION

PART	TEMP RANGE	PIN-PACKAGE
DS21354L	0°C to +70°C	100 LQFP
DS21354LN	-40°C to +85°C	100 LQFP
DS21554L	0°C to +70°C	100 LQFP
DS21554LN	-40°C to +85°C	100 LQFP

Note: *Some revisions of this device may incorporate deviations from published specifications known as errata. Multiple revisions of any device may be simultaneously available through various sales channels. For information about device errata, click here: www.maxim-ic.com/errata.*

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1. INTRODUCTION

The DS21354/DS21554 are superset versions of the popular DS2153 and DS2154 SCTs offering the new features listed below. All the original features of the DS2153 and DS2154 have been retained, and the software created for the original devices is transferable into the DS21354/DS21554.

New Features in the DS21354 and DS21554

FEATURE	SECTION
HDLC controller with 64-Byte Buffers for Sa Bits or DS0s or Sub DS0s	14
Interleaving PCM Bus Operation	17
IEEE 1149.1 JTAG-Boundary Scan Architecture	16
3.3V (DS21354 Only) Supply	1.1 and 2
Line Interface Support for the G.703 2.048 Synchronization Interface	15
Customer Disconnect Indication (...101010...) Generator	5.6
Open-Drain Line Driver Option	5.6

Additional Features in the DS21354 and DS21554

FEATURE	SECTION
Option for nonmultiplexed bus operation	1.1 and 20.2
Crystal-less jitter attenuation	15.3
Additional hardware signaling capability including: Receive signaling reinsertion to a backplane multiframe sync Availability of signaling in a separate PCM data stream Signaling freezing Interrupt generated on change of signaling data	9
Improved receive sensitivity: 0 to -43dB	1.1
Per-channel code insertion in both transmit and receive paths	10
Expanded access to Sa and Si bits	13
RCL, RLOS, RRA, and RAIS alarms now interrupt on change of state	6
8.192MHz clock synthesizer	1.1
Per-channel loopback	10
Addition of hardware pins to indicate carrier loss and signaling freeze	1.1
Line interface function can be completely decoupled from the framer/formatter to allow: Interface to optical, HDSL, and other NRZ interfaces “tap” the transmit and receive bipolar data streams for monitoring purposes Be able to corrupt data and insert framing errors, CRC errors, etc.	1.1
Transmit and receive elastic stores now have independent backplane clocks	1.1
Ability to monitor one DS0 channel in both the transmit and receive paths	8
Access to the data streams in between the framer/formatter and the elastic stores	1.1
AIS generation in the line interface that is independent of loopbacks	1.1 and 5
Transmit current limiter to meet the 50mA short circuit requirement	15
Option to extend carrier loss criteria to a 1ms period as per ETS 300 233	5.4
Automatic RAI generation to ETS 300 011 specifications	5.4

1.1. Functional Description

The analog AMI/HDB3 waveform off the E1 line is transformer coupled into the RRING and RTIP pins of the DS21354/554. The device recovers clock and data from the analog signal and passes it through the jitter attenuation mux to the receive-side framer where the digital serial stream is analyzed to locate the framing/multiframe pattern. The DS21354/DS21554 contain an active filter that reconstructs the analog-received signal for the nonlinear losses that occur in transmission. The devices have a usable receive sensitivity of 0 to -43dB, which allows the device to operate on cables over 2km in length. The receive-side framer locates FAS frame and CRC and CAS multiframe boundaries as well as detects incoming alarms including, carrier loss, loss of synchronization, AIS, and Remote Alarm. If needed, the receive-side elastic store can be enabled to absorb the phase and frequency differences between the recovered E1 data stream and an asynchronous backplane clock, which is provided at the RSYSCLK input. The clock applied at the RSYSCLK input can be either a 2.048MHz/4.096MHz/8.192MHz clock or a 1.544MHz clock.

The transmit-side framer is totally independent from the receive side in both the clock requirements and characteristics. Data off a backplane can be passed through a transmit-side elastic store if necessary. The transmit formatter provides the necessary frame/multiframe data overhead for E1 transmission.

Reader's Note: This data sheet assumes a particular nomenclature of the E1 operating environment. In each 125µs frame, there are 32 eight-bit time slots numbered 0 to 31. Time slot 0 is transmitted first and received first. These 32 time slots are also referred to as channels with a numbering scheme of 1 to 32. Time slot 0 is identical to channel 1, time slot 1 is identical to Channel 2, and so on. Each time slot (or channel) is made up of eight bits, which are numbered 1 to 8. Bit number 1 is the most significant bit (MSB) and is transmitted first. Bit number 8 is the least significant bit (LSB) and is transmitted last. The term "locked" refers to two clock signals that are phase or frequency locked, or derived from a common clock (i.e., a 1.544MHz clock may be locked to a 2.048MHz clock if they share the same 8kHz component). Throughout this data sheet, the following abbreviations are used:

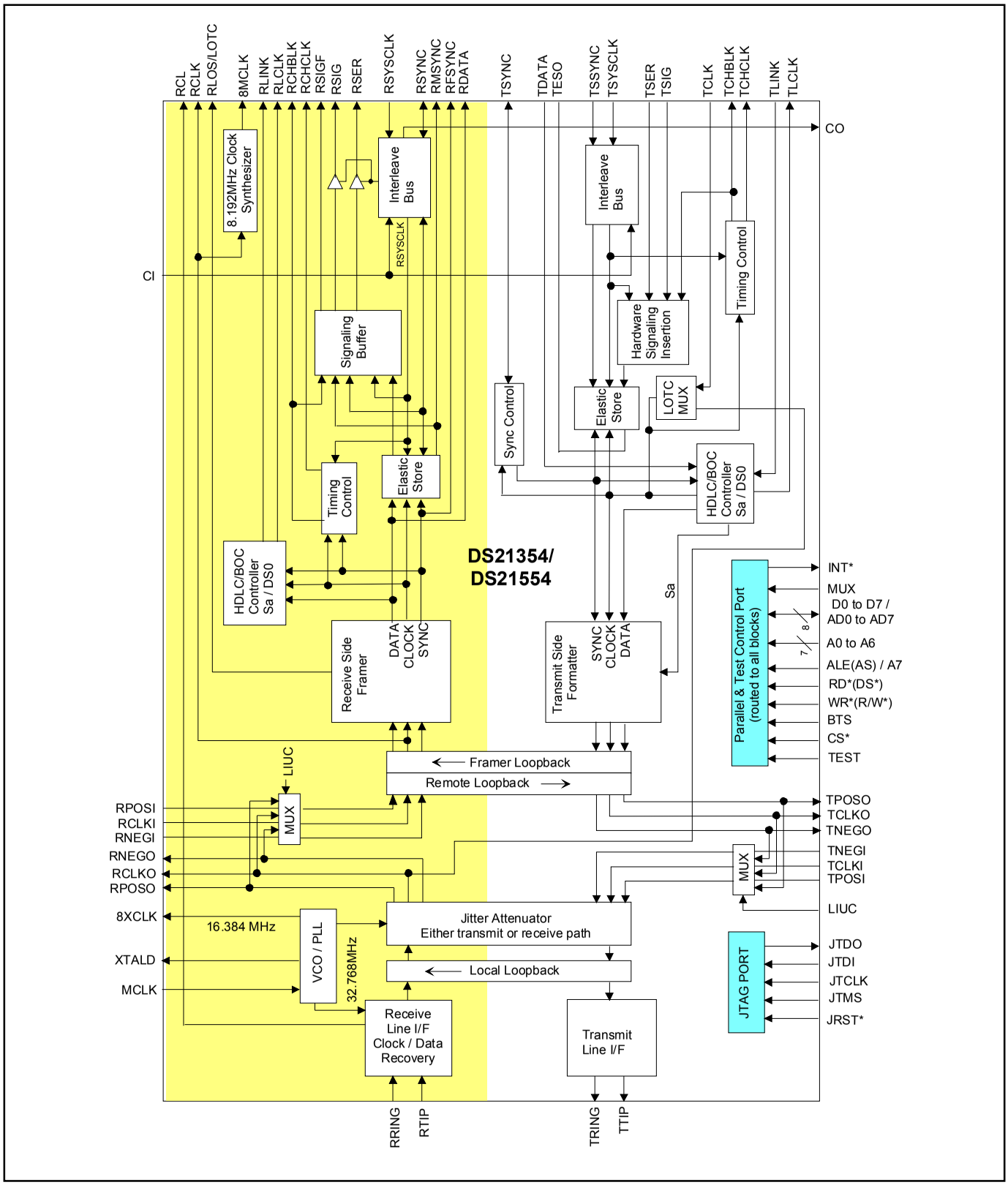
NAME	FUNCTION
FAS	Frame-Alignment Signal
CAS	Channel-Associated Signaling
MF	Multiframe
Si	International Bits
CRC4	Cyclical Redundancy Check
CCS	Common-Channel Signaling
Sa	Additional Bits
E-Bit	CRC4 Error Bits

1.2. Document Revision History

REVISION	DESCRIPTION
012799	Initial release
012899	Corrected TSYSCLK and RSYSCLK timing and added 4.096MHz and 8.192MHz timing
020399	Corrected definition and label of TUDR bit in the THIR register.
021199	Corrected address of IBO register in text.
040199	Added Receive Monitor Mode section
041599	Added section on Protected Interfaces
050799	Corrected pin number and description of FMS in JTAG section
072999	Added list of tables and figures
091499	Added 10µF cap to interface examples
092399	Corrected definition of $\overline{DS}$ in pin description.
072401	Typo corrected in JTAG Test Access Port Pins.
021004	Added note to the Receive Information Register, FAS Resync Criteria Met. Corrected Figures 20-1, 20-2, 20-3 with respect to $\overline{CS}$. Corrected typo in Figure 18-14 (RCR1.1 reference corrected). Corrected formatting issues.

2. BLOCK DIAGRAM

Figure 2-1. DS21354/554 Block Diagram



3. PIN DESCRIPTION

Table 3-1. Pin Description Sorted by Pin Number

PIN	NAME	TYPE	FUNCTION
1	RCHBLK	O	Receive Channel Block
2	JTMS	I	IEEE 1149.1 Test Mode Select
3	8MCLK	O	8.192 MHz Clock
4	JTCLK	I	IEEE 1149.1 Test Clock Signal
5	$\overline{\text{JTRST}}$	I	IEEE 1149.1 Test Reset, Active Low
6	RCL	O	Receive Carrier Loss
7	JTDI	I	IEEE 1149.1 Test Data Input
8, 9, 15, 23, 26, 27, 28	N.C.	—	No Connect. Do not connect any signal to this pin.
10	JTDO	O	IEEE 1149.1 Test Data Output
11	BTS	I	Bus Type Select
12	LIUC	I	Line Interface Connect
13	8XCLK	O	Eight Times Clock
14	TEST	I	Test
16	RTIP	I	Receive Analog Tip Input
17	RRING	I	Receive Analog Ring Input
18	RVDD	–	Receive Analog Positive Supply
19, 20, 24	RVSS	–	Receive Analog Signal Ground
21	MCLK	I	Master Clock Input
22	XTALD	O	Quartz Crystal Driver
25	$\overline{\text{INT}}$	O	Interrupt, Active Low
29	TTIP	O	Transmit Analog Tip Output
30	TVSS	–	Transmit Analog Signal Ground
31	TVDD	–	Transmit Analog Positive Supply
32	TRING	O	Transmit Analog Ring Output
33	TCHBLK	O	Transmit Channel Block
34	TLCLK	O	Transmit Link Clock
35	TLINK	I	Transmit Link Data
36	CI	I	Carry In
37	TSYNC	I/O	Transmit Sync
38	TPOSI	I	Transmit Positive Data Input
39	TNEGI	I	Transmit Negative Data Input
40	TCLKI	I	Transmit Clock Input
41	TCLKO	O	Transmit Clock Output
42	TNEGO	O	Transmit Negative Data Output
43	TPOSO	O	Transmit Positive Data Output
44, 61, 81,83	DVDD	—	Digital Positive Supply
45, 60, 80, 84	DVSS	—	Digital Signal Ground
46	TCLK	I	Transmit Clock
47	TSER	I	Transmit Serial Data
48	TSIG	I	Transmit Signaling Input

PIN	NAME	TYPE	FUNCTION
49	TESO	O	Transmit Elastic Store Output
50	TDATA	I	Transmit Data
51	TSYSCLK	I	Transmit System Clock
52	TSSYNC	I	Transmit System Sync
53	TCHCLK	O	Transmit Channel Clock
54	CO	O	Carry Out
55	MUX	I	Bus Operation
56	D0/AD0	I/O	Data Bus Bit0/Address/Data Bus Bit 0
57	D1/AD1	I/O	Data Bus Bit1/Address/Data Bus Bit 1
58	D2/AD2	I/O	Data Bus Bit 2/Address/Data Bus 2
59	D3/AD3	I/O	Data Bus Bit 3/Address/Data Bus Bit 3
62	D4/AD4	I/O	Data Bus Bit4/Address/Data Bus Bit 4
63	D5/AD5	I/O	Data Bus Bit 5/Address/Data Bus Bit 5
64	D6/AD6	I/O	Data Bus Bit 6/Address/Data Bus Bit 6
65	D7/AD7	I/O	Data Bus Bit 7/Address/Data Bus Bit 7
66	A0	I	Address Bus Bit 0
67	A1	I	Address Bus Bit 1
68	A2	I	Address Bus Bit 2
69	A3	I	Address Bus Bit 3
70	A4	I	Address Bus Bit 4
71	A5	I	Address Bus Bit 5
72	A6	I	Address Bus Bit 6
73	ALE (AS)/A7	I	Address Latch Enable/Address Bus Bit 7
74	$\overline{RD}$ ($\overline{DS}$)	I	Read Input (Data Strobe), Active Low
75	$\overline{CS}$	I	Chip Select, Active Low
76	FMS	I	Framer Mode Select
77	$\overline{WR}$ (R/$\overline{W}$)	I	Write Input (Read/Write), Active Low
78	RLINK	O	Receive Link Data
79	RLCLK	O	Receive Link Clock
82	RCLK	O	Receive Clock
85	RDATA	O	Receive Data
86	RPOSI	I	Receive Positive Data Input
87	RNEGI	I	Receive Negative Data Input
88	RCLKI	I	Receive Clock Input
89	RCLKO	O	Receive Clock Output
90	RNEGO	O	Receive Negative Data Output
91	RPOSO	O	Receive Positive Data Output
92	RCHCLK	O	Receive Channel Clock
93	RSIGF	O	Receive Signaling Freeze Output
94	RSIG	O	Receive Signaling Output
95	RSER	O	Receive Serial Data
96	RMSYNC	O	Receive Multiframe Sync
97	RFSYNC	O	Receive Frame Sync
98	RSYNC	I/O	Receive Sync
99	RLOS/LOTC	O	Receive Loss Of Sync/ Loss Of Transmit Clock
100	RSYSCLK	I	Receive System Clock

Table 3-2. Pin Description by Symbol

PIN	NAME	TYPE	FUNCTION
3	8MCLK	O	8.192MHz Clock
13	8XCLK	O	Eight-Times Clock
66	A0	I	Address Bus Bit 0
67	A1	I	Address Bus Bit 1
68	A2	I	Address Bus Bit 2
69	A3	I	Address Bus Bit 3
70	A4	I	Address Bus Bit 4
71	A5	I	Address Bus Bit 5
72	A6	I	Address Bus Bit 6
73	ALE (AS)/A7	I	Address Latch Enable/Address Bus Bit 7
11	BTS	I	Bus Type Select
36	CI	I	Carry In
54	CO	O	Carry Out
75	$\overline{CS}$	I	Chip Select, Active Low
56	D0/AD0	I/O	Data Bus Bit0/ Address/Data Bus Bit 0
57	D1/AD1	I/O	Data Bus Bit1/ Address/Data Bus Bit 1
58	D2/AD2	I/O	Data Bus Bit 2/Address/Data Bus 2
59	D3/AD3	I/O	Data Bus Bit 3/Address/Data Bus Bit 3
62	D4/AD4	I/O	Data Bus Bit4/Address/Data Bus Bit 4
63	D5/AD5	I/O	Data Bus Bit 5/Address/Data Bus Bit 5
64	D6/AD6	I/O	Data Bus Bit 6/Address/Data Bus Bit 6
65	D7/AD7	I/O	Data Bus Bit 7/Address/Data Bus Bit 7
44, 61, 81, 83	DVDD	—	Digital Positive Supply
45, 60, 80, 84	DVSS	—	Digital Signal Ground
76	FMS	I	Framer Mode Select
25	$\overline{INT}$	O	Interrupt
4	JTCLK	I	IEEE 1149.1 Test Clock Signal
7	JTDI	I	IEEE 1149.1 Test Data Input
10	JTDO	O	IEEE 1149.1 Test Data Output
2	JTMS	I	IEEE 1149.1 Test Mode Select
5	$\overline{JTRST}$	I	IEEE 1149.1 Test Reset, Active Low
12	LIUC	I	Line Interface Connect
21	MCLK	I	Master Clock Input
55	MUX	I	Bus Operation
8, 9, 15, 23, 26, 27, 28	N.C.	—	No Connect. Do not connect any signal to this pin.
1	RCHBLK	O	Receive Channel Block
92	RCHCLK	O	Receive Channel Clock
6	RCL	O	Receive Carrier Loss
82	RCLK	O	Receive Clock
88	RCLKI	I	Receive Clock Input
89	RCLKO	O	Receive Clock Output
74	$\overline{RD}$ ($\overline{DS}$)	I	Read Input (Data Strobe), Active Low
85	RDATA	O	Receive Data
97	RFSYNC	O	Receive Frame Sync
79	RLCLK	O	Receive Link Clock

PIN	NAME	TYPE	FUNCTION
78	RLINK	O	Receive Link Data
99	RLOS/LOTC	O	Receive Loss of Sync/Loss of Transmit Clock
96	RMSYNC	O	Receive Multiframe Sync
87	RNEGI	I	Receive Negative Data Input
90	RNEGO	O	Receive Negative Data Output
86	RPOSI	I	Receive Positive Data Input
91	RPOSO	O	Receive Positive Data Output
17	RRING	I	Receive Analog Ring Input
95	RSER	O	Receive Serial Data
94	RSIG	O	Receive Signaling Output
93	RSIGF	O	Receive Signaling Freeze Output
98	RSYNC	I/O	Receive Sync
100	RSYSCLK	I	Receive System Clock
16	RTIP	I	Receive Analog Tip Input
18	RVDD	—	Receive Analog Positive Supply
19, 20, 24	RVSS	—	Receive Analog Signal Ground
33	TCHBLK	O	Transmit Channel Block
53	TCHCLK	O	Transmit Channel Clock
46	TCLK	I	Transmit Clock
40	TCLKI	I	Transmit Clock Input
41	TCLKO	O	Transmit Clock Output
50	TDATA	I	Transmit Data
49	TESO	O	Transmit Elastic Store Output
14	TEST	I	Test
34	TLCLK	O	Transmit Link Clock
35	TLINK	I	Transmit Link Data
39	TNEGI	I	Transmit Negative Data Input
42	TNEGO	O	Transmit Negative Data Output
38	TPOSI	I	Transmit Positive Data Input
43	TPOSO	O	Transmit Positive Data Output
32	TRING	O	Transmit Analog Ring Output
47	TSER	I	Transmit Serial Data
48	TSIG	I	Transmit Signaling Input
52	TSSYNC	I	Transmit System Sync
37	TSYNC	I/O	Transmit Sync
51	TSYSCLK	I	Transmit System Clock
29	TTIP	O	Transmit Analog Tip Output
31	TVDD	—	Transmit Analog Positive Supply
30	TVSS	—	Transmit Analog Signal Ground
77	$\overline{WR}$ (R/$\overline{W}$)	I	Write Input (Read/Write), Active Low
22	XTALD	O	Quartz Crystal Driver

3.1. Pin Function Description

3.1.1. Transmit-Side Pins

Signal Name: **TCLK**
Signal Description: **Transmit Clock**
Signal Type: **Input**
A 2.048MHz primary clock. Used to clock data through the transmit side formatter.

Signal Name: **TSER**
Signal Description: **Transmit Serial Data**
Signal Type: **Input**
Transmit NRZ serial data. Sampled on the falling edge of TCLK when the transmit side elastic store is disabled. Sampled on the falling edge of TSYSCLK when the transmit side elastic store is enabled.

Signal Name: **TCHCLK**
Signal Description: **Transmit Channel Clock**
Signal Type: **Output**
A 256kHz clock that pulses high during the LSB of each channel. Synchronous with TCLK when the transmit side elastic store is disabled. Synchronous with TSYSCLK when the transmit side elastic store is enabled. Useful for parallel to serial conversion of channel data.

Signal Name: **TCHBLK**
Signal Description: **Transmit Channel Block**
Signal Type: **Output**
A user-programmable output that can be forced high or low during any of the 32 E1 channels. Synchronous with TCLK when the transmit side elastic store is disabled. Synchronous with TSYSCLK when the transmit-side elastic store is enabled. Useful for blocking clocks to a serial UART or LAPD controller in applications where not all E1 channels are used such as Fractional E1, 384kbps (H0), 768kbps, or ISDN–PRI. Also useful for locating individual channels in drop-and-insert applications, for external per-channel loopback, and for per-channel conditioning. See Section 12 for details.

Signal Name: **TSYSCLK**
Signal Description: **Transmit System Clock**
Signal Type: **Input**
1.544MHz, 2.048MHz, 4.096MHz, or 8.192MHz clock. Only used when the transmit-side elastic store function is enabled. Should be tied low in applications that do not use the transmit-side elastic store. See Section 17 for details on 4.096MHz and 8.192MHz operation using the Interleave Bus Option.

Signal Name: **TLCLK**
Signal Description: **Transmit Link Clock**
Signal Type: **Output**
4kHz to 20kHz demand clock (Sa bits) for the TLINK input. See Section 17 for details.

Signal Name: **TLINK**
Signal Description: **Transmit Link Data**
Signal Type: **Input**
If enabled, this pin will be sampled on the falling edge of TCLK for data insertion into any combination of the Sa bit positions (Sa4 to Sa8). See Section 13 for details.

Signal Name: **TSYNC**
Signal Description: **Transmit Sync**
Signal Type: **Input/Output**
A pulse at this pin will establish either frame or multiframe boundaries for the transmit side. Via TCR1.1, the DS21354/DS21554 can be programmed to output either a frame or multiframe pulse at this pin. This pin can also be configured as an input via TCR1.0. See Section 18 for details.

Signal Name: **TSSYNC**
Signal Description: **Transmit System Sync**
Signal Type: **Input**
Only used when the transmit-side elastic store is enabled. A pulse at this pin will establish either frame or multiframe boundaries for the transmit side. Should be tied low in applications that do not use the transmit-side elastic store.

Signal Name: **TSIG**
Signal Description: **Transmit Signaling Input**
Signal Type: **Input**
When enabled, this input will sample signaling bits for insertion into outgoing PCM E1 data stream. Sampled on the falling edge of TCLK when the transmit-side elastic store is disabled. Sampled on the falling edge of TSYSCLK when the transmit-side elastic store is enabled.

Signal Name: **TESO**
Signal Description: **Transmit Elastic Store Data Output**
Signal Type: **Output**
Updated on the rising edge of TCLK with data out of the transmit-side elastic store whether the elastic store is enabled or not. This pin is normally tied to TDATA.

Signal Name: **TDATA**
Signal Description: **Transmit Data**
Signal Type: **Input**
Sampled on the falling edge of TCLK with data to be clocked through the transmit-side formatter. This pin is normally tied to TESO.

Signal Name: **TPOSO**
Signal Description: **Transmit Positive Data Output**
Signal Type: **Output**
Updated on the rising edge of TCLKO with the bipolar data out of the transmit-side formatter. Can be programmed to source NRZ data via the Output Data Format (TCR2.2) control bit. This pin is normally tied to TPOSI.

Signal Name: **TNEGO**
Signal Description: **Transmit Negative Data Output**
Signal Type: **Output**
Updated on the rising edge of TCLKO with the bipolar data out of the transmit-side formatter. This pin is normally tied to TNEGI.

Signal Name: **TCLKO**
Signal Description: **Transmit Clock Output**
Signal Type: **Output**
Buffered output of signal that is clocking data through the transmit-side formatter. This pin is normally tied to TCLKI.

Signal Name: **TPOSI**
Signal Description: **Transmit Positive Data Input**
Signal Type: **Input**
Sampled on the falling edge of TCLKI for data to be transmitted out onto the T1 line. Can be internally connected to TPOSO by tying the LIUC pin high. TPOSI and TNEGI can be tied together in NRZ applications.

Signal Name: **TNEGI**
Signal Description: **Transmit Negative Data Input**
Signal Type: **Input**
Sampled on the falling edge of TCLKI for data to be transmitted out onto the T1 line. Can be internally connected to TNEGO by tying the LIUC pin high. TPOSI and TNEGI can be tied together in NRZ applications.

Signal Name: **TCLKI**
Signal Description: **Transmit Clock Input**
Signal Type: **Input**
Line interface transmit clock. Can be internally connected to TCLKO by tying the LIUC pin high.

3.1.2. Receive-Side Pins

Signal Name: **RLINK**
Signal Description: **Receive Link Data**
Signal Type: **Output**
Updated with the fully recovered E1 data stream on the rising edge of RCLK.

Signal Name: **RLCLK**
Signal Description: **Receive Link Clock**
Signal Type: **Output**
4kHz to 20kHz clock (Sa bits) for the RLINK output. See Section 13 for details.

Signal Name: **RCLK**
Signal Description: **Receive Clock**
Signal Type: **Output**
2.048MHz clock that is used to clock data through the receive-side framer.

Signal Name: **RCHCLK**
Signal Description: **Receive Channel Clock**
Signal Type: **Output**
A 256kHz clock that pulses high during the LSB of each channel. Synchronous with RCLK when the receive-side elastic store is disabled. Synchronous with RSYSCLK when the receive-side elastic store is enabled. Useful for parallel to serial conversion of channel data.

Signal Name: **RCHBLK**
Signal Description: **Receive Channel Block**
Signal Type: **Output**
A user-programmable output that can be forced high or low during any of the 32 E1 channels. Synchronous with RCLK when the receive-side elastic store is disabled. Synchronous with RSYSCLK when the receive-side elastic store is enabled. Useful for blocking clocks to a serial UART or LAPD controller in applications where not all E1 channels are used such as Fractional E1, 384kbps service, 768kbps, or ISDN–PRI. Also useful for locating individual channels in drop-and-insert applications, for external per-channel loopback, and for per-channel conditioning. See Section 10 for details.

Signal Name: **RSER**
Signal Description: **Receive Serial Data**
Signal Type: **Output**
Received NRZ serial data. Updated on rising edges of RCLK when the receive-side elastic store is disabled. Updated on the rising edges of RSYSCLK when the receive-side elastic store is enabled.

Signal Name: **RSYNC**
Signal Description: **Receive Sync**
Signal Type: **Input/Output**
An extracted pulse, one RCLK wide, is output at this pin that identifies either frame or CAS/CRC multiframe boundaries. If the receive-side elastic store is enabled, then this pin can be enabled to be an input at which a frame or multiframe boundary pulse synchronous with RSYSCLK is applied.

Signal Name: **RFSYNC**
Signal Description: **Receive Frame Sync**
Signal Type: **Output**
An extracted 8kHz pulse, one RCLK wide, is output at this pin that identifies frame boundaries.

Signal Name: **RMSYNC**
Signal Description: **Receive Multiframe Sync**
Signal Type: **Output**
If the receive-side elastic store is enabled, an extracted pulse, one RSYSCLK wide, is output at this pin that identifies multiframe boundaries. If the receive-side elastic store is disabled, then this output will output multiframe boundaries associated with RCLK.

Signal Name: **RDATA**
Signal Description: **Receive Data**
Signal Type: **Output**
Updated on the rising edge of RCLK with the data out of the receive-side framer.

Signal Name: **RSYSCLK**
Signal Description: **Receive System Clock**
Signal Type: **Input**
1.544MHz, 2.048MHz, 4.096MHz, or 8.192MHz clock. Only used when the receive-side elastic store function is enabled. Should be tied low in applications that do not use the receive-side elastic store. See Section 17 for details on 4.096MHz and 8.192MHz operation using the Interleave Bus Option.

Signal Name: **RSIG**
Signal Description: **Receive Signaling Output**
Signal Type: **Output**
Outputs signaling bits in a PCM format. Updated on rising edges of RCLK when the receive-side elastic store is disabled. Updated on the rising edges of RSYSCLK when the receive-side elastic store is enabled.

Signal Name: **RLOS/LOTC**
Signal Description: **Receive Loss of Sync / Loss of Transmit Clock**
Signal Type: **Output**
A dual function output that is controlled by the TCR2.0 control bit. This pin can be programmed to either toggle high when the synchronizer is searching for the frame and multiframe or to toggle high if the TCLK pin has not been toggled for 5µs.

Signal Name: **RCL**
Signal Description: **Receive Carrier Loss**
Signal Type: **Output**
Set high when the line interface detects a carrier loss.

Signal Name: **RSIGF**
Signal Description: **Receive Signaling Freeze**
Signal Type: **Output**
Set high when the signaling data is frozen via either automatic or manual intervention. Used to alert downstream equipment of the condition.

Signal Name: **8MCLK**
Signal Description: **8MHz Clock**
Signal Type: **Output**
An 8.192MHz clock output that is referenced to the clock that is output at the RCLK pin.

Signal Name: **RPOSO**
Signal Description: **Receive Positive Data Input**
Signal Type: **Output**
Updated on the rising edge of RCLKO with bipolar data out of the line interface. This pin is normally tied to RPOSI.

Signal Name: **RNEGO**
Signal Description: **Receive Negative Data Input**
Signal Type: **Output**
Updated on the rising edge of RCLKO with the bipolar data out of the line interface. This pin is normally tied to RNEGI.

Signal Name: **RCLKO**
Signal Description: **Receive Clock Output**
Signal Type: **Output**
Buffered recovered clock from the T1 line. This pin is normally tied to RCLKI.

Signal Name: **RPOSI**
Signal Description: **Receive Positive Data Input**
Signal Type: **Input**
Sampled on the falling edge of RCLKI for data to be clocked through the receive-side framer. RPOSI and RNEGI can be tied together for a NRZ interface. Can be internally connected to RPOSO by tying the LIUC pin high.

Signal Name: **RNEGI**
Signal Description: **Receive Negative Data Input**
Signal Type: **Input**
Sampled on the falling edge of RCLKI for data to be clocked through the receive-side framer. RPOSI and RNEGI can be tied together for a NRZ interface. Can be internally connected to RNEGO by tying the LIUC pin high.

Signal Name: **RCLKI**
Signal Description: **Receive Clock Input**
Signal Type: **Input**
Clock used to clock data through the receive-side framer. This pin is normally tied to RCLKO. Can be internally connected to RCLKO by tying the LIUC pin high.

3.1.3. Parallel Control Port Pins

Signal Name: **$\overline{\text{INT}}$**
Signal Description: **Interrupt**
Signal Type: **Output**
Active-low, open-drain output that flags host controller during conditions and change of conditions defined in the Status Registers 1 and 2 and the HDLC Status Register.

Signal Name: **FMS**
Signal Description: **Framer Mode Select**
Signal Type: **Input**
Selects the DS2154 mode when high or the DS21354/DS21554 mode when low. If high, the $\overline{\text{JTRST}}$ is internally pulled low. If low, $\overline{\text{JTRST}}$ has normal JTAG functionality. This pin has a 10kΩ pullup resistor.

Signal Name: **TEST**
Signal Description: **Tri-State Control**
Signal Type: **Input**
Set high to tri-state all output and I/O pins (including the parallel control port). Set low for normal operation. Useful in board-level testing.

Signal Name: **MUX**
Signal Description: **Bus Operation**
Signal Type: **Input**
Set low to select nonmultiplexed bus operation. Set high to select multiplexed bus operation.

Signal Name: **AD0 to AD7**
Signal Description: **Data Bus [D0 to D7] or Address/Data Bus**
Signal Type: **Input**
In nonmultiplexed bus operation (MUX = 0), serves as the data bus. In multiplexed bus operation (MUX = 1), serves as an 8-bit multiplexed address/data bus.

Signal Name: **A0 to A6**
Signal Description: **Address Bus**
Signal Type: **Input**
In nonmultiplexed bus operation (MUX = 0), serves as the address bus. In multiplexed bus operation (MUX = 1), these pins are not used and should be tied low.

Signal Name: **BTS**
Signal Description: **Bus Type Select**
Signal Type: **Input**
Strap high to select Motorola bus timing; strap low to select Intel bus timing. This pin controls the function of the $\overline{\text{RD}}$ ($\overline{\text{DS}}$), ALE (AS), and $\overline{\text{WR}}$ (R/$\overline{\text{W}}$) pins. If BTS = 1, then these pins assume the function listed in parentheses ().

Signal Name: **$\overline{RD}$ ($\overline{DS}$)**
Signal Description: **Read Input—Data Strobe**
Signal Type: **Input**
In Intel Mode, $\overline{RD}$ determines when data is read from the device. In Motorola Mode, $\overline{DS}$ is used to write to the device. See the *Bus Timing Diagrams* section.

Signal Name: **$\overline{CS}$**
Signal Description: **Chip Select**
Signal Type: **Input**
Must be low to read or write to the device. $\overline{CS}$ is an active-low signal.

Signal Name: **ALE (AS)/A7**
Signal Description: **Address Latch Enable (Address Strobe) or A7**
Signal Type: **Input**
In nonmultiplexed bus operation (MUX = 0), serves as the upper address bit. In multiplexed bus operation (MUX = 1), serves to demultiplex the bus on a positive-going edge.

Signal Name: **$\overline{WR}$ (R/$\overline{W}$)**
Signal Description: **Write Input (Read/Write)**
Signal Type: **Input**
$\overline{WR}$ is an active-low signal.

3.1.4. JTAG Test Access Port Pins

Signal Name: $\overline{\text{JTRST}}$
Signal Description: **IEEE 1149.1 Test Reset**
Signal Type: **Input**
This signal is used to asynchronously reset the test access port controller. At power up, $\overline{\text{JTRST}}$ must be toggled from low to high. This action will set the device into JTAG DEVICE ID mode enabling the test access port features. This pin has a 10kΩ pullup resistor. When FMS = 1, this pin is tied low internally. Tie $\overline{\text{JTRST}}$ low if JTAG is not used and the framer is in DS21354/DS21554 mode (FMS low).

Signal Name: **JTMS**
Signal Description: **IEEE 1149.1 Test Mode Select**
Signal Type: **Input**
This pin is sampled on the rising edge of JTCLK and is used to place the test access port into the various defined IEEE 1149.1 states. This pin has a 10kΩ pullup resistor.

Signal Name: **JTCLK**
Signal Description: **IEEE 1149.1 Test Clock Signal**
Signal Type: **Input**
This signal is used to shift data into JTDI on the rising edge and out of JTDO on the falling edge.

Signal Name: **JTDI**
Signal Description: **IEEE 1149.1 Test Data Input**
Signal Type: **Input**
Test instructions and data are clocked into this pin on the rising edge of JTCLK. This pin has a 10kΩ pullup resistor.

Signal Name: **JTDO**
Signal Description: **IEEE 1149.1 Test Data Output**
Signal Type: **Output**
Test instructions and data are clocked out of this pin on the falling edge of JTCLK. If not used, this pin should be left unconnected.

3.1.5. Interleave Bus Operation Pins

Signal Name: **CI**
Signal Description: **Carry In**
Signal Type: **Input**
A rising edge on this pin causes RSER and RSIG to come out of high-Z state and TSER and TSIG to start sampling on the next rising edge of RSYSCLK/TSYSCLK beginning an I/O sequence of 8 or 256 bits of data. This pin has a 10kΩ pullup resistor.

Signal Name: **CO**
Signal Description: **Carry Out**
Signal Type: **Output**
An output that is set high when the last bit of the 8 or 256 IBO output sequence has occurred on RSER and RSIG.

3.1.6. Line Interface Pins

Signal Name: **MCLK**
Signal Description: **Master Clock Input**
Signal Type: **Input**
A 2.048MHz (±50ppm) clock source with TTL levels is applied at this pin. This clock is used internally for both clock/data recovery and for jitter attenuation. A quartz crystal of 2.048MHz may be applied across MCLK and XTALD instead of the TTL level clock source.

Signal Name: **XTALD**
Signal Description: **Quartz Crystal Driver**
Signal Type: **Output**
A quartz crystal of 2.048MHz may be applied across MCLK and XTALD instead of a TTL level clock source at MCLK. Leave open circuited if a TTL clock source is applied at MCLK.

Signal Name: **8XCLK**
Signal Description: **Eight-Times Clock**
Signal Type: **Output**
A 16.384MHz clock that is frequency locked to the 2.048MHz clock provided from the clock/data recovery block (if the jitter attenuator is enabled on the receive side) or from the TCLKI pin (if the jitter attenuator is enabled on the transmit side). Can be internally disabled via TEST2 register if not needed.

Signal Name: **LIUC**
Signal Description: **Line Interface Connect**
Signal Type: **Input**
Tie low to separate the line interface circuitry from the framer/formatter circuitry and activate the TPOSI/TNEGI/TCLKI/RPOSI/RNEGI/RCLKI pins. Tie high to connect the line interface circuitry to the framer/formatter circuitry and deactivate the TPOSI/TNEGI/TCLKI/RPOSI/RNEGI/RCLKI pins. When LIUC is tied high, the TPOSI/TNEGI/TCLKI/ RPOSI/RNEGI/RCLKI pins should be tied low.

Signal Name: **RTIP and RRING**
Signal Description: **Receive Tip and Ring**
Signal Type: **Input**
Analog inputs for clock recovery circuitry. These pins connect via a 1:1 transformer to the E1 line. See Section 15 for details.

Signal Name: **TTIP and TRING**
Signal Description: **Transmit Tip and Ring**
Signal Type: **Output**
Analog line-driver outputs. These pins connect via a step-up transformer to the E1 line. See Section 15 for details.

3.1.7. Supply Pins

Signal Name: **DVDD**
Signal Description: **Digital Positive Supply**
Signal Type: **Supply**
5.0V ±5% (DS21554) or 3.3V ±5% (DS21354). Should be tied to the RVDD and TVDD pins.

Signal Name: **RVDD**
Signal Description: **Receive Analog Positive Supply**
Signal Type: **Supply**
5.0V ±5% (DS21554) or 3.3V ±5% (DS21354). Should be tied to the DVDD and TVDD pins.

Signal Name: **TVDD**
Signal Description: **Transmit Analog Positive Supply**
Signal Type: **Supply**
5.0V ±5% (DS21554) or 3.3V ±5% (DS21354). Should be tied to the RVDD and DVDD pins.

Signal Name: **DVSS**
Signal Description: **Digital Signal Ground**
Signal Type: **Supply**
0.0V. Should be tied to the RVSS and TVSS pins.

Signal Name: **RVSS**
Signal Description: **Receive Analog Signal Ground**
Signal Type: **Supply**
0.0V. Should be tied to DVSS and TVSS.

Signal Name: **TVSS**
Signal Description: **Transmit Analog Signal Ground**
Signal Type: **Supply**
0.0V. Should be tied to DVSS and RVSS.

4. PARALLEL PORT

The DS21354/DS21554 are controlled through either a nonmultiplexed (MUX = 0) or a multiplexed (MUX = 1) bus by an external microcontroller or microprocessor. The device can operate with either Intel or Motorola bus timing configurations. If the BTS pin is tied low, Intel timing is selected; if tied high, Motorola timing is selected. All Motorola bus signals are listed in parentheses (). See the timing diagrams in Section 18 for more details.

4.1. Register Map

Table 4-1. Register Map Sorted by Address

ADDRESS	TYPE	REGISTER	NAME
00	R	BPV or Code Violation Count 1	VCR1
01	R	BPV or Code Violation Count 2	VCR2
02	R	CRC4 Error Count 1/FAS Error Count 1	CRCCR1
03	R	CRC4 Error Count 2	CRCCR2
04	R	E-Bit Count 1/FAS Error Count 2	EBCR1
05	R	E-Bit Count 2	EBCR2
06	R/W	Status 1	SR1
07	R/W	Status 2	SR2
08	R/W	Receive Information	RIR
09	—	Not used	(set to 00h)
0A	—	Not used	(set to 00h)
0B	—	Not used	(set to 00h)
0C	—	Not used	(set to 00h)
0D	—	Not used	(set to 00h)
0E	—	Not used	(set to 00h)
0F	R	Device ID	IDR
10	R/W	Receive Control 1	RCR1
11	R/W	Receive Control 2	RCR2
12	R/W	Transmit Control 1	TCR1
13	R/W	Transmit Control 2	TCR2
14	R/W	Common Control 1	CCR1
15	R/W	Test 1	TEST1 (set to 00h)
16	R/W	Interrupt Mask 1	IMR1
17	R/W	Interrupt Mask 2	IMR2
18	R/W	Line Interface Control Register	LICR
19	R/W	Test 2	TEST2 (set to 00h)
1A	R/W	Common Control 2	CCR2
1B	R/W	Common Control 3	CCR3
1C	R/W	Transmit Sa Bit Control	TSaCR
1D	R/W	Common Control 6	CCR6
1E	R	Synchronizer Status	SSR
1F	R	Receive Non-Align Frame	RNAF
20	R/W	Transmit Align Frame	TAF
21	R/W	Transmit Non-Align Frame	TNAF
22	R/W	Transmit Channel Blocking 1	TCBR1
23	R/W	Transmit Channel Blocking 2	TCBR2
24	R/W	Transmit Channel Blocking 3	TCBR3