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DS21448
3.3V E1/T1/J1 Quad Line Interface

www.maxim-ic.com

GENERAL DESCRIPTION

The DS21448 is a quad-port E1 or T1 line interface unit (LIU) for short-haul and long-haul applications. It incorporates four independent transmitters and four independent receivers in a single 144-pin PBGA or 128-pin LQFP package. The transmit drivers generate the necessary G.703 E1 waveshapes in 75Ω or 120Ω applications and the DSX-1 or CSU line build-outs of 0dB, -7.5dB, -15dB, and -22.5dB for T1 applications.

APPLICATIONS

Integrated Multiservice Access Platforms
T1/E1 Cross-Connects, Multiplexers, and Channel Banks
Central-Office Switches and PBX Interfaces
T1/E1 LAN/WAN Routers
Wireless Base Stations

ORDERING INFORMATION

PART*	TEMP RANGE	PIN-PACKAGE
DS21448	0°C to +70°C	144 TE-PBGA
DS21448+	0°C to +70°C	144 TE-PBGA
DS21448N	-40°C to +85°C	144 TE-PBGA
DS21448N+	-40°C to +85°C	144 TE-PBGA
DS21448L	0°C to +70°C	128 LQFP
DS21448L+	0°C to +70°C	128 LQFP
DS21448LN	-40°C to +85°C	128 LQFP
DS21448LN+	-40°C to +85°C	128 LQFP

+ Denotes lead-free/RoHS-compliant package.
**All devices rated at 3.3V.*

Pin Configurations appear in Section 11.

FEATURES

- Four Complete E1, T1, or J1 LIUs
- Supports Long- and Short-Haul Trunks
- Internal Software-Selectable Receive-Side Termination for 75Ω/100Ω/120Ω
- 3.3V Power Supply
- 32-Bit or 128-Bit Crystal-Less Jitter Attenuator Requires Only a 2.048MHz Master Clock for E1 and T1, with the Option to Use 1.544MHz for T1
- Generates the Appropriate Line Build-Outs With and Without Return Loss for E1, and DSX-1 and CSU Line Build-Outs for T1
- AMI, HDB3, and B8ZS Encoding/Decoding
- 16.384MHz, 8.192MHz, 4.096MHz, or 2.048MHz Clock Output Synthesized to Recovered Clock
- Programmable Monitor Mode for Receiver
- Loopbacks and PRBS Pattern Generation/ Detection with Output for Received Errors
- Generates/Detects In-Band Loop Codes, 1 to 16 Bits, Including CSU Loop Codes
- 8-Bit Parallel or Serial Interface with Optional Hardware Mode
- Muxed and Nonmuxed Parallel Bus Supports Intel or Motorola
- Detects/Generates Blue (AIS) Alarms
- NRZ/Bipolar Interface for Tx/Rx Data I/O
- Transmit Open-Circuit Detection
- Receive Carrier Loss (RCL) Indication (G.775)
- High-Z State for TTIP and TRING
- 50mA$_{RMS}$ Transmit Current Limiter
- JTAG Boundary Scan Test Port per IEEE 1149.1
- Meets Latest E1 and T1 Specifications Including ANSI.403-1999, ANSI T1.408, AT&T TR 62411, ITU G.703, G.704, G.706, G.736, G.775, G.823, I.431, O.151, O.161, ETSI ETS 300 166, JTG.703, JTI.431, TBR12, TBR13, and CTR4

***Note:** Some revisions of this device may incorporate deviations from published specifications known as errata. Multiple revisions of any device may be simultaneously available through various sales channels. For information about device errata, click here: www.maxim-ic.com/errata.*

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1. BLOCK DIAGRAMS

Figure 1-1. Block Diagram

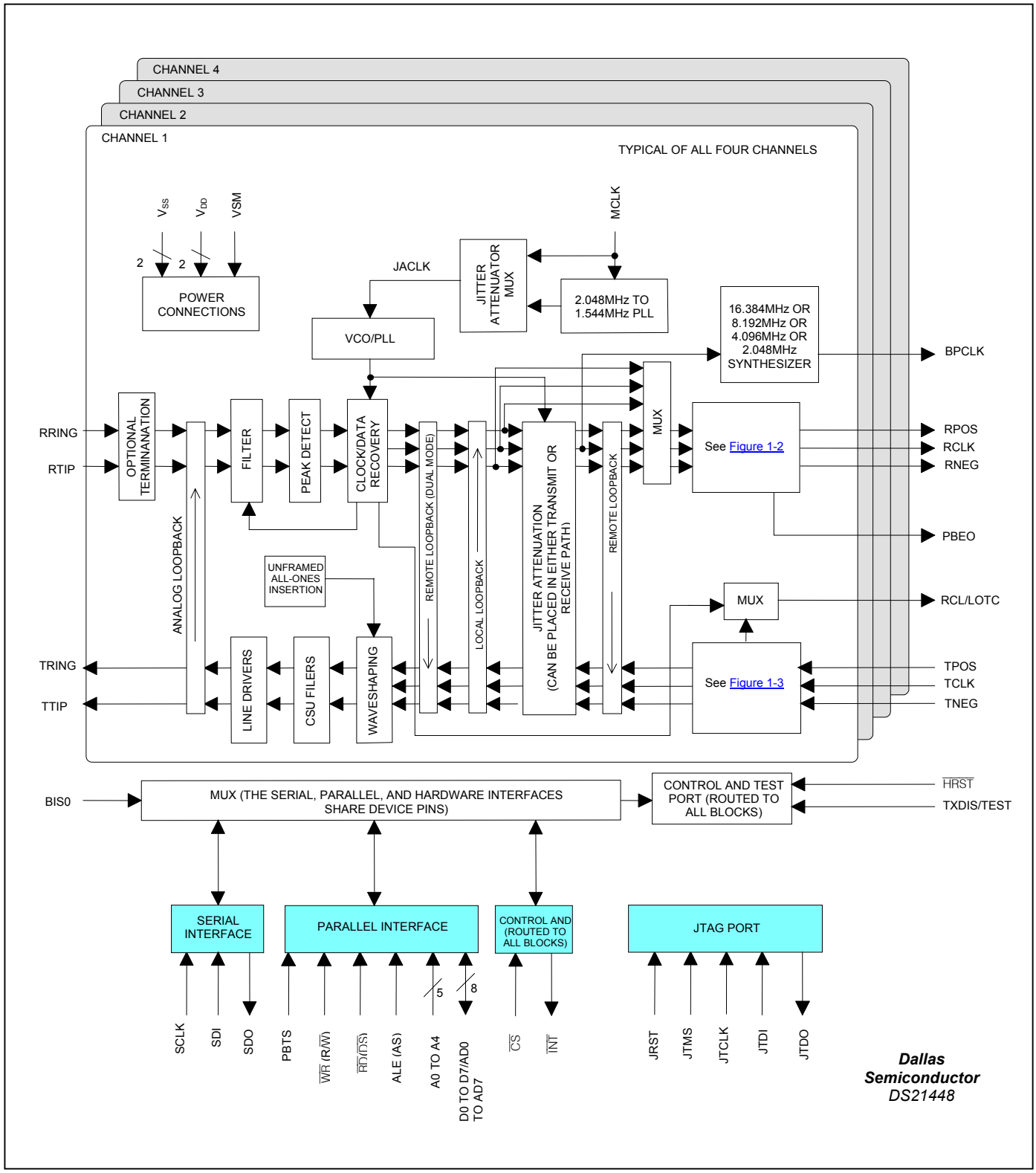


Figure 1-2. Receive Logic Detail

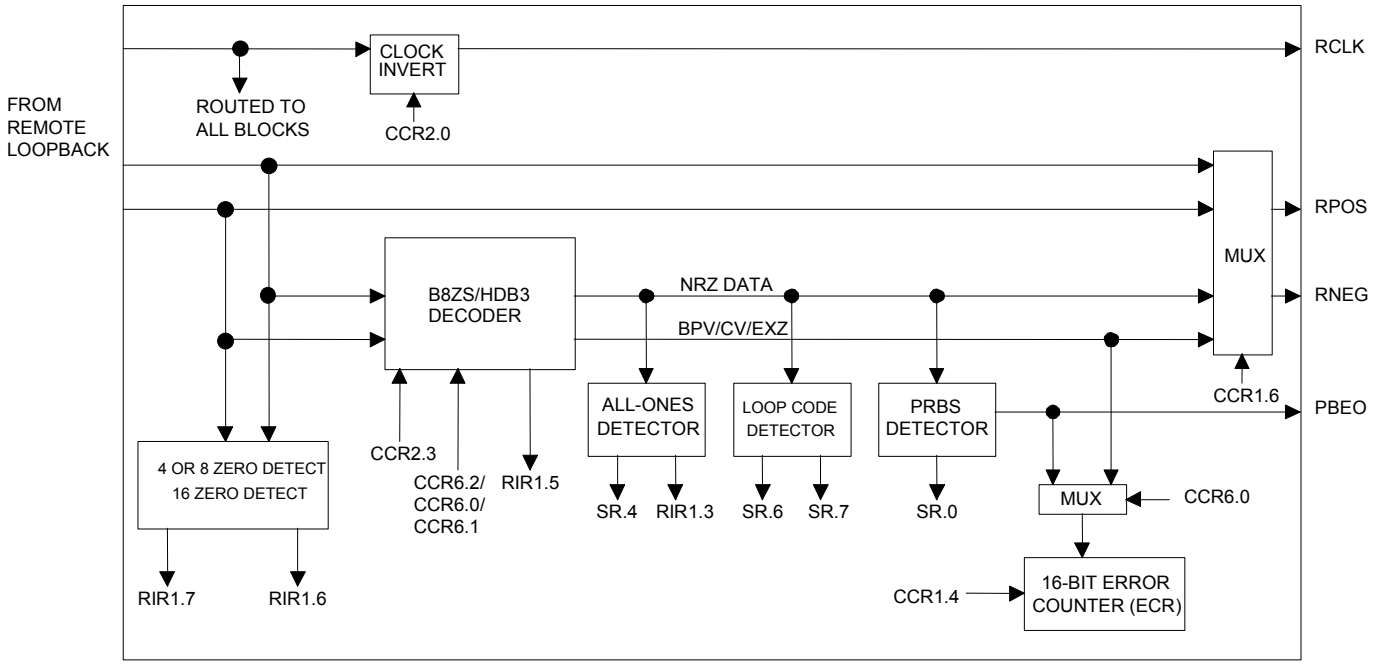
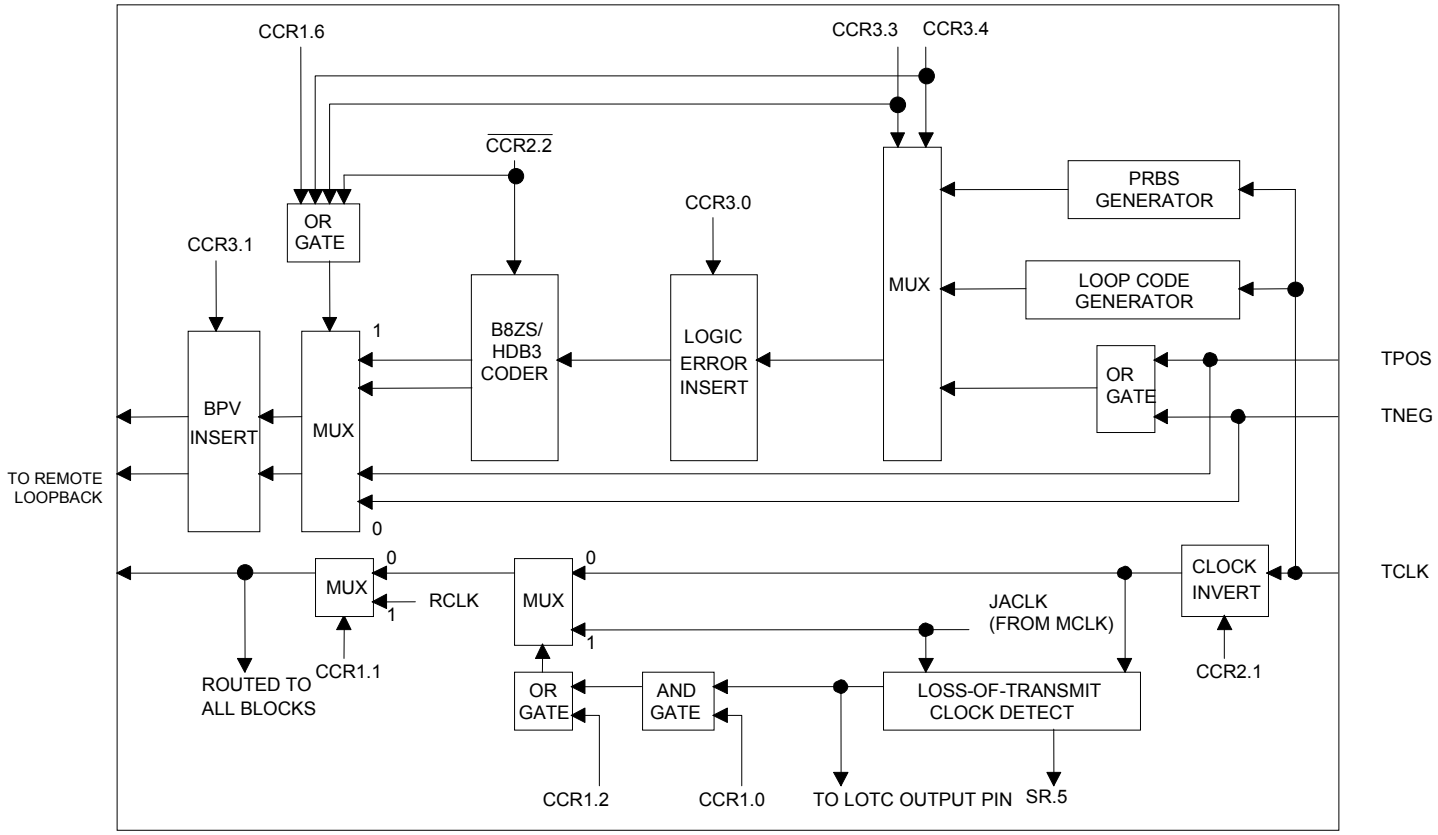


Figure 1-3. Transmit Logic Detail



2. PIN DESCRIPTION

The DS21448 can be controlled in parallel port mode, serial port mode, or hardware mode. The bus interface select bits 0 and 1 (BIS0, BIS1) determine the device mode and pin assignments (Table 2-A).

Table 2-A. Bus Interface Selection

BIS1	BIS0	BUS INTERFACE TYPE
0	0	Parallel Port Mode (multiplexed)
0	1	Parallel Port Mode (nonmultiplexed)
1	0	Serial Port Mode
1	1	Hardware Mode

Table 2-B. Pin Assignments

PIN		I/O	PARALLEL PORT MODE	SERIAL PORT MODE	HARDWARE MODE
BGA	LQFP				
J3	18	I	$\overline{CS1}$	$\overline{CS1}$	EGL1
D3	57	I	$\overline{CS2}$	$\overline{CS2}$	EGL2
D10	84	I	$\overline{CS3}$	$\overline{CS3}$	EGL3
K10	114	I	$\overline{CS4}$	$\overline{CS4}$	EGL4
J2	91	I	$\overline{RD}$ ($\overline{DS}$)	N/A	ETS
H1	92	I	$\overline{WR}$ (R/$\overline{W}$)	N/A	NRZE
K2	95	I	ALE (AS)	N/A	SCLKE
J1	35	I	N/A	SCLK	L2
K3	36	I	N/A	SDI	L1
K1	62	I/O	A4	SDO	L0
L1	63	I	A3	ICES	DJA
H11	64	I	A2	OCES	JAMUX
H12	65	I	A1	N/A	JAS
G12	66	I	A0	N/A	HBE
J10	75	I/O	D7/AD7	N/A	CES
H10	76	I/O	D6/AD6	N/A	TPD
G11	77	I/O	D5/AD5	N/A	TX0
J9	78	I/O	D4/AD4	N/A	TX1
E3	79	I/O	D3/AD3	N/A	LOOP0
D4	80	I/O	D2/AD2	N/A	LOOP1
F3	81	I/O	D1/AD1	N/A	MM0
D5	82	I/O	D0/AD0	N/A	MM1
—	3	I	VSM	VSM	VSM
L5	115–117	—	VDD1	VDD1	VDD1
E4	19–21	—	VDD2	VDD2	VDD2
D8	49–51	—	VDD3	VDD3	VDD3
J8	85–87	—	VDD4	VDD4	VDD4
M4	118–120	—	VSS1	VSS1	VSS1
F4	22–24	—	VSS2	VSS2	VSS2
D9	52–54	—	VSS3	VSS3	VSS3
H9	88–90	—	VSS4	VSS4	VSS4
K9	97	I/O	$\overline{INT}$	$\overline{INT}$	RT1
K5	110	O	PBEO1	PBEO1	PBEO1
G3	111	O	PBEO2	PBEO2	PBEO2
E10	121	O	PBEO3	PBEO3	PBEO3
K8	123	O	PBEO4	PBEO4	PBEO4
L6	126	O	RCL1/LOTC1	RCL1/LOTC1	RCL1
D7	128	O	RCL2/LOTC2	RCL2/LOTC2	RCL2
F9	1	O	RCL3/LOTC3	RCL3/LOTC3	RCL3
J7	2	O	RCL4/LOTC4	RCL4/LOTC4	RCL4
K7	98	I	TXDIS/TEST	TXDIS/TEST	TXDIS/TEST
A1	124	I	RTIP1	RTIP1	RTIP1
A4	28	I	RTIP2	RTIP2	RTIP2
A7	60	I	RTIP3	RTIP3	RTIP3
A10	93	I	RTIP4	RTIP4	RTIP4
B2	125	I	RRING1	RRING1	RRING1
B5	29	I	RRING2	RRING2	RRING2

PIN		I/O	PARALLEL PORT MODE	SERIAL PORT MODE	HARDWARE MODE
BGA	LQFP				
B8	61	I	RRING3	RRING3	RRING3
B11	94	I	RRING4	RRING4	RRING4
L9	106	I	$\overline{\text{HRST}}$	$\overline{\text{HRST}}$	$\overline{\text{HRST}}$
J6	109	I	MCLK	MCLK	MCLK
H4	122	O	BPCLK1	BPCLK1	BPCLK1
D6	47	O	BPCLK2	BPCLK2	BPCLK2
F10	56	O	BPCLK3	BPCLK3	BPCLK3
L8	112	O	BPCLK4	BPCLK4	BPCLK4
L7	107	I	BIS0	BIS0	BIS0
M8	68	I	BIS1	BIS1	BIS1
A2	6	O	TTIP1	TTIP1	TTIP1
A5	38	O	TTIP2	TTIP2	TTIP2
A8	71	O	TTIP3	TTIP3	TTIP3
A11	102	O	TTIP4	TTIP4	TTIP4
J4	7	—	TVSS1	TVSS1	TVSS1
D1	39	—	TVSS2	TVSS2	TVSS2
E9	72	—	TVSS3	TVSS3	TVSS3
L10	103	—	TVSS4	TVSS4	TVSS4
J5	8	—	TVDD1	TVDD1	TVDD1
D2	40	—	TVDD2	TVDD2	TVDD2
G9	73	—	TVDD3	TVDD3	TVDD3
M9	104	—	TVDD4	TVDD4	TVDD4
B3	9	O	TRING1	TRING1	TRING1
B6	41	O	TRING2	TRING2	TRING2
B9	74	O	TRING3	TRING3	TRING3
B12	105	O	TRING4	TRING4	TRING4
K4	10	O	RPOS1	RPOS1	RPOS1
E1	12	O	RPOS2	RPOS2	RPOS2
D11	14	O	RPOS3	RPOS3	RPOS3
K11	16	O	RPOS4	RPOS4	RPOS4
G2	11	O	RNEG1	RNEG1	RNEG1
E2	13	O	RNEG2	RNEG2	RNEG2
F11	15	O	RNEG3	RNEG3	RNEG3
M10	25	O	RNEG4	RNEG4	RNEG4
H3	127	O	RCLK1	RCLK1	RCLK1
F1	31	O	RCLK2	RCLK2	RCLK2
E11	58	O	RCLK3	RCLK3	RCLK3
L11	96	O	RCLK4	RCLK4	RCLK4
G1	26	I	TPOS1	TPOS1	TPOS1
F2	30	I	TPOS2	TPOS2	TPOS2
E12	33	I	TPOS3	TPOS3	TPOS3
M11	55	I	TPOS4	TPOS4	TPOS4
H2	27	I	TNEG1	TNEG1	TNEG1
M1	32	I	TNEG2	TNEG2	TNEG2
D12	34	I	TNEG3	TNEG3	TNEG3
K12	59	I	TNEG4	TNEG4	TNEG4
M2	17	I	TCLK1	TCLK1	TCLK1
L2	43	I	TCLK2	TCLK2	TCLK2
F12	83	I	TCLK3	TCLK3	TCLK3
L12	113	I	TCLK4	TCLK4	TCLK4
M12	108	I	PBTS	N/A	RT0
L3	42	I	JTRST	JTRST	JTRST
M3	48	I	JTMS	JTMS	JTMS
M5	44	I	JTCLK	JTCLK	JTCLK
M6	45	I	JTDI	JTDI	JTDI
M7	46	O	JTDO	JTDO	JTDO

Note 1: The VSM signal is not available with the BGA package option.
Note 2: The LQFP no-connect pin numbers are 4, 5, 37, 67, 69, 70, and 99–101.
Note 3: The BGA no-connect pin numbers are A3, A6, A9, A12, B1, B4, B7, B10, C1–C12, E5–E8, F5–F8, G4–G8, G10, H5–H8, J11, J12, K6, and L4.

Table 2-C. Parallel Interface Mode Pin Description

PIN	I/O	FUNCTION
$\overline{RD}$ ($\overline{DS}$)	I	Read Input (Data Strobe). $\overline{RD}$ and $\overline{DS}$ are active-low signals. DS is active low when in nonmultiplexed, Motorola mode. See the bus timing diagrams in Section 10.
$\overline{WR}$ (R/$\overline{W}$)	I	Write Input (Read/Write). $\overline{WR}$ is an active-low signal. See the bus timing diagrams in Section 10.
ALE (AS)	I	Address Latch Enable (Address Strobe). When using multiplexed bus mode (BIS0 = 0), this pin serves to demultiplex the bus on a positive-going edge. In nonmultiplexed bus mode (BIS0 = 1), ALE should be wired low.
A4–A0	I	Address Bus. In nonmultiplexed bus operation (BIS0 = 1), these pins serve as the address bus. In multiplexed bus operation (BIS0 = 0), these pins are not used and should be wired low.
D7/AD7–D0/AD0	I/O	Data Bus/Address/Data Bus. In nonmultiplexed bus operation (BIS0 = 1), these pins serve as the data bus. In multiplexed bus operation (BIS0 = 0), these pins serve as an 8-bit multiplexed address/data bus.
$\overline{INT}$	O	Interrupt ($\overline{INT}$). The interrupt flags the host controller during conditions and change of conditions defined in the status register. It is an active-low, open-drain output.
TXDIS/TEST	I	Tri-State Control, Multifunctional. Set this pin high, with all $\overline{CS1}$–$\overline{CS4}$ inputs inactive, to tri-state TTIP1–TTIP4 and TRING1–TRING4. Set this pin high with any of the $\overline{CS1}$–$\overline{CS4}$ inputs active to tri-state all outputs and I/O pins (including the parallel control port). Set low for normal operation.
$\overline{HRST}$	I	Hardware Reset. Bringing $\overline{HRST}$ low resets the DS21448, setting all control bits to the all-zeros default state.
MCLK	I	Master Clock. A 2.048MHz (±50ppm) clock source with TTL levels is applied at this pin. This clock is used internally for both clock/data recovery and for jitter attenuation. Use of a T1 1.544MHz clock source is optional (Note 1).
BIS0/BIS1	I	Bus Interface Select Bit 0 and 1. Used to select bus interface option. See Table 2-A for details.
PBTS	I	Parallel Bus Type Select. When using the parallel port, set PBTS high to select Motorola bus timing; set low to select Intel bus timing. This pin controls the function of the $\overline{RD}$ ($\overline{DS}$), ALE (AS), and $\overline{WR}$ (R/$\overline{W}$) pins.
$\overline{CS1}$–$\overline{CS4}$	I	Chip Select 1. Must be low to read or write to channel 1 of the device. $\overline{CS1}$ is an active-low signal.
		Chip Select 2. Must be low to read or write to channel 2 of the device. $\overline{CS2}$ is an active-low signal.
		Chip Select 3. Must be low to read or write to channel 3 of the device. $\overline{CS3}$ is an active-low signal.
		Chip Select 4. Must be low to read or write to channel 4 of the device. $\overline{CS4}$ is an active-low signal.
PBEO1–PBEO4	O	PRBS Bit-Error Output. The receiver constantly searches for a 2^{15} - 1 (E1) or a QRSS (T1) PRBS, depending on the ETS bit setting (CCR1.7). It remains high if it is out of synchronization with the PRBS pattern. It goes low when synchronized to the PRBS pattern. Any errors in the received pattern after synchronization cause a positive-going pulse (with same period as E1 or T1 clock) synchronous with RCLK. PRBS bit errors can also be reported to the ECR1 and ECR2 registers by setting CCR6.2 to logic 1.
RCL1/LOTC1–RCL4/LOTC4	O	Receive Carrier Loss/Loss-of-Transmit Clock. An output that toggles high during a receive carrier loss (CCR2.7 = 0) or toggles high if the TCLK pin has not been toggled for 5µs ± 2µs (CCR2.7 = 1). CCR2.7 defaults to logic 0 when in hardware mode.
RTIP1–RTIP4	I	Receive Tip and Ring. Analog inputs for clock recovery circuitry. These pins connect through a 1:1 transformer to the line. See Section 7 for details.
RRING1–RRING4	I	
BPCLK1–BPCLK4	O	Backplane Clock. A 16.384MHz, 8.192MHz, 4.096MHz, or 2.048MHz clock output that is referenced to RCLK selectable through CCR5.7 and CCR5.6.
TTIP1–TTIP4	O	Transmit Tip and Ring. Analog line-driver outputs. These pins connect through a step-up transformer to the line. See Section 7 for details.
TRING1–TRING4	O	
RPOS1–RPOS4	O	Receive Positive Data. These bits are updated on the rising edge (CCR2.0 = 0) or the falling edge (CCR2.0 = 1) of RCLK with bipolar data out of the line interface. Set NRZE (CCR1.6) to 1 for NRZ applications. In NRZ mode, data is output on RPOS, and a received error (BPV, CV, or EXZ) causes a positive-going pulse synchronous with RCLK at RNEG.
RNEG1–RNEG4	O	Receive Negative Data. Updated on the rising edge (CCR2.0 = 0) or the falling edge (CCR2.0 = 1) of RCLK with the bipolar data out of the line interface. Set NRZE (CCR1.6) to 1 for NRZ applications. In NRZ mode, data is output on RPOS, and a received error (BPV, CV, or EXZ) causes a positive-going pulse synchronous with RCLK at RNEG.

PIN	I/O	FUNCTION
RCLK1–RCLK4	O	Receive Clock. Buffered recovered clock from the line. Synchronous to MCLK in absence of signal at RTIP and RRING.
TPOS1–TPOS4	I	Transmit Positive Data. Sampled on the falling edge (CCR2.1 = 0) or the rising edge (CCR2.1 = 1) of TCLK for data to be transmitted out onto the line.
TNEG1–TNEG4	I	Transmit Negative Data. Sampled on the falling edge (CCR2.1 = 0) or the rising edge (CCR2.1 = 1) of TCLK for data to be transmitted out onto the line.
TCLK1–TCLK4	I	Transmit Clock. A 2.048MHz or 1.544MHz primary clock. It is used to clock data through the transmit-side formatter. It can be sourced internally by MCLK or RCLK. See Common Control Register 1 and Figure 1-3.
JTRST	I	JTAG Reset
JTMS	I	JTAG Mode Select
JTCLK	I	JTAG Clock
JTDI	I	JTAG Data In
JTDO	O	JTAG Data Out
VSM	I	Voltage Supply Mode (LQFP only). Should be wired low for correct operation.
TVDD1–TVDD4	—	3.3V, ±5% Transmitter Positive Supply
VDD1–VDD4	—	3.3V, ±5% Positive Supply
TVSS1–TVSS4	—	Transmitter Signal Ground
VSS1–VSS4	—	Signal Ground

Table 2-D. Serial Interface Mode Pin Description

PIN	I/O	FUNCTION
$\overline{INT}$	I/O	Interrupt ($\overline{INT}$). Flags host controller during conditions and change of conditions defined in the status register. Active-low, open-drain output.
TXDIS/TEST	I	Tri-State Control, Multifunctional. Set this pin high with all $\overline{CS1}$–$\overline{CS4}$ inputs inactive to tri-state TTIP1–TTIP4 and TRING1–TRING4. Set this pin high with any of the $\overline{CS1}$–$\overline{CS4}$ inputs active to tri-state all outputs and I/O pins (including the parallel control port). Set low for normal operation.
$\overline{HRST}$	I	Hardware Reset. Bringing $\overline{HRST}$ low resets the DS21448, setting all control bits to the all-zeros default state.
MCLK	I	Master Clock. A 2.048MHz (±50ppm) clock source with TTL levels is applied at this pin. This clock is used internally for both clock/data recovery and for jitter attenuation. A T1 1.544MHz clock source is optional (Note 1).
BIS0/BIS1	I	Bus Interface Select Bit 0 and 1. Used to select bus interface option. See Table 2-A for details.
$\overline{CS1}$	I	Chip Select 1. Must be low to read or write to channel 1 of the device. $\overline{CS1}$ is an active-low signal.
$\overline{CS2}$	I	Chip Select 2. Must be low to read or write to channel 2 of the device. $\overline{CS2}$ is an active-low signal.
$\overline{CS3}$	I	Chip Select 3. Must be low to read or write to channel 3 of the device. $\overline{CS3}$ is an active-low signal.
$\overline{CS4}$	I	Chip Select 4. Must be low to read or write to channel 4 of the device. $\overline{CS4}$ is an active-low signal.
ICES	I	Input Clock-Edge Select. Selects whether the serial interface data input (SDI) is sampled on the rising (ICES = 0) or falling edge (ICES = 1) of SCLK.
OCES	I	Output Clock-Edge Select. Selects whether the serial interface data output (SDO) changes on the rising (OCES = 1) or falling edge (OCES = 0) of SCLK.
SCLK	I	Serial Clock. Serial interface clock.
SDI	I	Serial Data Input. Serial interface data input.
SDO	O	Serial Data Output. Serial interface data output.
PBEO1–PBEO4	O	PRBS Bit-Error Output. The receiver constantly searches for a 2^{15} - 1 (E1) or a QRSS (T1) PRBS, depending on the ETS bit setting (CCR1.7). It remains high if it is out of synchronization with the PRBS pattern. It goes low when synchronized to the PRBS pattern. Any errors in the received pattern after synchronization cause a positive-going pulse (with same period as E1 or T1 clock) synchronous with RCLK. PRBS bit errors can also be reported to the ECR1 and ECR2 registers by setting CCR6.2 to logic 1.
RCL1/LOTC1–RCL4/LOTC4	O	Receive Carrier Loss/Loss-of-Transmit Clock. An output that toggles high during a receive carrier loss (CCR2.7 = 0) or toggles high if the TCLK pin has not been toggled for 5µs ± 2µs (CCR2.7 = 1). CCR2.7 defaults to logic 0 when in hardware mode.
RTIP1–RTIP4 RRING1–RRING4	I	Receive Tip and Ring. Analog inputs for clock recovery circuitry. These pins connect through a 1:1 transformer to the line. See Section 7 for details.

PIN	I/O	FUNCTION
BPCLK1–BPCLK4	O	Backplane Clock. A 16.384MHz, 8.192MHz, 4.096MHz, or 2.048MHz clock output that is referenced to RCLK selectable through CCR5.7 and CCR5.6.
TTIP1–TTIP4	O	Transmit Tip and Ring. Analog line-driver outputs. These pins connect through a step-up transformer to the line. See Section 7 for details.
TRING–TRING4	O	
RPOS1–RPOS4	O	Receive Positive Data. Updated on the rising edge (CCR2.0 = 0) or the falling edge (CCR2.0 = 1) of RCLK with bipolar data out of the line interface. Set NRZE (CCR1.6) to 1 for NRZ applications. In NRZ mode, data is output on RPOS, and a received error (BPV, CV, or EXZ) causes a positive-going pulse synchronous with RCLK at RNEG.
RNEG1–RNEG4	O	Receive Negative Data. Updated on the rising edge (CCR2.0 = 0) or the falling edge (CCR2.0 = 1) of RCLK with the bipolar data out of the line interface. Set NRZE (CCR1.6) to 1 for NRZ applications. In NRZ mode, data is output on RPOS, and a received error (BPV, CV, or EXZ) causes a positive-going pulse synchronous with RCLK at RNEG.
RCLK1–RCLK4	O	Receive Clock. Buffered recovered clock from the line. Synchronous to MCLK in absence of signal at RTIP and RRING.
TPOS1–TPOS4	I	Transmit Positive Data. Sampled on the falling edge (CCR2.1 = 0) or the rising edge (CCR2.1 = 1) of TCLK for data to be transmitted out onto the line.
TNEG1–TNEG4	I	Transmit Negative Data. Sampled on the falling edge (CCR2.1 = 0) or the rising edge (CCR2.1 = 1) of TCLK for data to be transmitted out onto the line.
TCLK1–TCLK4	I	Transmit Clock. A 2.048MHz or 1.544MHz primary clock used to clock data through the transmit side formatter. They can be sourced internally by MCLK or RCLK. See Common Control Register 1 and Figure 1-3.
JTRST	I	JTAG Reset
JTMS	I	JTAG Mode Select
JTCLK	I	JTAG Clock
JTDI	I	JTAG Data In
JTDO	O	JTAG Data Out
VSM	I	Voltage Supply Mode (LQFP only). VSM should be wired low for correct operation.
TVDD1–TVDD4	—	3.3V, ±5% Transmitter Positive Supply
VDD1–VDD4	—	3.3V, ±5% Positive Supply
TVSS1–TVSS4	—	Transmitter Signal Ground for Transmitter Outputs
VSS1–VSS4	—	Signal Ground

Table 2-E. Hardware Interface Mode Pin Description

PIN	I/O	FUNCTION
ETS	I	E1/T1 Select 0 = E1 1 = T1
NRZE	I	NRZ Enable 0 = bipolar data at RPOS/RNEG and TPOS/TNEG 1 = NRZ data at RPOS and TPOS or TNEG; RNEG outputs a positive-going pulse when the device receives a BPV, CV, or EXZ.
SCLKE	I	Receive and Transmit Synchronization Clock Enable. SCLKE combines RSCLKE (CCR5.3) and TSCLKE (CCR5.2). 0 = disable 2.048MHz synchronization transmit and receive mode 1 = enable 2.048MHz synchronization transmit and receive mode
DJA	I	Disable Jitter Attenuator 0 = jitter attenuator enabled 1 = jitter attenuator disabled
JAMUX	I	Jitter Attenuator Clock Mux. Controls the source for JACLK. 0 = JACLK sourced from MCLK (2.048MHz or 1.544MHz at MCLK). 1 = JACLK sourced from internal PLL (2.048 MHz at MCLK).
JAS	I	Jitter Attenuator Path Select 0 = place the jitter attenuator on the receive side 1 = place the jitter attenuator on the transmit side
HBE	I	Receive and Transmit HDB3/B8ZS Enable. HBE combines RHBE (CCR2.3) and THBE (CCR2.2). 0 = enable HDB3 (E1)/B8ZS (T1) 1 = disable HDB3 (E1)/B8ZS (T1)
L0/L1/L2	I	Line Build-Out Select Bits 0,1, and 2. These pins set the transmitter build-out; see (Table 7-A (E1) and Table 7-B (T1).

PIN	I/O	FUNCTION
CES	I	Receive and Transmit Clock Select. Selects which RCLK edge to update RPOS and RNEG and which TCLK edge to sample TPOS and TNEG. CES combines TCES and RCES. 0 = update RPOS/RNEG on rising edge of RCLK; sample TPOS/TNEG on falling edge of TCLK 1 = update RPOS/RNEG on falling edge of RCLK; sample TPOS/TNEG on rising edge of TCLK
TPD	I	Transmit Power-Down 0 = normal transmitter operation 1 = powers down the transmitter and tri-states TTIP and TRING pins
TX0/TX1	I	Transmit Data Source Select Bits 0 and 1. These inputs determine the source of the transmit data (Table 4-B).
LOOP0/LOOP1	I	Loopback Select Bits 0 and 1. These inputs determine the active loopback mode (Table 4-A).
MM0/MM1	I	Monitor Mode Select Bits 0 and 1. These inputs determine if the receive equalizer is in a monitor mode (Table 4-D).
RT1/RT0	I	Receive LIU Termination Select Bits 0 and 1. These inputs determine the receive termination (Table 4-E).
TEST	I	Tri-State Control. Set high to tri-state all outputs and I/O pins (including the parallel control port). Set low for normal operation. Useful in board-level testing.
$\overline{\text{HRST}}$	I	Hardware Reset. Bringing $\overline{\text{HRST}}$ low resets the DS21448, setting all control bits to the all-zero default state.
MCLK	I	Master Clock. A 2.048MHz (±50ppm) clock source with TTL levels is applied at this pin. This clock is used internally for both clock/data recovery and for jitter attenuation. A T1 1.544MHz clock source is optional (Note 1). See Table 4-F for details.
BIS0/BIS1	I	Bus Interface Select Bit 0 and 1. Used to select bus interface option (Table 2-A).
EGL1–EGL4	I	Receive Equalizer Gain-Limit Select. These bits control the sensitivity of the receive equalizers (Table 4-C).
PBEO1–PBEO4	O	PRBS Bit-Error Output. The receiver constantly searches for a 2^{15} - 1 PRBS (ETS = 0) or a QRSS PRBS (ETS = 1). The pattern is chosen automatically by the value of the ETS pin. It remains high if it is out of synchronization with the PRBS pattern. It goes low when synchronized to the PRBS pattern. Any errors in the received pattern after synchronization cause a positive-going pulse (with same period as E1 or T1 clock) synchronous with RCLK.
RCL1–RCL4	O	Receive Carrier Loss. An output that toggles high during a receive carrier loss.
RTIP1–RTIP4	I	Receive Tip and Ring. Analog inputs for clock recovery circuitry. These pins connect through a 1:1 transformer to the line. See Section 7 for details.
RRING1–RRING4	I	
BPCLK1–BPCLK4	O	Backplane Clock. A 16.384MHz clock output that is referenced to RCLK.
TTIP1–TTIP4	O	Transmit Tip and Ring. Analog line-driver outputs. These pins connect through a step-up transformer to the line. See Section 7 for details.
TRING1–TRING4		
RPOS1–RPOS4	O	Receive Positive Data. Updated on the rising edge (CES = 0) or the falling edge (CES = 1) of RCLK with bipolar data out of the line interface. In NRZ mode (NRZE = 1), data is output on RPOS, and a received error (BPV, CV, or EXZ) causes a positive-going pulse synchronous with RCLK at RNEG.
RNEG1–RNEG4	O	Receive Negative Data. Updated on the rising edge (CES = 0) or the falling edge (CES = 1) of RCLK with bipolar data out of the line interface. In NRZ mode (NRZE = 1), data is output on RPOS, and a received error (BPV, CV, or EXZ) causes a positive-going pulse synchronous with RCLK at RNEG.
RCLK1–RCLK4	O	Receive Clock. Buffered recovered clock from the line. Synchronous to MCLK in absence of signal at RTIP and RRING.
TPOS1–TPOS4	I	Transmit Positive Data. Sampled on the falling edge (CES = 0) or the rising edge (CES = 1) of TCLK for data to be transmitted out onto the line.
TNEG1–TNEG4	I	Transmit Negative Data. Sampled on the falling edge (CES = 0) or the rising edge (CES = 1) of TCLK for data to be transmitted out onto the line.
TCLK1–TCLK4	I	Transmit Clock. A 2.048MHz or 1.544MHz primary clock used to clock data through the transmit side formatter. It can be sourced internally by MCLK or RCLK. See Common Control Register 1 and Figure 1-3.
JTRST	I	JTAG Reset
JTMS	I	JTAG Mode Select
JTCLK	I	JTAG Clock
JTDI	I	JTAG Data In
JTDO	O	JTAG Data Out
VSM	I	Voltage Supply Mode (LQFP only). VSM should be wired low for correct operation.
TVDD1–TVDD4	–	3.3V, ±5% Transmitter Positive Supply
VDD1–VDD4	—	3.3V, ±5% Positive Supply

PIN	I/O	FUNCTION
TVSS1–TVSS4	—	Transmitter Signal Ground for Transmitter Outputs
VSS1–VSS4	—	Signal Ground

Note 1: G.703 requires an accuracy of ±50ppm for T1 and E1. TR62411 and ANSI specs require ±32ppm accuracy for T1 interfaces.

3. DETAILED DESCRIPTION

The DS21448 has a usable receiver sensitivity of 0 to -43dB for E1 applications and 0 to -36dB for T1 that allows it to operate on 0.63mm (22AWG) cables up to 2.5km (E1) and 6000ft (T1) in length. The user has the option to use internal receive termination, software selectable for 75Ω, 100Ω, and 120Ω applications, or external termination. The on-board crystal-less jitter attenuator can be placed in either the transmit or the receive data path, and requires only a 2.048MHz MCLK for both E1 and T1 applications (with the option of using a 1.544MHz MCLK in T1 applications).

The DS21448 has diagnostic capabilities such as loopbacks and PRBS pattern generation and detection. 16-bit loop-up and loop-down codes can be generated and detected. A single input pin can power down all transmitters to allow the implementation of hitless protection switching (HPS) for 1+1 redundancy without the use of relays. The device can be controlled through an 8-bit parallel port (muxed or nonmuxed) or a serial port, and it can be used in hardware mode. A standard boundary scan interface supports board-level testing.

The DS21448 contains four independent LIUs that share a common interface for configuration and status. The user can choose between three different means of accessing the device: a parallel microprocessor interface, a serial interface, and a hardwired mode, which configures the device by setting levels on the device's pins. The DS21448's four chip selects ($\overline{CS1}$, $\overline{CS2}$, $\overline{CS3}$, and $\overline{CS4}$) determine which LIU is accessed when using the parallel or serial interface modes. Four sets of identical register maps exist, one for each channel. Using the appropriate chip select accesses a channel's register map.

The analog AMI/HDB3 waveform off the E1 line or the AMI/B8ZS waveform off the T1 line is transformer-coupled into the RTIP and RRING pins of the DS21448. The user has the option to use internal termination, software selectable for 75Ω/100Ω/120Ω applications, or external termination. The device recovers clock and data from the analog signal and passes it through the jitter attenuation mux, outputting the received line clock at RCLK and bipolar or NRZ data at RPOS and RNEG. The DS21448 contains an active filter that reconstructs the analog-received signal for the nonlinear losses that occur in transmission. The receive circuitry is also configurable for various monitor applications. The device has a usable receive sensitivity of 0 to -43dB for E1 and 0 to -36dB for T1 that allows the device to operate on 0.63mm (22AWG) cables up to 2.5km (E1) and 6k feet (T1) in length. Data input at TPOS and TNEG is sent through the jitter attenuation mux to the waveshaping circuitry and line driver. The DS21448 drives the E1 or T1 line from the TTIP and TRING pins through a coupling transformer. The line driver can handle both CEPT 30/ISDN-PRI lines for E1 and long-haul (CSU) or short-haul (DSX-1) lines for T1.

3.1 DS21448 and DS21Q348 Differences

The DS21448 BGA is a monolithic quad-port LIU that is a replacement for the DS21Q348. The additional features of JTAG, transmit driver disable, and the serial interface in the DS21448 have changed the function of several pins, as shown in Table 3-A.

Table 3-A. DS21448 vs. DS21Q348 Pin Differences

PIN	DS21Q348	DS21448
G4	VSM	N.C.
J1	VSS	SCLK
K1	A4	A4/SDO
K3	VSS	SDI
K7	TEST	TXDIS/TEST
L3	N.C.	JTRST*
M3	N.C.	JTMS*
M5	N.C.	JTCLK
M6	N.C.	JTDI*
M7	N.C.	JTDO

**DS21448 pin is internally pulled up.*

4. PORT OPERATION

4.1 Hardware Mode

The DS21448 supports a hardware configuration mode that allows the user to configure the device by setting levels on the device's pins. This mode allows the DS21448 configuration without the use of a microprocessor, simplifying designs. Not all of the device features are supported in the hardware mode.

In hardware mode (BIS0 = 1, BIS1 = 1) several pins have been redefined so they can be used for initializing the DS21448. Refer to Table 2-B and Table 2-E for pin assignment and definition. Because of limited pin count, several functions have been combined and affect all four channels in the device and/or treat the receive and transmit paths as one block. Restrictions when using the hardware mode include the following:

- BPCLK pins only output a 16.384MHz signal.
- The RCL/LOTC pins are designated to RCL.
- The RHBE and THBE control bits are combined and controlled by HBE.
- RSCLKE and TSCLKE bits are combined and controlled by SCLKE.
- TCES and RCES are combined and controlled by CES.
- The transmitter functions are combined and controlled by TX1 and TX0.
- Loopback functions are controlled by LOOP1 and LOOP0.
- JABDS defaults to 128-bit buffer depth.
- All other control bits default to logic 0.

Table 4-A. Loopback Control in Hardware Mode

LOOPBACK	SYMBOL	LOOP1	LOOP0
Remote Loopback	RLB	1	1
Local Loopback	LLB	1	0
Analog Loopback	ALB	0	1
No Loopback	—	0	0

Table 4-B. Transmit Data Control in Hardware Mode

TRANSMIT DATA	SYMBOL	TX1	TX0
Unframed All Ones	TUA1	1	1
Alternating Ones and Zeros	TAOZ	1	0
PRBS	TPRBSE	0	1
TPOS and TNEG	—	0	0

Table 4-C. Receive Sensitivity Settings in Hardware Mode

EGL	ETS	RECEIVE SENSITIVITY (dB)
0	0 (E1)	-12 (short haul)
1	0 (E1)	-43 (long haul)
1	1 (T1)	-30 (limited long haul)
0	1 (T1)	-36 (long haul)

Table 4-D. Monitor Gain Settings in Hardware Mode

MM1	MM0	INTERNAL LINEAR GAIN BOOST (dB)
0	0	Normal operation (no boost)
0	1	20
1	0	26
1	1	32

Table 4-E. Internal Rx Termination Select in Hardware Mode

RT1	RT0	INTERNAL RECEIVE TERMINATION CONFIGURATION
0	0	Internal receive-side termination disabled
0	1	Internal receive-side 120Ω enabled
1	0	Internal receive-side 100Ω enabled
1	1	Internal receive-side 75Ω enabled

Table 4-F. MCLK Selection in Hardware Mode

MCLK (MHz)	JAMUX	ETS
2.048	0	0
2.048	1	1
1.544	0	1

4.2 Serial Port Operation

Setting BIS1 = 1 and BIS0 = 0 enables the serial bus interface on the DS21448 (Table 2-A). Serial port read/write timing is unrelated to the system transmit and receive timing, allowing asynchronous reads or writes by the host. See Section 10 for the AC timing of the serial port. All serial port accesses are LSB first. See Figure 4-1, Figure 4-2, Figure 4-3, Figure 4-4, Figure 4-5, and Figure 4-6 for additional details.

A serial bus access requires the use of four signals: serial clock (SCLK), one of the four chip selects ($\overline{CS}$), serial data input (SDI), and serial data output (SDO). The DS21448 uses SCLK to sample data that is present on SDI and output data onto SDO. Input clock-edge select (ICES) allows the user to choose which SCLK edge input data is sampled on. Output clock-edge select (OCES) allows the user to choose which SCLK edge output data changes on. When ICES is low, input data is latched on the rising edge of SCLK, and when ICES is high, input data is latched on the falling edge of SCLK. When OCES is low, data is output on the falling edge of SCLK, and when OCES is high, data is output on the rising edge of SCLK. Data is held until the next falling or rising edge of SCLK. All data transfers are initiated by driving the appropriate port's $\overline{CS}$ input low and ends with $\overline{CS}$ going inactive. $\overline{CS}$ must go inactive between data transfers. See the serial bus timing information in Section 10 for details. All data transfers are terminated if the port's $\overline{CS}$ input transitions high. Port control logic is disabled, and SDO is tri-stated when all $\overline{CS}$ pins are inactive.

Reading from or writing to the internal registers requires writing one address/command byte prior to the transferring register data. Two types of serial bus transfers exist, standard and burst. The standard serial bus access always consists of two bytes, an address/command byte that is always supplied by the user on SDI, and a data byte that can either be written to the DS21448 using SDI (write operation) or output by the DS21448 on SDO (read operation). The burst serial bus access consists of a single address/command byte followed either by 22 read or 22 write data bytes.

The first bit written (LSB) of the address/command byte specifies whether the access is to be a read (1) or a write (0). The next 5 bits identify the register address. Valid register addresses are 00h through 15h. Bit 7 is reserved and must be set to 0 for proper operation. Bit 8, the last bit (MSB) of the address/command byte, is the burst mode-enable bit. When the burst bit is enabled (set to 0) and a READ operation is performed, the DS21448 automatically outputs the contents of registers 00h through 15h sequentially, starting with register address 00h. When the burst bit is enabled and a WRITE operation is performed, data supplied on SDI is sequentially written into the DS21448's register space starting at address 00h. Burst operation is stopped once address 15h is read or $\overline{CS}$ goes inactive. For both burst read and burst write transfers, the address/command byte's register address bits must be set to 0.

The user can broadcast register write accesses to multiple ports simultaneously by enabling the desired channels' chip selects at the same time. However, only one port can be read at a time. Any attempt to read multiple ports simultaneously results in invalid data being returned on SDO.

Figure 4-1. Serial Port Operation for Read Access (R = 1) Mode 1

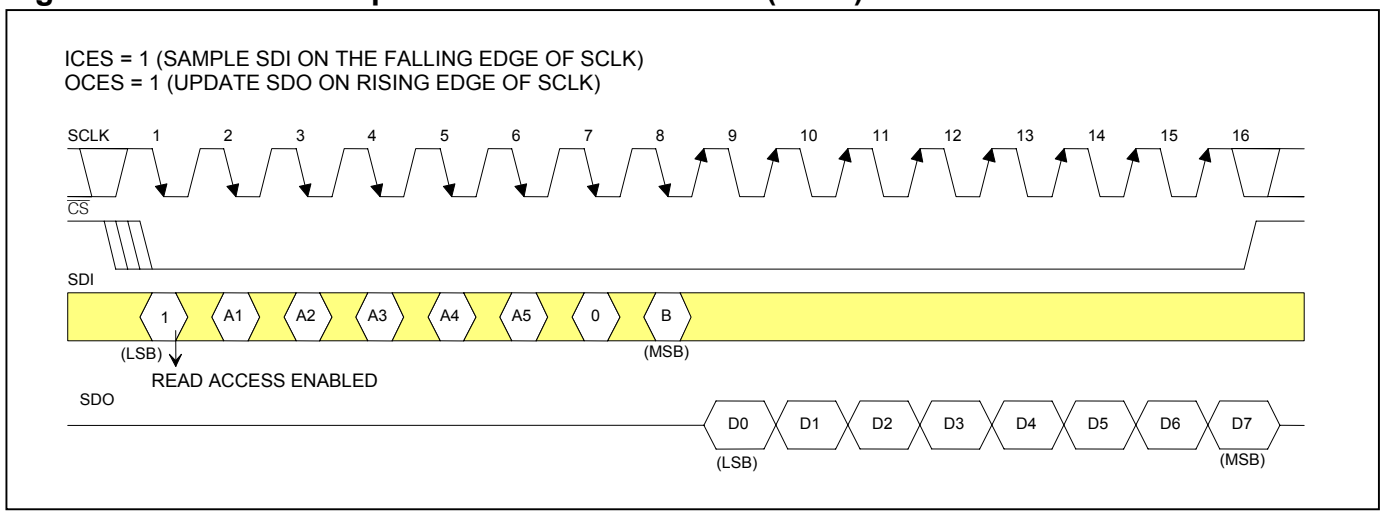


Figure 4-2. Serial Port Operation for Read Access (R = 1) Mode 2

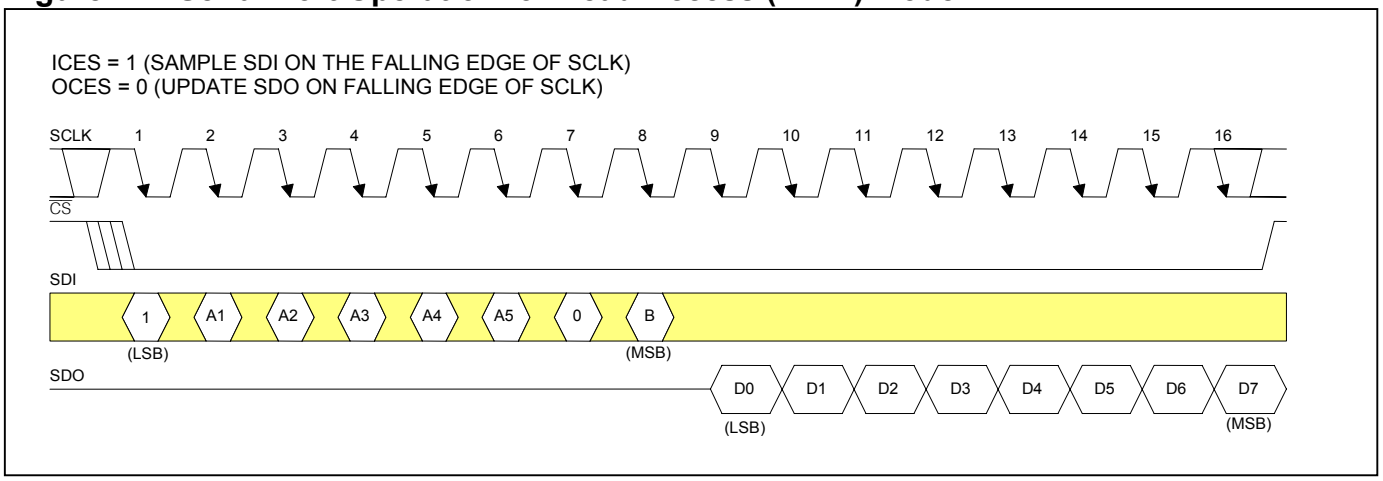


Figure 4-3. Serial Port Operation for Read Access (R = 1) Mode 3

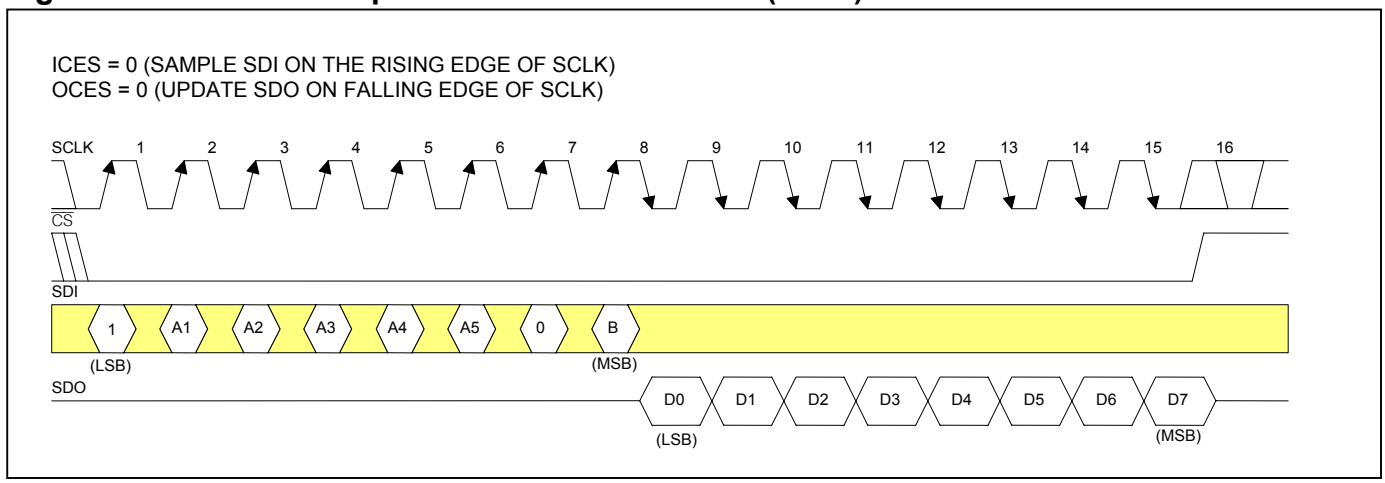


Figure 4-4. Serial Port Operation for Read Access (R = 1) Mode 4

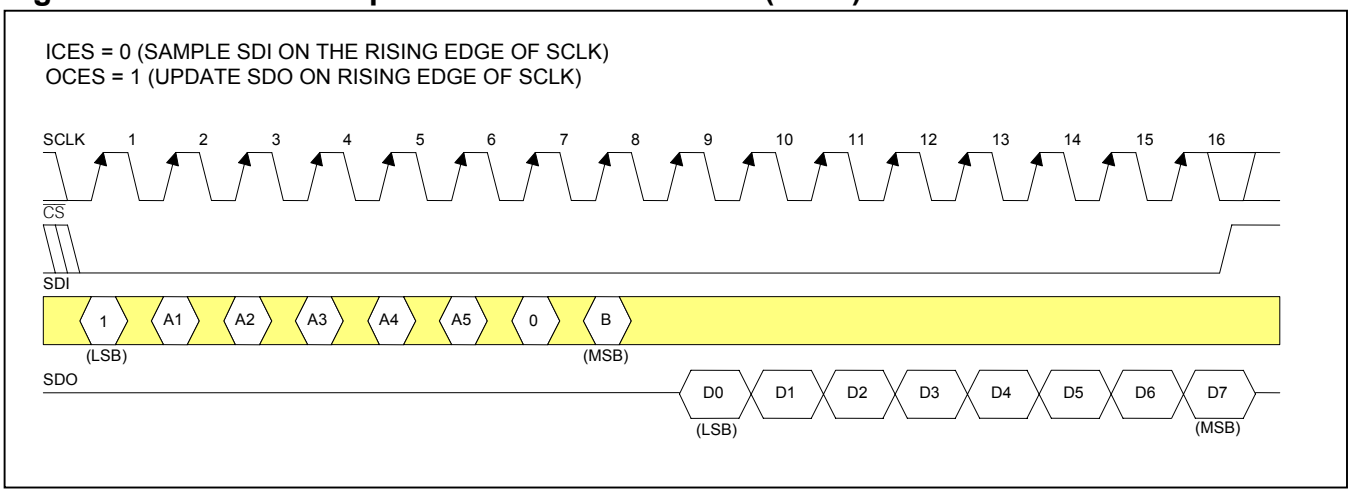


Figure 4-5. Serial Port Operation for Write Access (R = 0) Modes 1 and 2

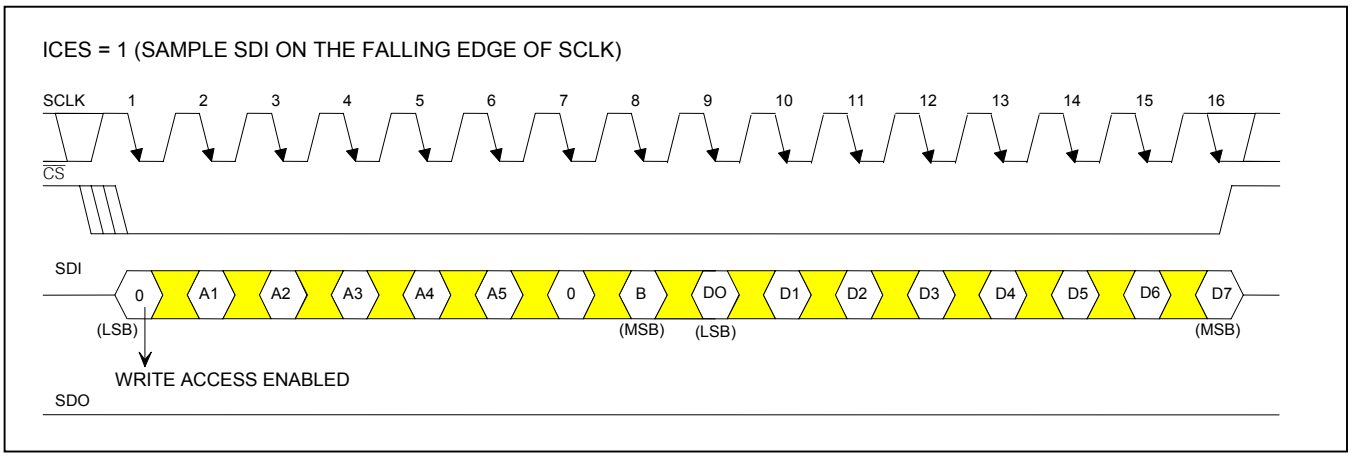
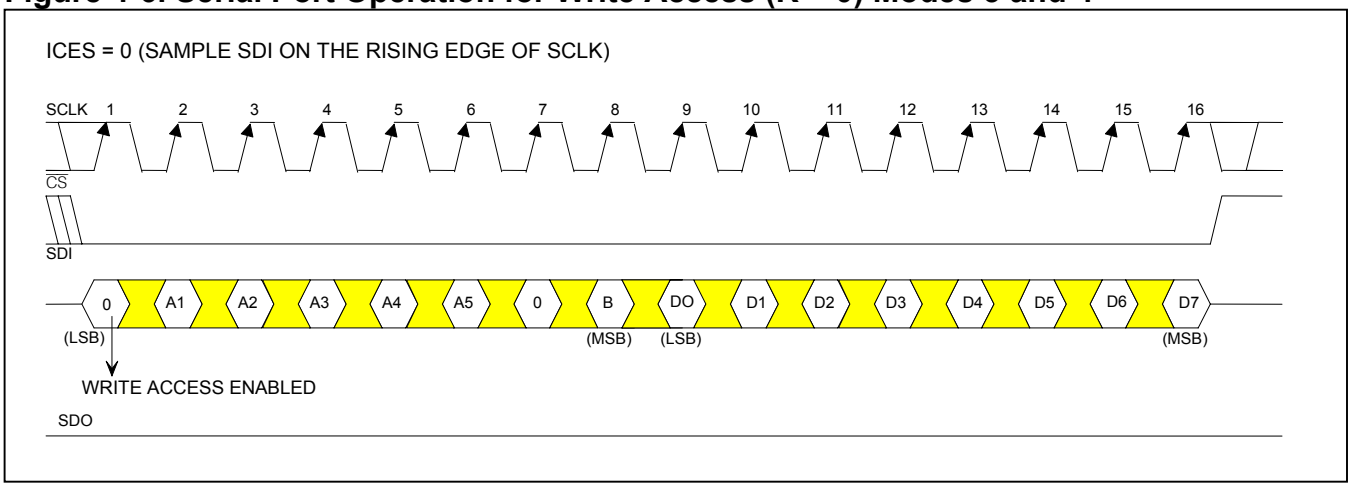


Figure 4-6. Serial Port Operation for Write Access (R = 0) Modes 3 and 4



4.3 Parallel Port Operation

The option for either multiplexed bus operation (BIS0 = 0) or nonmultiplexed bus operation (BIS0 = 1) is available when using the parallel interface. The DS21448 can operate with either Intel or Motorola bus timing configurations. If the PBTS pin is wired low, Intel timing is selected; if wired high, Motorola timing is selected. All Motorola bus signals are listed in parentheses (). Four sets of identical register maps exist, one for each channel. See Table 4-H for register names and addresses. Use the appropriate chip select ($\overline{CS1}$, $\overline{CS2}$, $\overline{CS3}$, or $\overline{CS4}$) to access a channel's register map. See the timing diagrams in Section 10 for more details. Hardware and serial port modes are not supported when using parallel port operation.

4.3.1 Device Power-Up and Reset

The DS21448 resets itself upon power-up, setting all writeable registers to 00h and clearing the status and information registers. CCR3.7 (TUA1) = 0 results in the LIU transmitting unframed all ones. After the power supplies have settled, initialize all control registers to the desired settings, then toggle the LIRST bit (CCR3.2). The DS21448 can at any time be reset to the default settings by bringing $\overline{HRST}$ low (level triggered) or by powering down and powering up again.

Table 4-G. Parallel Port Mode Selection

PBTS	BIS0	PROCESSOR	BUS INTERFACE TYPE
0	0	Intel	Parallel Port Mode (Multiplexed)
0	1	Intel	Parallel Port Mode (Nonmultiplexed)
1	0	Motorola	Parallel Port Mode (Multiplexed)
1	1	Motorola	Parallel Port Mode (Nonmultiplexed)

4.3.2 Register Map

Table 4-H shows the typical register map for all four ports. Use the appropriate chip select ($\overline{CS1}$, $\overline{CS2}$, $\overline{CS3}$, or $\overline{CS4}$) to access a channel's register map.

Table 4-H. Register Map

NAME	R/W	ADDRESS	FUNCTION
CCR1	R/W	00h	Common Control Register 1
CCR2	R/W	01h	Common Control Register 2
CCR3	R/W	02h	Common Control Register 3
CCR4	R/W	03h	Common Control Register 4
CCR5	R/W	04h	Common Control Register 5
CCR6	R/W	05h	Common Control Register 6
SR	R	06h	Status Register
IMR	R/W	07h	Interrupt Mask Register
RIR1	R	08h	Receive Information Register 1
RIR2	R	09h	Receive Information Register 2
IBCC	R/W	0Ah	In-Band Code Control Register
TCD1	R/W	0Bh	Transmit Code Definition Register 1
TCD2	R/W	0Ch	Transmit Code Definition Register 2
RUPCD1	R/W	0Dh	Receive-Up Code Definition Register 1
RUPCD2	R/W	0Eh	Receive-Up Code Definition Register 2
RDNCD1	R/W	0Fh	Receive-Down Code Definition Register 1
RDNCD2	R/W	10h	Receive-Down Code Definition Register 2
ECR1	R	11h	Error Count Register 1
ECR2	R	12h	Error Count Register 2
TEST1	R/W	13h	Test 1
TEST2	R/W	14h	Test 2
TEST2	R/W	15h	Test 3
—	—	(Note 1)	—

Note 1: Register addresses 16h–1Fh do not exist.

4.3.3 Control Registers

CCR1 (00H): Common Control Register 1

(MSB)							(LSB)
ETS	NRZE	RCLA	ECUE	JAMUX	TTOJ	TTOR	LOTCMC

NAME	POSITION	FUNCTION
ETS	CCR1.7	E1/T1 Select 0 = E1 1 = T1
NRZE	CCR1.6	NRZ Enable 0 = bipolar data at RPOS/RNEG and TPOS/TNEG 1 = NRZ data at RPOS and TPOS or TNEG; RNEG outputs a positive-going pulse when the device receives a BPV, CV, or EXZ
RCLA	CCR1.5	Receive-Carrier-Loss Alternate Criteria 0 = RCL declared upon 255 (E1) or 192 (T1) consecutive zeros 1 = RCL declared upon 2048 (E1) or 1544 (T1) consecutive zeros
ECUE	CCR1.4	Error Counter Update Enable. A 0-to-1 transition forces the next receive clock cycle to load the error counter registers with the latest counts and reset the counters. The user must wait a minimum of two clock cycles (976ns for E1 and 1296ns for T1) before reading the error count registers to allow for a proper update. See Section 6 for details.
JAMUX	CCR1.3	Jitter Attenuator Clock Mux. Controls the source for JACLK (Figure 1-1). 0 = JACLK sourced from MCLK (2.048MHz or 1.544MHz at MCLK) 1 = JACLK sourced from internal PLL (2.048MHz at MCLK)
TTOJ	CCR1.2	TCLK to JACLK. Internally connects TCLK to JACLK (Figure 1-3). 0 = disabled 1 = enabled
TTOR	CCR1.1	TCLK to RCLK. Internally connects TCLK to RCLK (Figure 1-3). 0 = disabled 1 = enabled
LOTCMC	CCR1.0	Loss-of-Transmit Clock Mux Control. Determines whether the transmit logic should switch to JACLK if the TCLK input should fail to transition (Figure 1-3). 0 = do not switch to JACLK if TCLK stops 1 = switch to JACLK if TCLK stops

CCR2 (01H): Common Control Register 2

(MSB)							(LSB)
RLPIN	—	SCLD	CLDS	RHBE	THBE	TCES	RCES

NAME	POSITION	FUNCTION
RLPIN	CCR2.7	RCL/LOTC Pin Function Select. Forced to logic 0 in hardware mode. 0 = toggles high during a receive-carrier loss condition 1 = toggles high if TCLK does not transition for at least 5μs
—	CCR2.6	Not Assigned. Should be set to 0 when written to.
SCLD	CCR2.5	Short Circuit-Limit Disable (ETS = 0). Controls the 50mA (RMS) current limiter. 0 = enable 50mA current limiter 1 = disable 50mA current limiter
CLDS	CCR2.4	Custom Line-Driver Select. Setting this bit to 1 redefines the operation of the transmit line driver. When this bit is set to 1 and CCR4.5 = CCR4.6 = CCR4.7 = 0, the device generates a square wave at the TTIP and TRING outputs instead of a normal waveform. When this bit is set to 1 and CCR4.5 = CCR4.6 = CCR4.7 ≠ 0, the device forces TTIP and TRING outputs to become open-drain drivers instead of their normal push-pull operation. This bit should be set to 0 for normal operation of the device. Contact the factory for more details about how to use this bit.
RHBE	CCR2.3	Receive HDB3/B8ZS Enable 0 = enable HDB3 (E1)/B8ZS (T1) 1 = disable HDB3 (E1)/B8ZS (T1)
THBE	CCR2.2	Transmit HDB3/B8ZS Enable 0 = enable HDB3 (E1)/B8ZS (T1) 1 = disable HDB3 (E1)/B8ZS (T1)
TCES	CCR2.1	Transmit Clock-Edge Select. Selects which TCLK edge to sample TPOS and TNEG. 0 = sample TPOS and TNEG on falling edge of TCLK 1 = sample TPOS and TNEG on rising edge of TCLK
RCES	CCR2.0	Receive Clock-Edge Select. Selects which RCLK edge to update RPOS and RNEG. 0 = update RPOS and RNEG on rising edge of RCLK 1 = update RPOS and RNEG on falling edge of RCLK

CCR3 (02H): Common Control Register 3

(MSB)							(LSB)
TUA1	ATUA1	TAOZ	TPRBSE	TLCE	LIRST	IBPV	IBE

NAME	POSITION	FUNCTION
TUA1	CCR3.7	Transmit Unframed All Ones. The polarity of this bit is set such that the device transmits an all-ones pattern on power-up or device reset. This bit must be set to 1 to allow the device to transmit data. The transmission of this data pattern is always timed off JACLK (Figure 1-1). 0 = transmit all ones at TTIP and TRING 1 = transmit data normally
ATUA1	CCR3.6	Automatic Transmit Unframed All Ones. Automatically transmit an unframed all-ones pattern at TTIP and TRING during an RCL condition. 0 = disabled 1 = enabled
TAOZ	CCR3.5	Transmit Alternate Ones and Zeros. Transmit a …101010… pattern at TTIP and TRING. The transmission of this data pattern is always timed off TCLK. 0 = disabled 1 = enabled
TPRBSE	CCR3.4	Transmit PRBS Enable. Transmit a 2^{15} - 1 (E1) or a QRSS (T1) PRBS at TTIP and TRING. 0 = disabled 1 = enabled
TLCE	CCR3.3	Transmit Loop-Code Enable. Enables the transmit side to transmit the loop-up code in the transmit code definition registers (TCD1 and TCD2). See Section 6 for details. 0 = disabled 1 = enabled
LIRST	CCR3.2	Line Interface Reset. Setting this bit from 0 to 1 initiates an internal reset that resets the clock recovery state machine and recenters the jitter attenuator. Normally this bit is only toggled on power-up. It must be cleared and set again for a subsequent reset.
IBPV	CCR3.1	Insert Bipolar Violation (BPV). A 0-to-1 transition on this bit causes a single bipolar violation to be inserted into the transmit data stream. Once this bit has been toggled from 0 to 1, the device waits for the next occurrence of three consecutive 1s to insert the BPV. This bit must be cleared and set again for a subsequent error to be inserted (Figure 1-3).
IBE	CCR3.0	Insert Bit Error. A 0-to-1 transition on this bit causes a single logic error to be inserted into the transmit data stream. This bit must be cleared and set again for a subsequent error to be inserted (Figure 1-3).

CCR4 (03H): Common Control Register 4

(MSB)							(LSB)
L2	L1	L0	EGL	JAS	JABDS	DJA	TPD

NAME	POSITION	FUNCTION
L2	CCR4.7	Line Build-Out Select Bit 2. Sets the transmitter build-out (Table 7-A for E1, Table 7-B for T1).
L1	CCR4.6	Line Build Out Select Bit 1. Sets the transmitter build-out (Table 7-A for E1, Table 7-B for T1).
L0	CCR4.5	Line Build Out Select Bit 0. Sets the transmitter build-out (Table 7-A for E1, Table 7-B for T1).
EGL	CCR4.4	Receive Equalizer Gain Limit. This bit controls the sensitivity of the receive equalizer (Table 4-I).
JAS	CCR4.3	Jitter Attenuator Path Select 0 = place the jitter attenuator on the receive side 1 = place the jitter attenuator on the transmit side
JABDS	CCR4.2	Jitter Attenuator Buffer Depth Select 0 = 128 bits 1 = 32 bits (use for delay-sensitive applications)
DJA	CCR4.1	Disable Jitter Attenuator 0 = jitter attenuator enabled 1 = jitter attenuator disabled
TPD	CCR4.0	Transmit Power-Down 0 = normal transmitter operation 1 = powers down the transmitter and tri-states the TTIP and TRING pins

Table 4-I. Receive Sensitivity Settings

EGL (CCR4.4)	ETS (CCR1.7)	RECEIVE SENSITIVITY (dB)
0	0 (E1)	-12 (short haul)
1	0 (E1)	-43 (long haul)
1	1 (T1)	-30 (limited long haul)
0	1 (T1)	-36 (long haul)

CCR5 (04H): Common Control Register 5

(MSB)							(LSB)
BPCS1	BPCS0	MM1	MM0	RSCLKE	TSCLKE	RT1	RT0

NAME	POSITION	FUNCTION
BPCS1	CCR5.7	Backplane Clock Frequency Select 1. See Table 4-J for details.
BPCS0	CCR5.6	Backplane Clock Frequency Select 0. See Table 4-J for details.
MM1	CCR5.5	Monitor Mode Gain Select 1 (Table 4-K.)
MM0	CCR5.4	Monitor Mode Gain Select 0. See (Table 4-K.
RSCLKE	CCR5.3	Receive Synchronization Clock Enable 0 = disable 2.048MHz synchronization receive mode 1 = enable 2.048MHz synchronization receive mode
TSCLKE	CCR5.2	Transmit Synchronization Clock Enable 0 = disable 2.048MHz transmit synchronization clock 1 = enable 2.048MHz transmit synchronization clock
RT1	CCR5.1	Receive Termination Select 1. See Table 4-L for details.
RT0	CCR5.0	Receive Termination Select 0. See Table 4-L for details.

Table 4-J. Backplane Clock Select

BPCS1 (CCR5.7)	BPCS0 (CCR5.6)	BPCLK FREQUENCY (MHz)
0	0	16.384
0	1	8.192
1	0	4.096
1	1	2.048

Table 4-K. Monitor Gain Settings

MM1 (CCR5.5)	MM0 (CCR5.4)	INTERNAL LINEAR GAIN BOOST (dB)
0	0	Normal operation (no boost)
0	1	20
1	0	26
1	1	32

Table 4-L. Internal Rx Termination Select

RT1 (CCR5.1)	RT0 (CCR5.0)	INTERNAL RECEIVE TERMINATION CONFIGURATION
0	0	Internal receive-side termination disabled
0	1	Internal receive-side 120Ω enabled
1	0	Internal receive-side 100Ω enabled
1	1	Internal receive-side 75Ω enabled

CCR6 (05H): Common Control Register 6

(MSB)							(LSB)
LLB	RLB	ARLBE	ALB	RJAB	ECRS2	ECRS1	ECRS0

NAME	POSITION	FUNCTION
LLB	CCR6.7	Local Loopback. In local loopback, transmit data is looped back to the receive path, passing through the jitter attenuator if it is enabled. Data in the transmit path acts as normal. See Section 6.2 for details. 0 = loopback disabled 1 = loopback enabled
RLB	CCR6.6	Remote Loopback. In remote loopback, data output from the clock/data recovery circuitry is looped back to the transmit path, passing through the jitter attenuator if it is enabled. Data in the receive path acts as normal, while data presented at TPOS and TNEG is ignored. See Section 6.2 for details. 0 = loopback disabled 1 = loopback enabled
ARLBE	CCR6.5	Automatic Remote Loopback Enable and Reset. When this bit is set high, the device automatically goes into remote loopback when it detects loop-up code programmed into the receive loop-up code definition registers (RUPCD1 and RUPCD2) for a minimum of 5 seconds; it also sets the RIR2.1 status bit. Once it is in an RLB state, the bit remains in this state until it has detected the loop code programmed into the receive loop-down code definition registers (RDNCD1 and RDNCD2) for a minimum of 5 seconds, at which point it forces the device out of RLB and clears RIR2.1. Toggling this bit from 1 to 0 resets the automatic RLB circuitry. The action of the automatic remote loopback circuitry is logically ORed with the RLB (CCR6.6) control bit (i.e., either one can cause a RLB to occur).
ALB	CCR6.4	Analog Loopback. In analog loopback, signals at TTIP and TRING are internally connected to RTIP and RRING. The incoming line signals at RTIP and RRING are ignored. The signals at TTIP and TRING are transmitted as normal. See Section 6.2 for more details. 0 = loopback disabled 1 = loopback enabled
RJAB	CCR6.3	RCLK Jitter Attenuator Bypass. This control bit allows the receive-recovered clock and data to bypass the jitter attenuation, while still allowing the BPCLK output to use the jitter attenuator. See Section 7.3 for details. 0 = disabled 1 = enabled
ECRS2	CCR6.2	Error Count Register Select 2. See Section 6.4 for details.
ECRS1	CCR6.1	Error Count Register Select 1. See Section 6.4 for details.
ECRS0	CCR6.0	Error Count Register Select 0. See Section 6.4 for details.

5. STATUS REGISTERS

The three registers that contain information about the device's real-time status are the status register (SR) and receive information registers 1 and 2 (RIR1/RIR2). When a particular event has occurred (or is occurring), the appropriate bit in one of these registers is set to 1. Some bits in SR, RIR1, and RIR2 are latched bits and some are real-time bits (denoted in the following register descriptions). For latched status bits, when an event or an alarm occurs, the bit is set to 1 and remains set until the user reads that bit. The bit is cleared when it is read, and it is not set until the event has occurred again. Two of the latched status bits (RUA1 and RCL) remain set after reading if the alarm is still present.

The user always precedes a read of any of the three status registers with a write. The byte written to the register informs the DS21448 which bits the user wishes to read and have cleared. The user writes a byte to one of these registers with a 1 in the bit positions to be read and a 0 in the other bit positions. When a 1 is written to a bit location, that location is updated with the latest information. When a 0 is written to a bit position, that bit position is not updated, and the previous value is held. A write to the status and information registers is immediately followed by a read of the same register. The read result should be logically ANDed with the mask byte that was just written, and this value should be written back into the same register to ensure that bit does indeed clear. This second write step is necessary because the alarms and events in the status registers occur asynchronously with respect to their access through the parallel port. This write-read-write scheme allows an external microcontroller or microprocessor to individually poll certain bits without disturbing the other bits in the register. This operation is key in controlling the DS21448 with higher-order software languages.

The bits in the SR register have the unique ability to initiate a hardware interrupt through the $\overline{INT}$ output pin. Each of the alarms and events in the SR can be either masked or unmasked from the interrupt pin through the interrupt mask register (IMR). The interrupts caused by the RCL, RUA1, and LOTC bits in the SR act differently than the interrupts caused by the other status bits in the SR. The RCL, RUA1, and LOTC bits forces the $\overline{INT}$ pin low whenever they change state (i.e., go active or inactive). The $\overline{INT}$ pin is allowed to return high (if no other interrupts are present) when the user reads the alarm bit that caused the interrupt to occur, even if the alarm is still present. The other status bits in the SR can force the $\overline{INT}$ pin low when they are set. The $\overline{INT}$ pin is allowed to return high (if no other interrupts are present) when the user reads the event bit that caused the interrupt to occur.

The host can quickly determine which of the four LIU channels is generating an interrupt by reading one of the unused addresses in the 16h–1Fh range in any LIU channel. See the following LIU channel interrupt status description for additional information.

LIU Channel Interrupt Status

(MSB)							(LSB)
—	—	—	—	LIU4	LIU3	LIU2	LIU1

NAME	POSITION	FUNCTION
N/A	7	Not Assigned. Could be any value when read.
N/A	6	Not Assigned. Could be any value when read.
N/A	5	Not Assigned. Could be any value when read.
N/A	4	Not Assigned. Could be any value when read.
LIU4	3	LIU4 Status Register. A 1 in this bit position indicates that the status register (SR) in channel 4 is asserting an interrupt.
LIU3	2	LIU3 Status Register. A 1 in this bit position indicates that the status register (SR) in channel 3 is asserting an interrupt.
LIU2	1	LIU2 Status Register. A 1 in this bit position indicates that the status register (SR) in channel 2 is asserting an interrupt.
LIU1	0	LIU1 Status Register. A 1 in this bit position indicates that the status register (SR) in channel 1 is asserting an interrupt.

SR (06H): Status Register

(MSB)							(LSB)
LUP	LDN	LOTC	RUA1	RCL	TCLE	TOCD	PRBSD

NAME	POSITION	FUNCTION
LUP (Latched)	SR.7	Loop-Up Code Detected. This bit is set when the loop-up code defined in registers RUPCD1 and RUPCD2 is being received. See Section 6.1 for details.
LDN (Latched)	SR.6	Loop-Down Code Detected. This bit is set when the loop-down code defined in registers RDNCD1 and RDNCD2 is being received. See Section 6.1 for details.
LOTC (Real Time)	SR.5	Loss-of-Transmit Clock. This bit is set when the TCLK pin has not transitioned for 5µs (±2µs), forcing the LOTC pin high.
RUA1 (Latched)	SR.4	Receive Unframed All Ones. This bit is set when an unframed all-ones code is received at RRING and RTIP (Table 5-A).
RCL (Latched)	SR.3	Receive Carrier Loss. This bit is set when an RCL condition exists at RRING and RTIP. See (Table 5-A) for details.
TCLE (Real Time)	SR.2	Transmit Current-Limit Exceeded. This bit is set when the 50mA (RMS) current limiter is activated whether or not the current limiter is enabled.
TOCD (Real Time)	SR.1	Transmit Open-Circuit Detect. This bit is set when the device detects that the TTIP and TRING outputs are open circuited.
PRBSD (Real Time)	SR.0	PRBS Detect. This bit is set when the receive side detects a 2^{15} - 1 (E1) or a QRSS (T1) pseudorandom bit sequence (PRBS).

Table 5-A. Received Alarm Criteria

ALARM	E1/T1	SET CRITERIA	CLEAR CRITERIA
RUA1	E1	Fewer than two 0s in two frames (512 bits)	More than two 0s in two frames (512 bits)
RUA1	T1	Over a 3ms window, five or fewer 0s are received.	Over a 3ms window, six or more 0s are received.
RCL (Note 1)	E1	255 (or 2048) consecutive 0s received (G.775) (Note 2)	In 255-bit times, at least 32 1s are received.
RCL (Note 1)	T1	192 (or 1544) consecutive 0s are received (Note 2)	14 or more 1s out of 112 possible bit positions are received, starting with the first 1 received.

Note 1: RCL is also known as a loss of signal (LOS) or Red Alarm in T1.
Note 2: See CCR1.5 for details.

IMR (07H): Interrupt Mask Register

(MSB)							(LSB)
LUP	LDN	LOTC	RUA1	RCL	TCLE	TOCD	PRBSD

NAME	POSITION	FUNCTION
LUP	IMR.7	Loop-Up Code Detected 0 = interrupt masked 1 = interrupt enabled
LDN	IMR.6	Loop-Down Code Detected 0 = interrupt masked 1 = interrupt enabled
LOTC	IMR.5	Loss-of-Transmit Clock 0 = interrupt masked 1 = interrupt enabled
RUA1	IMR.4	Receive Unframed All Ones 0 = interrupt masked 1 = interrupt enabled
RCL	IMR.3	Receive Carrier Loss 0 = interrupt masked 1 = interrupt enabled
TCLE	IMR.2	Transmit Current-Limiter Exceeded 0 = interrupt masked 1 = interrupt enabled
TOCD	IMR.1	Transmit Open-Circuit Detect 0 = interrupt masked 1 = interrupt enabled
PRBSD	IMR.0	PRBS Detection 0 = interrupt masked 1 = interrupt enabled