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Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
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DS21455/DS21458
Quad T1/E1/J1 Transceivers

www.maxim-ic.com

GENERAL DESCRIPTION

The DS21455 and DS21458 are quad monolithic devices featuring independent transceivers that can be software configured for T1, E1, or J1 operation. Each is composed of a line interface unit (LIU), framer, HDLC controllers, and a TDM backplane interface, and is controlled via an 8-bit parallel port configured for Intel or Motorola bus operations. The DS21455* is a direct replacement for the older DS21Q55 quad MCM device. The DS21458, in a smaller package (17mm CSBGA) and featuring an improved controller interface, is software compatible with the older DS21Q55.

**The JTAG function on the DS21455/DS21458 is a single controller for all four transceivers, unlike the DS21Q55, which has a JTAG controller-per-transceiver architecture.*

APPLICATIONS

Routers
Channel Service Units (CSUs)
Data Service Units (DSUs)
Muxes
Switches
Channel Banks
T1/E1 Test Equipment

ORDERING INFORMATION

PART	TEMP RANGE	PIN-PACKAGE
DS21455	0°C to +70°C	256 BGA (27mm x 27mm)
DS21455+	0°C to +70°C	256 BGA (27mm x 27mm)
DS21455N	-40°C to +85°C	256 BGA (27mm x 27mm)
DS21455N+	-40°C to +85°C	256 BGA (27mm x 27mm)
DS21458	0°C to +70°C	256 CSBGA (17mm x 17mm)
DS21458+	0°C to +70°C	256 CSBGA (17mm x 17mm)
DS21458N	-40°C to +85°C	256 CSBGA (17mm x 17mm)
DS21458N+	-40°C to +85°C	256 CSBGA (17mm x 17mm)

+ Denotes a lead(Pb)-free/RoHS-compliant package.

FEATURES

Four Independent Transceivers, Each Having the Following Features:

- Complete T1 (DS1)/ISDN-PRI/J1 Transceiver Functionality
- Complete E1 (CEPT) PCM-30/ISDN-PRI Transceiver Functionality
- Short- and Long-Haul Line Interface for Clock/Data Recovery and Waveshaping
- CMI Coder/Decoder
- Crystal-Less Jitter Attenuator
- Fully Independent Transmit and Receive Functionality
- Dual HDLC Controllers
- On-Chip Programmable BERT Generator and Detector
- Internal Software-Selectable Receive- and Transmit-Side Termination Resistors for 75Ω/100Ω/120Ω T1 and E1 Interfaces
- Dual Two-Frame Elastic-Store Slip Buffers that can Connect to Asynchronous Backplanes Up to 16.384MHz
- 16.384MHz, 8.192MHz, 4.096MHz, or 2.048MHz Clock Output Synthesized to Recovered Network Clock
- Programmable Output Clocks for Fractional T1, E1, H0, and H12 Applications
- Interleaving PCM Bus Operation
- 8-Bit Parallel Control Port, Multiplexed or Nonmultiplexed, Intel or Motorola
- IEEE 1149.1 JTAG-Boundary Scan
- 3.3V Supply with 5V Tolerant Inputs and Outputs
- DS21455 Directly Replaces DS21Q55
- Signaling System 7 (SS7) Support
- RAI-CI, AIS-CI Support

Note: *Some revisions of this device may incorporate deviations from published specifications known as errata. Multiple revisions of any device may be simultaneously available through various sales channels. For information about device errata, click here: www.maxim-ic.com/errata.*

DOCUMENT REVISION HISTORY

REVISION	CHANGES
040804	New Product Release.
091304	1. An incorrect Device ID was shown in the IDR register. A table was added to clearly show the Device IDs for the DS21455 and DS21458. 2. Corrected multiple incorrect pin names in Figure 5-2. The pin names were changed to match the correct pin names shown in Table 5-2. Pin A1 was changed from TNEG0 to TNEGO3. Pin F11 was changed from TLINK3 to TLINK2. Pin K1 was changed from RTIP to RTIP1. Pin K9 was changed from UNUSED to N.C. Pin K15 was changed from JSTRST to TSTRST. Pin P3 was changed from UNUSED to N.C. 3. The 8X clock reference was removed from Figure 3-1 and Figure 3-2. 4. The thermal data shown in Section 37 was corrected and the LQFP package information was removed. 5. The supply current shown in Section 37 was corrected and a typical power dissipation number was added, as well as a note explaining the testing conditions.
101304	Removed CCR4.0, CCR4.1, CCR4.2, and CCR4.3 bits from CCR4. These were listed as User Programmable Outputs but these do not exist on the DS21458 or the DS21455.
042105	Removed references to TESO and TDATA in the pin description list, as these pins are not available on the DS21455/DS21458.
081805	Added the MCLKS bit to CCR1.7 (was missing in previous data sheet revisions) in Section 12.
042106	Replaced Figure 25-5 and Figure 25-6, added Table 25-6 and Table 25-7.
052406	Added lead-free part numbers to *Ordering Information* table (page 1).
051507	Removed description for RCL pin (device does not have this pin) (page 23); corrected register setting for Transmit Signaling Registers E1 CCS mode (page 102).

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1. DESCRIPTION

The DS21455 and DS21458 are quad monolithic devices featuring independent transceivers that can be software configured for T1, E1, or J1 operation. Each is composed of a line interface unit (LIU), framer, HDLC controllers, and a TDM backplane interface, and is controlled via an 8-bit parallel port configured for Intel or Motorola bus operations. The DS21455* is a direct replacement for the older DS21Q55 quad MCM device. The DS21458, which comes in a smaller package (17mm CSBGA) and features an improved controller interface, is software compatible with the older DS21Q55.

The LIU is composed of a transmit interface, receive interface, and a jitter attenuator. The transmit interface is responsible for generating the necessary waveshapes for driving the network and providing the correct source impedance depending on the type of media used. T1 waveform generation includes DSX-1 line build-outs as well as CSU line build-outs of -7.5dB, -15dB, and -22.5dB. E1 waveform generation includes G.703 waveshapes for both 75Ω coax and 120Ω twisted cables. The receive interface provides network termination and recovers clock and data from the network. The receive sensitivity adjusts automatically to the incoming signal and can be programmed for 0dB to 43dB or 0dB to 12dB for E1 applications and 0dB to 15dB or 0dB to 36dB for T1 applications. The jitter attenuator removes phase jitter from the transmitted or received signal. The crystal-less jitter attenuator requires only a 2.048MHz MCLK for both E1 and T1 applications (with the option of using a 1.544MHz MCLK in T1 applications) and can be placed in either transmit or receive data paths. An additional feature of the LIU is a CMI coder/decoder for interfacing to optical networks.

On the transmit side, clock/data, and frame-sync signals are provided to the framer by the backplane interface section. The framer inserts the appropriate synchronization framing patterns and alarm information, calculates and inserts the CRC codes, and provides the B8ZS/HDB3 (zero code suppression) and AMI line coding. The receive-side framer decodes AMI, B8ZS, and HDB3 line coding, synchronizes to the data stream, reports alarm information, counts framing/coding/CRC errors, and provides clock/data and frame-sync signals to the backplane interface section.

Both the transmit and receive path have two HDLC controllers. The HDLC controllers transmit and receive data via the framer block. The HDLC controllers can be assigned to any time slot, group of time slots, portion of a time slot, or to FDL (T1) or Sa bits (E1). Each controller has 128-bit FIFOs, thus reducing the amount of processor overhead required to manage the flow of data. In addition, built-in support for reducing the processor time required handles SS7 applications.

The backplane interface provides a versatile method of sending and receiving data from the host system. Elastic stores provide a method for interfacing to asynchronous systems, converting from a T1/E1 network to a 2.048MHz, 4.096MHz, 8.192MHz, or N x 64kHz system backplane. The elastic stores also manage slip conditions (asynchronous interface). An interleave bus option (IBO) is provided to allow up to eight transceivers (two DS21455s/DS21458s) to share a high-speed backplane.

The parallel port provides access for control and configuration of all the DS21455/DS21458's features. The Extended System Information Bus (ESIB) function allows up to eight transceivers, two DS21455s or two DS21458s to be accessed via a single read for interrupt status or other user-selectable alarm status information. Diagnostic capabilities include loopbacks, PRBS pattern generation/detection, and 16-bit loop-up and loop-down code generation and detection.

*** The JTAG function on the DS21455/DS21458 is a single controller for all four transceivers, unlike the DS21Q55, which has a JTAG controller-per-transceiver architecture.**

1.1 Standards

- ANSI: T1.403-1995, T1.231-1993, T1.408
- AT&T: TR54016, TR62411
- ITU: G.703, G.704, G.706, G.736, G.775, G.823, G.932, I.431, O.151, O.161
- ETSI: ETS 300 011, ETS 300 166, ETS 300 233, CTR4, CTR12
- Japanese: JTG.703, JTI.431, JJ-20.11 (CMI coding only)

2. FEATURE HIGHLIGHTS

2.1 General

- DS21455: 27mm, 1.27 pitch BGA, compatible replacement for the DS21Q55
- DS21458: 17mm, 1.00 pitch CSBGA
- 3.3V supply with 5V tolerant inputs and outputs
- Evaluation kits
- IEEE 1149.1 JTAG-boundary scan
- Driver source code available from the factory

2.2 Line Interface

- Requires a single master clock (MCLK) for both E1 and T1 operation. Master clock can be 2.048MHz, 4.096MHz, 8.192MHz, or 16.384MHz. Option to use 1.544MHz, 3.088MHz, 6.276MHz, or 12.552MHz for T1-only operation
- Fully software configurable
- Short- and long-haul applications
- Automatic receive sensitivity adjustments
- Ranges include 0dB to -43dB or 0dB to -12dB for E1 applications; 0dB to -36dB or 0dB to -15dB for T1 applications
- Receive level indication in 2.5dB steps from -42.5dB to -2.5dB
- Internal receive termination option for 75Ω, 100Ω, and 120Ω lines
- Monitor application gain settings of 20dB, 26dB, and 32dB
- G.703 receive-synchronization signal-mode
- Flexible transmit-waveform generation
- T1 DSX-1 line build-outs
- T1 CSU line build-outs of -7.5dB, -15dB, and -22.5dB
- E1 waveforms include G.703 waveshapes for both 75Ω coax and 120Ω twisted cables
- AIS generation independent of loopbacks
- Alternating ones and zeros generation
- Square-wave output
- Open-drain output option
- NRZ format option
- Transmitter power-down
- Transmitter 50mA short-circuit limiter with exceeded indication of current limit
- Transmit open-circuit-detected indication
- Line interface function can be completely decoupled from the framer/formatter

2.3 Clock Synthesizer

- Output frequencies include 2.048MHz, 4.096MHz, 8.192MHz, and 16.384MHz
- Derived from recovered line clock or master clock

2.4 Jitter Attenuator

- 32-bit or 128-bit crystal-less jitter attenuator
- Requires only a 2.048MHz master clock for both E1 and T1 operation with the option to use 1.544MHz for T1 operation
- Can be placed in either the receive or transmit path or disabled
- Limit trip indication

2.5 Framer/Formatter

- Fully independent transmit and receive functionality
- Full receive- and transmit-path transparency
- T1 framing formats include D4, ESF, J1-D4, J1-ESF and SLC-96
- Japanese J1 support for CRC6 and yellow alarm
- E1 framing formats include FAS, CAS, and CRC-4
- Detailed alarm- and status-reporting with optional interrupt support
- Large path- and line-error counters for:
  - T1 – BPV, CV, CRC6, and framing bit errors
  - E1 – BPV, CV, CRC-4, E-bit, and frame alignment errors
  - Timed or manual update modes
- User-defined Idle Code Generation on a per-channel basis in both transmit and receive paths
- Digital milliwatt code generation on the receive path
- ANSI T1.403-1998 support
- G.965 V5.2 link detect
- RAI-CI detection and generation
- AIS-CI detection and generation
- Ability to monitor one DS0 channel in both the transmit and receive paths
- In-band repeating-pattern generators and detectors
  - Three independent generators and detectors
  - Patterns from 1 bit to 8 bits or 16 bits in length
- RCL, RLOS, RRA, and RAIS alarms interrupt on change of state
- Flexible signaling support
  - Software- or hardware-based
  - Interrupt generated on change of signaling data
  - Receive-signaling freeze on loss of sync, carrier loss, or frame slip
- Hardware pins to indicate carrier loss and signaling freeze
- Automatic RAI generation to ETS 300 011 specifications
- Expanded access to Sa and Si bits
- Option to extend carrier-loss criteria to a 1ms period as per ETS 300 233

2.6 System Interface

- Dual two-frame, independent receive and transmit elastic stores
  - Independent control and clocking
  - Controlled-slip capability with status
  - Minimum-delay mode supported
- Supports T1 to E1 conversion
- Ability to pass the T1 F-bit position through the elastic stores in the 2.048MHz backplane mode
- Programmable output clocks for fractional T1, E1, H0, and H12 applications
- Interleaving PCM bus operation with rates of 4.096MHz, 8.192MHz, and 16.384MHz
- Hardware-signaling capability
  - Receive-signaling reinsertion to a backplane, multiframe sync
  - Availability of signaling in a separate PCM data stream
  - Signaling freezing
- Access to the data streams in between the framer/formatter and the elastic stores (DS21455)
- User-selectable synthesized clock output

2.7 HDLC Controllers

- Two independent HDLC controllers
- Fast load and unload features for FIFOs
- SS7 support for FISU transmit and receive
- Independent 128-byte Rx and Tx buffers with interrupt support
- Access FDL, Sa, or single/multiple DS0 channels
- DS0 access includes Nx64 or Nx56
- Compatible with polled or interrupt-driven environments
- Bit Oriented Code (BOC) support

2.8 Test and Diagnostics

- Programmable Bit Error Rate Testing (BERT)
- Pseudorandom patterns including QRSS
- User-defined repetitive patterns
- Daly pattern
- Error insertion for single bit or continuous
- Insertion options include continuous and absolute number with selectable insertion rates
- Total-bit and errored-bit counters
- Payload Error Insertion
- Errors can be inserted over the entire frame or selected channels
- F-bit corruption for line testing
- Loopbacks (remote, local, analog, and per-channel payload loopback)

2.9 Extended System Information Bus

- Host can read interrupt and alarm status on up to eight ports (two devices) with a single-bus read

2.10 Control Port

- 8-bit parallel control port
- Multiplexed or nonmultiplexed buses
- Intel or Motorola formats
- Supports polled or interrupt-driven environments
- Software access to device ID and silicon revision
- Software-reset supported with automatic clear on power-up
- Hardware reset pin

Note: This data sheet assumes a particular nomenclature of the T1 and E1 operating environment. In each 125µs T1 frame, there are 24 8-bit channels plus a framing bit. It is assumed that the framing bit is sent first followed by channel 1. For T1 and E1 each channel is made up of 8 bits, which are numbered 1 to 8. Bit 1, the MSB, is transmitted first. Bit 8, the LSB, is transmitted last. The term "locked" is used to refer to two clock signals that are phase- or frequency-locked or derived from a common clock (i.e., a 1.544MHz clock can be locked to a 2.048MHz clock if they share the same 8kHz component).

3. BLOCK DIAGRAM

Figure 3-1 shows a simplified block diagram highlighting the major components of the DS21458 and DS21455.

Figure 3-1. DS21458 Block Diagram

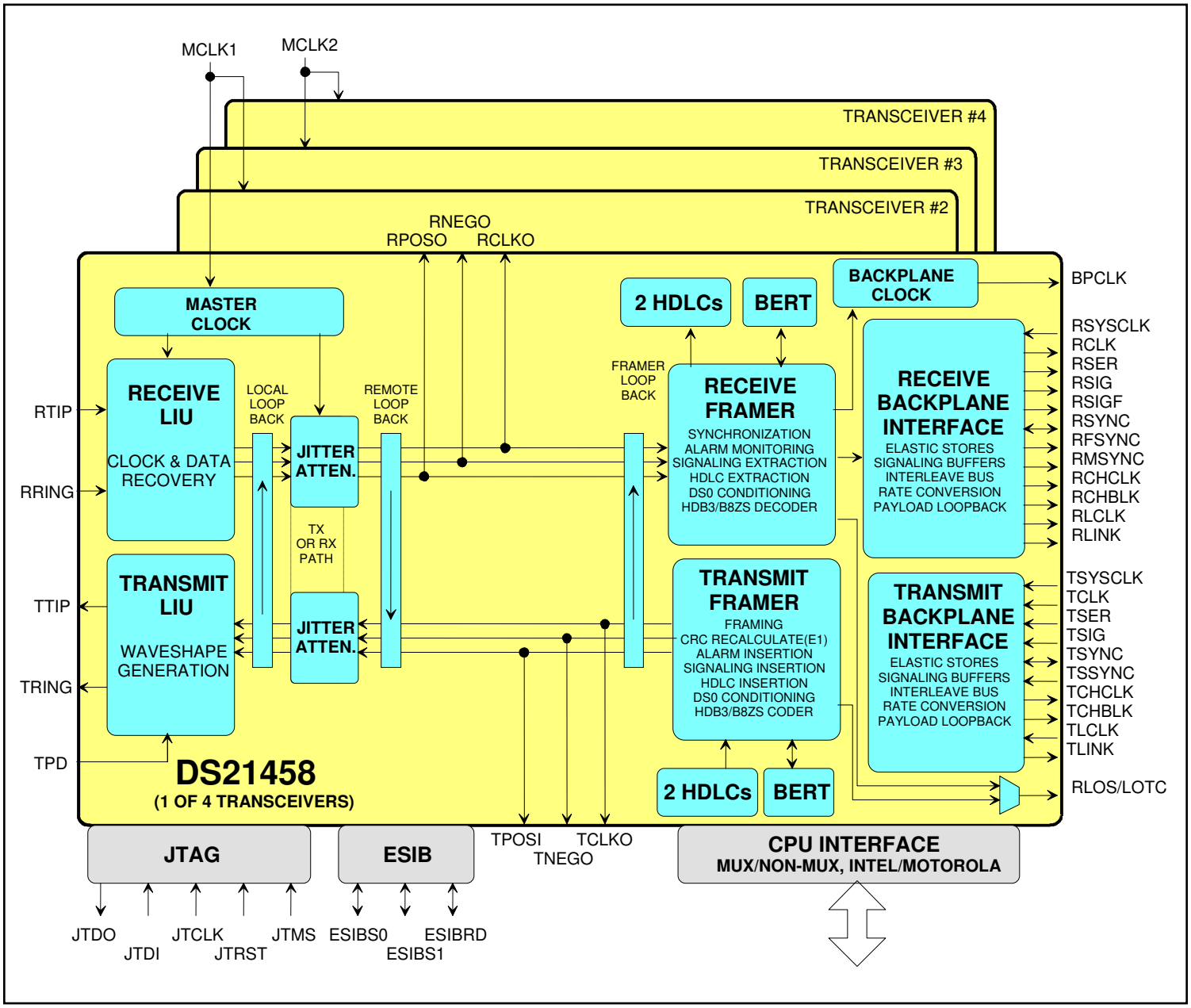
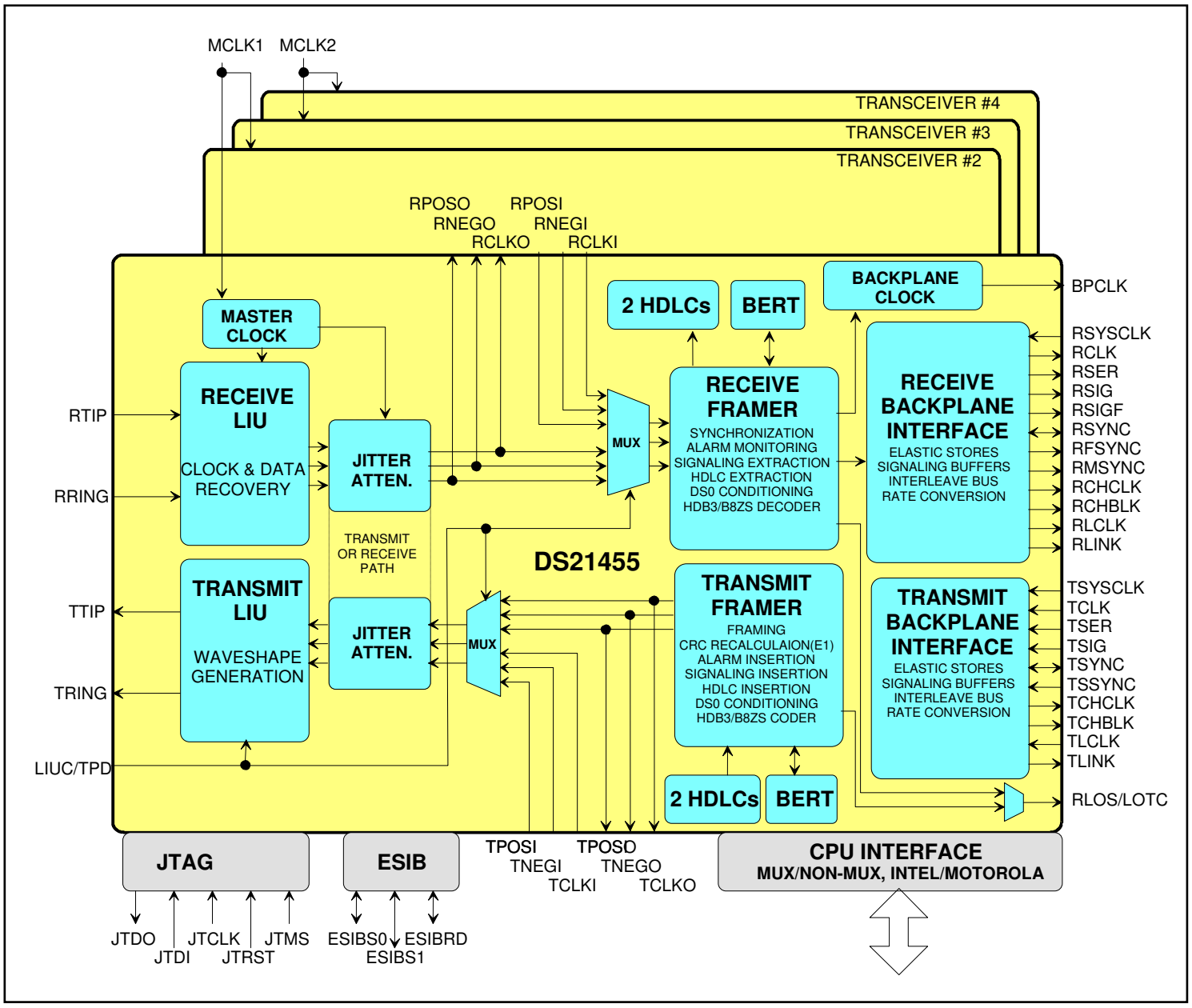


Figure 3-2. DS21455 Block Diagram



4. DS21455/DS21458 DELTA

This section describes the differences between the DS21455 and DS21458.

4.1 Package

DS21455: 27mm, 256-pin, 1.27 ball pitch, BGA (This package has the same footprint and pinout as the DS21Q55.)

DS21458: 17mm, 256-pin, 1.00 ball pitch, CSBGA

4.2 Controller Interface

DS21455: The CPU interface has 8 address lines with independent chip selects (4) per transceiver.

DS21458: The CPU interface has 10 address lines with a single chip select. The upper address lines, A8 and A9, act as coded transceiver selects.

4.3 ESIB Function

The ESIB function provides a fast method of determining interrupt and alarm status when multiple ports (up to 8) are being controlled by a single processor.

DS21455: The three ESIB signals are brought out for each transceiver. The user must externally configure the ESIB group.

DS21458: The ESIB signals are internally bused and only a single set of signals are brought out to enable the connection of another DS21458 into an 8-port ESIB.

4.4 Framer/LIU Interim Signals

Access to the clock and bipolar data signals between the framer and LIU function may be used for specialized applications. An internal MUX connects the framer and LIU if these signals are unused. The MUX is controlled via the LIUC/TPD pin and LIUC bit in the LBCR register. The unused inputs must be connected to ground.

DS21455: The user has access to all clock and data signals between the framer and LIU on all transceivers as shown in Figure 4-1.

DS21458: The user has limited access to clock and data signals between the framer and LIU on all transceivers as shown in Figure 4-2.

Figure 4-1. DS21455 Framer/LIU Interim Signals

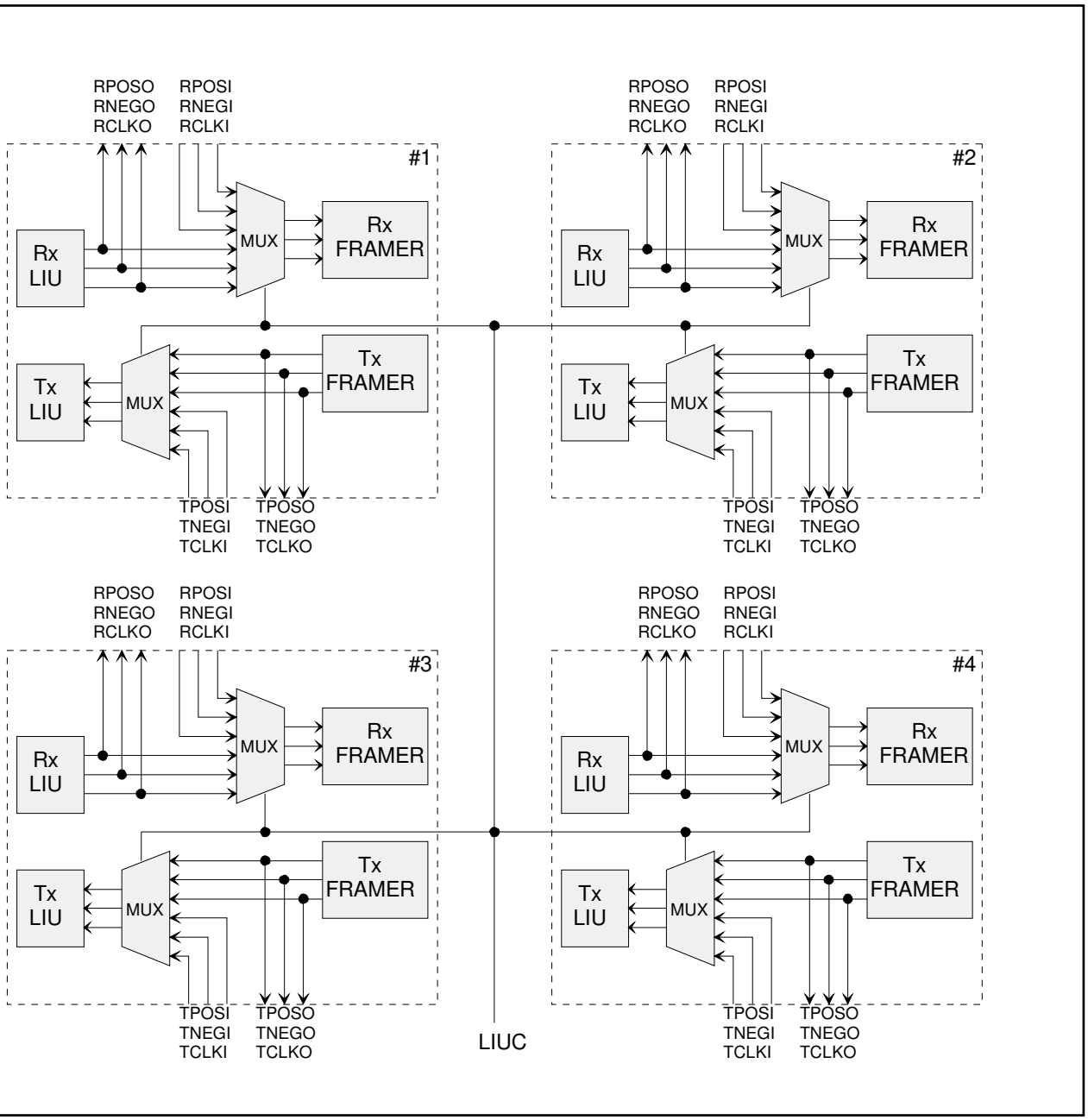
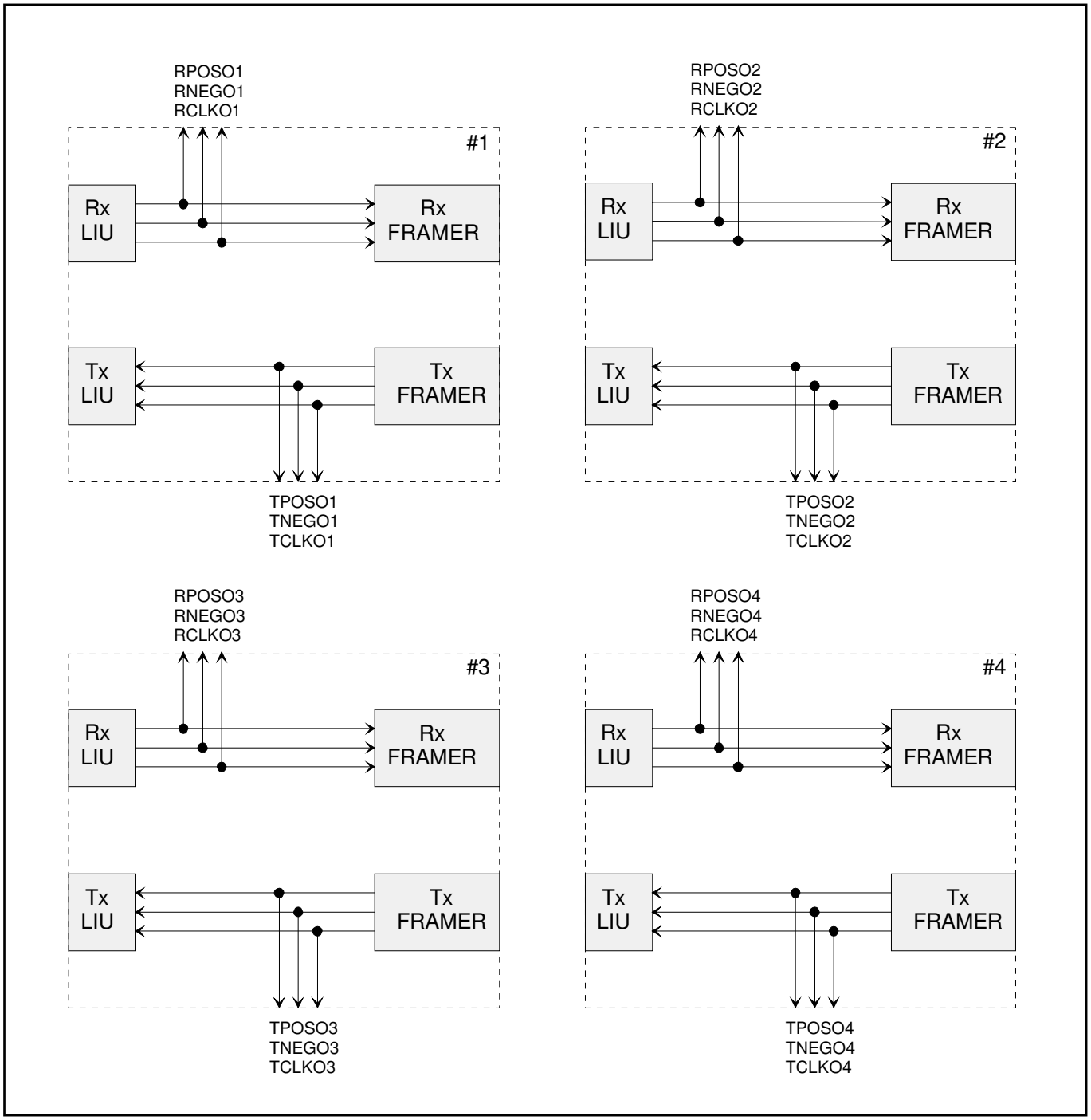


Figure 4-2. DS21458 Framer/LIU Interim Signals



5. PIN FUNCTION DESCRIPTION

5.1 Transmit Side Pins

Signal Name: **TCLK**
Signal Description: **Transmit Clock**
Signal Type: **Input**
A 1.544 MHz or a 2.048MHz primary clock. Used to clock data through the transmit-side formatter.

Signal Name: **TSER**
Signal Description: **Transmit Serial Data**
Signal Type: **Input**
Transmit NRZ serial data. Sampled on the falling edge of TCLK when the transmit-side elastic store is disabled. Sampled on the falling edge of TSYSCLK when the transmit-side elastic store is enabled.

Signal Name: **TCHCLK**
Signal Description: **Transmit Channel Clock**
Signal Type: **Output**
A 192kHz (T1) or 256kHz (E1) clock that pulses high during the LSB of each channel. Can also be programmed to output a gated transmit-bit clock for fractional T1/E1 applications. Synchronous with TCLK when the transmit-side elastic store is disabled. Synchronous with TSYSCLK when the transmit-side elastic store is enabled. Useful for parallel-to-serial conversion of channel data.

Signal Name: **TCHBLK**
Signal Description: **Transmit Channel Block**
Signal Type: **Output**
A user-programmable output that can be forced high or low during any of the channels. Synchronous with TCLK when the transmit-side elastic store is disabled. Synchronous with TSYSCLK when the transmit-side elastic store is enabled. Useful for locating individual channels in drop-and-insert applications, for external per-channel loopback, and for per-channel conditioning.

Signal Name: **TSYSCLK**
Signal Description: **Transmit System Clock**
Signal Type: **Input**
1.544MHz, 2.048MHz, 4.096MHz, 8.192MHz, or 16.384MHz clock. Only used when the transmit-side elastic-store function is enabled. Should be tied low in applications that do not use the transmit-side elastic store. See the *Interleaved PCM Bus Operation* section for details on 4.096MHz, 8.192MHz, and 16.384MHz operation using the IBO.

Signal Name: **TLCLK**
Signal Description: **Transmit Link Clock**
Signal Type: **Output**
Demand clock for the transmit link data [TLINK] input.
T1 Mode: A 4kHz or 2kHz (ZBTSI) clock.
E1 Mode: A 4kHz to 20kHz clock.

Signal Name: **TLINK**
Signal Description: **Transmit Link Data**
Signal Type: **Input**
If enabled, this pin will be sampled on the falling edge of TCLK for data insertion into either the FDL stream (ESF) or the Fs-bit position (D4) or the Z-bit position (ZBTSI) or any combination of the Sa bit positions (E1).

Signal Name: **TSYNC**
Signal Description: **Transmit Sync**
Signal Type: **Input/Output**
A pulse at this pin will establish either frame or multiframe boundaries for the transmit side. Can be programmed to output either a frame or multiframe pulse. If this pin is set to output pulses at frame boundaries, it can also be set via IOCR1.3 to output double-wide pulses at signaling frames in T1 mode.

Signal Name: **TSSYNC**
Signal Description: **Transmit System Sync**
Signal Type: **Input**
Only used when the transmit-side elastic store is enabled. A pulse at this pin will establish either frame or multiframe boundaries for the transmit side. Should be tied low in applications that do not use the transmit-side elastic store.

Signal Name: **TSIG**
Signal Description: **Transmit Signaling Input**
Signal Type: **Input**
When enabled, this input will sample signaling bits for insertion into outgoing PCM data stream. Sampled on the falling edge of TCLK when the transmit-side elastic store is disabled. Sampled on the falling edge of TSYSCLK when the transmit-side elastic store is enabled.

Signal Name: **TPOSO**
Signal Description: **Transmit Positive-Data Output**
Signal Type: **Output**
Updated on the rising edge of TCLKO with the bipolar data out of the transmit-side formatter. Can be programmed to source NRZ data via the output-data format (IOCR1.0)-control bit. This pin is normally tied to TPOSI.

Signal Name: **TNEGO**
Signal Description: **Transmit Negative-Data Output**
Signal Type: **Output**
Updated on the rising edge of TCLKO with the bipolar data out of the transmit-side formatter. This pin is normally tied to TNEGI.

Signal Name: **TCLKO**
Signal Description: **Transmit Clock Output**
Signal Type: **Output**
Buffered clock that is used to clock data through the transmit-side formatter (either TCLK or RCLKI). This pin is normally tied to TCLKI.

Signal Name: **TPOSI (DS21455 Only)**
Signal Description: **Transmit Positive-Data Input**
Signal Type: **Input**
Sampled on the falling edge of TCLKI for data to be transmitted out onto the T1 line. Can be internally connected to TPOSO by tying the LIUC/TPD pin high. See the LIUC/TPD pin description for a full explanation of this function. TPOSI and TNEGI can be tied together in NRZ applications.

Signal Name: **TNEGI (DS21455 Only)**
Signal Description: **Transmit Negative-Data Input**
Signal Type: **Input**
Sampled on the falling edge of TCLKI for data to be transmitted out onto the T1 line. Can be internally connected to TNEGO by tying the LIUC/TPD pin high. See the LIUC/TPD pin description for a full explanation of the LIUC/TPD function. TPOSI and TNEGI can be tied together in NRZ applications.

Signal Name: **TCLKI (DS21455 Only)**
Signal Description: **Transmit Clock Input**
Signal Type: **Input**
Line interface transmit clock. Can be internally connected to TCLKO by tying the LIUC/TPD pin high. See the LIUC/TPD pin description for a full explanation of the LIUC/TPD function.

5.2 Receive Side Pins

Signal Name: **RLINK**
Signal Description: **Receive Link Data**
Signal Type: **Output**
T1 Mode: Updated with either FDL data (ESF) or Fs bits (D4) or Z bits (ZBTSI) one RCLK before the start of a frame.
E1 Mode: Updated with the full E1 data stream on the rising edge of RCLK.

Signal Name: **RLCLK**
Signal Description: **Receive Link Clock**
Signal Type: **Output**
T1 Mode: A 4kHz or 2kHz (ZBTSI) clock for the RLINK output.
E1 Mode: A 4kHz to 20kHz clock.

Signal Name: **RCLK**
Signal Description: **Receive Clock**
Signal Type: **Output**
1.544MHz (T1) or 2.048MHz (E1) clock that is used to clock data through the receive-side framer.

Signal Name: **RCHCLK**
Signal Description: **Receive Channel Clock**
Signal Type: **Output**
A 192kHz (T1) or 256kHz (E1) clock that pulses high during the LSB of each channel can also be programmed to output a gated receive-bit clock for fractional T1/E1 applications. Synchronous with RCLK when the receive-side elastic store is disabled. Synchronous with RSYSCLK when the receive-side elastic store is enabled. Useful for parallel-to-serial conversion of channel data.

Signal Name: **RCHBLK**
Signal Description: **Receive Channel Block**
Signal Type: **Output**
A user-programmable output that can be forced high or low during any of the 24 T1 or 32 E1 channels. Synchronous with RCLK when the receive-side elastic store is disabled. Synchronous with RSYSCLK when the receive-side elastic store is enabled. Also useful for locating individual channels in drop-and-insert applications, for external per-channel loopback, and for per-channel conditioning. See the *Channel Blocking Registers* section.

Signal Name: **RSER**
Signal Description: **Receive Serial Data**
Signal Type: **Output**
Received NRZ serial data. Updated on rising edges of RCLK when the receive-side elastic store is disabled. Updated on the rising edges of RSYSCLK when the receive-side elastic store is enabled.

Signal Name: **RSYNC**
Signal Description: **Receive Sync**
Signal Type: **Input/Output**
An extracted pulse, one RCLK wide, is output at this pin which identifies either frame (IOCR1.5 = 0) or multiframe (IOCR1.5 = 1) boundaries. If set to output-frame boundaries then via IOCR1.6, RSYNC can also be set to output double-wide pulses on signaling frames in T1 mode. If the receive-side elastic store is enabled, then this pin can be enabled to be an input via IOCR1.4 at which a frame or multiframe boundary pulse is applied.

Signal Name: **RFSYNC**
Signal Description: **Receive Frame Sync**
Signal Type: **Output**
An extracted 8kHz pulse, one RCLK wide, is output at this pin, which identifies frame boundaries.

Signal Name: **RMSYNC**
Signal Description: **Receive Multiframe Sync**
Signal Type: **Output**
An extracted pulse, one RCLK wide (elastic store disabled) or one RSYSCLK wide (elastic store enabled), is output at this pin, which identifies multiframe boundaries.

Signal Name: **RDATA**
Signal Description: **Receive Data**
Signal Type: **Output**
Updated on the rising edge of RCLK with the data out of the receive-side framer.

Signal Name: **RSYSCLK**
Signal Description: **Receive System Clock**
Signal Type: **Input**
1.544MHz, 2.048MHz, 4.096MHz, or 8.192MHz clock. Only used when the receive-side elastic-store function is enabled. Should be tied low in applications that do not use the receive-side elastic store. See the *Interleaved PCM Bus Operation* section for details on 4.096MHz and 8.192MHz operation using the IBO.

Signal Name: **RSIG**
Signal Description: **Receive Signaling Output**
Signal Type: **Output**
Outputs signaling bits in a PCM format. Updated on rising edges of RCLK when the receive-side elastic store is disabled. Updated on the rising edges of RSYSCLK when the receive-side elastic store is enabled.

Signal Name: **RLOS/LOTC**
Signal Description: **Receive Loss of Sync/Loss of Transmit Clock**
Signal Type: **Output**
A dual-function output that is controlled by the CCR1.0 control bit. This pin can be programmed to either toggle high when the synchronizer is searching for the frame and multiframe or to toggle high if the TCLK pin has not been toggled for 5µs.

Signal Name: **RSIGF**
Signal Description: **Receive Signaling Freeze**
Signal Type: **Output**
Set high when the signaling data is frozen via either automatic or manual intervention. Used to alert downstream equipment of the condition.

Signal Name: **BPCLK**
Signal Description: **Backplane Clock**
Signal Type: **Output**
A user-selectable synthesized clock output that is referenced to the clock that is output at the RCLK pin.

Signal Name: **RPOSO**
Signal Description: **Receive Positive-Data Output**
Signal Type: **Output**
Updated on the rising edge of RCLKO with bipolar data out of the line interface. This pin is normally tied to RPOSI.

Signal Name: **RNEGO**
Signal Description: **Receive Negative-Data Output**
Signal Type: **Output**
Updated on the rising edge of RCLKO with the bipolar data out of the line interface. This pin is normally tied to RNEGI.

Signal Name: **RCLKO**
Signal Description: **Receive Clock Output**
Signal Type: **Output**
Buffered recovered clock from the network. This pin is normally tied to RCLKI.

Signal Name: **RPOSI (DS21455 Only)**
Signal Description: **Receive Positive Data Input**
Signal Type: **Input**
Sampled on the falling edge of RCLKI for data to be clocked through the receive-side framer. RPOSI and RNEGI can be tied together for a NRZ interface. Can be internally connected to RPOSO by tying the LIUC/TPD pin high. See the LIUC/TPD pin description for a full explanation of the LIUC/TPD function.

Signal Name: **RNEGI (DS21455 Only)**
Signal Description: **Receive Negative Data Input**
Signal Type: **Input**
Sampled on the falling edge of RCLKI for data to be clocked through the receive-side framer. RPOSI and RNEGI can be tied together for a NRZ interface. Can be internally connected to RNEGO by tying the LIUC/TPD pin high. See the LIUC/TPD pin description for a full explanation of the LIUC/TPD function.

Signal Name: **RCLKI (DS21455 Only)**
Signal Description: **Receive Clock Input**
Signal Type: **Input**
Clock used to clock data through the receive-side framer. This pin is normally tied to RCLKO. Can be internally connected to RCLKO by tying the LIUC/TPD pin high. See the LIUC/TPD pin description for a full explanation of the LIUC/TPD function.

5.3 Parallel Control Port Pins

Signal Name: **$\overline{\text{INT}}$**
Signal Description: **Interrupt**
Signal Type: **Output**
Flags host controller during events, alarms, and conditions defined in the status registers. Active-low open-drain output.

Signal Name: **TSTRST**
Signal Description: **Tri-State Control and Device Reset**
Signal Type: **Input**
A dual-function pin. A zero-to-one transition issues a hardware reset to the DS21455/DS21458 register set. A reset clears all configuration registers. Configuration register contents are set to zero. Leaving TSTRST high will tri-state all output and I/O pins (including the parallel control port). Set low for normal operation. Useful in board-level testing.

Signal Name: **MUX**
Signal Description: **Bus Operation**
Signal Type: **Input**
Set low to select nonmultiplexed bus operation. Set high to select multiplexed bus operation.

Signal Name: **AD0 to AD7**
Signal Description: **Data Bus [D0 to D7] or Address/Data Bus**
Signal Type: **Input/Output**
In nonmultiplexed bus operation (MUX = 0), it serves as the data bus. In multiplexed bus operation (MUX = 1), it serves as an 8-bit, multiplexed address/data bus.

Signal Name: **A0 to A6**
Signal Description: **Address Bus**
Signal Type: **Input**
In nonmultiplexed bus operation (MUX = 0), it serves as the address bus. In multiplexed bus operation (MUX = 1), these pins are not used and should be tied low.

Signal Name: **A8 and A9 (DS21458 Only)**
Signal Description: **Address Bus**
Signal Type: **Input**
Upper address pins for nonmultiplexed (MUX = 0), and multiplexed (MUX = 1) bus operation.

Signal Name: **BTS**
Signal Description: **Bus Type Select**
Signal Type: **Input**
Strap high to select Motorola bus timing; strap low to select Intel bus timing. This pin controls the function of the $\overline{RD}$ ($\overline{DS}$), ALE (AS), and $\overline{WR}$ (R/$\overline{W}$) pins. If BTS = 1, then these pins assume the function listed in parentheses ().

Signal Name: **$\overline{RD}$ ($\overline{DS}$)**
Signal Description: **Read Input-Data Strobe**
Signal Type: **Input**
$\overline{RD}$ and $\overline{DS}$ are active-low signals. DS active HIGH when MUX = 0. See the bus timing diagrams.

Signal Name: **$\overline{CS1}$ (DS21455 Only)**
Signal Description: **Chip Select for Transceiver 1**
Signal Type: **Input**
Must be low to read or write to Transceiver 1 of the device. $\overline{CS1}$ is an active-low signal.

Signal Name: **$\overline{CS2}$ (DS21455 Only)**
Signal Description: **Chip Select for Transceiver 2**
Signal Type: **Input**
Must be low to read or write to Transceiver 2 of the device. $\overline{CS2}$ is an active-low signal.

Signal Name: **$\overline{CS3}$ (DS21455 Only)**
Signal Description: **Chip Select for Transceiver 3**
Signal Type: **Input**
Must be low to read or write to Transceiver 3 of the device. $\overline{CS3}$ is an active-low signal.

Signal Name: **$\overline{CS4}$ (DS21455 Only)**
Signal Description: **Chip Select for Transceiver 4**
Signal Type: **Input**
Must be low to read or write to Transceiver 4 of the device. $\overline{CS4}$ is an active-low signal.