Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

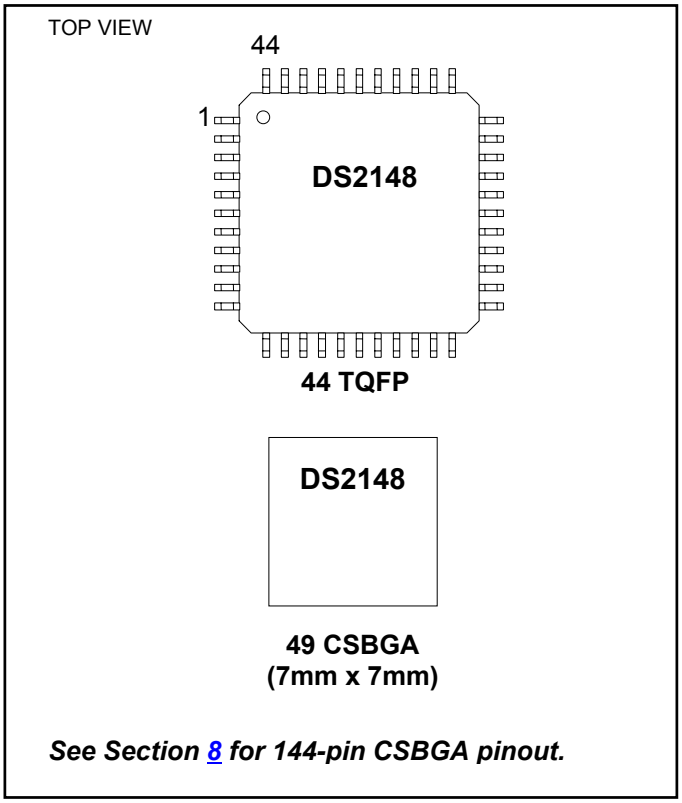
DS2148/DS21Q48
5V E1/T1/J1 Line Interface Unit

www.maxim-ic.com

FEATURES

- Complete E1, T1, or J1 Line Interface Unit (LIU)
- Supports Both Long- and Short-Haul Trunks
- Internal Software-Selectable Receive-Side Termination for 75Ω/100Ω/120Ω
- 5V Power Supply
- 32-Bit or 128-Bit Crystal-Less Jitter Attenuator Requires Only a 2.048MHz Master Clock for Both E1 and T1 with Option to Use 1.544MHz for T1
- Generates the Appropriate Line Build-Outs, With and Without Return Loss, for E1 and DSX-1 and CSU Line Build-Outs for T1
- AMI, HDB3, and B8ZS, Encoding/Decoding
- 16.384MHz, 8.192MHz, 4.096MHz, or 2.048MHz Clock Output Synthesized to Recovered Clock
- Programmable Monitor Mode for Receiver
- Loopbacks and PRBS Pattern Generation/ Detection with Output for Received Errors
- Generates/Detects In-Band Loop Codes, 1 to 16 Bits including CSU Loop Codes
- 8-Bit Parallel or Serial Interface with Optional Hardware Mode
- Multiplexed and Nonmultiplexed Parallel Bus Supports Intel or Motorola
- Detects/Generates Blue (AIS) Alarms
- NRZ/Bipolar Interface for Tx/Rx Data I/O
- Transmit Open-Circuit Detection
- Receive Carrier Loss (RCL) Indication (G.775)
- High-Z State for TTIP and TRING
- 50mA (RMS) Current Limiter

PIN CONFIGURATION



See Section 8 for 144-pin CSBGA pinout.

ORDERING INFORMATION

PART	CHANNEL	TEMP RANGE	PIN-PACKAGE
DS2148TN	Single	-40°C to +85°C	44 TQFP
DS2148TN+	Single	-40°C to +85°C	44 TQFP
DS2148T	Single	0°C to +70°C	44 TQFP
DS2148T+	Single	0°C to +70°C	44 TQFP
DS2148GN	Single	-40°C to +85°C	49 CSBGA
DS2148GN	Single	-40°C to +85°C	49 CSBGA
DS2148G	Single	0°C to +70°C	49 CSBGA
DS2148G+	Single	0°C to +70°C	49 CSBGA
DS21Q48N	Four	-40°C to +85°C	144 CSBGA
DS21Q48	Four	0°C to +70°C	144 CSBGA

+ Denotes lead-free/RoHS-compliant package.

Note: *Some revisions of this device may incorporate deviations from published specifications known as errata. Multiple revisions of any device may be simultaneously available through various sales channels. For information about device errata, click here: www.maxim-ic.com/errata.*

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

1 DETAILED DESCRIPTION

The DS2148 is a complete selectable E1 or T1 Line Interface Unit (LIU) for short- and long-haul applications. Throughout the data sheet, J1 is represented wherever T1 exists. Receive sensitivity adjusts automatically to the incoming signal and can be programmed for 0dB to 12dB or 0dB to 43dB for E1 applications and 0dB to 30dB or 0dB to 36dB for T1 applications. The device can generate the necessary G.703 E1 waveshapes in 75Ω or 120Ω applications and DSX-1 line built-outs or CSU line built-outs of 0dB, -7.5dB, -15dB, and -22.5dB for T1 applications. The crystal-less onboard jitter attenuator requires only a 2.048MHz MCLK for both E1 and T1 applications (with the option of using a 1.544MHz MCLK in T1 applications). The jitter attenuator FIFO is selectable to either 32 bits or 128 bits in depth and can be placed in either the transmit or receive data paths. An X 2.048MHz output clock synthesized to RCLK is available for use as a backplane system clock (where n = 1, 2, 4, or 8). The DS2148 has diagnostic capabilities such as loopbacks and PRBS pattern generation/detection. 16-bit loop-up and loop-down codes can be generated and detected. The device can be controlled via an 8-bit parallel muxed or nonmuxed port, serial port or used in hardware mode. The device fully meets all of the latest E1 and T1 specifications including ANSI T1.403-1999, ANSI T1.408, AT&T TR 62411, ITU G.703, G.704, G.706, G.736, G.775, G.823, I.431, O.151, O.161, ETSI ETS 300 166, JTG.703, JTI.431, JJ-20.1, TBR12, TBR13, and CTR4.

1.1 Function Description

The analog AMI/HDB3 waveform off the E1 line or the AMI/B8ZS waveform off the T1 line is transformer coupled into the RTIP and RRING pins of the DS2148. The user has the option to use internal software-selectable receive-side termination for 75Ω/100Ω/120Ω applications or external termination. The device recovers clock and data from the analog signal and passes it through the jitter attenuation MUX outputting the received line clock at RCLK and bipolar or NRZ data at RPOS and RNEG. The DS2148 contains an active filter that reconstructs the analog-received signal for the nonlinear losses that occur in transmission. The receive circuitry also is configurable for various monitor applications. The device has a usable receive sensitivity of 0dB to -43dB (E1) and 0dB to -36dB (T1), which allows the device to operate on 0.63mm (22AWG) cables up to 2.5km (E1) and 6k feet (T1) in length. Data input at TPOS and TNEG is sent via the jitter attenuation MUX to the waveshaping circuitry and line driver. The DS2148 will drive the E1 or T1 line from the TTIP and TRING pins via a coupling transformer. The line driver can handle both CEPT 30/ISDN-PRI lines for E1 and long-haul (CSU) or short-haul (DSX-1) lines for T1.

1.2 Document Revision History

1) 100Ω/60Ω termination reversed in *Internal Rx Termination Select* tables, 091799.
2) Add DS21Q48 pinout, 092899.
3) Correct VSM pin number in Q48 (12 x 12 BGA) from G5 to G4, 120699.
4) Add timing diagram for Status Register (write access mode); Add mechanical dimensions for the quad version, 032900.
5) Timing diagram for Status Register (write access mode) added; elaboration on burst mode bit; add mechanical dimensions for the quad version, 050300.
6) Changes to datasheet to indicate 5V only part, 011801.
7) Added supply current measurement; added thermal characteristics of quad package, 092001.
8) Corrected typos and removed instances of 3V operation, 082504.
9) In *Absolute Maximum Ratings*, changed the spec for soldering temperature from IPC/JEDEC J-STD-020A to J-STD-020; defined the storage temperature range as –55°C to +125°C.
10) Added lead-free packages to Ordering Information table on page 1; updated style of data sheet, 011206.

Figure 1-1. DS2148 Block Diagram

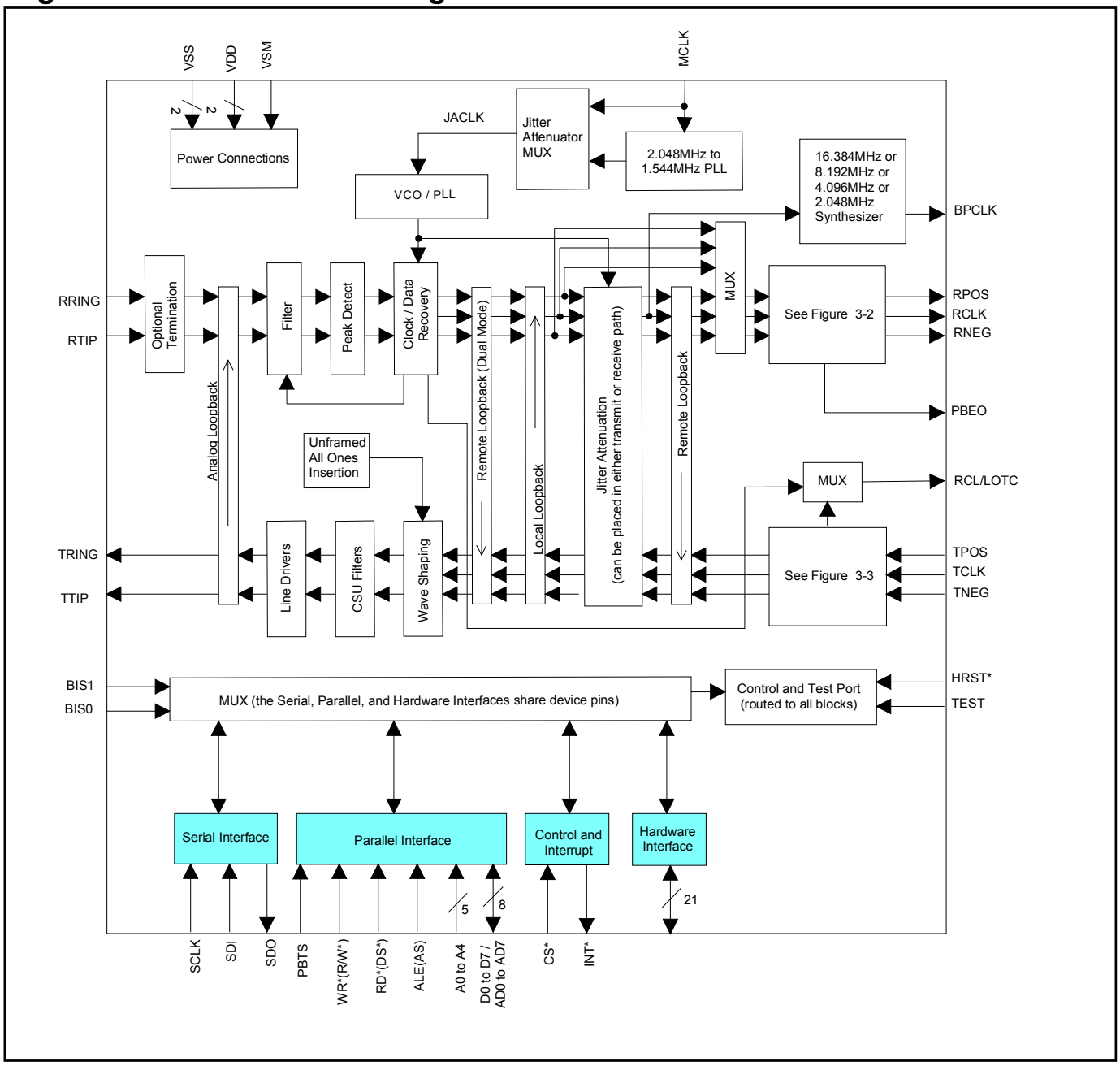


Figure 1-2. Receive Logic

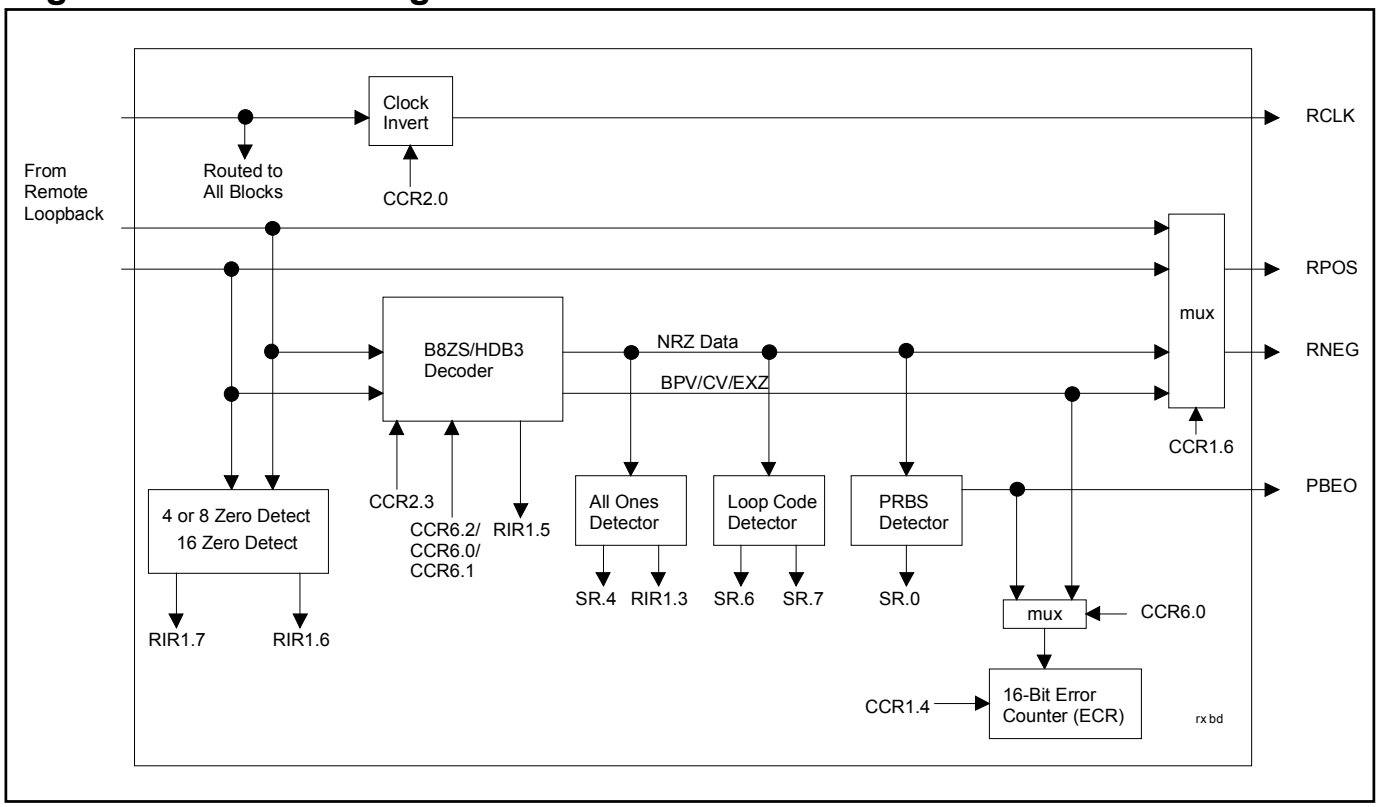
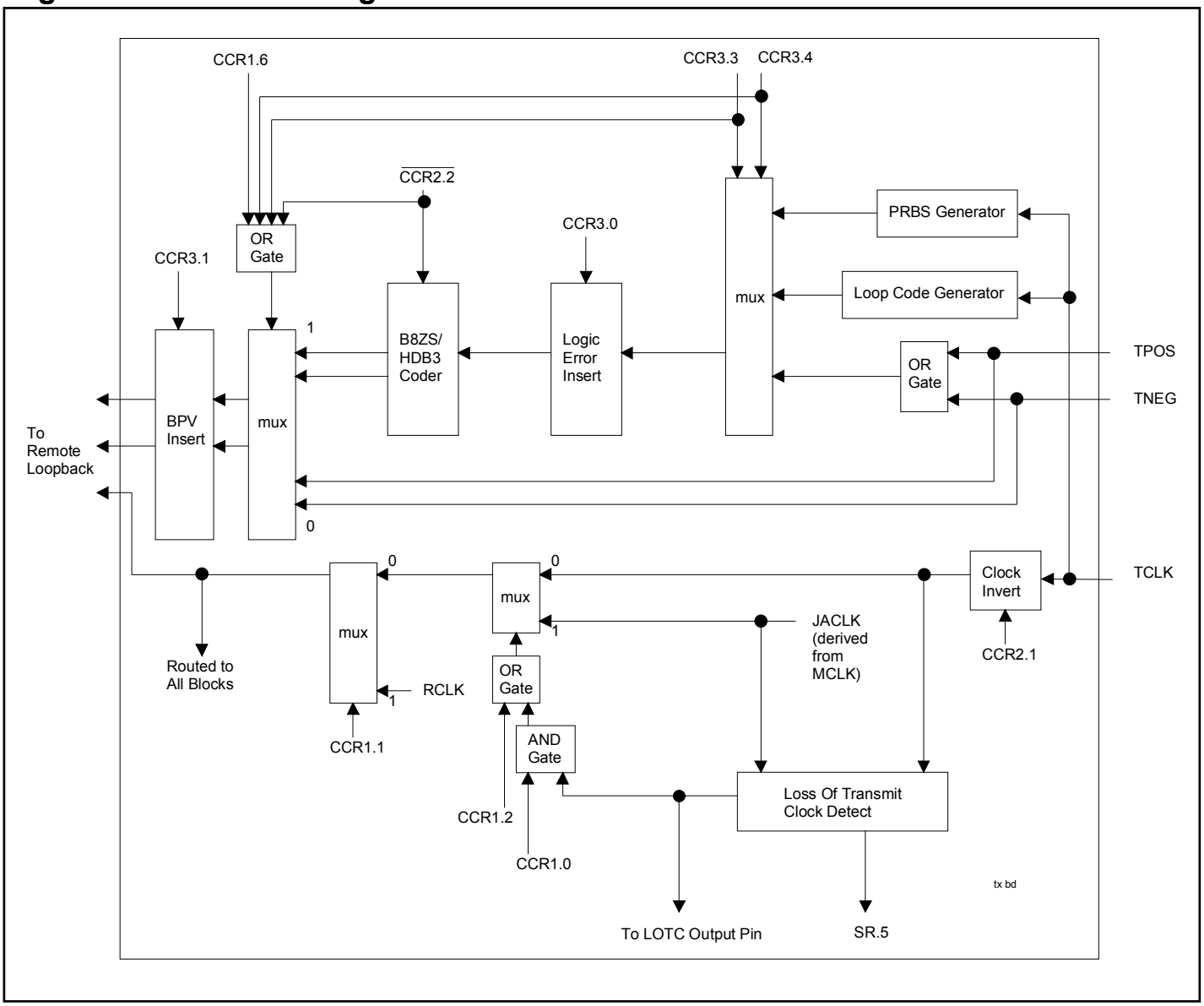


Figure 1-3. Transmit Logic



2 PIN DESCRIPTION

The DS2148 can be controlled in a parallel port mode, a serial port mode, or a hardware mode (Table 2-1, Table 2-2, and Table 2-3). The parallel and serial port modes are described in Section 3.2 and 3.3, and the hardware mode is described below.

Table 2-1. Bus Interface Selection

BIS1	BIS0	PBTS	BUS INTERFACE TYPE
0	0	0	Muxed Intel
0	0	1	Muxed Motorola
0	1	0	Nonmuxed Intel
0	1	1	Nonmuxed Motorola
1	0	-	Serial Port
1	1	-	Hardware

Table 2-2. Pin Assignment in Parallel Port Mode

DS2148T PIN #	DS2148G PIN#	I/O	PARALLEL PORT MODE
1	C3	I	$\overline{CS}$
2	C2	I	$\overline{RD}(\overline{DS})$
3	B1	I	$\overline{WR}(R/\overline{W})$
4	D2	I	ALE(AS)
5	C1	I	NA
6	D3	I	NA
7	D1	I/O	A4
8	E1	I	A3
9	F2	I	A2
10	F1	I	A1
11	G1	I	A0
12	E3	I/O	D7/AD7
13	F3	I/O	D6/AD6
14	G2	I/O	D5/AD5
15	F4	I/O	D4/AD4
16	G3	I/O	D3/AD3
17	E4	I/O	D2/AD2
18	G4	I/O	D1/AD1
19	F5	I/O	D0/AD0
20	G5	I	VSM
21	F6	-	V_{DD}
22	G6	-	V_{SS}
23	E5	I/O	$\overline{INT}$
24	E6	O	PBEO
25	F7	O	RCL/LOTC
26	D6	I	TEST
27	D5	I	RTIP
28	D7	I	RRING

DS2148T PIN #	DS2148G PIN#	I/O	PARALLEL PORT MODE
29	C6	I	$\overline{\text{HRST}}$
30	C7	I	MCLK
31	B6	O	BPCLK
32	B7	I	BIS0
33	A7	I	BIS1
34	C5	O	TTIP
35	B5	-	V_{SS}
36	A6	-	V_{DD}
37	B4	O	TRING
38	C4	O	RPOS
39	A4	O	RNEG
40	B3	O	RCLK
41	A3	I	TPOS
42	B2	I	TNEG
43	A2	I	TCLK
44	A1	I	PBTS

Table 2-3. Pin Descriptions in Parallel Port Mode (Sorted by Pin Name, DS2148T)

NAME	PIN	I/O	FUNCTION
A0 to A4	11 to 7	I	**Address Bus.** In nonmultiplexed bus operation (BIS1 = 0, BIS0 = 1), serves as the address bus. In multiplexed bus operation (BIS1 = 0, BIS0 = 0), these pins are not used and should be tied low.
ALE(AS)	4	I	**Address Latch Enable (Address Strobe).** When using the parallel port (BIS1 = 0) in multiplexed bus mode (BIS0 = 0), serves to demultiplex the bus on a positive-going edge. In nonmultiplexed bus mode (BIS0 = 1), should be tied low.
BIS0/BIS1	32/33	I	**Bus Interface Select Bits 0 & 1.** Used to select bus interface option. See Table 2-1 for details.
BPCLK	31	O	**Backplane Clock.** A 16.384MHz, 8.192MHz, 4.096MHz, or 2.048MHz clock output that is referenced to RCLK selectable via CCR5.7 and CCR5.6. In hardware mode, defaults to 16.384MHz output.
$\overline{CS}$	1	I	**Active-Low Chip Select.** Must be low to read or write to the device.
D0/AD0 to D7/AD7	19 to 12	I/O	**Data Bus/Address/Data Bus.** In non-multiplexed bus operation (BIS1 = 0, BIS0 = 1), serves as the data bus. In multiplexed bus operation (BIS1 = 0, BIS0 = 0), serves as an 8-bit multiplexed address/data bus.
$\overline{HRST}$	29	I	**Active-Low Hardware Reset.** Bringing $\overline{HRST}$ low will reset the DS2148 setting all control bits to their default state of all zeros.
$\overline{INT}$	23	O	**Active-Low Interrupt.** Flags host controller during conditions and change of conditions defined in the Status Register. Active low, open drain output.
MCLK	30	I	**Master Clock.** A 2.048MHz (±50ppm) clock source with TTL levels is applied at this pin. This clock is used internally for both clock/data recovery and for jitter attenuation. Use of a T1 1.544MHz clock source is optional. See Note 1 on clock accuracy at the end of this table.
NA	-	I	**Not Assigned.** Should be tied low.
PBEO	24	O	**PRBS Bit Error Output.** The receiver will constantly search for a 2^{15}-1 or a 2^{20}-1 PRBS depending on the ETS bit setting (CCR1.7). Remains high if out of synchronization with the PRBS pattern. Goes low when synchronized to the PRBS pattern. Any errors in the received pattern after synchronization will cause a positive going pulse (with same period as E1 or T1 clock) synchronous with RCLK. PRBS bit errors can also be reported to the ECR1 and ECR2 registers by setting CCR6.2 to a logic 1.
PBTS	44	I	**Parallel Bus Type Select.** When using the parallel port (BIS1 = 0), set high to select Motorola bus timing, set low to select Intel bus timing. This pin controls the function of the $\overline{RD}(\overline{DS})$, ALE(AS), and $\overline{WR}(R/\overline{W})$ pins. If PBTS = 1 and BIS1 = 0, then these pins assume the Motorola function listed in parenthesis (). In serial port mode, this pin should be tied low.
RCLK	40	O	**Receive Clock.** Buffered recovered clock from the line. Synchronous to MCLK in absence of signal at RTIP and RRING.
$\overline{RD}(\overline{DS})$	2	I	**Active-Low Read Input (Data Strobe).** DS is active low when in nonmultiplexed, Motorola mode. See the bus timing diagrams in Section 10.
RCL/LOTC	25	O	**Receive Carrier Loss/Loss of Transmit Clock.** An output which will toggle high during a receive carrier loss (CCR2.7 = 0) or will toggle high if the TCLK pin has not been toggled for 5µs ±2µs (CCR2.7 = 1). CCR2.7 defaults to logic 0 when in hardware mode.

NAME	PIN	I/O	FUNCTION
RNEG	39	O	**Receive Negative Data.** Updated on the rising edge (CCR2.0 = 0) or the falling edge (CCR2.0 = 1) of RCLK with the bipolar data out of the line interface. Set NRZE (CCR1.6) to a one for NRZ applications. In NRZ mode, data will be output on RPOS while a received error will cause a positive-going pulse synchronous with RCLK at RNEG. See Section 6.4 for details.
RPOS	38	O	**Receive Positive Data.** Updated on the rising edge (CCR2.0 = 0) or the falling edge (CCR2.0 = 1) of RCLK with bipolar data out of the line interface. Set NRZE (CCR1.6) to a one for NRZ applications. In NRZ mode, data will be output on RPOS while a received error will cause a positive-going pulse synchronous with RCLK at RNEG. See Section 6.2 for details.
RTIP/RRING	27/28	I	**Receive Tip and Ring.** Analog inputs for clock recovery circuitry. These pins connect via a 1:1 transformer to the line. See Section 5 for details.
TCLK	43	I	**Transmit Clock.** A 2.048MHz or 1.544MHz primary clock. Used to clock data through the transmit side formatter. Can be sourced internally by MCLK or RCLK. See Common Control Register 1 and Figure 1-3.
TEST	26	I	**Tri-state Control.** Set high to tri-state all outputs and I/O pins (including the parallel control port). Set low for normal operation. Useful in board level testing.
TNEG	42	I	**Transmit Negative Data.** Sampled on the falling edge (CCR2.1 = 0) or the rising edge (CCR2.1 = 1) of TCLK for data to be transmitted out onto the line.
TPOS	41	I	**Transmit Positive Data.** Sampled on the falling edge (CCR2.1 = 0) or the rising edge (CCR2.1 = 1) of TCLK for data to be transmitted out onto the line.
TTIP/TRING	34/37	O	**Transmit Tip and Ring.** Analog line driver outputs. These pins connect via a step-up transformer to the line. See Section 5 for details.
V_{DD}	21/36	-	**5.0V ±5% Positive Supply**
VSM	20	I	**Voltage Supply Mode.** Should be tied high for 5V operation
V_{SS}	22/35	-	**Signal Ground**
$\overline{WR}$ ($R/\overline{W}$)	3	I	**Active-Low Write Input (Read/Write).** See the bus timing diagrams in Section 10.

Table 2-4. Pin Assignment in Serial Port Mode

DS2148T PIN #	DS2148G PIN#	I/O	SERIAL PORT MODE
1	C3	I	$\overline{CS}$
2	C2	I	NA
3	B1	I	NA
4	D2	I	NA
5	C1	I	SCLK
6	D3	I	SDI
7	D1	I/O	SDO
8	E1	I	ICES
9	F2	I	OCES
10	F1	I	NA
11	G1	I	NA
12	E3	I/O	NA
13	F3	I/O	NA
14	G2	I/O	NA
15	F4	I/O	NA
16	G3	I/O	NA
17	E4	I/O	NA
18	G4	I/O	NA
19	F5	I/O	NA
20	G5	I	VSM
21	F6	-	V_{DD}
22	G6	-	V_{SS}
23	E5	I/O	$\overline{INT}$
24	E6	O	PBEO
25	F7	O	RCL/LOTC
26	D6	I	TEST
27	D5	I	RTIP
28	D7	I	RRING
29	C6	I	$\overline{HRST}$
30	C7	I	MCLK
31	B6	O	BPCLK
32	B7	I	BIS0
33	A7	I	BIS1
34	C5	O	TTIP
35	B5	-	V_{SS}
36	A6	-	V_{DD}
37	B4	O	TRING
38	C4	O	RPOS
39	A4	O	RNEG
40	B3	O	RCLK
41	A3	I	TPOS
42	B2	I	TNEG
43	A2	I	TCLK
44	A1	I	NA

Table 2-5. Pin Descriptions in Serial Port Mode (Sorted by Pin Name, DS2148T)

NAME	PIN	I/O	FUNCTION
BIS0/BIS1	32/33	I	**Bus Interface Select Bits 0 & 1.** Used to select bus interface option. See Table 2-1 for details.
BPCLK	31	O	**Backplane Clock.** A 16.384MHz, 8.192MHz, 4.096MHz, or 2.048MHz clock output that is referenced to RCLK selectable via CCR5.7 and CCR5.6. In hardware mode, defaults to 16.384MHz output.
$\overline{CS}$	1	I	**Active-Low Chip Select.** Must be low to read or write to the device.
$\overline{HRST}$	29	I	**Hardware Reset.** Bringing $\overline{HRST}$ low will reset the DS2148 setting all control bits to their default state of all zeros.
ICES	8	I	**Input Clock Edge Select.** Selects whether the serial port data input (SDI) is sampled on rising (ICES =0) or falling edge (ICES = 1) of SCLK.
$\overline{INT}$	23	O	**Active-Low Interrupt.** Flags host controller during conditions and change of conditions defined in the Status Register. Active low, open drain output.
MCLK	30	I	**Master Clock.** A 2.048MHz (±50ppm) clock source with TTL levels is applied at this pin. This clock is used internally for both clock/data recovery and for jitter attenuation. Use of a T1 1.544MHz clock source is optional. See Note 1 on clock accuracy at the end of this table.
NA	-	I	**Not Assigned.** Should be tied low.
OCES	9	I	**Output Clock Edge Select.** Selects whether the serial port data output (SDO) is valid on the rising (OCES = 1) or falling edge (OCES = 0) of SCLK.
PBEO	24	O	**PRBS Bit Error Output.** The receiver will constantly search for a 2^{15}-1 or a 2^{20}-1 PRBS depending on the ETS bit setting (CCR1.7). Remains high if out of synchronization with the PRBS pattern. Goes low when synchronized to the PRBS pattern. Any errors in the received pattern after synchronization will cause a positive going pulse (with same period as E1 or T1 clock) synchronous with RCLK. PRBS bit errors can also be reported to the ECR1 and ECR2 registers by setting CCR6.2 to a logic 1.
RCLK	40	O	**Receive Clock.** Buffered recovered clock from the line. Synchronous to MCLK in absence of signal at RTIP and RRING.
RCL/LOTC	25	O	**Receive Carrier Loss/Loss of Transmit Clock.** An output which will toggle high during a receive carrier loss (CCR2.7 = 0) or will toggle high if the TCLK pin has not been toggled for 5 µs ± 2 µs (CCR2.7 = 1). CCR2.7 defaults to logic 0 when in hardware mode.
RNEG	39	O	**Receive Negative Data.** Updated on the rising edge (CCR2.0 = 0) or the falling edge (CCR2.0 = 1) of RCLK with the bipolar data out of the line interface. Set NRZE (CCR1.6) to a one for NRZ applications. In NRZ mode, data will be output on RPOS while a received error will cause a positive-going pulse synchronous with RCLK at RNEG. See Section 6.4 for details.
RPOS	38	O	**Receive Positive Data.** Updated on the rising edge (CCR2.0 = 0) or the falling edge (CCR2.0 = 1) of RCLK with bipolar data out of the line interface. Set NRZE (CCR1.6) to a one for NRZ applications. In NRZ mode, data will be output on RPOS while a received error will cause a positive-going pulse synchronous with RCLK at RNEG. See Section 6.4 for details.
RTIP/RRING	27/28	I	**Receive Tip and Ring.** Analog inputs for clock recovery circuitry. These pins connect via a 1:1 transformer to the line. See Section 5 for details.
SCLK	5	I	**Serial Clock.** Serial bus clock input.

NAME	PIN	I/O	FUNCTION
SDI	6	I	**Serial Data Input.** Sampled on rising edge (ICES = 0) or the falling edge (ICES = 1) of SCLK.
SDO	7	O	**Serial Data Output.** Valid on the falling edge (OCES = 0) or the rising edge (OCES = 1) of SCLK.
TCLK	43	I	**Transmit Clock.** A 2.048 MHz or 1.544 MHz primary clock. Used to clock data through the transmit side formatter. Can be sourced internally by MCLK or RCLK. See Common Control Register 1 and Figure 1-3.
TEST	26	I	**Tri-State Control.** Set high to tri-state all outputs and I/O pins (including the parallel control port). Set low for normal operation. Useful in board level testing.
TNEG	42	I	**Transmit Negative Data.** Sampled on the falling edge (CCR2.1 = 0) or the rising edge (CCR2.1 = 1) of TCLK for data to be transmitted out onto the line.
TPOS	41	I	**Transmit Positive Data.** Sampled on the falling edge (CCR2.1 = 0) or the rising edge (CCR2.1 = 1) of TCLK for data to be transmitted out onto the line.
TTIP/TRING	34/37	O	**Transmit Tip and Ring .** Analog line driver outputs. These pins connect via a step-up transformer to the line. See Section 5 for details.
V_{DD}	21/36	-	**5.0V ±5% Positive Supply**
VSM	20	I	**Voltage Supply Mode.** Should be tied high for 5V operation.
V_{SS}	22/35	-	**Signal Ground**

Table 2-6. Pin Assignment in Hardware Mode

DS2148T PIN #	DS2148G PIN#	I/O	HARDWARE MODE
1	C3	I	EGL
2	C2	I	ETS
3	B1	I	NRZE
4	D2	I	SCLKE
5	C1	I	L2
6	D3	I	L1
7	D1	I/O	L0
8	E1	I	DJA
9	F2	I	JAMUX
10	F1	I	JAS
11	G1	I	HBE
12	E3	I/O	CES
13	F3	I/O	TPD
14	G2	I/O	TX0
15	F4	I/O	TX1
16	G3	I/O	LOOP0
17	E4	I/O	LOOP1
18	G4	I/O	MM0
19	F5	I/O	MM1
20	G5	I	VSM
21	F6	-	V_{DD}
22	G6	-	V_{SS}
23	E5	I/O	RT1
24	E6	O	PBEO
25	F7	O	RCL
26	D6	I	TEST
27	D5	I	RTIP
28	D7	I	RRING
29	C6	I	$\overline{\text{HRST}}$
30	C7	I	MCLK
31	B6	O	BPCLK
32	B7	I	BIS0
33	A7	I	BIS1
34	C5	O	TTIP
35	B5	-	V_{SS}
36	A6	-	V_{DD}
37	B4	O	TRING
38	C4	O	RPOS
39	A4	O	RNEG
40	B3	O	RCLK
41	A3	I	TPOS
42	B2	I	TNEG
43	A2	I	TCLK
44	A1	I	RT0

Table 2-7. Pin Description in Hardware Mode (Sorted by Pin Name, DS2148T)

NAME	PIN	I/O	FUNCTION
BIS0/BIS1	32/33	I	**Bus Interface Select Bits 0 & 1.** Used to select bus interface option. BIS0 = 1 and BIS1 = 1 selects hardware mode.
BPCLK	31	O	**Backplane Clock.** 16.384MHz output.
CES	12	I	**Receive & Transmit Clock Edge Select.** Selects which RCLK edge to update RPOS and RNEG and which TCLK edge to sample TPOS and TNEG. 0 = update RNEG/RPOS on rising edge of RCLK; sample TPOS/TNEG on falling edge of TCLK 1 = update RNEG/RPOS on falling edge of RCLK; sample TPOS/TNEG on rising edge of TCLK
DJA	8	I	**Disable Jitter Attenuator** 0 = jitter attenuator enabled 1 = jitter attenuator disabled
EGL	1	I	**Receive Equalizer Gain Limit.** This pin controls the sensitivity of the receive equalizer. **EGL E1 (ETS = 0)** 0 = -12dB (short haul) 1 = -43dB (long haul) **EGL T1 (ETS = 1)** 0 = -36dB (long haul) 1 = -30dB (limited long haul)
ETS	2	I	**E1/T1 Select.** 0 = E1 1 = T1
HBE	11	I	**Receive & Transmit HDB3/B8ZS Enable.** 0 = enable HDB3 (E1)/B8ZS (T1) 1 = disable HDB3 (E1)/B8ZS (T1)
$\overline{\text{HRST}}$	29	I	**Hardware Reset.** Bringing $\overline{\text{HRST}}$ low will reset the DS2148.
JAMUX	9	I	**Jitter Attenuator MUX.** Controls the source for JACLK. See Figure 1-1 and Table 2-13. **E1 (ETS = 0) JAMUX** MCLK = 2.048MHz 0 **T1 (ETS = 1)** MCLK = 2.048MHz 1 MCLK = 1.544MHz 0
JAS	10	I	**Jitter Attenuator Select** 0 = place the jitter attenuator on the receive side 1 = place the jitter attenuator on the transmit side
L0/L1/L2	7/6/5	I	**Transmit LIU Waveshape Select Bits 0 & 1 [H/W Mode].** These inputs determine the waveshape of the transmitter. See Table 7-1 and Table 7-2.
LOOP0/ LOOP1	16/17	I	**Loopback Select Bits 0 & 1 [H/W Mode].** These inputs determine the active loopback mode (if any). See Table 2-8.
MCLK	30	I	**Master Clock.** A 2.048MHz (±50ppm) clock source with TTL levels is applied at this pin. This clock is used internally for both clock/data recovery and for jitter attenuation. Use of a T1 1.544MHz clock source is optional. G.703 requires an accuracy of ±50ppm for both T1 and E1. TR62411 and ANSI specs require an accuracy of ±32ppm for T1 interfaces.
MM0/MM1	18/19	I	**Monitor Mode Select Bits 0 & 1 [H/W Mode].** These inputs determine if the receive equalizer is in a monitor mode. See Table 2-11.
NA	-	I	**Not Assigned.** Should be tied low.

NAME	PIN	I/O	FUNCTION
NRZE	3	I	**NRZ Enable [H/W Mode]** 0 = Bipolar data at RPOS/RNEG and TPOS/TNEG 1 = NRZ data at RPOS and TPOS or TNEG; RNEG outputs a positive going pulse when device receives a BPV, CV, or EXZ.
PBEO	24	O	**PRBS Bit Error Output.** The receiver will constantly search for a QRSS (T1) or a 2^{15}-1 (E1) PRBS depending on whether T1 or E1 mode is selected. Remains high if out of synchronization with the PRBS pattern. Goes low when synchronized to the PRBS pattern. Any errors in the received pattern after synchronization will cause a positive going pulse (with same period as E1 or T1 clock) synchronous with RCLK.
RCLK	40	O	**Receive Clock.** Buffered recovered clock from the line. Synchronous to MCLK in absence of signal at RTIP and RRING.
RCL	25	O	**Receive Carrier Loss.** An output which will toggle high during a receive carrier loss.
RNEG	39	O	**Receive Negative Data.** Updated on the rising edge (CES = 0) or the falling edge (CES = 1) of RCLK with the bipolar data out of the line interface. Set NRZE to a one for NRZ applications. In NRZ mode, data will be output on RPOS while a received error will cause a positive-going pulse synchronous with RCLK at RNEG. See Section 6.4 for details.
RPOS	38	O	**Receive Positive Data.** Updated on the rising edge (CES = 0) or the falling edge (CES = 1) of RCLK with bipolar data out of the line interface. Set NRZE pin to a one for NRZ applications. In NRZ mode, data will be output on RPOS while a received error will cause a positive-going pulse synchronous with RCLK at RNEG. See Section 6.4 for details.
RT0/RT1	44/23	I	**Receive LIU Termination Select Bits 0 & 1 [H/W Mode].** These inputs determine the receive termination. See Table 2-12.
RTIP/ RRING	27/28	I	**Receive Tip and Ring.** Analog inputs for clock recovery circuitry. These pins connect via a 1:1 transformer to the line. See Section 5 for details.
SCLKE	4	I	**Receive & Transmit Synchronization Clock Enable.** 0 = disable 2.048MHz synchronization transmit and receive mode 1 = enable 2.048MHz synchronization transmit and receive mode
TCLK	43	I	**Transmit Clock.** A 2.048MHz or 1.544MHz primary clock. Used to clock data through the transmit side formatter.
TEST	26	I	**Tri-State Control.** Set high to tri-state all outputs and I/O pins (including the parallel control port). Set low for normal operation. Useful in board level testing.
TNEG	42	I	**Transmit Negative Data.** Sampled on the falling edge (CES = 0) or the rising edge (CES = 1) of TCLK for data to be transmitted out onto the line.
TPD	13	I	**Transmit Power-Down** 0 = normal transmitter operation 1 = powers down the transmitter and tri-states the TTIP and TRING pins
TPOS	41	I	**Transmit Positive Data.** Sampled on the falling edge (CES = 0) or the rising edge (CES = 1) of TCLK for data to be transmitted out onto the line.
TTIP/ TRING	34/37	O	**Transmit Tip and Ring.** Analog line driver outputs. These pins connect via a step-up transformer to the line. See Section 5 for details.
TX0/TX1	14/15	I	**Transmit Data Source Select Bits 0 & 1 [H/W Mode].** These inputs determine the source of the transmit data. See Table 2-9.
V_{DD}	21/36	-	**5.0V ±5% Positive Supply**
VSM	20	I	**Voltage Supply Mode.** Should be tied high for 5V operation
V_{SS}	22/35	-	**Signal Ground**

Note 1: *G.703 requires an accuracy of ±50ppm for both T1 and E1. TR62411 and ANSI specs require an accuracy of ±32ppm for T1 interfaces.*

Table 2-8. Loopback Control in Hardware Mode

LOOPBACK	SYMBOL	CONTROL BIT	LOOP1	LOOP0
Remote Loopback	RLB	CCR6.6	1	1
Local Loopback	LLB	CCR6.7	1	0
Analog Loopback	ALB	CCR6.4	0	1
No Loopback	–	–	0	0

Table 2-9. Transmit Data Control in Hardware Mode

TRANSMIT DATA	SYMBOL	CONTROL BIT	TX1	TX0
Transmit Unframed All Ones	TUA1	CCR3.7	1	1
Transmit Alternating Ones and Zeros	TAOZ	CCR3.5	1	0
Transmit PRBS	TPRBSE	CCR3.4	0	1
TPOS and TNEG	–	–	0	0

Table 2-10. Receive Sensitivity Settings

EGL (CCR4.4)	ETS (CCR1.7)	RECEIVE SENSITIVITY
0	0 (E1)	-12dB (short haul)
1	0 (E1)	-43dB (long haul)
1	1 (T1)	-30dB (limited long haul)
0	1 (T1)	-36dB (long haul)

Table 2-11. Monitor Gain Settings

MM1 (CCR5.5)	MM0 (CCR5.4)	INTERNAL LINEAR GAIN BOOST (dB)
0	0	Normal operation (no boost)
0	1	20
1	0	26
1	1	32

Table 2-12. Internal Rx Termination Select

RT1 (CCR5.1)	RT0 (CCR5.0)	INTERNAL RECEIVE TERMINATION CONFIGURATION
0	0	Internal receive-side termination disabled
0	1	Internal receive-side 120Ω enabled
1	0	Internal receive-side 100Ω enabled
1	1	Internal receive-side 75Ω enabled

Table 2-13. MCLK Selection

MCLK	JAMUX (CCR1.3)	ETS (CCR1.7)
2.048MHz	0	0
2.048MHz	1	1
1.544MHz	0	1

Figure 2-1. Parallel Port Mode Pinout (BIS1 = 0, BIS0 = 1 or 0) (TQFP Package)

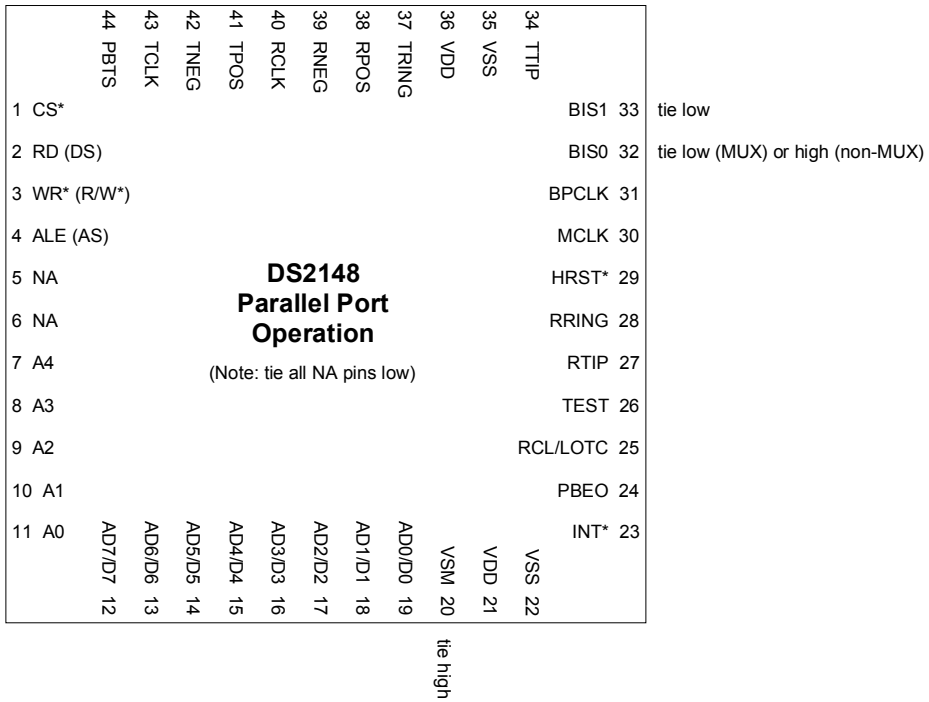


Figure 2-2. Serial Port Mode Pinout (BIS1 = 1, BIS0 = 0) (TQFP Package)

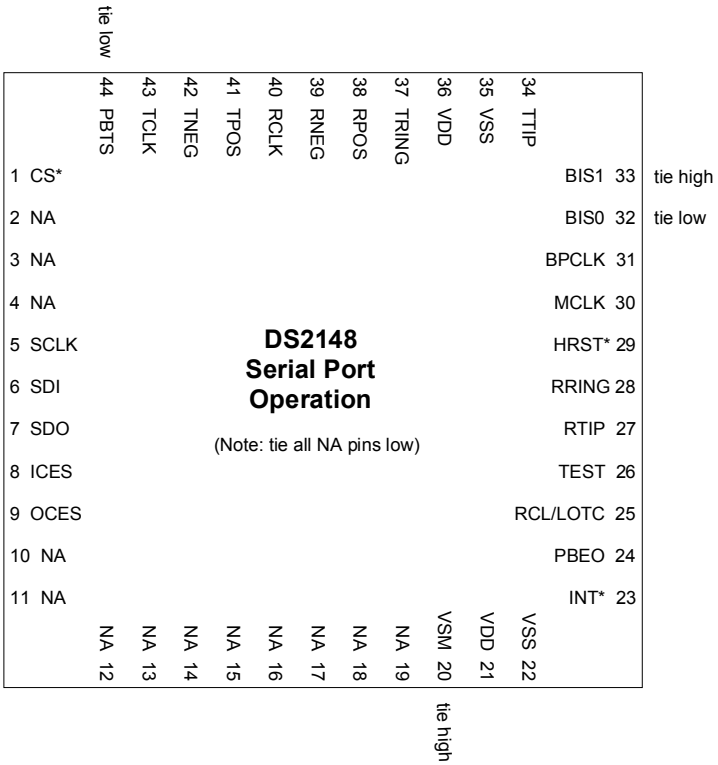
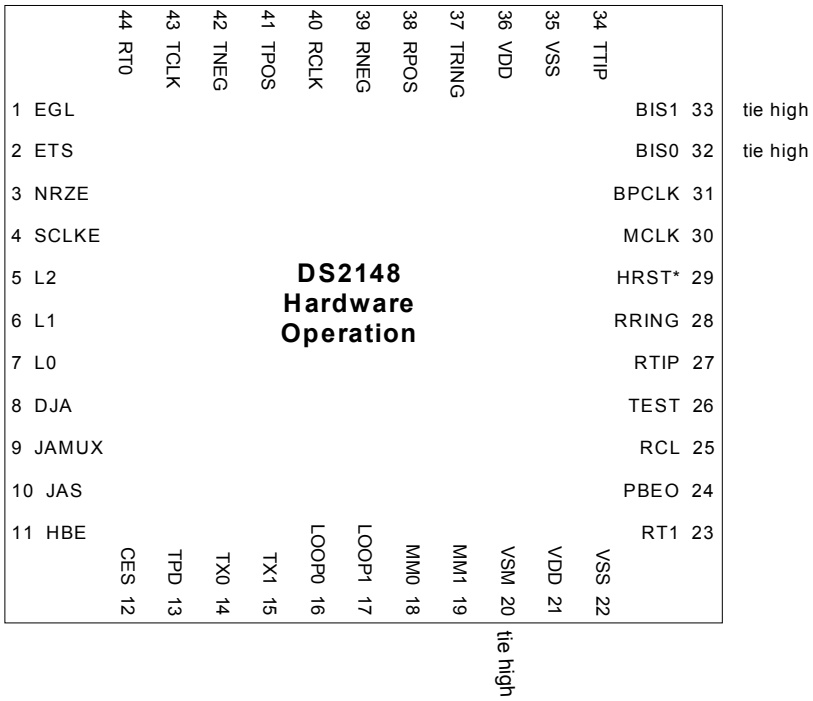


Figure 2-3. Hardware Mode Pinout (BIS1 = 1, BIS0 = 1) (TQFP Package)



3 HARDWARE MODE

In hardware mode (BIS1 = 1, BIS0 = 1), pins 1-19, 23, 25, 31, and 44 are redefined to be used for initializing the DS2148. BPCLK (pin 31) defaults to a 16.384MHz output when in hardware mode. The RCL/LOTC (pin 25) is designated to RCL when in hardware mode. JABDS (CCR4.2) defaults to logic 0. The RHBE (CCR2.3) and THBE (CCR2.2) control bits are combined and controlled by HBE at pin 11 while the RSCLKE (CCR5.3) and TSCLKE (CCR5.2) bits are combined and controlled by SCLKE at pin 4. TCES (CCR2.1) and RCES (CCR2.0) are combined and controlled by CES at pin 12. The transmitter functions are combined and controlled by TX1 (pin 15) and TX0 (pin 14). LOOP1 (pin 17) and LOOP0 (pin 16) control the loopback functions. All other control bits default to the logic 0 setting.

3.1 Register Map

Table 3-1. Register Map

NAME	REGISTER NAME	R/W	PARALLEL PORT MODE	SERIAL PORT MODE (Notes 2–5) (msb) (lsb)
CCR1	Common Control Register 1	R/W	00h	B000 000A
CCR2	Common Control Register 2	R/W	01h	B000 001A
CCR3	Common Control Register 3	R/W	02h	B000 010A
CCR4	Common Control Register 4	R/W	03h	B000 011A
CCR5	Common Control Register 5	R/W	04h	B000 100A
CCR6	Common Control Register 6	R/W	05h	B000 101A
SR	Status Register	R	06h	B000 110A
IMR	Interrupt Mask Register	R/W	07h	B000 111A
RIR1	Receive Information Register 1	R	08h	B001 000A
RIR2	Receive Information Register 2	R	09h	B001 001A
IBCC	In-Band Code Control Register	R/W	0Ah	B001 010A
TCD1	Transmit Code Definition Register 1	R/W	0Bh	B001 011A
TCD2	Transmit Code Definition Register 2	R/W	0Ch	B001 100A
RUPCD1	Receive Up Code Definition Register 1	R/W	0Dh	B001 101A
RUPCD2	Receive Up Code Definition Register 2	R/W	0Eh	B001 110A
RDNCD1	Receive Down Code Definition Register 1	R/W	0Fh	B001 111A
RDNCD2	Receive Down Code Definition Register 2	R/W	10h	B010 000A
ECR1	Error Count Register 1	R	11h	B010 001A
ECR2	Error Count Register 2	R	12h	B010 010A
TEST1	Test 1	R/W	13h	B010 011A
TEST2	Test 2	R/W	14h	B010 100A
TEST3	Test 3	R/W	15h	B010 101A
–	–	–	Note 1	–

NOTES:
1) Register addresses 16h to 1Fh do not exist.
2) In the Serial Port Mode, the LSB is on the right hand side.
3) In the Serial Port Mode, data is read and written LSB first.
4) In the Serial Port Mode, the A bit (the LSB) determines whether the access is a read (A = 1) or a write (A = 0).
5) In the Serial Port Mode, the B bit (the MSB) determines whether the access is a burst access (B = 1) or a single register access (B = 0).

3.2 Parallel Port Operation

When using the parallel interface on the DS2148 (BIS1 = 0) the user has the option for either multiplexed bus operation (BIS1 = 0, BIS0 = 0) or nonmultiplexed bus operation (BIS1 = 0, BIS0 = 1). The DS2148 can operate with either Intel or Motorola bus timing configurations. If the PBTS pin is tied low, Intel timing will be selected; if tied high, Motorola timing will be selected. All Motorola bus signals are listed in parentheses. See the timing diagrams in Section 10 for more details.

3.3 Serial Port Operation

Setting BIS1 = 1 and BIS0 = 0 enables the serial bus interface on the DS2148. Port read/write timing is unrelated to the system transmit and receive timing, allowing asynchronous reads or writes by the host. See Section 10 for the AC timing of the serial port. All serial port accesses are LSB first. See Figure 3-1, Figure 3-2, Figure 3-3, and Figure 3-4 for more details.

Reading or writing to the internal registers requires writing one address/command byte prior to transferring register data. The first bit written (LSB) of the address/command byte specifies whether the access is a read (1) or a write (0). The next 5 bits identify the register address. Bit 7 is reserved and must be set to 0 for proper operation.

The last bit (MSB) of the address/command byte is the burst mode bit. When the burst bit is enabled (B = 1) and a READ operation is performed, addresses 0 through 15h are read sequentially, starting at address 0h. And when the burst bit is enabled and a WRITE operation is performed, addresses 0 through 16h are written sequentially, starting at address 0h. Burst operation is stopped once address 15h is read. See Figure 3-5 and Figure 3-6 for more details.

All data transfers are initiated by driving the $\overline{CS}$ input low. When input clock-edge select (ICES) is low, input data is latched on the rising edge of SCLK and when ICES is high, input data is latched on the falling edge of SCLK. When output clock-edge select (OCES) is low, data is output on the falling edge of SCLK and when OCES is high, data is output on the rising edge of SCLK. Data is held until the next falling or rising edge. All data transfers are terminated if the $\overline{CS}$ input transitions high. Port control logic is disabled and SDO is tri-stated when $\overline{CS}$ is high.

Figure 3-1. Serial Port Operation for Read Access (R = 1) Mode 1

ICES = 1 (sample SDI on the falling edge of SCLK)
OCES = 1 (update SDO on rising edge of SCLK)

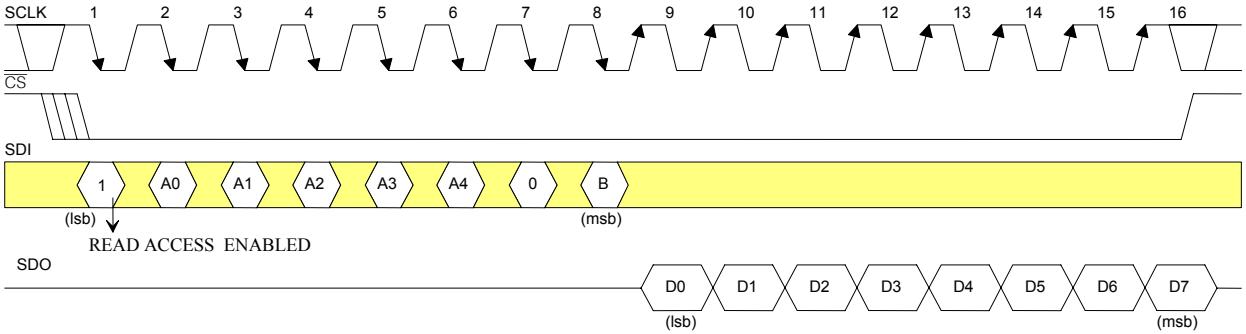


Figure 3-2. Serial Port Operation for Read Access Mode 2

ICES = 1 (sample SDI on the falling edge of SCLK)
OCES = 0 (update SDO on falling edge of SCLK)