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# DS2151Q
# T1 Single-Chip Transceiver

www.maxim-ic.com

## FEATURES

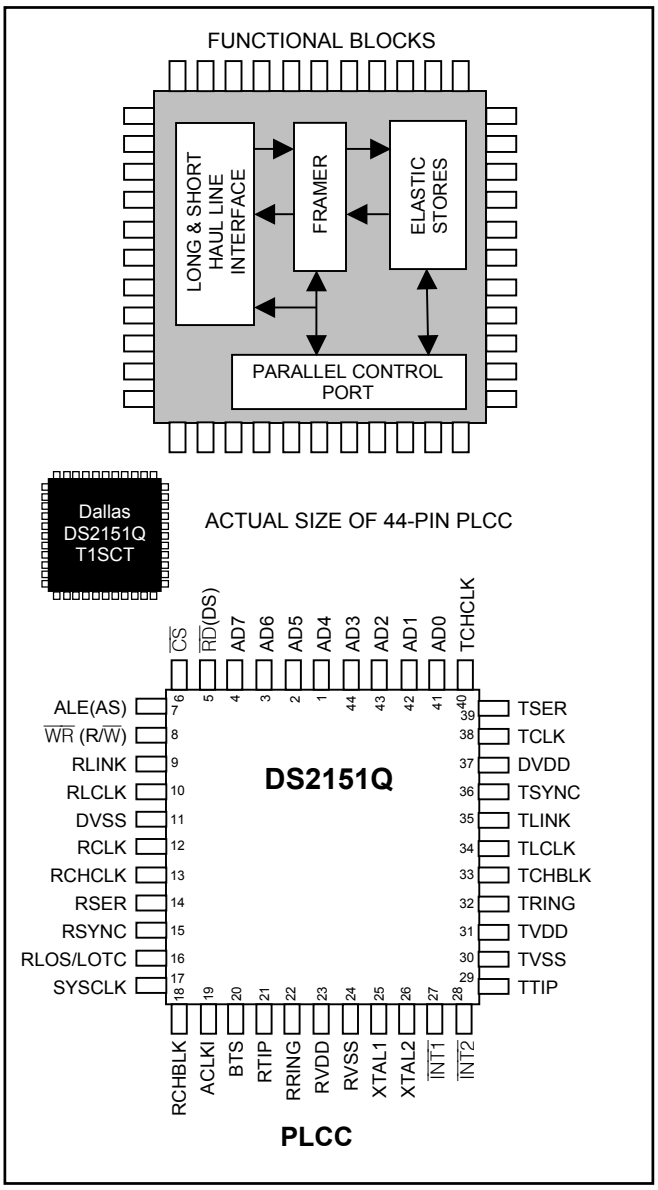
- Complete DS1/ISDN-PRI Transceiver Functionality
- Line Interface Can Handle Both Long- and Short-Haul Trunks
- 32-Bit or 128-Bit Jitter Attenuator
- Generates DSX-1 and CSU Line Build-Outs
- Frames to D4, ESF, and SLC-96® Formats
- Dual On-Board Two-Frame Elastic Store Slip Buffers that Connect to Backplanes Up to 8.192MHz
- 8-Bit Parallel Control Port That can be Used on Either Multiplexed or Nonmultiplexed Buses
- Extracts and Inserts Robbed-Bit Signaling
- Detects and Generates Yellow and Blue Alarms
- Programmable Output Clocks for Fractional T1
- Fully Independent Transmit and Receive Functionality
- On-Board FDL Support Circuitry
- Generates and Detects CSU Loop Codes
- Contains ANSI One's Density Monitor and Enforcer
- Large Path and Line Error Counters Including BPV, CV, CRC6, and Framing Bit Errors
- Pin Compatible with DS2153Q E1 Single-Chip Transceiver
- 5V Supply; Low-Power CMOS

## ORDERING INFORMATION

| PART | TEMP RANGE | PIN-PACKAGE |
|---|---|---|
| DS2151Q | 0°C to +70°C | 44 PLCC |
| DS2151Q+ | 0°C to +70°C | 44 PLCC |
| DS2151QN | -40°C to +85°C | 44 PLCC |
| DS2151QN+ | -40°C to +85°C | 44 PLCC |

*+Denotes lead-free/RoHS-compliant package.*

## PIN CONFIGURATION




**Note:** *Some revisions of this device may incorporate deviations from published specifications known as errata. Multiple revisions of any device may be simultaneously available through various sales channels. For information about device errata, click here: www.maxim-ic.com/errata.*

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# 1 DETAILED DESCRIPTION

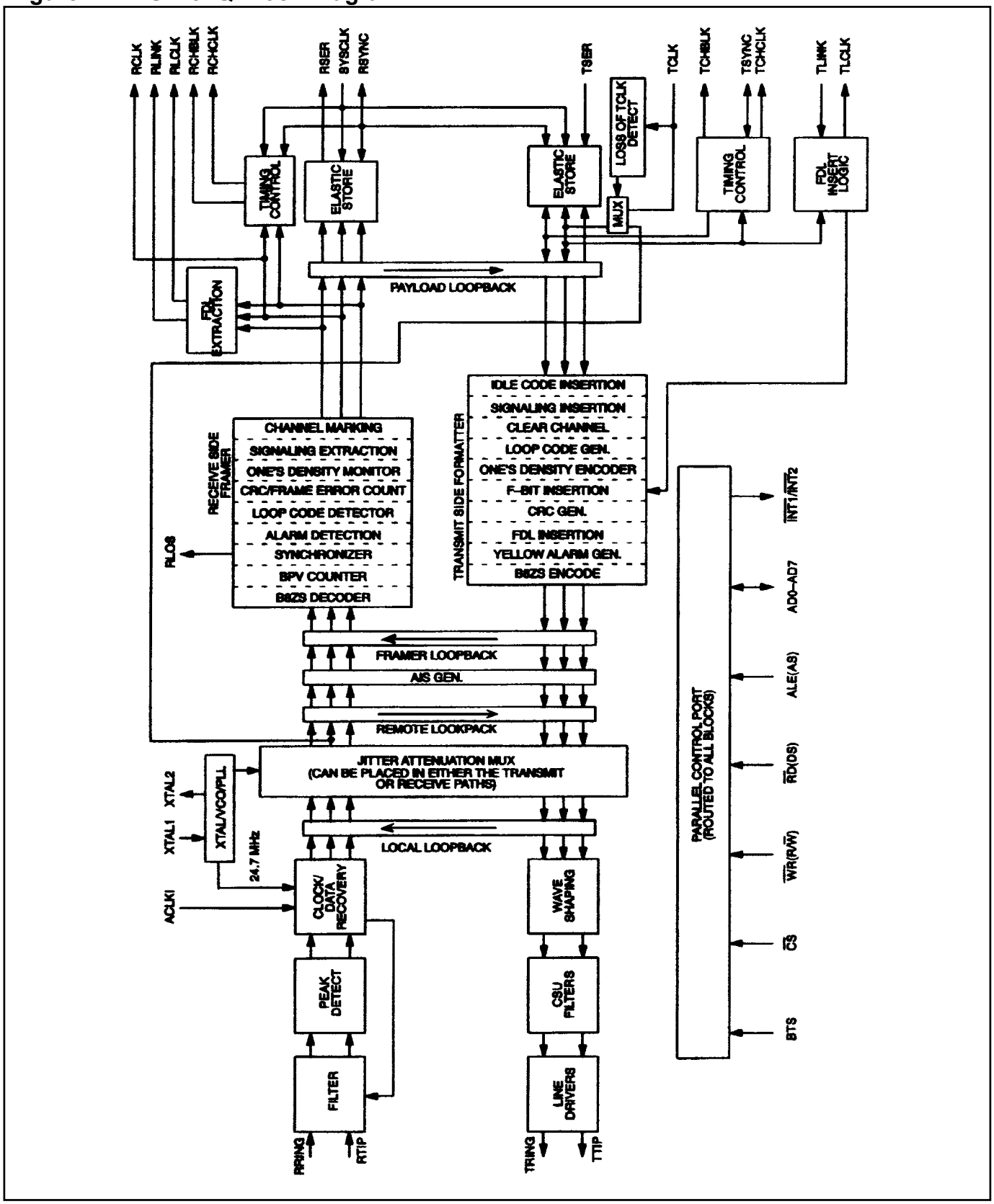
The DS2151Q T1 single-chip transceiver (SCT) contains all the necessary functions for connection to T1 lines whether they be DS-1 long haul or DSX-1 short haul. The clock recovery circuitry automatically adjusts to T1 lines from 0 feet to over 6000 feet in length. The device can generate both DSX-1 line build-outs as well as CSU build-outs of -7.5dB, -15dB, and -22.5dB. The on-board jitter attenuator (selectable to either 32 bits or 128 bits) can be placed in either the transmit or receive data paths. The framer locates the frame and multiframe boundaries and monitors the data stream for alarms. It is also used for extracting and inserting robbed-bit signaling data and FDL data. The device contains a set of 64 8-bit internal registers that the user can access to control the operation of the unit. Quick access via the parallel control port allows a single micro to handle many T1 lines. The device fully meets all of the latest T1 specifications including ANSI T1.403-199X, AT&T TR 62411 (12-90), and ITU G.703, G.704, G.706, G.823, and I.431.

## 1.1 Introduction

The analog AMI waveform off of the T1 line is transformer coupled into the RRING and RTIP pins of the DS2151Q. The device recovers clock and data from the analog signal and passes it through the jitter attenuation mux to the receive side framer where the digital serial stream is analyzed to locate the framing pattern. If needed, the receive side elastic store can be enabled in order to absorb the phase and frequency differences between the recovered T1 data stream and an asynchronous backplane clock which is provided at the SYSCLK input.

The transmit side of the DS2151Q is totally independent from the receive side in both the clock requirements and characteristics. Data can be either provided directly to the transmit formatter or via an elastic store. The transmit formatter will provide the necessary data overhead for T1 transmission. Once the data stream has been prepared for transmission, it is sent via the jitter attenuation mux to the waveshaping and line driver functions. The DS2151Q will drive the T1 line from the TTIP and TRING pins via a coupling transformer.

**Figure 1-1. DS2151Q Block Diagram**



# 2 PIN DESCRIPTION

| PIN | NAME | TYPE | FUNCTION |
|---|---|---|---|
| 1–4, 41–44 | AD4–AD7, AD0–AD3 | I/O | **Address/Data Bus.** An 8-bit multiplexed address/data bus. |
| 5 | $\overline{RD}$(DS) | I | **Active-Low Read Input (Data Strobe)** |
| 6 | $\overline{CS}$ | I | **Active-Low Chip Select.** Must be low to read or write the port. |
| 7 | ALE(AS) | I | **Address Latch Enable (Address Strobe).** A positive going edge serves to demultiplex the bus. |
| 8 | $\overline{WR}$(R/$\overline{W}$) | I | **Active-Low Write Input (Read/Write)** |
| 9 | RLINK | O | **Receive Link Data.** Updated with either FDL data (ESF) or Fs bits (D4) or Z bits (ZBTSI) one RCLK before the start of a frame. See Section 14 for timing details. |
| 10 | RLCLK | O | **Receive Link Clock.** 4kHz or 2kHz (ZBTSI) demand clock for the RLINK output. See Section 14 for timing details. |
| 11 | DVSS | — | **Digital Signal Ground.** 0.0V. Should be tied to local ground plane. |
| 12 | RCLK | O | **Receive Clock**. Recovered 1.544MHz clock. |
| 13 | RCHCLK | O | **Receive Channel Clock**. 192kHz clock that pulses high during the LSB of each channel. Useful for parallel to serial conversion of channel data, locating Robbed-Bit signaling bits, and for blocking clocks in DDS applications. See Section 14 for timing details. |
| 14 | RSER | O | **Receive Serial Data.** Received NRZ serial data, updated on rising edges of RCLK or SYSCLK. |
| 15 | RSYNC | I/O | **Receive Sync.** An extracted pulse, one RCLK wide, is output at this pin, which identifies either frame (RCR2.4 = 0) or multiframe boundaries (RCR2.4 = 1). If set to output frame boundaries, then via RCR2.5, RSYNC can also be set to output double-wide pulses on signaling frames. If the elastic store is enabled via the CCR1.2, then this pin can be enabled to be an input via RCR2.3 at which a frame boundary pulse is applied. See Section 14 for timing details. |
| 16 | RLOS/LOTC | O | **Receive Loss of Sync/Loss of Transmit Clock.** A dual function output. If CCR3.5 = 0, will toggle high when the synchronizer is searching for the T1 frame and multiframe; if CCR3.5 = 1, will toggle high if the TCLK pin has not toggled for 5µs. |
| 17 | SYSCLK | I | **System Clock.** 1.544MHz or 2.048MHz clock. Only used when the elastic store functions are enabled via either CCR1.7 or CCR1.2. Should be tied low in applications that do not use the elastic store. If tied high for more than 100µs, will force all output pins (including the parallel port) to tri-state. |
| 18 | RCHBLK | O | **Receive Channel Block.** A user-programmable output that can be forced high or low during any of the 24 T1 channels. Useful for blocking clocks to a serial UART or LAPD controller in applications where not all T1 channels are used such as Fractional T1, 384kbps service, 768kbps, or ISDN-PRI. Also useful for locating individual channels in drop-and-insert applications. See Section 14 for timing details. |
| 19 | ACLKI | I | **Alternate Clock Input.** Upon a receive carrier loss, the clock applied at this pin (normally 1.544MHz) will be routed to the RCLK pin. If no clock is routed to this pin, then it should be tied to DVSS via a 1kΩ resistor. |

| PIN | NAME | TYPE | FUNCTION |
|---|---|---|---|
| 20 | BTS | I | **Bus Type Select.** Strap high to select Motorola bus timing; strap low to select Intel bus timing. This pin controls the function of the $\overline{RD}$(DS), ALE(AS), and $\overline{WR}$(R/$\overline{W}$) pins. If BTS = 1, then these pins assume the function listed in parentheses. |
| 21, 22 | RTIP, RRING | — | **Receive Tip and Ring.** Analog inputs for clock recovery circuitry; connects to a 1:1 transformer (see Section 13 for details). |
| 23 | RVDD | — | **Receive Analog Positive Supply**. 5.0V. Should be tied to DVDD and TVDD pins. |
| 24 | RVSS | — | **Receive Signal Ground.** 0V. Should be tied to local ground plane. |
| 25, 26 | XTAL1, XTAL2 | — | **Crystal Connections.** A pullable 6.176MHz crystal must be applied to these pins. See Section 13 for crystal specifications. |
| 27 | $\overline{INT1}$ | O | **Receive Alarm Interrupt 1.** Flags host controller during alarm conditions defined in Status Register 1. Active low, open drain output. |
| 28 | $\overline{INT2}$ | O | **Receive Alarm Interrupt 2.** Flags host controller during conditions defined in Status Register 2. Active low, open drain output. |
| 29 | TTIP | — | **Transmit Tip.** Analog line driver output; connects to a step-up transformer (see Section 13 for details). |
| 30 | TVSS | — | **Transmit Signal Ground.** 0V. Should be tied to local ground plane. |
| 31 | TVDD | — | **Transmit Analog Positive Supply.** 5.0V. Should be tied to DVDD and RVDD pins. |
| 32 | TRING | — | **Transmit Ring**. Analog line driver outputs; connects to a step-up transformer (see Section 13 for details). |
| 33 | TCHBLK | O | **Transmit Channel Block**. A user-programmable output that can be forced high or low during any of the 24 T1 channels. Useful for blocking clocks to a serial UART or LAPD controller in applications where not all T1 channels are used such as Fractional T1, 384kbps service, 768kbps, or ISDN-PRI. Also useful for locating individual channels in drop-and-insert applications. See Section 14 for timing details. |
| 34 | TLCLK | O | **Transmit Link Clock.** 4kHz or 2kHz (ZBTSI) demand clock for the TLINK input. See Section 14 for timing details. |
| 35 | TLINK | I | **Transmit Link Data.** If enabled via TCR1.2, this pin will be sampled during the F-bit time on the falling edge of TCLK for data insertion into either the FDL stream (ESF) or the Fs bit position (D4) or the Z-bit position (ZBTSI). See Section 14 for timing details. |
| 36 | TSYNC | I/O | **Transmit Sync.** A pulse at this pin will establish either frame or multiframe boundaries for the DS2151Q. Via TCR2.2, the DS2151Q can be programmed to output either a frame or multiframe pulse at this pin. If this pin is set to output pulses at frame boundaries, it can also be set via TCR2.4 to output double-wide pulses at signaling frames. See Section 14 for timing details. |
| 37 | DVDD | — | **Digital Positive Supply.** 5.0V. Should be tied to RVDD and TVDD pins. |
| 38 | TCLK | I | **Transmit Clock.** 1.544MHz primary clock. |
| 39 | TSER | I | **Transmit Serial Data.** Transmit NRZ serial data, sampled on the falling edge of TCLK. |
| 40 | TCHCLK | O | **Transmit Channel Clock.** 192kHz clock that pulses high during the LSB of each channel. Useful for parallel to serial conversion of channel data, locating robbed-bit signaling bits, and for blocking clocks in DDS applications. See Section 14 for timing details. |

## 2.1 DS2151Q Register Map

| ADDRESS | R/W | REGISTER NAME | ADDRESS | R/W | REGISTER NAME |
|---|---|---|---|---|---|
| 20 | R/W | Status Register 1 | 30 | R/W | Common Control Register 3 |
| 21 | R/W | Status Register 2 | 31 | R/W | Receive Information Register 2 |
| 22 | R/W | Receive Information Register 1 | 32 | R/W | Transmit Channel Blocking Register 1 |
| 23 | R | Line Code Violation Count Register 1 | 33 | R/W | Transmit Channel Blocking Register 2 |
| 24 | R | Line Code Violation Count Register 2 | 34 | R/W | Transmit Channel Blocking Register 3 |
| 25 | R | Path Code Violation Count Register 1 (Note 1) | 35 | R/W | Transmit Control Register 1 |
| 26 | R | Path Code Violation Count Register 2 | 36 | R/W | Transmit Control Register 2 |
| 27 | R | Multiframe Out of Sync Count Register 2 | 37 | R/W | Common Control Register 1 |
| 28 | R | Receive FDL Register | 38 | R/W | Common Control Register 2 |
| 29 | R/W | Receive FDL Match Register 1 | 39 | R/W | Transmit Transparency Register 1 |
| 2A | R/W | Receive FDL Match Register 2 | 3A | R/W | Transmit Transparency Register 2 |
| 2B | R/W | Receive Control Register 1 | 3B | R/W | Transmit Transparency Register 3 |
| 2C | R/W | Receive Control Register 2 | 3C | R/W | Transmit Idle Register 1 |
| 2D | R/W | Receive Mark Register 1 | 3D | R/W | Transmit Idle Register 2 |
| 2E | R/W | Receive Mark Register 2 | 3E | R/W | Transmit Idle Register 3 |
| 2F | R/W | Receive Mark Register 3 | 3F | R/W | Transmit Idle Definition Register |
| 60 | R | Receive Signaling Register 1 | 70 | R/W | Transmit Signaling Register 1 |
| 61 | R | Receive Signaling Register 2 | 71 | R/W | Transmit Signaling Register 2 |
| 62 | R | Receive Signaling Register 3 | 72 | R/W | Transmit Signaling Register 3 |
| 63 | R | Receive Signaling Register 4 | 73 | R/W | Transmit Signaling Register 4 |
| 64 | R | Receive Signaling Register 5 | 74 | R/W | Transmit Signaling Register 5 |
| 65 | R | Receive Signaling Register 6 | 75 | R/W | Transmit Signaling Register 6 |
| 66 | R | Receive Signaling Register 7 | 76 | R/W | Transmit Signaling Register 7 |
| 67 | R | Receive Signaling Register 8 | 77 | R/W | Transmit Signaling Register 8 |
| 68 | R | Receive Signaling Register 9 | 78 | R/W | Transmit Signaling Register 9 |
| 69 | R | Receive Signaling Register 10 | 79 | R/W | Transmit Signaling Register 10 |
| 6A | R | Receive Signaling Register 11 | 7A | R/W | Transmit Signaling Register 11 |
| 6B | R | Receive Signaling Register 12 | 7B | R/W | Transmit Signaling Register 12 |
| 6C | R/W | Receive Channel Blocking Register 1 | 7C | R/W | Line Interface Control Register |
| 6D | R/W | Receive Channel Blocking Register 2 | 7D | R/W | Test Register (Note 2) |
| 6E | R/W | Receive Channel Blocking Register 3 | 7E | R/W | Transmit FDL Register |
| 6F | R/W | Interrupt Mask Register 2 | 7F | R/W | Interrupt Mask Register 1 |

***Note 1:*** *Address 25 also contains Multiframe Out of Sync Count Register 1.*
***Note 2:*** *The Test Register is used only by the factory; this register must be cleared (set to all 0s) on power-up initialization to insure proper operation.*

# 3 PARALLEL PORT

The DS2151Q is controlled via a multiplexed bidirectional address/data bus by an external microcontroller or microprocessor. The DS2151Q can operate with either Intel or Motorola bus timing configurations. If the BTS pin is tied low, Intel timing will be selected; if tied high, Motorola timing will be selected. All Motorola bus signals are listed in parentheses (). See the timing diagrams in Section 14 for more details. The multiplexed bus on the DS2151Q saves pins because the address information and data information share the same signal paths. The addresses are presented to the pins in the first portion of the bus cycle and data will be transferred on the pins during second portion of the bus cycle. Addresses must be valid prior to the falling edge of ALE (AS), at which time the DS2151Q latches the address from the AD0 to AD7 pins. Valid write data must be present and held stable during the later portion of the DS or $\overline{WR}$ pulses. In a read cycle, the DS2151Q outputs a byte of data during the latter portion of the DS or $\overline{RD}$ pulses. The read cycle is terminated and the bus returns to a high impedance state as $\overline{RD}$ transitions high in Intel timing or as DS transitions low in Motorola timing. The DS2151Q can also be easily connected to nonmultiplexed buses. Refer to the separate application note for a detailed discussion of this topic.

# 4 CONTROL REGISTERS

The operation of the DS2151Q is configured via a set of eight registers. Typically, the control registers are only accessed when the system is first powered up. Once the DS2151Q has been initialized, the control registers will only need to be accessed when there is a change in the system configuration. There are two Receive Control Registers (RCR1 and RCR2), two Transmit Control Registers (TCR1 and TCR2), a Line Interface Control Register (LICR), and three Common Control Registers (CCR1, CCR2, and CCR3). Seven of the eight registers are described below. The LICR is described in Section 13.

## RCR1: RECEIVE CONTROL REGISTER 1 (Address = 2B Hex)

| (MSB) | | | | | | | (LSB) |
|---|---|---|---|---|---|---|---|
| LCVCRF | ARC | OOF1 | OOF2 | SYNCC | SYNCT | SYNCE | RESYNC |

| SYMBOL | POSITION | NAME AND DESCRIPTION |
|---|---|---|
| LCVCRF | RCR1.7 | **Line Code Violation Count Register Function Select.**<br>0 = do not count excessive 0s<br>1 = count excessive 0s |
| ARC | RCR1.6 | **Auto Resync Criteria.**<br>0 = Resync on OOF or RCL event<br>1 = Resync on OOF only |
| OOF1 | RCR1.5 | **Out Of Frame Select 1.**<br>0 = 2/4 frame bits in error<br>1 = 2/5 frame bits in error |
| OOF2 | RCR1.4 | **Out Of Frame Select 2.**<br>0 = follow RCR1.5<br>1 = 2/6 frame bits in error |
| SYNCC | RCR1.3 | **Sync Criteria.**<br>In D4 Framing Mode<br>0 = search for Ft pattern, then search for Fs pattern<br>1 = cross couple Ft and Fs pattern<br>In ESF Framing Mode<br>0 = search for FPS pattern only<br>1 = search for FPS and verify with CRC6 |
| SYNCT | RCR1.2 | **Sync Time**.<br>0 = qualify 10 bits<br>1 = qualify 24 bits |
| SYNCE | RCR1.1 | **Sync Enable**.<br>0 = auto resync enabled<br>1 = auto resync disabled |
| RESYNC | RCR1.0 | **Resync**. When toggled from low to high, a resynchronization of the receive side framer is initiated. Must be cleared and set again for a subsequent resync. |

## RCR2: RECEIVE CONTROL REGISTER 2 (Address = 2C Hex)

| (MSB) | | | | | | | (LSB) |
|---|---|---|---|---|---|---|---|
| RCS | RZBTSI | RSDW | RSM | RSIO | RD4YM | FSBE | MOSCRF |

| SYMBOL | POSITION | NAME AND DESCRIPTION |
|---|---|---|
| RCS | RCR2.7 | **Receive Code Select.**<br>0 = idle code (7F Hex)<br>1 = digital milliwatt code (1E/0B/0B/1E/9E/8B/8B/9E Hex) |
| RZBTSI | RCR2.6 | **Receive Side ZBTSI Enable.**<br>0 = ZBTSI disabled<br>1 = ZBTSI enabled |
| RSDW | RCR2.5 | **RSYNC Double-Wide.**<br>0 = do not pulse double-wide in signaling frames<br>1 = do pulse double-wide in signaling frames (Note: this bit must be set to 0 when RCR2.4 = 1 or when RCR2.3 = 1.) |
| RSM | RCR2.4 | **RSYNC Mode Select.**<br>0 = frame mode (see the timing in Section 14)<br>1 = multiframe mode (see the timing in Section 14) |
| RSIO | RCR2.3 | **RSYNC I/O Select.**<br>0 = RSYNC is an output<br>1 = RSYNC is an input (only valid if elastic store enabled)<br>(Note: this bit must be set to 0 when CCR1.2 = 0.) |
| RD4YM | RCR2.2 | **Receive Side D4 Yellow Alarm Select.**<br>0 = 0s in bit 2 of all channels<br>1 = a 1 in the S-bit position of frame 12 |
| FSBE | RCR2.1 | **PCVCR Fs Bit Error Report Enable.**<br>0 = do not report bit errors in Fs bit position; only Ft bit position<br>1 = report bit errors in Fs bit position as well as Ft bit position |
| MOSCRF | RCR2.0 | **Multiframe Out of Sync Count Register Function Select**.<br>0 = count errors in the framing bit position<br>1 = count the number of multiframes out of sync |

## TCR1: TRANSMIT CONTROL REGISTER 1 (Address = 35 Hex)

| (MSB) | | | | | | | (LSB) |
|---|---|---|---|---|---|---|---|
| LOTCMC | TFPT | TCPT | RBSE | GB7S | TLINK | TBL | TYEL |

| SYMBOL | POSITION | NAME AND DESCRIPTION |
|---|---|---|
| LOTCMC | TCR1.7 | **Loss Of Transmit Clock Mux Control**. Determines whether the transmit side formatter should switch to the ever present RCLK if the TCLK input should fail to transition (Figure 1-1).<br>0 = do not switch to RCLK if TCLK stops<br>1 = switch to RCLK if TCLK stops |
| TFPT | TCR1.6 | **Transmit Framing Pass Through**. (See note below.)<br>0 = Ft or FPS bits sourced internally<br>1 = Ft or FPS bits sampled at TSER during F-bit time |
| TCPT | TCR1.5 | **Transmit CRC Pass Through**. (See note below.)<br>0 = source CRC6 bits internally<br>1 = CRC6 bits sampled at TSER during F-bit time |
| RBSE | TCR1.4 | **Robbed-Bit Signaling Enable**. (See note below.)<br>0 = no signaling is inserted in any channel<br>1 = signaling is inserted in all channels (the TTR registers can be used to block insertion on a channel by channel basis) |
| GB7S | TCR1.3 | **Global Bit 7 Stuffing**. (See note below.)<br>0 = allow the TTR registers to determine which channels containing all 0s are to be Bit 7 stuffed<br>1 = force Bit 7 stuffing in all 0 byte channels regardless of how the TTR registers are programmed |
| TLINK | TCR1.2 | **TLINK Select**. (See note below.)<br>0 = source FDL or Fs bits from TFDL register<br>1 = source FDL or Fs bits from the TLINK pin |
| TBL | TCR1.1 | **Transmit Blue Alarm**. (See note below.)<br>0 = transmit data normally<br>1 = transmit an unframed all 1s code at TPOS and TNEG |
| TYEL | TCR1.0 | **Transmit Yellow Alarm**. (See note below.)<br>0 = do not transmit yellow alarm<br>1 = transmit yellow alarm |

**Note:** For a detailed description of how the bits in TCR1 affect the transmit side formatter of the DS2151Q, see Figure 14-9.

## TCR2: TRANSMIT CONTROL REGISTER 2 (Address = 36 Hex)

| (MSB) | | | | | | | (LSB) |
|---|---|---|---|---|---|---|---|
| TEST1 | TEST0 | TZBTSI | TSDW | TSM | TSIO | TD4YM | B7ZS |

| SYMBOL | POSITION | NAME AND DESCRIPTION |
|---|---|---|
| TEST1 | TCR2.7 | **Test Mode Bit 1 for Output Pins.** See Table 4-1. |
| TEST0 | TCR2.6 | **Test Mode Bit 0 for Output Pins.** See Table 4-1. |
| TZBTSI | TCR2.5 | **Transmit Side ZBTSI Enable.**<br>0 = ZBTSI disabled<br>1 = ZBTSI enabled |
| TSDW | TCR2.4 | **TSYNC Double-Wide.** (Note: This bit must be set to 0 when TCR2.3 = 1 or when TCR2.2 = 0.)<br>0 = do not pulse double-wide in signaling frames<br>1 = do pulse double-wide in signaling frames |
| TSM | TCR2.3 | **TSYNC Mode Select.**<br>0 = frame mode (see the timing in Section 14)<br>1 = multiframe mode (see the timing in Section 14) |
| TSIO | TCR2.2 | **TSYNC I/O Select.**<br>0 = TSYNC is an input<br>1 = TSYNC is an output |
| TD4YM | TCR2.1 | **Transmit Side D4 Yellow Alarm Select.**<br>0 = 0s in bit 2 of all channels<br>1 = 1 in the S-bit position of frame 12 |
| B7ZS | XTCR2.0 | **Bit 7 Zero Suppression Enable.**<br>0 = No stuffing occurs<br>1 = Bit 7 force to a 1 in channels with all 0s |

### Table 4-1. Output Pin Test Modes

| TEST1 | TEST0 | EFFECT ON OUTPUT PINS |
|---|---|---|
| 0 | 0 | Operate normally |
| 0 | 1 | Force all output pins tri-state (including all I/O pins and parallel port pins) |
| 1 | 0 | Force all output pins low (including all I/O pins except parallel port pins) |
| 1 | 1 | Force all output pins high (including all I/O pins except parallel port pins) |

## CCR1: COMMON CONTROL REGISTER 1 (Address = 37 Hex)

| (MSB) | | | | | | | (LSB) |
|---|---|---|---|---|---|---|---|
| TESE | LLB | RSAO | RLB | SCLKM | RESE | PLB | FLB |

| SYMBOL | POSITION | NAME AND DESCRIPTION |
|---|---|---|
| TESE | CCR1.7 | **Transmit Elastic Store Enable.**<br>0 = elastic store is bypassed<br>1 = elastic store is enabled |
| LLB | CCR1.6 | **Local Loopback.**<br>0 = loopback disabled<br>1 = loopback enabled |
| RSAO | CCR1.5 | **Receive Signaling All 1s.**<br>0 = allow robbed signaling bits to appear at RSER<br>1 = force all robbed signaling bits at RSER to 1 |
| RLB | CCR1.4 | **Remote Loopback.**<br>0 = loopback disabled<br>1 = loopback enabled |
| SCLKM | CCR1.3 | **SYSCLK Mode Select.**<br>0 = if SYSCLK is 1.544MHz<br>1 = if SYSCLK is 2.048MHz |
| RESE | CCR1.2 | **Receive Elastic Store Enable.**<br>0 = elastic store is bypassed<br>1 = elastic store is enabled |
| PLB | CCR1.1 | **Payload Loopback.**<br>0 = loopback disabled<br>1 = loopback enabled |
| FLB | CCR1.0 | **Framer Loopback.**<br>0 = loopback disabled<br>1 = loopback enabled |

## 4.1 Local Loopback

When CCR1.6 is set to a 1, the DS2151Q will be forced into Local Loopback (LLB). In this loopback, data will continue to be transmitted as normal through the transmit side of the SCT. Data being received at RTIP and RRING will be replaced with the data being transmitted. Data in this loopback will pass through the jitter attenuator and the jitter attenuator should be programmed to be in the transmit path. LLB is primarily used in debug and test applications. See Figure 1-1 for more details.

## 4.2 Remote Loopback

When CCR1.4 is set to a 1, the DS2151Q will be forced into Remote Loopback (RLB). In this loopback, data recovered off the T1 line from the RTIP and RRING pins will be transmitted back onto the T1 line (with any BPVs that might have occurred intact) via the TTIP and TRING pins. Data will continue to pass through the receive side of the DS2151Q as it would normally and the data at the TSER input will be ignored. Data in this loopback will pass through the jitter attenuator. RLB is used to place the DS2151Q into "line" loopback, which is a requirement of both ANSI T1.403 and AT&T TR62411. See Figure 1-1 for more details.

## 4.3 Payload Loopback

When CCR1.1 is set to a 1, the DS2151Q will be forced into Payload Loopback (PLB). Normally, this loopback is only enabled when ESF framing is being performed. In a PLB situation, the DS2151Q will loop the 192 bits of payload data (with BPVs corrected) from the receive section back to the transmit section. The FPS framing pattern, CRC6 calculation, and the FDL bits are not looped back, they are reinserted by the DS2151Q. When PLB is enabled, the following will occur:

1) Data will be transmitted from the TTIP and TRING pins synchronous with RCLK instead of TCLK.
2) All the receive side signals will continue to operate normally.
3) The TCHCLK and TCHBLK signals are forced low.
4) Data at the TSER pin is ignored.
5) The TLCLK signal will become synchronous with RCLK instead of TCLK.

## 4.4 Framer Loopback

When CCR1.0 is set to a 1, the DS2151Q will enter a Framer Loopback (FLB) mode. This loopback is useful in testing and debugging applications. In FLB, the DS2151Q will loop data from the transmit side back to the receive side. When FLB is enabled, the following will occur:

1) Unless the RLB is active, an unframed all 1s code will be transmitted at TTIP and TRING.
2) Data off the T1 line at RTIP and RRING will be ignored.
3) The RCLK output will be replaced with the TCLK input.

## CCR2: COMMON CONTROL REGISTER 2 (Address = 38 Hex)

| (MSB) | | | | | | | (LSB) |
|---|---|---|---|---|---|---|---|
| TFM | TB8ZS | TSLC96 | TFDL | RFM | RB8ZS | RSLC96 | RFDL |

| SYMBOL | POSITION | NAME AND DESCRIPTION |
|---|---|---|
| TFM | CCR2.7 | **Transmit Frame Mode Select.**<br>0 = D4 framing mode<br>1 = ESF framing mode |
| TB8ZS | CCR2.6 | **Transmit B8ZS Enable.**<br>0 = B8ZS disabled<br>1 = B8ZS enabled |
| TSLC96 | CCR2.5 | **Transmit SLC-96/Fs Bit Loading Enable.**<br>0 = SLC-96/Fs bit Loading disabled<br>1 = SLC-96/Fs bit Loading enabled |
| TFDL | CCR2.4 | **Transmit FDL 0 Stuffer Enable.**<br>0 = 0 stuffer disabled<br>1 = 0 stuffer enabled |
| RFM | CCR2.3 | **Receive Frame Mode Select.**<br>0 = D4 framing mode<br>1 = ESF framing mode |
| RB8ZS | CCR2.2 | **Receive B8ZS Enable.**<br>0 = B8ZS disabled<br>1 = B8ZS enabled |
| RSLC96 | CCR2.1 | **Receive SLC-96 Enable.**<br>0 = SLC-96 disabled<br>1 = SLC-96 enabled |
| RFDL | CCR2.0 | **Receive FDL 0 Destuffer Enable.**<br>0 = 0 destuffer disabled<br>1 = 0 destuffer enabled |

## CCR3: COMMON CONTROL REGISTER 3 (Address = 30 Hex)

| (MSB) | | | | | | | (LSB) |
|---|---|---|---|---|---|---|---|
| ESMDM | ESR | P16F | RSMS | PDE | TLD | TLU | LIRST |

| SYMBOL | POSITION | NAME AND DESCRIPTION |
|---|---|---|
| ESMDM | CCR3.7 | **Elastic Store Minimum Delay Mode.** See Section 11 for details.<br>0=elastic stores operate at full two-frame depth<br>1=elastic stores operate at 32-bit depth |
| ESR | CCR3.6 | **Elastic Store Reset.** Setting this bit from a 0 to a 1 will force the elastic stores to a known depth. Should be toggled after SYSCLK has been applied and is stable. Must be cleared and set again for a subsequent reset. |
| P16F | CCR3.5 | **Function of Pin 16.**<br>0 = Receive Loss of Sync (RLOS).<br>1 = Loss of Transmit Clock (LOTC). |
| RSMS | CCR3.4 | **RSYNC Multiframe Skip Control.** Useful in framing format conversions from D4 to ESF.<br>0 = RSYNC will output a pulse at every multiframe<br>1 = RSYNC will output a pulse at every other multiframe note: for this bit to have any affect, the RSYNC must be set to output multiframe pulses (RCR2.4 = 1 and RCR2.3 = 0) and the receive elastic store must be bypassed. (CCR1.2 = 0). |
| PDE | CCR3.3 | **Pulse Density Enforcer Enable.**<br>0 = disable transmit pulse density enforcer<br>1 = enable transmit pulse density enforcer |
| TLD | CCR3.2 | **Transmit Loop Down Code (001).**<br>0 = transmit data normally<br>1 = replace normal transmitted data with Loop Down code |
| TLU | CCR3.1 | **Transmit Loop Up Code (00001).**<br>0 = transmit data normally<br>1 = replace normal transmitted data with Loop Up code |
| LIRST | CCR3.0 | **Line Interface Reset.** Setting this bit from a 0 to a one will initiate an internal reset that affects the slicer, AGC, clock recovery state machine and jitter attenuator. Normally this bit is only toggled on power-up. Must be cleared and set again for a subsequent reset. |

## 4.5 Loop Code Generation

When either the CCR3.1 or CCR3.2 bits are set to 1, the DS2151Q will replace the normal transmitted payload with either the Loop Up or Loop Down code, respectively. The DS2151Q will overwrite the repeating loop code pattern with the framing bits. The SCT will continue to transmit the loop codes as long as either bit is set. It is an illegal state to have both CCR3.1 and CCR3.2 set to 1 at the same time.

## 4.6 Pulse Density Enforcer

The SCT always examines both the transmit and receive data streams for violations of the following rules which are required by ANSI T1.403-199X:

- no more than 15 consecutive 0s
- at least N 1s in each and every time window of 8 x (N +1) bits where N = 1 through 23

Violations for the transmit and receive data streams are reported in the RIR2.0 and RIR2.1 bits respectively.

When the CCR3.3 is set to 1, the DS2151Q will force the transmitted stream to meet this requirement no matter the content of the transmitted stream. When running B8ZS, the CCR3.3 bit should be set to 0, since B8ZS encoded data streams cannot violate the pulse density requirements.

## 4.7 Power-Up Sequence

On power-up, after the supplies are stable, the DS2151Q should be configured for operation by writing to all of the internal registers (this includes setting the Test Register to 00Hex) since the contents of the internal registers cannot be predicted on power-up. Next, the LIRST bit should be toggled from 0 to 1 to reset the line interface (it will take the DS2151Q about 40ms to recover from the LIRST being toggled). Finally, after the SYSCLK input is stable, the ESR bit should be toggled from a 0 to a 1 (this step can be skipped if the elastic stores are disabled).

# 5 STATUS AND INFORMATION REGISTERS

There is a set of four registers that contain information on the current real time status of the DS2151Q: Status Register 1 (SR1), Status Register 2 (SR2), Receive Information Register 1 (RIR1), and Receive Information Register 2 (RIR2). When a particular event has occurred (or is occurring), the appropriate bit in one of these four registers will be set to a 1. All of the bits in these registers operate in a latched fashion. This means that if an event occurs and a bit is set to a 1 in any of the registers, it will remain set until the user reads that bit. The bit will be cleared when it is read and it will not be set again until the event has occurred again or if the alarm(s) is still present.

The user will always precede a read of these registers with a write. The byte written to the register will inform the DS2151Q which bits the user wishes to read and have cleared. The user will write a byte to one of these four registers, with a 1 in the bit positions he or she wishes to read and a 0 in the bit positions he or she does not wish to obtain the latest information on. When a 1 is written to a bit location, the read register will be updated with current value and the previous value will be cleared. When a 0 is written to a bit position, the read register will not be updated and the previous value will be held. A write to the status and information registers will be immediately followed by a read of the same register. The read result should be logically ANDed with the mask byte that was just written and this value should be written back into the same register to ensure that the bit does indeed clear. This second write is necessary because the alarms and events in the status registers occur asynchronously in respect to their access via the parallel port. The write-read-write scheme is unique to the four status registers and it allows an external microcontroller or microprocessor to individually poll certain bits without disturbing the other bits in the register. This operation is key in controlling the DS2151Q with higher-order software languages.

The SR1 and SR2 registers have the unique ability to initiate a hardware interrupt via the $\overline{\text{INT1}}$ and $\overline{\text{INT2}}$ pins, respectively. Each of the alarms and events in the SR1 and SR2 can be either masked or unmasked from the interrupt pins via the Interrupt Mask Register 1 (IMR1) and Interrupt Mask Register 2 (IMR2) respectively.

## RIR1: RECEIVE INFORMATION REGISTER 1 (Address = 22 Hex)

| (MSB) | | | | | | | (LSB) |
|---|---|---|---|---|---|---|---|
| COFA | 8ZD | 16ZD | RESF | RESE | SEFE | B8ZS | FBE |

| SYMBOL | POSITION | NAME AND DESCRIPTION |
|---|---|---|
| COFA | RIR1.7 | **Change of Frame Alignment.** Set when the last resync resulted in a change of frame or multiframe alignment. |
| 8ZD | RIR1.6 | **Eight 0 Detect.** Set when a string of eight consecutive 0s have been received at RPOS and RNEG. |
| 16ZD | RIR1.5 | **Sixteen 0 Detect.** Set when a string of 16 consecutive 0s have been received at RPOS and RNEG. |
| RESF | RIR1.4 | **Receive Elastic Store Full.** Set when the receive elastic store buffer fills and a frame is deleted. |
| RESE | RIR1.3 | **Receive Elastic Store Empty.** Set when the receive elastic store buffer empties and a frame is repeated. |
| SEFE | RIR1.2 | **Severely Errored Framing Event.** Set when 2 out of 6 framing bits (Ft or FPS) are received in error. |
| B8ZS | RIR1.1 | **B8ZS Codeword Detect.** Set when a B8ZS codeword is detected at RPOS and RNEG independent of whether the B8ZS mode is selected or not via CCR2.6. |
| FBE | RIR1.0 | **Frame Bit Error.** Set when a Ft (D4) or FPS (ESF) framing bit is received in error. |

## RIR2: RECEIVE INFORMATION REGISTER 2 (Address = 31 Hex)

| (MSB) | | | | | | | (LSB) |
|---|---|---|---|---|---|---|---|
| RL1 | RL0 | TESF | TESE | TSLIP | JALT | RPDV | TPDV |

| SYMBOL | POSITION | NAME AND DESCRIPTION |
|---|---|---|
| RL1 | RIR2.7 | **Receive Level Bit 1.** See Table 5-1. |
| RL0 | RIR2.6 | **Receive Level Bit 0.** See Table 5-1. |
| TESF | RIR2.5 | **Transmit Elastic Store Full.** Set when the transmit elastic store buffer fills and a frame is deleted. |
| TESE | RIR2.4 | **Transmit Elastic Store Empty.** Set when the transmit elastic store buffer empties and a frame is repeated. |
| TSLIP | RIR2.3 | **Transmit Elastic Store Slip Occurrence.** Set when the transmit elastic store has either repeated or deleted a frame. |
| JALT | RIR2.2 | **Jitter Attenuator Limit Trip.** Set when the jitter attenuator FIFO reaches to within 4 bits of its limit; useful for debugging jitter attenuation operation. |
| RPDV | RIR2.1 | **Receive Pulse Density Violation.** Set when the receive data stream does not meet the ANSI T1.403 requirements for pulse density. |
| TPDV | RIR2.0 | **Transmit Pulse Density Violation.** Set when the transmit data stream does not meet the ANSI T1.403 requirements for pulse density. |

### Table 5-1. Receive T1 Level Indication

| RL1 | RL0 | TYPICAL LEVEL RECEIVED (dB) |
|---|---|---|
| 0 | 0 | +2 to -7.5 |
| 0 | 1 | -7.5 to -15 |
| 1 | 0 | -15 to -22.5 |
| 1 | 1 | Less than -22.5 |

## SR1: STATUS REGISTER 1 (Address = 20 Hex)

| (MSB) | | | | | | | (LSB) |
|---|---|---|---|---|---|---|---|
| LUP | LDN | LOTC | RSLIP | RBL | RYEL | RCL | RLOS |

| SYMBOL | POSITION | NAME AND DESCRIPTION |
|---|---|---|
| LUP | SR1.7 | **Loop Up Code Detected**. Set when the repeating ...00001... loop up code is being received. |
| LDN | SR1.6 | **Loop Down Code Detected**. Set when the repeating ...001... loop down code is being received. |
| LOTC | SR1.5 | **Loss of Transmit Clock**. Set when the TCLK pin has not transitioned for one channel time (or 5.2µs). Will force pin 16 high if enabled via CCR1.6. Based on RCLK. |
| RSLIP | SR1.4 | **Receive Elastic Store Slip Occurrence**. Set when the receive elastic store has either repeated or deleted a frame. |
| RBL | SR1.3 | **Receive Blue Alarm**. Set when a blue alarm is received at RTIP and RRING. See note below. |
| RYEL | SR1.2 | **Receive Yellow Alarm**. Set when a yellow alarm is received at RTIP and RRING. |
| RCL | SR1.1 | **Receive Carrier Loss**. Set when 192 consecutive 0s have been detected at RTIP and RRING. |
| RLOS | SR1.0 | **Receive Loss of Sync**. Set when the device is not synchronized to the receive T1 stream. |

**Table 5-2. Alarm Set and Clear Criteria**

| ALARM | SET CRITERIA | CLEAR CRITERIA |
|---|---|---|
| **Blue Alarm** (AIS) (see note below) | When over a 3ms window, five or less 0s are received | When over a 3ms window, six or more 0s are received |
| **Yellow Alarm**<br>1. D4 bit 2 mode (RCR2.2=0)<br><br>2. D4 12th F-bit mode (RCR2.2=1; this mode is also referred to as the "Japanese Yellow Alarm")<br><br>3. ESF Mode | When bit 2 of 256 consecutive channels is set to 0 for at least 254 occurrences<br><br>When the 12th framing bit is set to 1 for two consecutive occurrences<br><br>When 16 consecutive patterns of 00FF hex appear in the FDL | When bit 2 of 256 consecutive channels is set to 0 for less than 254 occurrences<br><br>When the 12th framing bit is set to 0 for two consecutive occurrences<br><br>When 14 or less patterns of 00FF hex out of 16 possible appear in the FDL |
| **Red Alarm** (RCL) (this alarm is also referred to as Loss of Signal) | When 192 consecutive 0s are received | When 14 or more 1s out of 112 possible bit positions are received starting with the first 1 received |

***Note:*** *The definition of Blue Alarm (or Alarm Indication Signal) is an unframed all-ones signal. Blue alarm detectors should be able to operate properly in the presence of a 10-3 error rate and they should not falsely trigger on a framed all-ones signal. The blue alarm criteria in the DS2151Q has been set to achieve this performance. It is recommended that the RBL bit be qualified with the RLOS status bit in detecting a blue alarm.*

## 5.1 Loop Up/Down Code Detection

Bits SR1.7 and SR1.6 will indicate when either the standard Loop Up or Loop Down codes are being received by the DS2151Q. When a Loop Up code has been received for 5 seconds, the CPE is expected to loop the recovered data (without correcting BPVs) back to the source. The Loop Down code indicates that the loopback should be discontinued. See the AT&T publication TR 62411 for more details. The DS2151Q will detect the Loop Up/Down codes in both framed and unframed circumstances with bit error rates as high as 10**-2. The loop code detector has a nominal integration period of 48ms. Hence, after about 48ms of receiving either code, the proper status bit will be set to a 1. After this initial indication, it is recommended that the software poll the DS2151Q every 100ms to 500ms until 5 seconds have elapsed to insure that the code is continuously present. Once 5 seconds have passed, the DS2151Q should be taken into or out of loopback via the Remote Loopback (RLB) bit in CCR1.

## SR2: STATUS REGISTER 2 (Address = 21 Hex)

| (MSB) | | | | | | | (LSB) |
|---|---|---|---|---|---|---|---|
| RMF | TMF | SEC | RFDL | TFDL | RMTCH | RAF | - |

| SYMBOL | POSITION | NAME AND DESCRIPTION |
|---|---|---|
| RMF | SR2.7 | **Receive Multiframe**. Set on receive multiframe boundaries. |
| TMF | SR2.6 | **Transmit Multiframe**. Set on transmit multiframe boundaries. |
| SEC | SR2.5 | **One Second Timer**. Set on increments of 1 second based on RCLK; will be set in increments of 999ms, 999ms, and 1002ms every 3 seconds. |
| RFDL | SR2.4 | **Receive FDL Buffer Full**. Set when the receive FDL buffer (RFDL) fills to capacity (8 bits). |
| TFDL | SR2.3 | **Transmit FDL Buffer Empty**. Set when the transmit FDL buffer (TFDL) empties. |
| RMTCH | SR2.2 | **Receive FDL Match Occurrence**. Set when the RFDL matches either RFDLM1 or RFDLM2. |
| RAF | SR2.1 | **Receive FDL Abort**. Set when eight consecutive ones are received in the FDL. |
| — | SR2.0 | **Not Assigned**. Should be set to 0 when written. |

## IMR1: INTERRUPT MASK REGISTER 1 (Address = 7F Hex)

| (MSB) | | | | | | | (LSB) |
|---|---|---|---|---|---|---|---|
| LUP | LDN | LOTC | SLIP | RBL | RYEL | RCL | RLOS |

| SYMBOL | POSITION | NAME AND DESCRIPTION |
|---|---|---|
| LUP | IMR1.7 | **Loop Up Code Detected.**<br>0 = interrupt masked<br>1 = interrupt enabled |
| LDN | IMR1.6 | **Loop Down Code Detected.**<br>0 = interrupt masked<br>1 = interrupt enabled |
| LOTC | IMR1.5 | **Loss of Transmit Clock.**<br>0 = interrupt masked<br>1 = interrupt enabled |
| SLIP | IMR1.4 | **Elastic Store Slip Occurrence.**<br>0 = interrupt masked<br>1 = interrupt enabled |
| RBL | IMR1.3 | **Receive Blue Alarm.**<br>0 = interrupt masked<br>1 = interrupt enabled |
| RYEL | IMR1.2 | **Receive Yellow Alarm.**<br>0 = interrupt masked<br>1 = interrupt enabled |
| RCL | IMR1.1 | **Receive Carrier Loss.**<br>0 = interrupt masked<br>1 = interrupt enabled |
| RLOS | IMR1.0 | **Receive Loss of Sync.**<br>0 = interrupt masked<br>1 = interrupt enabled |