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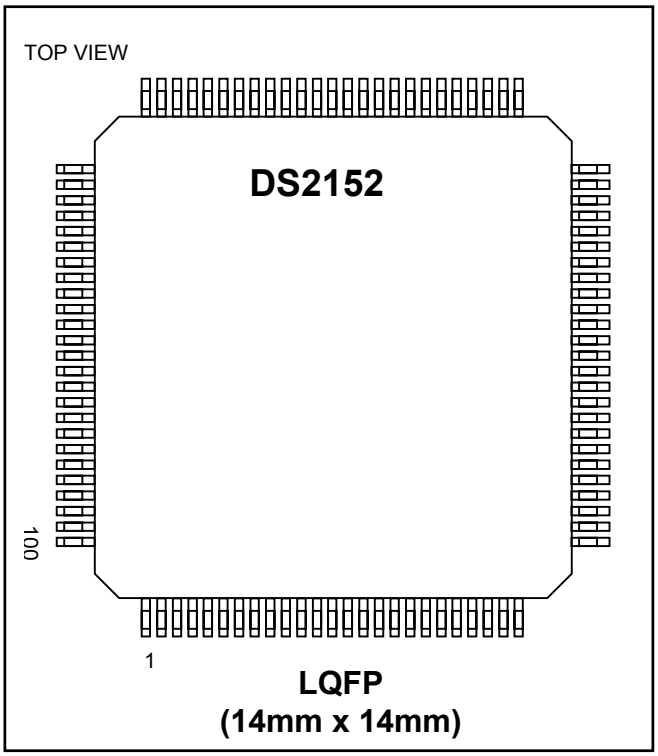
# DS2152
# Enhanced T1 Single-Chip Transceiver

www.maxim-ic.com

## FEATURES

- Complete DS1/ISDN-PRI Transceiver Functionality
- Line Interface can Handle Both Long- and Short-Haul Trunks
- 32-Bit or 128-Bit Crystal-Less Jitter Attenuator
- Generates DSX-1 and CSU Line Build-Outs
- Frames to D4, ESF, and SLC-96$^{R}$ Formats
- Dual On-Board Two-Frame Elastic Store Slip Buffers That can Connect to Asynchronous Backplanes Up to 8.192MHz
- 8-Bit Parallel Control Port That can be Used Directly on Either Multiplexed or Nonmultiplexed Buses (Intel or Motorola)
- Extracts and Inserts Robbed-Bit Signaling
- Detects and Generates Yellow (RAI) and Blue (AIS) Alarms
- Programmable Output Clocks for Fractional T1
- Fully Independent Transmit and Receive Functionality
- Integral HDLC Controller with 16-Byte Buffers for the FDL
- Generates and Detects In-Band Loop Codes from 1 to 8 bits in Length Including CSU Loop Codes
- Contains ANSI Ones Density Monitor and Enforcer
- Large Path and Line Error Counters Including BPV, CV, CRC6, and Framing Bit Errors
- Pin Compatible with DS2154 E1 Enhanced Single-Chip Transceiver
- 5V Supply; Low-Power CMOS
- 100-Pin, 14mm$^2$ LQFP Package

## PIN CONFIGURATION




## ORDERING INFORMATION

| PART | TEMP RANGE | PIN-PACKAGE |
|---|---|---|
| DS2152L | 0°C to +70°C | 100 LQFP |
| DS2152L+ | 0°C to +70°C | 100 LQFP |
| DS2152LN | -40°C to +85°C | 100 LQFP |
| DS2152LN+ | -40°C to +85°C | 100 LQFP |

+*Denotes lead-free/RoHS-compliant package.*

***Note:*** *Some revisions of this device may incorporate deviations from published specifications known as errata. Multiple revisions of any device may be simultaneously available through various sales channels. For information about device errata, click here: www.maxim-ic.com/errata.*

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# 1 DETAILED DESCRIPTION

The DS2152 T1 enhanced single-chip transceiver (SCT) contains all the necessary functions for connection to T1 lines, whether they be DS-1 long haul or DSX-1 short haul. The clock recovery circuitry automatically adjusts to T1 lines from 0 feet to over 6000 feet in length. The device can generate both DSX-1 line build-outs as well as CSU line build-outs of -7.5dB, -15dB, and -22.5dB. The on-board jitter attenuator (selectable to either 32 bits or 128 bits) can be placed in either the transmit or receive data paths. The framer locates the frame and multiframe boundaries and monitors the data stream for alarms. It is also used for extracting and inserting robbed-bit signaling data and FDL data. The device contains a set of internal registers that the user can access and control the operation of the unit. Quick access via the parallel control port allows a single controller to handle many T1 lines. The device fully meets all the latest T1 specifications including ANSI T1.403-1995, ANSI T1.231-1993, AT&T TR 62411 (12-90), AT&T TR54016, and ITU G.703, G.704, G.706, G.823, and I.431.

## 1.1 Introduction

The DS2152 is a superset version of the popular DS2151 T1 single-chip transceiver offering the new features listed below. All of the original features of the DS2151 have been retained and software created for the original devices is transferable into the DS2152.

### 1.1.1 New Features

- Option for non-multiplexed bus operation
- Crystal-less jitter attenuation
- Additional hardware signaling capability including:
  - Receive signaling reinsertion to a backplane multiframe sync
  - Availability of signaling in a separate PCM data stream
  - Signaling freezing
  - Interrupt generated on change of signaling data
- Per-channel code insertion in both transmit and receive paths
- Full HDLC controller for the FDL with 16-byte buffers in both transmit and receive paths
- RCL, RLOS, RRA, and RAIS alarms now interrupt on change of state
- 8.192MHz clock synthesizer
- Per-channel loopback
- Addition of hardware pins to indicate carrier loss and signaling freeze
- Line interface function can be completely decoupled from the framer/formatter to allow:
  - Interface to optical, HDSL, and other NRZ interfaces
  - Ability to “tap” the transmit and receive bipolar data streams for monitoring purposes
  - Ability to corrupt data and insert framing errors, CRC errors, etc.
- Transmit and receive elastic stores now have independent backplane clocks
- Ability to monitor one DS0 channel in both the transmit and receive paths
- Access to the data streams in between the framer/formatter and the elastic stores
- AIS generation in the line interface that is independent of loopbacks
- Ability to calculate and check CRC6 according to the Japanese standard
- Ability to pass the F-bit position through the elastic stores in the 2.048MHz backplane mode
- Programmable in-band loop code generator and detector

## 1.2 Functional Description

The analog AMI/B8ZS waveform off the T1 line is transformer-coupled into the RRING and RTIP pins of the DS2152. The device recovers clock and data from the analog signal and passes it through the jitter attenuation mux to the receive side framer where the digital serial stream is analyzed to locate the framing/multi-frame pattern. The DS2152 contains an active filter that reconstructs the analog received signal for the non-linear losses that occur in transmission. The device has a usable receive sensitivity of 0dB to -36dB, which allows the device to operate on cables up to 6000 feet in length. The receive side framer locates D4 (SLC-96) or ESF multiframe boundaries as well as detects incoming alarms, including carrier loss, loss of synchronization, blue (AIS) and yellow alarms. If needed, the receive side elastic store can be enabled in order to absorb the phase and frequency differences between the recovered T1 data stream and an asynchronous backplane clock which is provided at the RSYSCLK input. The clock applied at the RSYSCLK input can be either a 2.048MHz clock or a 1.544MHz clock. The RSYSCLK can be a bursty clock with speeds up to 8.192MHz.

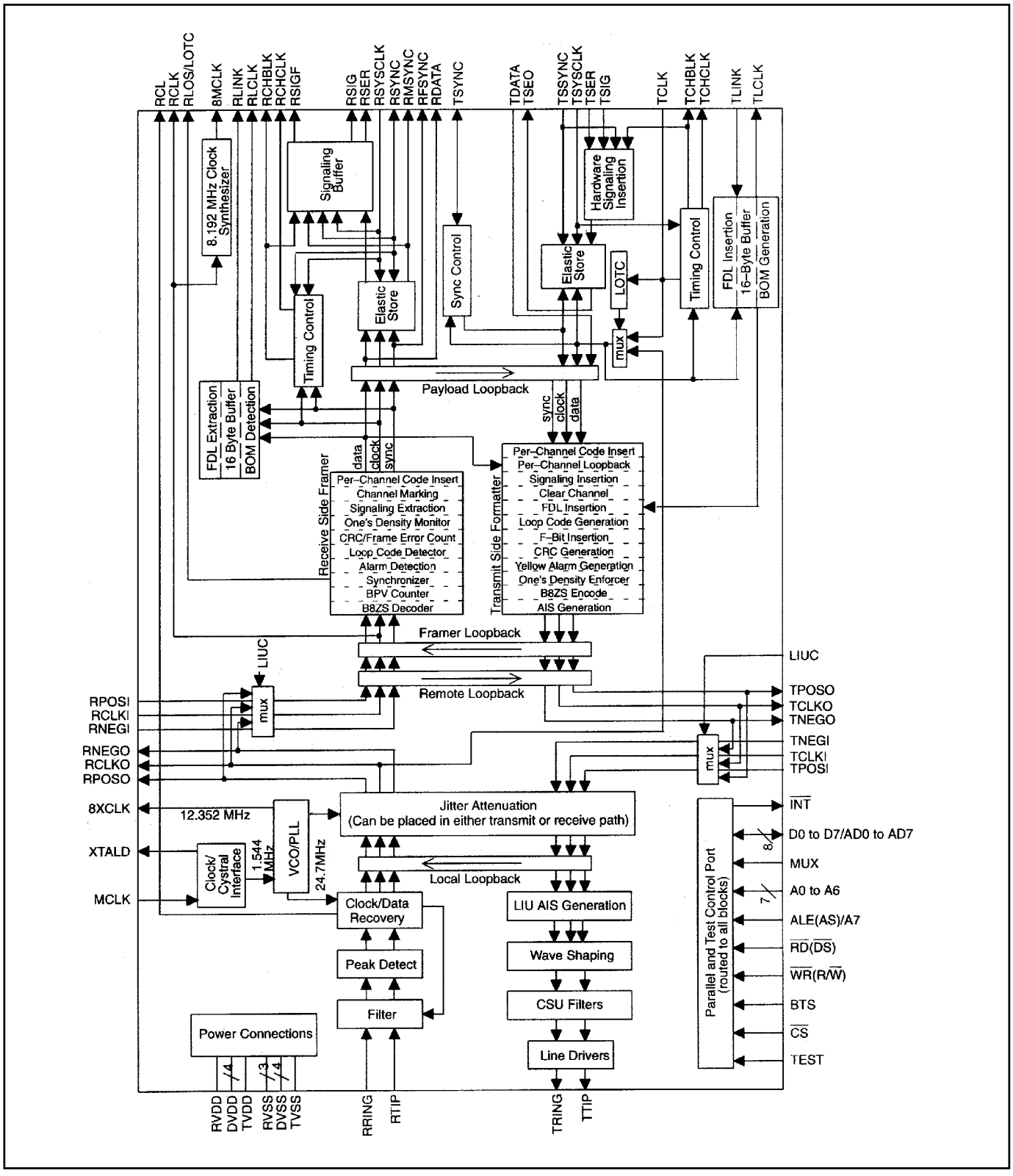
The transmit side of the DS2152 is totally independent from the receive side in both the clock requirements and characteristics. Data off of a backplane can be passed through a transmit side elastic store if necessary. The transmit formatter will provide the necessary frame/multiframe data overhead for T1 transmission. Once the data stream has been prepared for transmission, it is sent via the jitter attenuation mux to the waveshaping and line driver functions. The DS2152 will drive the T1 line from the TTIP and TRING pins via a coupling transformer. The line driver can handle both long (CSU) and short haul (DSX-1) lines.

## 1.3 Reader's Note

This data sheet assumes a particular nomenclature of the T1 operating environment. In each 125µs frame, there are 24 8-bit channels plus a framing bit. It is assumed that the framing bit is sent first followed by channel 1. Each channel is made up of 8 bits that are numbered 1 to 8. Bit number 1 is the MSB and is transmitted first. Bit number 8 is the LSB and is transmitted last. Throughout this data sheet, the following abbreviations are used:

| | |
|---|---|
| D4 | Superframe (12 frames per multiframe) Multiframe Structure |
| SLC-96 | Subscriber Loop Carrier - 96 Channels (SLC-96 is an AT&T registered trademark) |
| ESF | Extended Superframe (24 frames per multiframe) Multiframe Structure |
| B8ZS | Bipolar with 8 0 Substitution |
| CRC | Cyclical Redundancy Check |
| Ft | Terminal Framing Pattern in D4 |
| Fs | Signaling Framing Pattern in D4 |
| FPS | Framing Pattern in ESF |
| MF | Multiframe |
| BOC | Bit Oriented Code |
| HDLC | High Level Data Link Control |
| FDL | Facility Data Link |

## Figure 1-1. DS2152 Enhanced T1 Single-Chip Transceiver



# 2 PIN DESCRIPTION

| PIN | NAME | TYPE | FUNCTION |
|---|---|---|---|
| 1 | RCHBLK | O | Receive Channel Block |
| 2, 4, 5, 7–10, 15, 23, 26, 27, 28, 36, 54, 76 | N.C. | — | No Connection. These pins should be left open circuited. |
| 3 | 8MCLK | O | 8.192MHz Clock |
| 6 | RCL | O | Receive Carrier Loss |
| 11 | BTS | I | Bus Type Select |
| 12 | LIUC | I | Line Interface Connect |
| 13 | 8XCLK | O | Eight Times Clock |
| 14 | TEST | I | Test |
| 16 | RTIP | I | Receive Analog Tip Input |
| 17 | RRING | I | Receive Analog Ring Input |
| 18 | RVDD | — | Receive Analog Positive Supply |
| 19, 20, 24 | RVSS | — | Receive Analog Signal Ground |
| 21 | MCLK | I | Master Clock Input |
| 22 | XTALD | O | Quartz Crystal Driver |
| 25 | $\overline{\text{INT}}$ | O | Active-Low Interrupt |
| 29 | TTIP | O | Transmit Analog Tip Output |
| 30 | TVSS | — | Transmit Analog Signal Ground |
| 31 | TVDD | — | Transmit Analog Positive Supply |
| 32 | TRING | O | Transmit Analog Ring Output |
| 33 | TCHBLK | O | Transmit Channel Block |
| 34 | TLCLK | O | Transmit Link Clock |
| 35 | TLINK | I | Transmit Link Data |
| 37 | TSYNC | I/O | Transmit Sync |
| 38 | TPOSI | I | Transmit Positive Data Input |
| 39 | TNEGI | I | Transmit Negative Data Input |
| 40 | TCLKI | I | Transmit Clock Input |
| 41 | TCLKO | O | Transmit Clock Output |
| 42 | TNEGO | O | Transmit Negative Data Output |
| 43 | TPOSO | O | Transmit Positive Data Output |
| 44, 61, 81, 83 | DVDD | — | Digital Positive Supply |
| 45, 60, 80, 84 | DVSS | — | Digital Signal Ground |
| 46 | TCLK | I | Transmit Clock |
| 47 | TSER | I | Transmit Serial Data |
| 48 | TSIG | I | Transmit Signaling Input |
| 49 | TESO | O | Transmit Elastic Store Output |
| 50 | TDATA | I | Transmit Data |
| 51 | TSYSCLK | I | Transmit System Clock |
| 52 | TSSYNC | I | Transmit System Sync |
| 53 | TCHCLK | O | Transmit Channel Clock |
| 55 | MUX | I | Bus Operation |
| 56 | D0/AD0 | I/O | Data Bus Bit 0/Address/Data Bus Bit 0 |

| PIN | NAME | TYPE | FUNCTION |
|---|---|---|---|
| 57 | D1/AD1 | I/O | Data Bus Bit 1/Address/Data Bus Bit 1 |
| 58 | D2/AD2 | I/O | Data Bus Bit 2/Address/Data Bus Bit 2 |
| 59 | D3/AD3 | I/O | Data Bus Bit 3/Address/Data Bus Bit 3 |
| 62 | D4/AD4 | I/O | Data Bus Bit 4/Address/Data Bus Bit 4 |
| 63 | D5/AD5 | I/O | Data Bus Bit 5/Address/Data Bus Bit 5 |
| 64 | D6/AD6 | I/O | Data Bus Bit 6/Address/Data Bus Bit 6 |
| 65 | D7/AD7 | I/O | Data Bus Bit 7/Address/Data Bus Bit 7 |
| 66–72 | A0–A6 | I | Address Bus Bit 0 |
| 73 | A7/ALE | I | Address Bus Bit 7/Address Latch Enable |
| 74 | $\overline{RD}(\overline{DS})$ | I | Active-Low Read Input (Data Strobe) |
| 75 | $\overline{CS}$ | I | Active-Low Chip Select |
| 77 | $\overline{WR}(R/\overline{W})$ | I | Active-Low Write Input (Read/Write) |
| 78 | RLINK | O | Receive Link Data |
| 79 | RLKCLK | O | Receive Link Clock |
| 82 | RCLK | O | Receive Clock |
| 85 | RDATA | O | Receive Data |
| 86 | RPOSI | I | Receive Positive Data Input |
| 87 | RNEGI | I | Receive Negative Data Input |
| 88 | RCLKI | I | Receive Clock Input |
| 89 | RCLKO | O | Receive Clock Output |
| 90 | RNEGO | O | Receive Negative Data Output |
| 91 | RPOSO | O | Receive Positive Data Output |
| 92 | RCHCLK | O | Receive Channel Clock |
| 93 | RSIGF | O | Receive Signaling Freeze Output |
| 94 | RSIG | O | Receive Signaling Output |
| 95 | RSER | O | Receive Serial Data |
| 96 | RMSYNC | O | Receive Multiframe Sync |
| 97 | RFSYNC | O | Receive Frame Sync |
| 98 | RSYNC | I/O | Receive Sync |
| 99 | RLOS/LOTC | O | Receive Loss of Sync/Loss of Transmit Clock |
| 100 | RSYSCLK | I | Receive System Clock |

## 2.1 Transmit Side Digital Pins

| PIN | NAME | FUNCTION |
|---|---|---|
| 46 | TCLK | **Transmit Clock.** A 1.544MHz primary clock. Used to clock data through the transmit side formatter. |
| 47 | TSER | **Transmit Serial Data.** Transmit NRZ serial data. Sampled on the falling edge of TCLK when the transmit side elastic store is disabled. Sampled on the falling edge of TSYSCLK when the transmit side elastic store is enabled. |
| 53 | TCHCLK | **Transmit Channel Clock.** A 192kHz clock that pulses high during the LSB of each channel. Synchronous with TCLK when the transmit side elastic store is disabled. Synchronous with TSYSCLK when the transmit side elastic store is enabled. Useful for parallel to serial conversion of channel data. |
| 33 | TCHBLK | **Transmit Channel Block.** A user-programmable output that can be forced high or low during any of the 24 T1 channels. Synchronous with TCLK when the transmit side elastic store is disabled. Synchronous with TSYSCLK when the transmit side elastic store is enabled. Useful for blocking clocks to a serial UART or LAPD controller in applications where not all T1 channels are used such as Fractional T1, 384kbps (H0), 768kbps, or ISDN-PRI. Also useful for locating individual channels in drop-and-insert applications, for external per-channel loopback, and for per-channel conditioning. See Section 10 for details. |
| 51 | TSYSCLK | **Transmit System Clock.** 1.544MHz or 2.048MHz clock. Only used when the transmit side elastic store function is enabled. Should be tied low in applications that do not use the transmit side elastic store. Can be burst at rates up to 8.192MHz. |
| 34 | TLCLK | **Transmit Link Clock.** 4 kHz or 2kHz (ZBTSI) demand clock for the TLINK input. See Section 12 for details. Transmit Link Data [TLINK]. |
| 35 | TLINK | **Transmit Link Data.** If enabled via TCR1.2, this pin will be sampled on the falling edge of TCLK for data insertion into either the FDL stream (ESF) or the Fs-bit position (D4) or the Z-bit position (ZBTSI). See Section 12 for details. |
| 37 | TSYNC | **Transmit Sync.** A pulse at this pin will establish either frame or multiframe boundaries for the transmit side. Via TCR2.2, the DS2152 can be programmed to output either a frame or multiframe pulse at this pin. If this pin is set to output pulses at frame boundaries, it can also be set via TCR2.4 to output double-wide pulses at signaling frames. See Section 16 for details. |
| 52 | TSSYNC | **Transmit System Sync.** Only used when the transmit side elastic store is enabled. A pulse at this pin will establish either frame or multiframe boundaries for the transmit side. Should be tied low in applications that do not use the transmit side elastic store. |
| 48 | TSIG | **Transmit Signaling Input.** When enabled, this input will sample signaling bits for insertion into outgoing PCM T1 data stream. Sampled on the falling edge of TCLK when the transmit side elastic store is disabled. Sampled on the falling edge of TSYSCLK when the transmit side elastic store is enabled. |
| 49 | TESO | **Transmit Elastic Store Data Output.** Updated on the rising edge of TCLK with data out of the transmit side elastic store whether the elastic store is enabled or not. This pin is normally tied to TDATA. |
| 50 | TDATA | **Transmit Data.** Sampled on the falling edge of TCLK with data to be clocked through the transmit side formatter. This pin is normally tied to TESO. |
| 43 | TPOSO | **Transmit Positive Data Output.** Updated on the rising edge of TCLKO with the bipolar data out of the transmit side formatter. Can be programmed to source NRZ data via the Output Data Format (CCR1.6) control bit. This pin is normally tied to TPOSI. |
| 42 | TNEGO | **Transmit Negative Data Output.** Updated on the rising edge of TCLKO with the bipolar data out of the transmit side formatter. This pin is normally tied to TNEGI. |
| 41 | TCLKO | **Transmit Clock Output.** Buffered clock that is used to clock data through the transmit side formatter (i.e., either TCLK or RCLKI). This pin is normally tied to TCLKI. |
| 38 | TPOSI | **Transmit Positive Data Input.** Sampled on the falling edge of TCLKI for data to be |

| PIN | NAME | FUNCTION |
|---|---|---|
| | | transmitted out onto the T1 line. Can be internally connected to TPOSO by tying the LIUC pin high. TPOSI and TNEGI can be tied together in NRZ applications. |
| 39 | TNEGI | **Transmit Negative Data Input.** Sampled on the falling edge of TCLKI for data to be transmitted out onto the T1 line. Can be internally connected to TNEGO by tying the LIUC pin high. TPOSI and TNEGI can be tied together in NRZ applications. |
| 40 | TCLKI | **Transmit Clock Input.** Line interface transmit clock. Can be internally connected to TCLKO by tying the LIUC pin high. |

## 2.2 Receive Side Digital Pins

| PIN | NAME | FUNCTION |
|---|---|---|
| 78 | RLINK | **Receive Link Data.** Updated with either FDL data (ESF) or Fs bits (D4) or Z bits (ZBTSI) one RCLK before the start of a frame. See Section 16 for details. |
| 79 | RLCLK | **Receive Link Clock.** A 4kHz or 2 kHz (ZBTSI) clock for the RLINK output. |
| 82 | RCLK | **Receive Clock.** 1.544MHz clock that is used to clock data through the receive side framer. |
| 92 | RCHCLK | **Receive Channel Clock.** A 192kHz clock that pulses high during the LSB of each channel. Synchronous with RCLK when the receive side elastic store is disabled. Synchronous with RSYSCLK when the receive side elastic store is enabled. Useful for parallel to serial conversion of channel data. |
| 1 | RCHBLK | **Receive Channel Block.** A user-programmable output that can be forced high or low during any of the 24 T1 channels. Synchronous with RCLK when the receive side elastic store is disabled. Synchronous with RSYSCLK when the receive side elastic store is enabled. Useful for blocking clocks to a serial UART or LAPD controller in applications where not all T1 channels are used, such as Fractional T1, 384kbps service, 768kbps, or ISDN-PRI. Also useful for locating individual channels in drop-and-insert applications, for external per-channel loopback, and for per-channel conditioning. See Section 10 for details. |
| 95 | RSER | **Receive Serial Data.** Received NRZ serial data. Updated on rising edges of RCLK when the receive side elastic store is disabled. Updated on the rising edges of RSYSCLK when the receive side elastic store is enabled. |
| 98 | RSYNC | **Receive Sync.** An extracted pulse, one RCLK wide, is output at this pin, which identifies either frame (RCR2.4 = 0) or multiframe (RCR2.4 = 1) boundaries. If set to output frame boundaries then via RCR2.5, RSYNC can also be set to output double-wide pulses on signaling frames. If the receive side elastic store is enabled via CCR1.2, then this pin can be enabled to be an input via RCR2.3 at which a frame or multiframe boundary pulse is applied. See Section 16 for details. |
| 97 | RFSYNC | **Receive Frame Sync.** An extracted 8kHz pulse 1 RCLK wide is output at this pin that identifies frame boundaries. |
| 96 | RMSYNC | **Receive Multiframe Sync.** Only used when the receive side elastic store is enabled. An extracted pulse, 1 RSYSCLK wide, is output at this pin, which identifies multiframe boundaries. If the receive side elastic store is disabled, then this output will output multiframe boundaries associated with RCLK. |
| 85 | RDATA | **Receive Data.** Updated on the rising edge of RCLK with the data out of the receive side framer. |
| 100 | RSYSCLK | **Receive System Clock.** 1.544MHz or 2.048MHz clock. Only used when the elastic store function is enabled. Should be tied low in applications that do not use the elastic store. Can be burst at rates up to 8.192MHz. |
| 94 | RSIG | **Receive Signaling Output.** Outputs signaling bits in a PCM format. Updated on rising edges of RCLK when the receive side elastic store is disabled. Updated on the rising edges of RSYSCLK when the receive side elastic store is enabled. |

| PIN | NAME | FUNCTION |
|---|---|---|
| 99 | RLOS/LOTC | **Receive Loss of Sync/Loss of Transmit Clock.** A dual function output that is controlled by the CCR3.5 control bit. This pin can be programmed to either toggle high when the synchronizer is searching for the frame and multiframe or to toggle high if the TCLK pin has not been toggled for 5µs. |
| 6 | RCL | **Receive Carrier Loss.** Set high when the line interface detects a loss of carrier. |
| 93 | RSIGF | **Receive Signaling Freeze.** Set high when the signaling data is frozen via either automatic or manual intervention. Used to alert downstream equipment of the condition. |
| 3 | 8MCLK | **8MHz Clock.** A 8.192MHz output clock that is referenced to the clock that is output at the RCLK pin and is used to clock data through the receive side framer. |
| 91 | RPOSO | **Receive Positive Data Output.** Updated on the rising edge of RCLKO with the bipolar data out of the line interface. This pin is normally tied to RPOSI. |
| 90 | RNEGO | **Receive Negative Data Output.** Updated on the rising edge of RCLKO with the bipolar data out of the line interface. This pin is normally tied to RNEGI. |
| 89 | RCLKO | **Receive Clock Output.** Buffered recovered clock from the T1 line. This pin is normally tied to RCLKI. |
| 86 | RPOSI | **Receive Positive Data Input.** Sampled on the falling edge of RCLKI for data to be clocked through the receive side framer. RPOSI and RNEGI can be tied together for a NRZ interface. Can be internally connected to RPOSO by tying the LIUC pin high. |
| 87 | RNEGI | **Receive Negative Data Input.** Sampled on the falling edge of RCLKI for data to be clocked through the receive side framer. RPOSI and RNEGI can be tied together for a NRZ interface. Can be internally connected to RNEGO by tying the LIUC pin high. |
| 88 | RCLKI | **Receive Clock Input.** Clock used to clock data through the receive side framer. This pin is normally tied to RCLKO. Can be internally connected to RCLKO by tying the LIUC pin high. |

## 2.3 Parallel Control Port Pins

| PIN | NAME | FUNCTION |
|---|---|---|
| 25 | $\overline{\text{INT}}$ | **Interrupt.** Flags host controller during conditions and change of conditions defined in the Status Registers 1 and 2 and the FDL Status Register. Active-low, open-drain output. |
| 14 | TEST | **Tri-State Control.** Set high to tri-state all output and I/O pins (including the parallel control port). Set low for normal operation. Useful in board-level testing. |
| 55 | MUX | **Bus Operation.** Set low to select nonmultiplexed bus operation. Set high to select multiplexed bus operation. |
| 56–65 | D0–D7/ AD0–AD7 | **Data Bus or Address/Data Bus.** In nonmultiplexed bus operation (MUX = 0), serves as the data bus. In multiplexed bus operation (MUX = 1), serves as an 8-bit multiplexed address/data bus. |
| 66–72 | A0–A6 | **Address Bus.** In nonmultiplexed bus operation (MUX = 0), serves as the address bus. In multiplexed bus operation (MUX = 1), these pins are not used and should be tied low. |
| 11 | BTS | **Bus Type Select.** Strap high to select Motorola bus timing; strap low to select Intel bus timing. This pin controls the function of the $\overline{\text{RD}}$ ($\overline{\text{DS}}$), ALE(AS), and $\overline{\text{WR}}$ (R/$\overline{\text{W}}$) pins. If BTS = 1, then these pins assume the function listed in parentheses. |
| 74 | $\overline{\text{RD}}$($\overline{\text{DS}}$) | **Read Input (Data Strobe).** $\overline{\text{RD}}$ and $\overline{\text{DS}}$ are active-low signals when MUX = 1. DS is active high when MUX = 0. See bus timing diagrams. |
| 75 | $\overline{\text{CS}}$ | **Chip Select.** Must be low to read or write to the device. $\overline{\text{CS}}$ is an active-low signal. |
| 73 | ALE(AS) | **A7 or Address Latch Enable (Address Strobe).** In non-multiplexed bus operation (MUX = 0), serves as the upper address bit. In multiplexed bus operation (MUX = 1), serves to demultiplex the bus on a positive-going edge. |
| 77 | $\overline{\text{WR}}$(R/$\overline{\text{W}}$) | **Write Input (Read/Write).** $\overline{\text{WR}}$ is an active-low signal. |

## 2.4 Line Interface Pins

| PIN | NAME | FUNCTION |
|---|---|---|
| 21 | MCLK | **Master Clock Input.** A 1.544MHz (±50ppm) clock source with TTL levels is applied at this pin. This clock is used internally for both clock/data recovery and for jitter attenuation. A quartz crystal of 1.544MHz may be applied across MCLK and XTALD instead of the TTL level clock source. |
| 22 | XTALD | **Quartz Crystal Driver.** A quartz crystal of 1.544MHz may be applied across MCLK and XTALD instead of a TTL level clock source at MCLK. Leave open circuited if a TTL clock source is applied at MCLK. |
| 13 | 8XCLK | **Eight Times Clock**. A 12.352MHz clock that is frequency locked to the 1.544MHz clock provided from the clock/data recovery block (if the jitter attenuator is enabled on the receive side) or from the TCLKI pin (if the jitter attenuator is enabled on the transmit side). Can be internally disabled via the TEST2 register if not needed. |
| 12 | LIUC | **Line Interface Connect.** Tie low to separate the line interface circuitry from the framer/formatter circuitry and activate the TPOSI/TNEGI/TCLKI/RPOSI/RNEGI/ RCLKI pins. Tie high to connect the line interface circuitry to the framer/formatter circuitry and deactivate the TPOSI/TNEGI/TCLKI/RPOSI/RNEGI/RCLKI pins. When LIUC is tied high, the TPOSI/TNEGI/TCLKI/RPOSI/RNEGI/RCLKI pins should be tied low. |
| 16, 17 | RTIP, RRING | **Receive Tip and Ring.** Analog inputs for clock recovery circuitry. These pins connect via a 1:1 transformer to the T1 line. See Section 15 for details. |
| 29, 32 | TTIP, TRING | **Transmit Tip and Ring.** Analog line driver outputs. These pins connect via a 1:1.15 or 1:1.36 step-up transformer to the T1 line. See Section 15 for details. |

## 2.5 Supply Pins

| PIN | NAME | FUNCTION |
|---|---|---|
| 44, 61, 81, 83 | DVDD | **Digital Positive Supply.** 5.0V ±5%. Should be tied to the RVDD and TVDD pins. |
| 18 | RVDD | **Receive Analog Positive Supply.** 5.0V ±5%. Should be tied to the DVDD and TVDD pins. |
| 31 | TVDD | **Transmit Analog Positive Supply.** 5.0V ±5%. Should be tied to the RVDD and DVDD pins. |
| 45, 60, 80, 84 | DVSS | **Digital Signal Ground.** Should be tied to the RVSS and TVSS pins. |
| 19, 20, 24 | RVSS | **Receive Analog Signal Ground.** 0V. Should be tied to the DVSS and TVSS pins. |
| 30 | TVSS | **Transmit Analog Ground.** 0V. Should be tied to the RVSS and DVSS pins. |

## Table 2-1. Register Map

| ADDRESS | R/W | REGISTER | |
|---|---|---|---|
| | | DESCRIPTION | NAME |
| 00 | R/W | FDL Control | FDLC |
| 01 | R/W | FDL Status | FDLS |
| 02 | R/W | FDL Interrupt Mask | FIMR |
| 03 | R/W | Receive Performance Report Message | RPRM |
| 04 | R/W | Receive Bit Oriented Code | RBOC |
| 05 | R | Receive FDL FIFO | RFFR |
| 06 | R/W | Transmit Performance Report Message | TPRM |
| 07 | R/W | Transmit Bit Oriented Code | TBOC |
| 08 | W | Transmit FDL FIFO | TFFR |
| 09 | R/W | Test 2 | TEST2 (set to 00h) |
| 0A | R/W | Common Control 7 | CCR7 |
| 0B–0E | — | Not present | — |
| 0F | R | Deceive ID | IDR |
| 10 | R/W | Receive Information 3 | RIR3 |
| 11 | R/W | Common Control 4 | CCR4 |
| 12 | R/W | In-Band Code Control | IBCC |
| 13 | R/W | Transmit Code Definition | TCD |
| 14 | R/W | Receive Up Code Definition | RUPCD |
| 15 | R/W | Receive Down Code Definition | RDNCD |
| 16 | R/W | Transmit Channel Control 1 | TCC1 |
| 17 | R/W | Transmit Channel Control 2 | TCC2 |
| 18 | R/W | Transmit Channel Control 3 | TCC3 |
| 19 | R/W | Common Control 5 | CCR5 |
| 1A | R | Transmit DS0 Monitor | TDS0M |
| 1B | R/W | Receive Channel Control 1 | RCC1 |
| 1C | R/W | Receive Channel Control 2 | RCC2 |
| 1D | R/W | Receive Channel Control 3 | RCC3 |
| 1E | R/W | Common Control 6 | CCR6 |
| 1F | R | Receive DS0 Monitor | RDS0M |
| 20 | R/W | Status 1 | SR1 |
| 21 | R/W | Status 2 | SR2 |
| 22 | R/W | Receive Information 1 | RIR1 |
| 23 | R | Line Code Violation Count 1 | LCVCR1 |
| 24 | R | Line Code Violation Count 2 | LCVCR2 |
| 25 | R | Path Code Violation Count 1 | PCVCR1 |
| 26 | R | Path Code Violation Count 2 | PCVCR2 |
| 27 | R | Multiframe Out of Sync Count 2 | MOSCR2 |
| 28 | R | Receive FDL Register | RFDL |
| 29 | R/W | Receive FDL Match 1 | RMTCH1 |
| 2A | R/W | Receive FDL Match 2 | RMTCH2 |
| 2B | R/W | Receive Control 1 | RCR1 |
| 2C | R/W | Receive Control 2 | RCR2 |
| 2D | R/W | Receive Mark 1 | RMR1 |
| 2E | R/W | Receive Mark 2 | RMR2 |
| 2F | R/W | Receive Mark 3 | RMR3 |
| 30 | R/W | Common Control 3 | CCR3 |
| 31 | R/W | Receive Information 2 | RIR2 |
| 32 | R/W | Transmit Channel Blocking 1 | TCBR1 |

| ADDRESS | R/W | REGISTER | |
|---|---|---|---|
| | | DESCRIPTION | NAME |
| 33 | R/W | Transmit Channel Blocking 2 | TCBR2 |
| 34 | R/W | Transmit Channel Blocking 3 | TCBR3 |
| 35 | R/W | Transmit Control 1 | TCR1 |
| 36 | R/W | Transmit Control 2 | TCR2 |
| 37 | R/W | Common Control 1 | CCR1 |
| 38 | R/W | Common Control 2 | CCR2 |
| 39 | R/W | Transmit Transparency 1 | TTR1 |
| 3A | R/W | Transmit Transparency 2 | TTR2 |
| 3B | R/W | Transmit Transparency 3 | TTR3 |
| 3C | R/W | Transmit Idle 1 | TIR1 |
| 3D | R/W | Transmit Idle 2 | TIR2 |
| 3E | R/W | Transmit Idle 3 | TIR3 |
| 3F | R/W | Transmit Idle Definition | TIDR |
| 40 | R/W | Transmit Channel 9 | TC9 |
| 41 | R/W | Transmit Channel 10 | TC10 |
| 42 | R/W | Transmit Channel 11 | TC11 |
| 43 | R/W | Transmit Channel 12 | TC12 |
| 44 | R/W | Transmit Channel 13 | TC13 |
| 45 | R/W | Transmit Channel 14 | TC14 |
| 46 | R/W | Transmit Channel 15 | TC15 |
| 47 | R/W | Transmit Channel 16 | TC16 |
| 48 | R/W | Transmit Channel 17 | TC17 |
| 49 | R/W | Transmit Channel 18 | TC18 |
| 4A | R/W | Transmit Channel 19 | TC19 |
| 4B | R/W | Transmit Channel 20 | TC20 |
| 4C | R/W | Transmit Channel 21 | TC21 |
| 4D | R/W | Transmit Channel 22 | TC22 |
| 4E | R/W | Transmit Channel 23 | TC23 |
| 4F | R/W | Transmit Channel 24 | TC24 |
| 50 | R/W | Transmit Channel 1 | TC1 |
| 51 | R/W | Transmit Channel 2 | TC2 |
| 52 | R/W | Transmit Channel 3 | TC3 |
| 53 | R/W | Transmit Channel 4 | TC4 |
| 54 | R/W | Transmit Channel 5 | TC5 |
| 55 | R/W | Transmit Channel 6 | TC6 |
| 56 | R/W | Transmit Channel 7 | TC7 |
| 57 | R/W | Transmit Channel 8 | TC8 |
| 58 | R/W | Receive Channel 1 | RC17 |
| 59 | R/W | Receive Channel 18 | RC18 |
| 5A | R/W | Receive Channel 19 | RC19 |
| 5B | R/W | Receive Channel 20 | RC20 |
| 5C | R/W | Receive Channel 21 | RC21 |
| 5D | R/W | Receive Channel 22 | RC22 |
| 5E | R/W | Receive Channel 23 | RC23 |
| 5F | R/W | Receive Channel 24 | RC24 |
| 60 | R | Receive Signaling 1 | RS1 |
| 61 | R | Receive Signaling 2 | RS2 |
| 62 | R | Receive Signaling 3 | RS3 |
| 63 | R | Receive Signaling 4 | RS4 |
| 64 | R | Receive Signaling 5 | RS5 |
| 65 | R | Receive Signaling 6 | RS6 |

| ADDRESS | R/W | REGISTER | |
|---|---|---|---|
| | | DESCRIPTION | NAME |
| 66 | R | Receive Signaling 7 | RS7 |
| 67 | R | Receive Signaling 8 | RS8 |
| 68 | R | Receive Signaling 9 | RS9 |
| 69 | R | Receive Signaling 10 | RS10 |
| 6A | R | Receive Signaling 11 | RS11 |
| 6B | R | Receive Signaling 12 | RS12 |
| 6C | R/W | Receive Channel Blocking 1 | RCBR1 |
| 6D | R/W | Receive Channel Blocking 2 | RCBR2 |
| 6E | R/W | Receive Channel Blocking 3 | RCBR3 |
| 6F | R/W | Interrupt Mask 2 | IMR2 |
| 70 | R/W | Transmit Signaling 1 | TS1 |
| 71 | R/W | Transmit Signaling 2 | TS2 |
| 72 | R/W | Transmit Signaling 3 | TS3 |
| 73 | R/W | Transmit Signaling 4 | TS4 |
| 74 | R/W | Transmit Signaling 5 | TS5 |
| 75 | R/W | Transmit Signaling 6 | TS6 |
| 76 | R/W | Transmit Signaling 7 | TS7 |
| 77 | R/W | Transmit Signaling 8 | TS8 |
| 78 | R/W | Transmit Signaling 9 | TS9 |
| 79 | R/W | Transmit Signaling 10 | TS10 |
| 7A | R/W | Transmit Signaling 11 | TS11 |
| 7B | R/W | Transmit Signaling 12 | TS12 |
| 7C | R/W | Line Interface Control | LICR |
| 7D | R/W | Test 1 | TEST1 (set to 00h) |
| 7E | R/W | Transmit FDL Register | TFDL |
| 7F | R/W | Interrupt Mask Register 1 | IMR1 |
| 80 | R/W | Receive Channel 1 | RC1 |
| 81 | R/W | Receive Channel 2 | RC2 |
| 82 | R/W | Receive Channel 3 | RC3 |
| 83 | R/W | Receive Channel 4 | RC4 |
| 84 | R/W | Receive Channel 5 | RC5 |
| 85 | R/W | Receive Channel 6 | RC6 |
| 86 | R/W | Receive Channel 7 | RC7 |
| 87 | R/W | Receive Channel 8 | RC8 |
| 88 | R/W | Receive Channel 9 | RC9 |
| 89 | R/W | Receive Channel 10 | RC10 |
| 8A | R/W | Receive Channel 11 | RC11 |
| 8B | R/W | Receive Channel 12 | RC12 |
| 8C | R/W | Receive Channel 13 | RC13 |
| 8D | R/W | Receive Channel 14 | RC14 |
| 8E | R/W | Receive Channel 15 | RC15 |
| 8F | R/W | Receive Channel 16 | RC16 |

***Note 1:*** *Test Registers 1 and 2 are used only by the factory; these registers must be cleared (set to all 0s) on power-up initialization to ensure proper operation.*
***Note 2:*** *Register banks 9xh, Axh, Bxh, Cxh, Dxh, Exh, and Fxh are not accessible.*

# 3 PARALLEL PORT

The DS2152 is controlled via either a nonmultiplexed (MUX = 0) or a multiplexed (MUX = 1) bus by an external microcontroller or microprocessor. The DS2152 can operate with either Intel or Motorola bus timing configurations. If the BTS pin is tied low, Intel timing will be selected; if tied high, Motorola timing will be selected. All Motorola bus signals are listed in parentheses. See the timing diagrams in the AC Electrical Characteristics in Section 18 for more details.

# 4 CONTROL, ID, AND TEST REGISTERS

The operation of the DS2152 is configured via a set of 11 control registers. Typically, the control registers are only accessed when the system is first powered up. Once the DS2152 has been initialized, the control registers will only need to be accessed when there is a change in the system configuration. There are two Receive Control Register (RCR1 and RCR2), two Transmit Control Registers (TCR1 and TCR2), and seven Common Control Registers (CCR1 to CCR7). Each of the 11 registers is described in this section.

There is a device Identification Register (IDR) at address 0Fh. The MSB of this read-only register is fixed to a 0 indicating that the DS2152 is present. The E1 pin-for-pin compatible version of the DS2152 is the DS2154, which also has an ID register at address 0Fh. The user can read the MSB to determine which chip is present since in the DS2152 the MSB will be set to 0 and in the DS2154 it will be set to 1. The lower 4 bits of the IDR are used to display the die revision of the chip.

## IDR: DEVICE IDENTIFICATION REGISTER (Address = 0F Hex)

| (MSB) | | | | | | | (LSB) |
|---|---|---|---|---|---|---|---|
| T1E1 | 0 | 0 | 0 | ID3 | ID2 | ID1 | ID0 |

| SYMBOL | POSITION | NAME AND DESCRIPTION |
|---|---|---|
| T1E1 | IDR.7 | **T1 or E1 Chip Determination Bit.**<br>0 = T1 chip<br>1 = E1 chip |
| ID3 | IDR.3 | **Chip Revision Bit 3.** MSB of a decimal code that represents the chip revision. |
| ID2 | IDR.1 | **Chip Revision Bit 2.** |
| ID1 | IDR.2 | **Chip Revision Bit 1.** |
| ID0 | IDR.0 | **Chip Revision Bit 0.** LSB of a decimal code that represents the chip revision. |

The two Test Registers at addresses 09 and 7D hex are used by the factory in testing the DS2152. On power-up, the Test Registers should be set to 00 hex for the DS2152 to operate properly.

## RCR1: RECEIVE CONTROL REGISTER 1 (Address = 2B Hex)

| (MSB) | | | | | | | (LSB) |
|---|---|---|---|---|---|---|---|
| LCVCRF | ARC | OOF1 | OOF2 | SYNCC | SYNCT | SYNCE | RESYNC |

| SYMBOL | POSITION | NAME AND DESCRIPTION |
|---|---|---|
| LCVCRF | RCR1.7 | **Line Code Violation Count Register Function Select.**<br>0 = do not count excessive 0s<br>1 = count excessive 0s |
| ARC | RCR1.6 | **Auto Resync Criteria.**<br>0 = Resync on OOF or RCL event<br>1 = Resync on OOF only |
| OOF1 | RCR1.5 | **Out Of Frame Select 1.**<br>0 = 2/4 frame bits in error<br>1 = 2/5 frame bits in error |
| OOF2 | RCR1.4 | **Out Of Frame Select 2.**<br>0 = follow RCR1.5<br>1 = 2/6 frame bits in error |
| SYNCC | RCR1.3 | **Sync Criteria.**<br>**In D4 Framing Mode**<br>0 = search for Ft pattern, then search for Fs pattern<br>1 = cross couple Ft and Fs pattern<br>**In ESF Framing Mode**<br>0 = search for FPS pattern only<br>1 = search for FPS and verify with CRC6 |
| SYNCT | RCR1.2 | **Sync Time.**<br>0 = qualify 10 bits<br>1 = qualify 24 bits |
| SYNCE | RCR1.1 | **Sync Enable.**<br>0 = auto resync enabled<br>1 = auto resync disabled |
| RESYNC | RCR1.0 | **Resync.** When toggled from low to high, a resynchronization of the receive side framer is initiated. Must be cleared and set again for a subsequent resync. |

## RCR2: RECEIVE CONTROL REGISTER 2 (Address = 2C Hex)

| (MSB) | | | | | | | (LSB) |
|---|---|---|---|---|---|---|---|
| RCS | RZBTSI | RSDW | RSM | RSIO | RD4YM | FSBE | MOSCRF |

| SYMBOL | POSITION | NAME AND DESCRIPTION |
|---|---|---|
| RCS | RCR2.7 | **Receive Code Select.** See Section 9 for more details.<br>0 = idle code (7F Hex)<br>1 = digital milliwatt code (1E/0B/0B/1E/9E/8B/8B/9E Hex) |
| RZBTSI | RCR2.6 | **Receive Side ZBTSI Enable.**<br>0 = ZBTSI disabled<br>1 = ZBTSI enabled |
| RSDW | RCR2.5 | **RSYNC Double-Wide.** (Note: This bit must be set to 0 when RCR2.4 = 1 or when RCR2.3 = 1.)<br>0 = do not pulse double-wide in signaling frames<br>1 = do pulse double-wide in signaling frames |
| RSM | RCR2.4 | **RSYNC Mode Select.** (A don't care if RSYNC is programmed as an input.)<br>0 = frame mode (see the timing diagrams in Section 16)<br>1 = multiframe mode (see the timing diagrams in Section 16) |
| RSIO | RCR2.3 | **RSYNC I/O Select.** (Note: This bit must be set to 0 when CCR1.2 = 0.)<br>0 = RSYNC is an output<br>1 = RSYNC is an input (only valid if elastic store enabled) |
| RD4YM | RCR2.2 | **Receive Side D4 Yellow Alarm Select.**<br>0 = 0s in bit 2 of all channels<br>1 = a 1 in the S-bit position of frame 12 |
| FSBE | RCR2.1 | **PCVCR Fs-Bit Error Report Enable.**<br>0 = do not report bit errors in Fs-bit position; only Ft bit position<br>1 = report bit errors in Fs-bit position as well as Ft bit position |
| MOSCRF | RCR2.0 | **Multiframe Out of Sync Count Register Function Select.**<br>0 = count errors in the framing bit position<br>1 = count the number of multiframes out of sync |

## TCR1: TRANSMIT CONTROL REGISTER 1 (Address = 35 Hex)

| (MSB) | | | | | | | (LSB) |
|---|---|---|---|---|---|---|---|
| LOTCMC | TFPT | TCPT | TSSE | GB7S | TFDLS | TBL | TYEL |

| SYMBOL | POSITION | NAME AND DESCRIPTION |
|---|---|---|
| LOTCMC | TCR1.7 | **Loss Of Transmit Clock Mux Control.** Determines whether the transmit side formatter should switch to the ever present RCLKO if the TCLK input should fail to transition (see Figure 1-1 for details).<br>0 = do not switch to RCLKO if TCLK stops<br>1 = switch to RCLKO if TCLK stops |
| TFPT | TCR1.6 | **Transmit F-Bit Pass Through.** (See note below.)<br>0 = F bits sourced internally<br>1 = F bits sampled at TSER |
| TCPT | TCR1.5 | **Transmit CRC Pass Through.** (See note below.)<br>0 = source CRC6 bits internally<br>1 = CRC6 bits sampled at TSER during F-bit time |
| TSSE | TCR1.4 | **Software Signaling Insertion Enable.** (See note below.)<br>0 = no signaling is inserted in any channel from the TS1–TS12 registers<br>1 = signaling is inserted in all channels from the TS1–TS12 registers (the TTR registers can be used to block insertion on a channel-by-channel basis) |
| GB7S | TCR1.3 | **Global Bit 7 Stuffing.** (See note below.)<br>0 = allow the TTR registers to determine which channels containing all 0s are to be Bit 7 stuffed<br>1 = force Bit 7 stuffing in all 0-byte channels regardless of how the TTR registers are programmed |
| TFDLS | TCR1.2 | **TFDL Register Select.** (See note below.)<br>0 = source FDL or Fs bits from the internal TFDL register (legacy FDL support mode)<br>1 = source FDL or Fs bits from the internal HDLC/BOC controller or the TLINK pin |
| TBL | TCR1.1 | **Transmit Blue Alarm.** (See note below.)<br>0 = transmit data normally<br>1 = transmit an unframed all 1s code at TPOSO and TNEGO |
| TYEL | TCR1.0 | **Transmit Yellow Alarm.** (See note below.)<br>0 = do not transmit yellow alarm<br>1 = transmit yellow alarm |

***Note:*** *For a description of how the bits in TCR1 affect the transmit side formatter, see Figure 16-11.*

## TCR2: TRANSMIT CONTROL REGISTER 2 (Address = 36 Hex)

| (MSB) | | | | | | | (LSB) |
|---|---|---|---|---|---|---|---|
| TEST1 | TEST0 | TZBTSI | TSDW | TSM | TSIO | TD4YM | TB7ZS |

| SYMBOL | POSITION | NAME AND DESCRIPTION |
|---|---|---|
| TEST1 | TCR2.7 | **Test Mode Bit 1 for Output Pins.** See Table 4-1. |
| TEST0 | TCR2.6 | **Test Mode Bit 0 for Output Pins.** See Table 4-1. |
| TZBTSI | TCR2.5 | **Transmit Side ZBTSI Enable.**<br>0 = ZBTSI disabled<br>1 = ZBTSI enabled |
| TSDW | TCR2.4 | **TSYNC Double-Wide.** (Note: this bit must be set to 0 when TCR2.3 = 1 or when TCR2.2 = 0.)<br>0 = do not pulse double-wide in signaling frames<br>1 = do pulse double-wide in signaling frames |
| TSM | TCR2.3 | **TSYNC Mode Select.**<br>0 = frame mode (see the timing diagrams in Section 16)<br>1 = multiframe mode (see the timing diagrams in Section 16) |
| TSIO | TCR2.2 | **TSYNC I/O Select.**<br>0 = TSYNC is an input<br>1 = TSYNC is an output |
| TD4YM | TCR2.1 | **Transmit Side D4 Yellow Alarm Select.**<br>0 = 0s in bit 2 of all channels<br>1 = a 1 in the S-bit position of frame 12 |
| TB7ZS | TCR2.0 | **Transmit Side Bit 7 Zero Suppression Enable.**<br>0 = no stuffing occurs<br>1 = Bit 7 force to a 1 in channels with all 0s |

## Table 4-1. Output Pin Test Modes

| TEST 1 | TEST 0 | EFFECT ON OUTPUT PINS |
|---|---|---|
| 0 | 0 | Operate normally |
| 0 | 1 | Force all output pins tri-state (including all I/O pins and parallel port pins) |
| 1 | 0 | Force all output pins low (including all I/O pins except parallel port pins) |
| 1 | 1 | Force all output pins high (including all I/O pins except parallel port pins) |

## CCR1: COMMON CONTROL REGISTER 1 (Address = 37 Hex)

| (MSB) | | | | | | | (LSB) |
|---|---|---|---|---|---|---|---|
| TESE | ODF | RSAO | TSCLKM | RSCLKM | RESE | PLB | FLB |

| SYMBOL | POSITION | NAME AND DESCRIPTION |
|---|---|---|
| TESE | CCR1.7 | **Transmit Elastic Store Enable.**<br>0 = elastic store is bypassed<br>1 = elastic store is enabled |
| ODF | CCR1.6 | **Output Data Format.**<br>0 = bipolar data at TPOSO and TNEGO<br>1 = NRZ data at TPOSO; TNEGO = 0 |
| RSAO | CCR1.5 | **Receive Signaling All 1s.** This bit should not be enabled if hardware signaling is being utilized. See Section 8 for more details.<br>0 = allow robbed signaling bits to appear at RSER<br>1 = force all robbed signaling bits at RSER to 1 |
| TSCLKM | CCR1.4 | **TSYSCLK Mode Select.**<br>0 = if TSYSCLK is 1.544MHz<br>1 = if TSYSCLK is 2.048MHz |
| RSCLKM | CCR1.3 | **RSYSCLK Mode Select.**<br>0 = if RSYSCLK is 1.544MHz<br>1 = if RSYSCLK is 2.048MHz |
| RESE | CCR1.2 | **Receive Elastic Store Enable.**<br>0 = elastic store is bypassed<br>1 = elastic store is enabled |
| PLB | CCR1.1 | **Payload Loopback.**<br>0 = loopback disabled<br>1 = loopback enabled |
| FLB | CCR1.0 | **Framer Loopback.**<br>0 = loopback disabled<br>1 = loopback enabled |

## 4.1 Payload Loopback

When CCR1.1 is set to 1, the DS2152 is forced into Payload Loopback (PLB). Normally, this loopback is only enabled when ESF framing is being performed but can be enabled also in D4 framing applications. In a PLB situation, the DS2152 loops the 192 bits of payload data (with BPVs corrected) from the receive section back to the transmit section. The FPS framing pattern, CRC6 calculation, and the FDL bits are not looped back, rather, they are reinserted by the DS2152. When PLB is enabled, the following occurs:

1) Data is transmitted from the TPOSO and TNEGO pins synchronous with RCLK instead of TCLK.
2) All the receive side signals continue to operate normally.
3) The TCHCLK and TCHBLK signals are forced low.
4) Data at the TSER, TDATA, and TSIG pins is ignored.
5) The TLCLK signal becomes synchronous with RCLK instead of TCLK.

## 4.2 Framer Loopback

When CCR1.0 is set to 1, the DS2152 enters a Framer Loopback (FLB) mode. This loopback is useful in testing and debugging applications. In FLB, the DS2152 loops data from the transmit side back to the receive side. When FLB is enabled, the following occurs:

1) An unframed all-1s code is transmitted at TPOSO and TNEGO.
2) Data at RPOSI and RNEGI is ignored.
3) All receive side signals take on timing synchronous with TCLK instead of RCLKI.

Note that it is not acceptable to have RCLK tied to TCLK during this loopback because this causes an unstable condition.

## 4.3 Pulse Density Enforcer

The SCT always examines both the transmit and receive data streams for violations of the following rules which are required by ANSI T1.403:

- No more than 15 consecutive 0s,
- At least N 1s in each and every time window of 8 x (N + 1) bits where N = 1 through 23,

Violations for the transmit and receive data streams are reported in the RIR2.0 and RIR2.1 bits, respectively. When the CCR3.3 is set to 1, the DS2152 forces the transmitted stream to meet this requirement no matter the content of the transmitted stream. When running B8ZS, the CCR3.3 bit should be set to 0 since B8ZS encoded data streams cannot violate the pulse density requirements.

## 4.4 Local Loopback

When CCR5.6 is set to 1, the DS2152 is forced into Local Loopback (LLB). In this loopback, data continues to be transmitted as normal through the transmit side of the DS2152 (unless LIAIS = 1). Data being received at RTIP and RRING is replaced with the data being transmitted. Data in this loopback passes through the jitter attenuator. See Figure 1-1 for more details. Note that it is not acceptable to have RCLKO tied to TCLKI during this loopback because this causes an unstable condition. Also, it is recommended that the jitter attenuator be placed on the transmit side during this loopback.

## CCR2: COMMON CONTROL REGISTER 2 (Address = 38 Hex)

| (MSB) | | | | | | | (LSB) |
|---|---|---|---|---|---|---|---|
| TFM | TB8ZS | TSLC96 | TFDL | RFM | RB8ZS | RSLC96 | RFDL |

| SYMBOL | POSITION | NAME AND DESCRIPTION |
|---|---|---|
| TFM | CCR2.7 | **Transmit Frame Mode Select.**<br>0 = D4 framing mode<br>1 = ESF framing mode |
| TB8ZS | CCR2.6 | **Transmit B8ZS Enable.**<br>0 = B8ZS disabled<br>1 = B8ZS enabled |
| TSLC96 | CCR2.5 | **Transmit SLC-96/Fs-Bit Loading Enable.** Only set this bit to a 1 in D4 framing applications. Must be set to 1 to source the Fs pattern. See Section 12 for details.<br>0 = SLC-96/Fs-bit loading disabled<br>1 = SLC-96/Fs-bit loading enabled |
| TFDL | CCR2.4 | **Transmit FDL 0 Stuffer Enable.** Set this bit to 0 if using the internal HDLC/BOC controller instead of the legacy support for the FDL. See Section 12 for details.<br>0 = 0 stuffer disabled<br>1 = 0 stuffer enabled |
| RFM | CCR2.3 | **Receive Frame Mode Select.**<br>0 = D4 framing mode<br>1 = ESF framing mode |
| RB8ZS | CCR2.2 | **Receive B8ZS Enable.**<br>0 = B8ZS disabled<br>1 = B8ZS enabled |
| RSLC96 | CCR2.1 | **Receive SLC-96 Enable.** Only set this bit to a 1 in D4/SLC-96 framing applications. See Section 12 for details.<br>0 = SLC-96 disabled<br>1 = SLC-96 enabled |
| RFDL | CCR2.0 | **Receive FDL 0 Destuffer Enable.** Set this bit to 0 if using the internal HDLC/BOC controller instead of the legacy support for the FDL. See Section 12 for details.<br>0 = 0 destuffer disabled<br>1 = 0 destuffer enabled |