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3.3V DS21352 and 5V DS21552 T1 Single-Chip Transceivers

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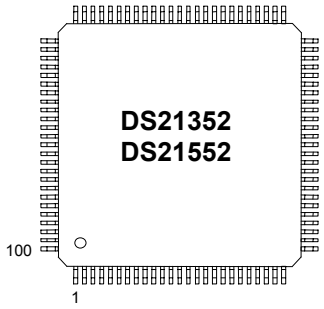
FEATURES

- Complete DS1/ISDN–PRI/J1 transceiver functionality
- Long and Short haul LIU
- Crystal–less jitter attenuator
- Generates DSX–1 and CSU line build-outs
- HDLC controller with 64-byte buffers Configurable for FDL or DS0 operation
- Dual two–frame elastic store slip buffers that can connect to asynchronous backplanes up to 8.192MHz
- 8.192MHz clock output locked to RCLK
- Interleaving PCM Bus Operation
- Per-channel loopback and idle code insertion
- 8-bit parallel control port muxed or nonmuxed buses (Intel or Motorola)
- Programmable output clocks for Fractional T1
- Fully independent transmit and receive functionality
- Generates/detects in-band loop codes from 1 to 8 bits in length including CSU loop codes
- IEEE 1149.1 JTAG-Boundary Scan
- Pin compatible with DS2152/54/354/554 SCTs
- 100-pin LQFP package (14 mm x 14 mm) 3.3V (DS21352) or 5V (DS21552) supply; low power CMOS

PIN ASSIGNMENT



ORDERING INFORMATION

DS21352L	(0°C to +70°C)
DS21352LN	(-40°C to +85°C)
DS21552L	(0°C to +70°C)
DS21552LN	(-40°C to +85°C)

DESCRIPTION

The DS21352/552 T1 single-chip transceiver contains all of the necessary functions for connection to T1 lines whether they are DS1 long haul or DSX–1 short haul. The clock recovery circuitry automatically adjusts to T1 lines from 0 feet to over 6000 feet in length. The device can generate both DSX–1 line build outs as well as CSU line build-outs of -7.5dB, -15dB, and -22.5dB. The onboard jitter attenuator (selectable to either 32 bits or 128 bits) can be placed in either the transmit or receive data paths. The framer locates the frame and multiframe boundaries and monitors the data stream for alarms. It is also used for extracting and inserting robbed-bit signaling data and FDL data. The device contains a set of internal registers which the user can access and control the operation of the unit. Quick access via the parallel control port allows a single controller to handle many T1 lines. The device fully meets all of the latest T1 specifications including ANSI T1.403-1995, ANSI T1.231-1993, AT&T TR 62411 (12–90), AT&T TR54016, and ITU G.703, G.704, G.706, G.823, and I.431.

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3. INTRODUCTION

The DS21352/552 are 3.3V/5V superset versions of the popular DS2152 T1 single-chip transceiver offering the new features listed below. All of the original features of the DS2152 have been retained and software created for the original devices is transferable into the DS21352/552.

NEW FEATURES (after the DS2152)

- Interleaving PCM Bus Operation
- Integral HDLC controller with 64-byte buffers Configurable for FDL or DS0 operation
- IEEE 1149.1 JTAG-Boundary Scan Architecture
- 3.3V (DS21352 only) supply

FEATURES

- option for non–multiplexed bus operation
- crystal–less jitter attenuation
- 3.3V I/O on all SCTs
- additional hardware signaling capability including:
  – receive signaling reinsertion to a backplane multiframe sync
  – availability of signaling in a separate PCM data stream
  – signaling freezing
  – interrupt generated on change of signaling data
- ability to calculate and check CRC6 according to the Japanese standard
- ability to pass the F–Bit position through the elastic stores in the 2.048 MHz backplane mode
- programmable in–band loop code generator and detector
- per channel loopback and idle code insertion
- RCL, RLOS, RRA, and RAIS alarms now interrupt on change of state
- 8.192 MHz clock output synthesized to RCLK
- HDLC controller can be configured for FDL
- addition of hardware pins to indicate carrier loss & signaling freeze
- line interface function can be completely decoupled from the framer/formatter to allow:
  – interface to optical, HDSL, and other NRZ interfaces
  – be able to “tap” the transmit and receive bipolar data streams for monitoring purposes
  – be able corrupt data and insert framing errors, CRC errors, etc.
- transmit and receive elastic stores now have independent backplane clocks

3.1 FUNCTIONAL DESCRIPTION

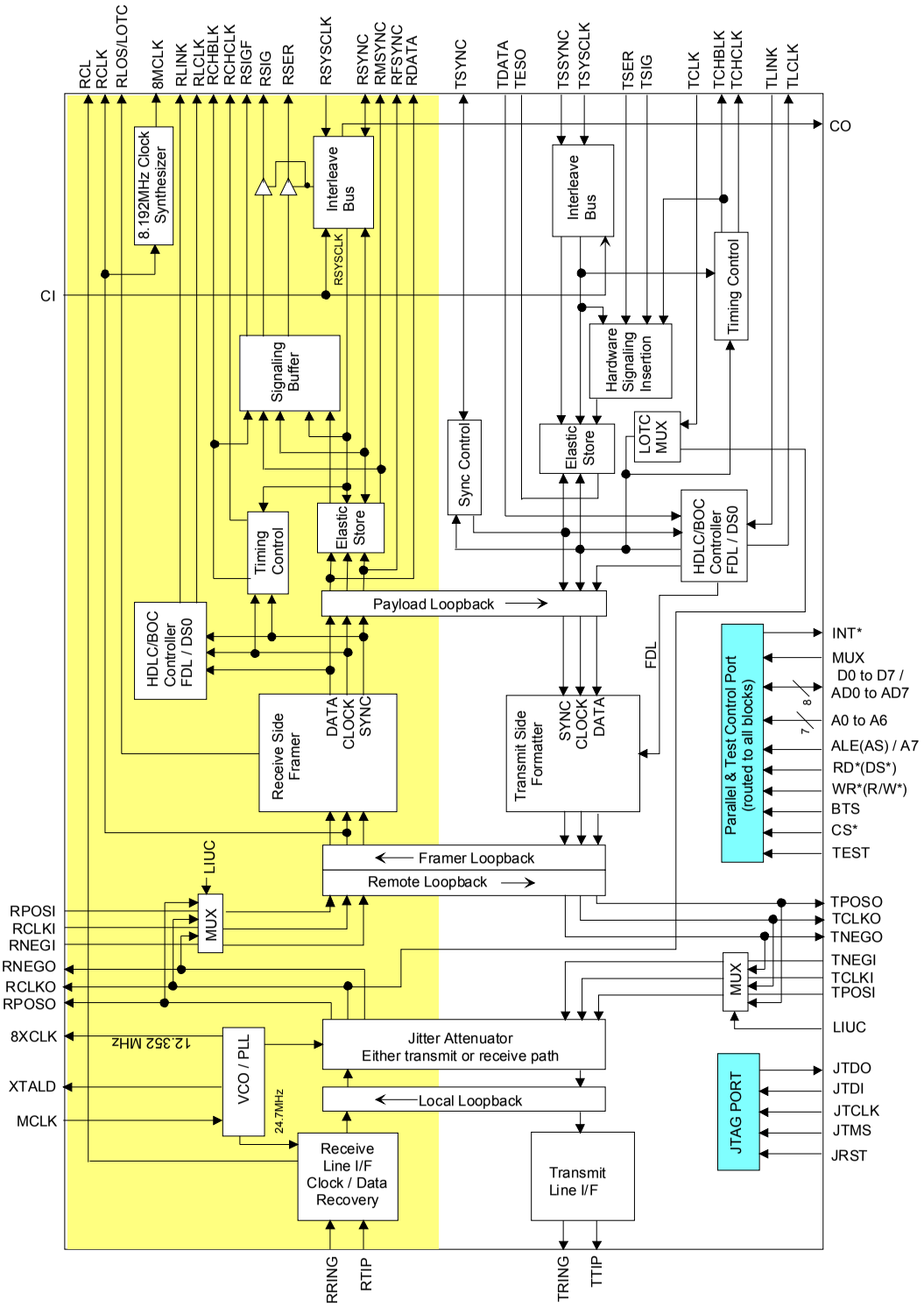
The analog AMI/B8ZS waveform off of the T1 line is transformer coupled into the RRING and RTIP pins of the DS21352/552. The device recovers clock and data from the analog signal and passes it through the jitter attenuation mux to the receive side framer where the digital serial stream is analyzed to locate the framing/multi-frame pattern. The DS21352/552 contains an active filter that reconstructs the analog received signal for the nonlinear losses that occur in transmission. The device has a usable receive sensitivity of 0 dB to –36 dB, which allows the device to operate on cables up to 6000 feet in length. The receive side framer locates D4 (SLC–96) or ESF multiframe boundaries as well as detects incoming alarms including, carrier loss, loss of synchronization, blue (AIS) and yellow alarms. If needed, the receive side elastic store can be enabled in order to absorb the phase and frequency differences between the recovered T1 data stream and an asynchronous backplane clock which is provided at the RSYSCLK input. The clock applied at the RSYSCLK input can be either a 2.048 MHz clock or a 1.544 MHz clock. The RSYSCLK can be a bursty clock with speeds up to 8.192 MHz.

The transmit side of the DS21352/552 is totally independent from the receive side in both the clock requirements and characteristics. Data off of a backplane can be passed through a transmit side elastic store if necessary. The transmit formatter will provide the necessary frame/multiframe data overhead for T1 transmission. Once the data stream has been prepared for transmission, it is sent via the jitter attenuation mux to the waveshaping and line driver functions. The DS21352/552 will drive the T1 line from the TTIP and TRING pins via a coupling transformer. The line driver can handle both long haul (CSU) and short haul (DSX–1) lines.

Reader's Note: This data sheet assumes a particular nomenclature of the T1 operating environment. In each 125 μs frame, there are 24 eight–bit channels plus a framing bit. It is assumed that the framing bit is sent first followed by channel 1. Each channel is made up of eight bits, which are numbered, 1 to 8. Bit number 1 is the MSB and is transmitted first. Bit number 8 is the LSB and is transmitted last. The term "locked" is used to refer to two clock signals that are phase or frequency locked or derived from a common clock (i.e., a 1.544 MHz clock may be locked to a 2.048MHz clock if they share the same 8 kHz component). Throughout this data sheet, the following abbreviations will be used:

B8ZS	Bipolar with 8 Zero Substitution
BOC	Bit Oriented Code
CRC	Cyclical Redundancy Check
D4	Superframe (12 frames per multiframe) Multiframe Structure
ESF	Extended Superframe (24 frames per multiframe) Multiframe Structure
FDL	Facility Data Link
FPS	Framing Pattern Sequence in ESF
Fs	Signaling Framing Pattern in D4
Ft	Terminal Framing Pattern in D4
HDLC	High Level Data Link Control
MF	Multiframe
SLC–96	Subscriber Loop Carrier – 96 Channels (SLC–96 is an AT&T registered trademark)

Figure 3-1 SCT BLOCK DIAGRAM



3.2 DOCUMENT REVISION HISTORY

Revision	Notes
12-10-98	Initial Release
12-18-98	Add LIUODO (LIU Open Drain Output) to CCR7.0 Add CDIG (Customer Disconnect Indication Generator) to CCR7.1 Add LIUSI (Line Interface Unit Synchronization Interface) to CCR7.2 Correct IBO register bit functions order Add bit level description to CCR3.6
1-4-99	Delete "**The elastic stores can be forced to a known depth via the Elastic Store Reset bit (CCR3.6). Toggling the CCR3.6 bit forces the read and write pointers into opposite frames**" from section 12.0
1-18-99	Add receive IBO operation PCM timing diagram
1-18-99	Correct Device ID register bit definitions
1-28-99	Correct TSYSCLK and RSYSCLK AC timing and add 4.096 MHz and 8.192 MHz AC timing
2-2-99	Correct definition and label or TUDR bit in TPRM register
2-11-99	Correct format of register definitions in body of data sheet
4-1-99	Add Receive Monitor Mode section
4-15-99	Add section on Protected Interfaces
5-7-99	Correct FMS pin # and description in JTAG section
5-17-99	Correct name of status registers in section 15.3.2
5-19-99	Correct definition of RIR3.4
7-27-99	Correct Receive Monitor Mode section
8-16-99	Remove "Preliminary" notice from data sheet

4. PIN DESCRIPTION

Table 4-1 PIN DESCRIPTION SORTED BY PIN NUMBER

PIN	SYMBOL	TYPE	DESCRIPTION
1	RCHBLK	O	Receive Channel Block
2	JTMS	I	IEEE 1149.1 Test Mode Select
3	8MCLK	O	8.192 MHz Clock
4	JTCLK	I	IEEE 1149.1 Test Clock Signal
5	JTRST	I	IEEE 1149.1 Test Reset
6	RCL	O	Receive Carrier Loss
7	JTDI	I	IEEE 1149.1 Test Data Input
8	NC	–	No Connect
9	NC	–	No Connect
10	JTDO	O	IEEE 1149.1 Test Data Output
11	BTS	I	Bus Type Select
12	LIUC	I	Line Interface Connect
13	8XCLK	O	Eight Times Clock
14	TEST	I	Test
15	NC	–	No Connect
16	RTIP	I	Receive Analog Tip Input
17	RRING	I	Receive Analog Ring Input
18	RVDD	–	Receive Analog Positive Supply
19	RVSS	–	Receive Analog Signal Ground
20	RVSS	–	Receive Analog Signal Ground
21	MCLK	I	Master Clock Input
22	XTALD	O	Quartz Crystal Driver
23	NC	–	No Connect
24	RVSS	–	Receive Analog Signal Ground
25	INT*	O	Interrupt
26	NC	–	No Connect
27	NC	–	No Connect
28	NC	–	No Connect
29	TTIP	O	Transmit Analog Tip Output
30	TVSS	–	Transmit Analog Signal Ground
31	TVDD	–	Transmit Analog Positive Supply
32	TRING	O	Transmit Analog Ring Output
33	TCHBLK	O	Transmit Channel Block
34	TLCLK	O	Transmit Link Clock
35	TLINK	I	Transmit Link Data
36	CI	I	Carry In
37	TSYNC	I/O	Transmit Sync
38	TPOSI	I	Transmit Positive Data Input
39	TNEGI	I	Transmit Negative Data Input
40	TCLKI	I	Transmit Clock Input
41	TCLKO	O	Transmit Clock Output
42	TNEGO	O	Transmit Negative Data Output
43	TPOSO	O	Transmit Positive Data Output

Table 4-1 PIN DESCRIPTION SORTED BY PIN NUMBER (cont.)

PIN	SYMBOL	TYPE	DESCRIPTION
44	DVDD	–	Digital Positive Supply
45	DVSS	–	Digital Signal Ground
46	TCLK	I	Transmit Clock
47	TSER	I	Transmit Serial Data
48	TSIG	I	Transmit Signaling Input
49	TESO	O	Transmit Elastic Store Output

50	TDATA	I	Transmit Data
51	TSYSCLK	I	Transmit System Clock
52	TSSYNC	I	Transmit System Sync
53	TCHCLK	O	Transmit Channel Clock
54	CO	O	Carry Out
55	MUX	I	Bus Operation
56	D0/AD0	I/O	Data Bus Bit0/ Address/Data Bus Bit 0
57	D1/AD1	I/O	Data Bus Bit1/ Address/Data Bus Bit 1
58	D2/AD2	I/O	Data Bus Bit 2/Address/Data Bus 2
59	D3/AD3	I/O	Data Bus Bit 3/Address/Data Bus Bit 3
60	DVSS	–	Digital Signal Ground
61	DVDD	-	Digital Positive Supply
62	D4/AD4	I/O	Data Bus Bit4/Address/Data Bus Bit 4
63	D5/AD5	I/O	Data Bus Bit 5/Address/Data Bus Bit 5
64	D6/AD6	I/O	Data Bus Bit 6/Address/Data Bus Bit 6
65	D7/AD7	I/O	Data Bus Bit 7/Address/Data Bus Bit 7
66	A0	I	Address Bus Bit 0
67	A1	I	Address Bus Bit 1
68	A2	I	Address Bus Bit 2
69	A3	I	Address Bus Bit 3
70	A4	I	Address Bus Bit 4
71	A5	I	Address Bus Bit 5
72	A6	I	Address Bus Bit 6
73	ALE (AS)/A7	I	Address Latch Enable/Address Bus Bit 7
74	RD*(DS*)	I	Read Input(Data Strobe)
75	CS*	I	Chip Select
76	FMS	I	Framer Mode Select
77	WR*(R/W*)	I	Write Input(Read/Write)
78	RLINK	O	Receive Link Data
79	RLCLK	O	Receive Link Clock
80	DVSS	–	Digital Signal Ground
81	DVDD	–	Digital Positive Supply
82	RCLK	O	Receive Clock
83	DVDD	–	Digital Positive Supply
84	DVSS	–	Digital Signal Ground
85	RDATA	O	Receive Data
86	RPOSI	I	Receive Positive Data Input
87	RNEGI	I	Receive Negative Data Input
88	RCLKI	I	Receive Clock Input

Table 4-1 PIN DESCRIPTION SORTED BY PIN NUMBER (cont.)

PIN	SYMBOL	TYPE	DESCRIPTION
89	RCLKO	O	Receive Clock Output
90	RNEGO	O	Receive Negative Data Output
91	RPOSO	O	Receive Positive Data Output
92	RCHCLK	O	Receive Channel Clock
93	RSIGF	O	Receive Signaling Freeze Output
94	RSIG	O	Receive Signaling Output
95	RSER	O	Receive Serial Data
96	RMSYNC	O	Receive Multiframe Sync
97	RFSYNC	O	Receive Frame Sync
98	RSYNC	I/O	Receive Sync
99	RLOS/LOTC	O	Receive Loss Of Sync/ Loss Of Transmit Clock
100	RSYSCLK	I	Receive System Clock

Table 4-1 PIN DESCRIPTION SORTED BY PIN SYMBOL

PIN	SYMBOL	TYPE	DESCRIPTION
3	8MCLK	O	8.192 MHz Clock
13	8XCLK	O	Eight Times Clock
66	A0	I	Address Bus Bit 0
67	A1	I	Address Bus Bit 1
68	A2	I	Address Bus Bit 2
69	A3	I	Address Bus Bit 3
70	A4	I	Address Bus Bit 4
71	A5	I	Address Bus Bit 5
72	A6	I	Address Bus Bit 6
73	ALE (AS)/A7	I	Address Latch Enable/Address Bus Bit 7
11	BTS	I	Bus Type Select
36	CI	I	Carry In
54	CO	O	Carry Out
75	CS*	I	Chip Select
56	D0/AD0	I/O	Data Bus Bit0/ Address/Data Bus Bit 0
57	D1/AD1	I/O	Data Bus Bit1/ Address/Data Bus Bit 1
58	D2/AD2	I/O	Data Bus Bit 2/Address/Data Bus 2
59	D3/AD3	I/O	Data Bus Bit 3/Address/Data Bus Bit 3
62	D4/AD4	I/O	Data Bus Bit4/Address/Data Bus Bit 4
63	D5/AD5	I/O	Data Bus Bit 5/Address/Data Bus Bit 5
64	D6/AD6	I/O	Data Bus Bit 6/Address/Data Bus Bit 6
65	D7/AD7	I/O	Data Bus Bit 7/Address/Data Bus Bit 7
44	DVDD	–	Digital Positive Supply
81	DVDD	–	Digital Positive Supply
45	DVSS	–	Digital Signal Ground
60	DVSS	–	Digital Signal Ground
80	DVSS	–	Digital Signal Ground
84	DVSS	–	Digital Signal Ground
76	FMS	I	Framer Mode Select
61	DVDD	-	Digital Positive Supply
83	DVDD	–	Digital Positive Supply
25	INT*	O	Interrupt
4	JTCLK	I	IEEE 1149.1 Test Clock Signal
7	JTDI	I	IEEE 1149.1 Test Data Input
10	JTDO	O	IEEE 1149.1 Test Data Output
2	JTMS	I	IEEE 1149.1 Test Mode Select
5	JTRST	I	IEEE 1149.1 Test Reset
12	LIUC	I	Line Interface Connect
21	MCLK	I	Master Clock Input
55	MUX	I	Bus Operation
8	NC	–	No Connect
9	NC	–	No Connect
15	NC	–	No Connect
23	NC	–	No Connect
26	NC	–	No Connect

Table 4-1 PIN DESCRIPTION SORTED BY PIN SYMBOL (cont.)

PIN	SYMBOL	TYPE	DESCRIPTION
27	NC	–	No Connect
28	NC	–	No Connect
1	RCHBLK	O	Receive Channel Block
92	RCHCLK	O	Receive Channel Clock
6	RCL	O	Receive Carrier Loss
82	RCLK	O	Receive Clock

88	RCLKI	I	Receive Clock Input
89	RCLKO	O	Receive Clock Output
74	RD*(DS*)	I	Read Input(Data Strobe)
85	RDATA	O	Receive Data
97	RFSYNC	O	Receive Frame Sync
79	RLCLK	O	Receive Link Clock
78	RLINK	O	Receive Link Data
99	RLOS/LOTC	O	Receive Loss Of Sync/ Loss Of Transmit Clock
96	RMSYNC	O	Receive Multiframe Sync
87	RNEGI	I	Receive Negative Data Input
90	RNEGO	O	Receive Negative Data Output
86	RPOSI	I	Receive Positive Data Input
91	RPOSO	O	Receive Positive Data Output
17	RRING	I	Receive Analog Ring Input
95	RSER	O	Receive Serial Data
94	RSIG	O	Receive Signaling Output
93	RSIGF	O	Receive Signaling Freeze Output
98	RSYNC	I/O	Receive Sync
100	RSYSCLK	I	Receive System Clock
16	RTIP	I	Receive Analog Tip Input
18	RVDD	–	Receive Analog Positive Supply
19	RVSS	–	Receive Analog Signal Ground
20	RVSS	–	Receive Analog Signal Ground
24	RVSS	–	Receive Analog Signal Ground
33	TCHBLK	O	Transmit Channel Block
53	TCHCLK	O	Transmit Channel Clock
46	TCLK	I	Transmit Clock
40	TCLKI	I	Transmit Clock Input
41	TCLKO	O	Transmit Clock Output
50	TDATA	I	Transmit Data
49	TESO	O	Transmit Elastic Store Output
14	TEST	I	Test
34	TLCLK	O	Transmit Link Clock
35	TLINK	I	Transmit Link Data
39	TNEGI	I	Transmit Negative Data Input
42	TNEGO	O	Transmit Negative Data Output
38	TPOSI	I	Transmit Positive Data Input
43	TPOSO	O	Transmit Positive Data Output
32	TRING	O	Transmit Analog Ring Output

Table 4-1 PIN DESCRIPTION SORTED BY PIN SYMBOL (cont.)

47	TSER	I	Transmit Serial Data
48	TSIG	I	Transmit Signaling Input
52	TSSYNC	I	Transmit System Sync
37	TSYNC	I/O	Transmit Sync
51	TSYSCLK	I	Transmit System Clock
29	TTIP	O	Transmit Analog Tip Output
31	TVDD	–	Transmit Analog Positive Supply
30	TVSS	–	Transmit Analog Signal Ground
77	WR*(R/W*)	I	Write Input(Read/Write)
22	XTALD	O	Quartz Crystal Driver

4. PIN FUNCTION DESCRIPTION

4.1.1 TRANSMIT SIDE PINS

Signal Name: **TCLK**
Signal Description: **Transmit Clock**
Signal Type: **Input**
A 1.544 MHz primary clock. Used to clock data through the transmit side formatter.

Signal Name: **TSER**
Signal Description: **Transmit Serial Data**
Signal Type: **Input**
Transmit NRZ serial data. Sampled on the falling edge of TCLK when the transmit side elastic store is disabled. Sampled on the falling edge of TSYSCLK when the transmit side elastic store is enabled.

Signal Name: **TCHCLK**
Signal Description: **Transmit Channel Clock**
Signal Type: **Output**
A 192 kHz clock which pulses high during the LSB of each channel. Synchronous with TCLK when the transmit side elastic store is disabled. Synchronous with TSYSCLK when the transmit side elastic store is enabled. Useful for parallel to serial conversion of channel data.

Signal Name: **TCHBLK**
Signal Description: **Transmit Channel Block**
Signal Type: **Output**
A user programmable output that can be forced high or low during any of the 24 T1 channels. Synchronous with TCLK when the transmit side elastic store is disabled. Synchronous with TSYSCLK when the transmit side elastic store is enabled. Useful for blocking clocks to a serial UART or LAPD controller in applications where not all T1 channels are used such as Fractional T1, 384 kbps (H0), 768 kbps or ISDN–PRI . Also useful for locating individual channels in drop–and–insert applications, for external per–channel loopback, and for per–channel conditioning. See section 13 on page 76 for more information.

Signal Name: **TSYSCLK**
Signal Description: **Transmit System Clock**
Signal Type: **Input**
1.544 MHz , 2.048 MHz , 4.096 MHz or 8.192 MHz clock. Only used when the transmit side elastic store function is enabled. Should be tied low in applications that do not use the transmit side elastic store. See section 20 on page 129 for details on 4.096 MHz and 8.192 MHz operation using the Interleave Bus Option.

Signal Name: **TLCLK**
Signal Description: **Transmit Link Clock**
Signal Type: **Output**
4 kHz or 2 kHz (ZBTSI) demand clock for the TLINK input. See Section 15 for details. Transmit Link Data [TLINK].

4.1.1 TRANSMIT SIDE PINS (cont.)

Signal Name: **TLINK**
Signal Description: **Transmit Link Data**
Signal Type: **Input**
If enabled via TCR1.2, this pin will be sampled on the falling edge of TCLK for data insertion into either the FDL stream (ESF) or the Fs–bit position (D4) or the Z–bit position (ZBTSI). See Section 15 for details.

Signal Name: **TSYNC**
Signal Description: **Transmit Sync**
Signal Type: **Input / Output**
A pulse at this pin will establish either frame or multiframe boundaries for the transmit side. Via TCR2.2, the DS21352/552 can be programmed to output either a frame or multiframe pulse at this pin. If this pin is set to output pulses at frame boundaries, it can also be set via TCR2.4 to output double–wide pulses at signaling frames. See Section 20 for details.

Signal Name: **TSSYNC**
Signal Description: **Transmit System Sync**
Signal Type: **Input**
Only used when the transmit side elastic store is enabled. A pulse at this pin will establish either frame or multiframe boundaries for the transmit side. Should be tied low in applications that do not use the transmit side elastic store.

Signal Name: **TSIG**
Signal Description: **Transmit Signaling Input**
Signal Type: **Input**
When enabled, this input will sample signaling bits for insertion into outgoing PCM T1 data stream. Sampled on the falling edge of TCLK when the transmit side elastic store is disabled. Sampled on the falling edge of TSYSCLK when the transmit side elastic store is enabled.

Signal Name: **TESO**
Signal Description: **Transmit Elastic Store Data Output**
Signal Type: **Output**
Updated on the rising edge of TCLK with data out of the transmit side elastic store whether the elastic store is enabled or not. This pin is normally tied to TDATA.

Signal Name: **TDATA**
Signal Description: **Transmit Data**
Signal Type: **Input**
Sampled on the falling edge of TCLK with data to be clocked through the transmit side formatter. This pin is normally tied to TESO.

Signal Name: **TPOSO**
Signal Description: **Transmit Positive Data Output**
Signal Type: **Output**
Updated on the rising edge of TCLKO with the bipolar data out of the transmit side formatter. Can be programmed to source NRZ data via the Output Data Format (CCR1.6) control bit. This pin is normally tied to TPOSI.

4.1.1 TRANSMIT SIDE PINS (cont.)

Signal Name: **TNEGO**
Signal Description: **Transmit Negative Data Output**
Signal Type: **Output**
Updated on the rising edge of TCLKO with the bipolar data out of the transmit side formatter. This pin is normally tied to TNEGI.

Signal Name: **TCLKO**
Signal Description: **Transmit Clock Output**
Signal Type: **Output**
Buffered clock that is used to clock data through the transmit side formatter (i.e., either TCLK or RCLKI). This pin is normally tied to TCLKI.

Signal Name: **TPOSI**
Signal Description: **Transmit Positive Data Input**
Signal Type: **Input**
Sampled on the falling edge of TCLKI for data to be transmitted out onto the T1 line. Can be internally connected to TPOSO by tying the LIUC pin high.

Signal Name: **TNEGI**
Signal Description: **Transmit Negative Data Input**
Signal Type: **Input**
Sampled on the falling edge of TCLKI for data to be transmitted out onto the T1 line. Can be internally connected to TNEGO by tying the LIUC pin high.

Signal Name: **TCLKI**
Signal Description: **Transmit Clock Input**
Signal Type: **Input**
Line interface transmit clock. Can be internally connected to TCLKO by tying the LIUC pin high.

4.1.2 RECEIVE SIDE PINS

Signal Name: **RLINK**
Signal Description: **Receive Link Data**
Signal Type: **Output**
Updated with either FDL data (ESF) or Fs bits (D4) or Z bits (ZBTSI) one RCLK before the start of a frame. See Section 20 for details.

Signal Name: **RLCLK**
Signal Description: **Receive Link Clock**
Signal Type: **Output**
A 4 kHz or 2 kHz (ZBTSI) clock for the RLINK output.

Signal Name: **RCLK**
Signal Description: **Receive Clock**
Signal Type: **Output**
1.544 MHz clock that is used to clock data through the receive side framer.

Signal Name: **RCHCLK**
Signal Description: **Receive Channel Clock**
Signal Type: **Output**
A 192 kHz clock which pulses high during the LSB of each channel. Synchronous with RCLK when the receive side elastic store is disabled. Synchronous with RSYSCLK when the receive side elastic store is enabled. Useful for parallel to serial conversion of channel data.

Signal Name: **RCHBLK**
Signal Description: **Receive Channel Block**
Signal Type: **Output**
A user programmable output that can be forced high or low during any of the 24 T1 channels. Synchronous with RCLK when the receive side elastic store is disabled. Synchronous with RSYSCLK when the receive side elastic store is enabled. Useful for blocking clocks to a serial UART or LAPD controller in applications where not all T1 channels are used such as Fractional T1, 384K bps service, 768K bps, or ISDN–PRI. Also useful for locating individual channels in drop–and–insert applications, for external per–channel loopback, and for per–channel conditioning. See Section 13 page 76 for details.

Signal Name: **RSER**
Signal Description: **Receive Serial Data**
Signal Type: **Output**
Received NRZ serial data. Updated on rising edges of RCLK when the receive side elastic store is disabled. Updated on the rising edges of RSYSCLK when the receive side elastic store is enabled.

Signal Name: **RSYNC**
Signal Description: **Receive Sync**
Signal Type: **Input/Output**
An extracted pulse, one RCLK wide, is output at this pin which identifies either frame (RCR2.4 = 0) or multiframe (RCR2.4 = 1) boundaries. If set to output frame boundaries then via RCR2.5, RSYNC can also be set to output double–wide pulses on signaling frames. If the receive side elastic store is enabled via CCR1.2, then this pin can be enabled to be an input via RCR2.3 at which a frame or multiframe boundary pulse is applied. See Section 21 for details.

4.1.2 RECEIVE SIDE PINS (cont.)

Signal Name: **RFSYNC**
Signal Description: **Receive Frame Sync**
Signal Type: **Output**
An extracted 8 kHz pulse, one RCLK wide, is output at this pin which identifies frame boundaries.

Signal Name: **RMSYNC**
Signal Description: **Receive Multiframe Sync**
Signal Type: **Output**
Only used when the receive side elastic store is enabled. An extracted pulse, one RSYSCLK wide, is output at this pin which identifies multiframe boundaries. If the receive side elastic store is disabled, then this output will output multiframe boundaries associated with RCLK.

Signal Name: **RDATA**
Signal Description: **Receive Data**
Signal Type: **Output**
Updated on the rising edge of RCLK with the data out of the receive side framer.

Signal Name: **RSYSCLK**
Signal Description: **Receive System Clock**
Signal Type: **Input**
1.544 MHz , 2.048 MHz , 4.096 MHz or 8.192 MHz clock. Only used when the receive side elastic store function is enabled. Should be tied low in applications that do not use the receive side elastic store. See section 20 on page 129 for details on 4.096 MHz and 8.192 MHz operation using the Interleave Bus Option.

Signal Name: **RSIG**
Signal Description: **Receive Signaling Output**
Signal Type: **Output**
Outputs signaling bits in a PCM format. Updated on rising edges of RCLK when the receive side elastic store is disabled. Updated on the rising edges of RSYSCLK when the receive side elastic store is enabled.

Signal Name: **RLOS/LOTC**
Signal Description: **Receive Loss of Sync / Loss of Transmit Clock**
Signal Type: **Output**
A dual function output that is controlled by the CCR3.5 control bit. This pin can be programmed to either toggle high when the synchronizer is searching for the frame and multiframe or to toggle high if the TCLK pin has not been toggled for 5 µsec.

Signal Name: **RCL**
Signal Description: **Receive Carrier Loss**
Signal Type: **Output**
Set high when the line interface detects a carrier loss.

Signal Name: **RSIGF**
Signal Description: **Receive Signaling Freeze**
Signal Type: **Output**
Set high when the signaling data is frozen via either automatic or manual intervention. Used to alert downstream equipment of the condition.

4.1.2 RECEIVE SIDE PINS (cont.)

Signal Name: **8MCLK**
Signal Description: **8 MHz Clock**
Signal Type: **Output**
An 8.192MHz clock output that is referenced to the clock that is output at the RCLK pin.

Signal Name: **RPOSO**
Signal Description: **Receive Positive Data Input**
Signal Type: **Output**

Updated on the rising edge of RCLKO with bipolar data out of the line interface. This pin is normally tied to RPOSI.

Signal Name: **RNEGO**
Signal Description: **Receive Negative Data Input**
Signal Type: **Output**
Updated on the rising edge of RCLKO with the bipolar data out of the line interface. This pin is normally tied to RPOSI.

Signal Name: **RCLKO**
Signal Description: **Receive Clock Output**
Signal Type: **Output**
Buffered recovered clock from the T1 line. This pin is normally tied to RCLKI.

Signal Name: **RPOSI**
Signal Description: **Receive Positive Data Input**
Signal Type: **Input**
Sampled on the falling edge of RCLKI for data to be clocked through the receive side framer. RPOSI and RNEGI can be tied together for a NRZ interface. Can be internally connected to RPOSO by tying the LIUC pin high.

Signal Name: **RNEGI**
Signal Description: **Receive Negative Data Input**
Signal Type: **Input**
Sampled on the falling edge of RCLKI for data to be clocked through the receive side framer. RPOSI and RNEGI can be tied together for a NRZ interface. Can be internally connected to RNEGO by tying the LIUC pin high.

Signal Name: **RCLKI**
Signal Description: **Receive Clock Input**
Signal Type: **Input**
Clock used to clock data through the receive side framer. This pin is normally tied to RCLKO. Can be internally connected to RCLKO by tying the LIUC pin high.

4.1.3 PARALLEL CONTROL PORT PINS

Signal Name: **INT***
Signal Description: **Interrupt**
Signal Type: **Output**
Flags host controller during conditions and change of conditions defined in the Status Registers 1 and 2 and the HDLC Status Register. Active low, open drain output

Signal Name: **FMS**
Signal Description: **Framer Mode Select**
Signal Type: **Input**
Selects the DS2152 mode when high or the DS21352/552 mode when low. If high, the JTRST is internally pulled low. If low, JTRST has normal JTAG functionality. This pin has a 10k pull up resistor.

Signal Name: **TEST**
Signal Description: **3–State Control**
Signal Type: **Input**
Set high to 3–state all output and I/O pins (including the parallel control port) when FMS = 1 or when FMS = 0 and JTRST* is tied low. Set low for normal operation. Ignored when FMS = 0 and JTRST* = 1. Useful for board level testing.

Signal Name: **MUX**
Signal Description: **Bus Operation**
Signal Type: **Input**
Set low to select non–multiplexed bus operation. Set high to select multiplexed bus operation.

Signal Name: **AD0 TO AD7**
Signal Description: **Data Bus [D0 to D7] or Address/Data Bus**
Signal Type: **Input**
In non–multiplexed bus operation (MUX = 0), serves as the data bus. In multiplexed bus operation (MUX = 1), serves as a 8–bit multiplexed address / data bus.

Signal Name: **A0 TO A6**
Signal Description: **Address Bus**
Signal Type: **Input**
In non–multiplexed bus operation (MUX = 0), serves as the address bus. In multiplexed bus operation (MUX = 1), these pins are not used and should be tied low.

Signal Name: **BTS**
Signal Description: **Bus Type Select**
Signal Type: **Input**
Strap high to select Motorola bus timing; strap low to select Intel bus timing. This pin controls the function of the RD*(DS*), ALE(AS), and WR*(R/W*) pins. If BTS = 1, then these pins assume the function listed in parenthesis ().

Signal Name: **RD*(DS*)**
Signal Description: **Read Input - Data Strobe**
Signal Type: **Input**
RD* and DS* are active low signals. DS active HIGH when MUX = 0. See bus timing diagrams.

4.1.3 PARALLEL CONTROL PORT PINS (cont.)

Signal Name: **CS***
Signal Description: **Chip Select**
Signal Type: **Input**
Must be low to read or write to the device. CS* is an active low signal.

Signal Name: **ALE(AS)/A7**
Signal Description: **Address Latch Enable(Address Strobe) or A7**
Signal Type: **Input**
In non–multiplexed bus operation (MUX = 0), serves as the upper address bit. In multiplexed bus operation (MUX = 1), serves to de-multiplex the bus on a positive–going edge.

Signal Name: **WR*(R/W*)**
Signal Description: **Write Input(Read/Write)**
Signal Type: **Input**
WR* is an active low signal.

4.1.4 JTAG TEST ACCESS PORT PINS

Signal Name: **JTRST**
Signal Description: **IEEE 1149.1 Test Reset**
Signal Type: **Input**
If FMS = 1: JTAG functionality is not available and JTRST is held LOW internally.
If FMS = 0: JTAG functionality is available and JTRST is pulled up internally by a 10kΩ resistor.
If FMS = 0 and boundary scan is not used, this pin should be held low. This signal is used to asynchronously reset the test access port controller. The device operates as a T1/E1 transceiver if JTRST is pulled low.

Signal Name: **JTMS**
Signal Description: **IEEE 1149.1 Test Mode Select**
Signal Type: **Input**
This pin is sampled on the rising edge of JTCLK and is used to place the test access port into the various defined IEEE 1149.1 states. This pin has a 10k pull up resistor.

Signal Name: **JTCLK**
Signal Description: **IEEE 1149.1 Test Clock Signal**
Signal Type: **Input**
This signal is used to shift data into JTDI on the rising edge and out of JTDO on the falling edge.

Signal Name: **JTDI**
Signal Description: **IEEE 1149.1 Test Data Input**
Signal Type: **Input**
Test instructions and data are clocked into this pin on the rising edge of JTCLK. This pin has a 10k pull up resistor.

Signal Name: **JTDO**
Signal Description: **IEEE 1149.1 Test Data Output**
Signal Type: **Output**
Test instructions and data are clocked out of this pin on the falling edge of JTCLK. If not used, this pin should be left unconnected.

4.1.5 INTERLEAVE BUS OPERATION PINS

Signal Name: **CI**
Signal Description: **Carry In**
Signal Type: **Input**
A rising edge on this pin causes RSER and RSIG to come out of high Z state and TSER and TSIG to start sampling on the next rising edge of RSYSCLK/TSYSCLK beginning an I/O sequence of 8 or 256 bits of data. This pin has a 10k pull up resistor.

Signal Name: **CO**
Signal Description: **Carry Out**
Signal Type: **Output**
An output that is set high when the last bit of the 8 or 256 IBO output sequence has occurred on RSER and RSIG.

4.1.6 LINE INTERFACE PINS

Signal Name: **MCLK**
Signal Description: **Master Clock Input**
Signal Type: **Input**
A 1.544 MHz (50 ppm) clock source with TTL levels is applied at this pin. This clock is used internally for both clock/data recovery and for jitter attenuation. A quartz crystal of 1.544 MHz may be applied across MCLK and XTALD instead of the TTL level clock source.

Signal Name: **XTALD**
Signal Description: **Quartz Crystal Driver**
Signal Type: **Output**
A quartz crystal of 1.544 MHz may be applied across MCLK and XTALD instead of a TTL level clock source at MCLK. Leave open circuited if a TTL clock source is applied at MCLK.

Signal Name: **8XCLK**
Signal Description: **Eight Times Clock**
Signal Type: **Output**
A 12.352 MHz clock that is locked to the 1.544 MHz clock provided from the clock/data recovery block (if the jitter attenuator is enabled on the receive side) or from the TCLKI pin (if the jitter attenuator is enabled on the transmit side). Can be internally disabled by writing a 08h to TEST2.3 if not needed.

Signal Name: **LIUC**
Signal Description: **Line Interface Connect**
Signal Type: **Input**
Tie low to separate the line interface circuitry from the framer/formatter circuitry and activate the TPOSI/TNEGI/TCLKI/RPOSI/RNEGI/ RCLKI pins. Tie high to connect the line interface circuitry to the framer/formatter circuitry and deactivate the TPOSI/TNEGI/TCLKI/RPOSI/RNEGI/RCLKI pins. When LIUC is tied high, the TPOSI/TNEGI/TCLKI/ RPOSI/RNEGI/RCLKI pins should be tied low.

Signal Name: **RTIP & RRING**
Signal Description: **Receive Tip and Ring**
Signal Type: **Input**
Analog inputs for clock recovery circuitry. These pins connect via a 1:1 transformer to the T1 line. See Section 16 for details.

Signal Name: **TTIP & TRING**
Signal Description: **Transmit Tip and Ring**
Signal Type: **Output**
Analog line driver outputs. These pins connect via a transformer to the T1 line. See Section 16 for details.

4.1.7 SUPPLY PINS

Signal Name: **DVDD**
Signal Description: **Digital Positive Supply**
Signal Type: **Supply**
5.0 volts +/-5% (DS21552) or 3.3 volts +/-5% (DS21352). Should be tied to the RVDD and TVDD pins.

Signal Name: **RVDD**
Signal Description: **Receive Analog Positive Supply**
Signal Type: **Supply**
5.0 volts +/-5% (DS21552) or 3.3 volts +/-5% (DS21352). Should be tied to the DVDD and TVDD pins.

Signal Name: **TVDD**
Signal Description: **Transmit Analog Positive Supply**
Signal Type: **Supply**
5.0 volts +/-5% (DS21552) or 3.3 volts +/-5% (DS21352). Should be tied to the RVDD and DVDD pins.

Signal Name: **DVSS**
Signal Description: **Digital Signal Ground**
Signal Type: **Supply**
Should be tied to the RVSS and TVSS pins.

Signal Name: **RVSS**
Signal Description: **Receive Analog Signal Ground**
Signal Type: **Supply**
0.0 volts. Should be tied to DVSS and TVSS.

Signal Name: **TVSS**
Signal Description: **Transmit Analog Signal Ground**
Signal Type: **Supply**
0.0 volts. Should be tied to DVSS and RVSS.