Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

DS2156
T1/E1/J1 Single-Chip Transceiver TDM/UTOPIA II Interface

www.maxim-ic.com

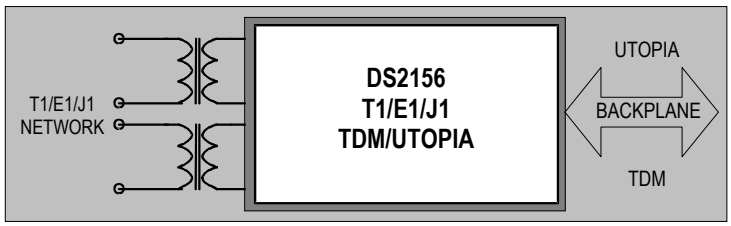
GENERAL DESCRIPTION

The DS2156 is a software-selectable T1, E1, or J1 single-chip transceiver (SCT) for short-haul and long-haul applications. The backplane is user-configurable for a TDM or UTOPIA II bus interface. The DS2156 is composed of a line interface unit (LIU), framer, HDLC controllers, and a UTOPIA/TDM backplane interface, and is controlled by an 8-bit parallel port configured for Intel or Motorola bus operations. The DS2156 is pin and software compatible with the DS2155.

The LIU is composed of transmit and receive interfaces and a jitter attenuator. The transmit interface is responsible for generating the necessary waveshapes for driving the network and providing the correct source impedance depending on the type of media used. T1 waveform generation includes DSX-1 line buildouts as well as CSU line buildouts of -7.5dB, -15dB, and -22.5dB. E1 waveform generation includes G.703 waveshapes for both 75Ω coax and 120Ω twisted cables. The receive interface provides network termination and recovers clock and data from the network.

APPLICATIONS

Inverse Mux ATM (IMA)
T1/E1/J1 Line Cards
Switches and Routers
Add-Drop Multiplexers



FEATURES

- Complete T1/DS1/ISDN-PRI/J1 Transceiver Functionality
- Complete E1 (CEPT) PCM-30/ISDN-PRI Transceiver Functionality
- User-Selectable TDM or UTOPIA II Bus Interface
- Long-Haul and Short-Haul Line Interface for Clock/Data Recovery and Waveshaping
- CMI Coder/Decoder for Optical I/F
- Crystal-Less Jitter Attenuator
- Fully Independent Transmit and Receive Functionality
- Dual HDLC Controllers
- Programmable BERT Generator and Detector
- Internal Software-Selectable Receive and Transmit-Side Termination Resistors for 75Ω/100Ω/120Ω T1 and E1 Interfaces
- Dual Two-Frame Elastic-Store Slip Buffers that Connect to Asynchronous Backplanes Up to 16.384MHz
- 16.384MHz, 8.192MHz, 4.096MHz, or 2.048MHz Clock Output Synthesized to Recovered Network Clock

Features continued in Section 1.

ORDERING INFORMATION

PART	TEMP RANGE	PIN-PACKAGE
DS2156L	0°C to +70°C	100 LQFP
DS2156L+	0°C to +70°C	100 LQFP
DS2156LN	-40°C to +85°C	100 LQFP
DS2156LN+	-40°C to +85°C	100 LQFP
DS2156G	0°C to +70°C	100 CSBGA
DS2156G+	0°C to +70°C	100 CSBGA
DS2156GN	-40°C to +85°C	100 CSBGA
DS2156GN+	-40°C to +85°C	100 CSBGA

+Denotes lead-free/RoHS-compliant package.

Note: *Some revisions of this device may incorporate deviations from published specifications known as errata. Multiple revisions of any device may be simultaneously available through various sales channels. For information about device errata, click here: www.maxim-ic.com/errata.*

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

1. MAIN FEATURES

The DS2156 contains all of the features of the previous generation of Dallas Semiconductor's T1 and E1 SCTs plus many new features such as a UTOPIA bus interface.

General

- Programmable output clocks for fractional T1, E1, H0, and H12 applications
- Interleaving PCM bus operation
- 8-bit parallel control port, multiplexed or nonmultiplexed, Intel or Motorola
- IEEE 1149.1 JTAG-Boundary Scan
- 3.3V supply with 5V tolerant inputs and outputs
- Pin compatible with DS2155, DS2152/DS2154, and DS21x5Y SCT family
- Signaling System 7 Support
- RAI-CI, AIS-CI support
- 100-pin LQFP package (14mm x 14mm) (DS2156)
- 3.3V supply with 5V tolerant inputs and outputs
- LQFP package that is pin compatible with DS2152/DS2154, DS21352/DS21354, DS21552/DS21554, and DS2155
- Evaluation kits
- IEEE 1149.1 JTAG boundary scan
- Driver source code available from the factory

Line Interface

- Requires only a 2.048MHz master clock for both E1 and T1 operation with the option to use 1.544MHz for T1 operation
- Fully software configurable
- Short-haul and long-haul applications
- Automatic receive sensitivity adjustments
- Ranges include 0 to 43dB or 0 to 12dB for E1 applications and 0 to 13dB or 0 to 36dB for T1 applications
- Receive level indication in 2.5dB steps from -42.5dB to -2.5dB
- Internal receive termination option for 75Ω, 100Ω, and 120Ω lines
- Internal transmit termination option for 75Ω, 100Ω, and 120Ω lines
- Monitor application gain settings of 20dB, 26dB, and 32dB
- G.703 receive synchronization-signal mode
- Flexible transmit waveform generation
- T1 DSX-1 line buildouts
- T1 CSU line buildouts of -7.5dB, -15dB, and -22.5dB
- E1 waveforms include G.703 waveshapes for both 75Ω coax and 120Ω twisted cables
- AIS generation independent of loopbacks
- Alternating ones and zeros generation
- Square-wave output
- Open-drain output option
- NRZ format option
- Transmitter power-down
- Transmitter 50mA short-circuit limiter with current-limit-exceeded indication
- Transmit open-circuit-detected indication
- Line interface function can be completely decoupled from the framer/formatter

Clock Synthesizer

- Output frequencies include 2.048MHz, 4.096MHz, 8.192MHz, and 16.384MHz
- Derived from recovered receive clock

Jitter Attenuator

- 32-bit or 128-bit crystal-less jitter attenuator
- Requires only a 2.048MHz master clock for both E1 and T1 operation with the option to use 1.544MHz for T1 operation
- Can be placed in either the receive or transmit path or disabled
- Limit trip indication

Framer/Formatter

- Fully independent transmit and receive functionality
- Full receive and transmit path transparency
- T1 framing formats include D4 (SLC-96) and ESF
- Detailed alarm and status reporting with optional interrupt support
- Large path and line error counters for:
  - T1: BPV, CV, CRC6, and framing bit errors
  - E1: BPV, CV, CRC4, E-bit, and frame alignment errors
- Timed or manual update modes
- DS1 idle code generation on a per-channel basis in both transmit and receive paths
  - User-defined
  - Digital milliwatt
- ANSI T1.403-1998 Support
- RAI-CI detection and generation
- AIS-CI detection and generation
- E1ETS 300 011 RAI generation
- G.965 V5.2 link detect
- Ability to monitor one DS0 channel in both the transmit and receive paths
- In-band repeating pattern generators and detectors
  - Three independent generators and detectors
  - Patterns from 1 to 8 bits or 16 bits in length

- RCL, RLOS, RRA, and RAIS alarms interrupt on change-of-state
- Flexible signaling support
  - Software or hardware based
  - Interrupt generated on change of signaling data
  - Receive signaling freeze on loss-of-sync, carrier loss, or frame slip
- Addition of hardware pins to indicate carrier loss and signaling freeze
- Automatic RAI generation to ETS 300 011 specifications
- Access to Sa and Si bits
- Option to extend carrier loss criteria to a 1ms period as per ETS 300 233
- Japanese J1 support
  - Ability to calculate and check CRC6 according to the Japanese standard
  - Ability to generate Yellow Alarm according to the Japanese standard

TDM Bus

- Dual two-frame independent receive and transmit elastic stores
  - Independent control and clocking
  - Controlled slip capability with status
  - Minimum delay mode supported
- 16.384MHz maximum backplane burst rate
- Supports T1 to CEPT (E1) conversion
- Programmable output clocks for fractional T1, E1, H0, and H12 applications
- Interleaving PCM bus operation
- Hardware signaling capability
  - Receive signaling reinsertion to a backplane multiframe sync
  - Availability of signaling in a separate PCM data stream
  - Signaling freezing
- Ability to pass the T1 F-bit position through the elastic stores in the 2.048MHz backplane mode
- Access to the data streams in between the framer/formatter and the elastic stores
- User-selectable synthesized clock output

UTOPIA Bus

- Supports fractional T1/E1 and arbitrary bit rates in multiples of 64kbps (DS0/TS) up to 2.048Mbps
- Supports clear E1
- Compliant to the ATM forum specifications for ATM over DS1 and E1, respectively
- Standard UTOPIA-II interface to the ATM layer
- Configurable UTOPIA address
- Supports diagnostic loopback
- Optional payload scrambling in transmit direction and descrambling in receive direction as per the ITU I.432 for the cell-based physical layer
- Optional HEC insertion in transmit direction with programmable COSET polynomial addition
- Option of using either idle or unassigned cells for cell-rate decoupling in transmit direction
- 1-Byte programmable pattern for payload of cells used for cell-rate decoupling
- Transmit FIFO depth configurable to either 2, 3, 4 cell deep, which provides control over cell latency
- Transmit FIFO depth indication for 2-cell space
- Optional single-bit HEC error insertion
- HEC-based cell delineation
- Optional single-bit HEC error correction in the receive direction
- Optional filtering of HEC errored cells received
- Optional receive idle/unassigned cell filtering
- Programmable loss-of-cell delineation (LCD) integration and optional interrupt
- Interrupt for FIFO overrun in receive direction
- Saturating counts for:
  - Number of error-free assigned cells received and transmitted
  - Number of correctable and uncorrectable HEC-errored cells received
- Optional internally generated clock (system clock divided by 8) in diagnostic loopback mode

HDLC Controllers

- Two independent HDLC controllers
- Fast load and unload features for FIFOs
- SS7 support for FISU transmit and receive
- Independent 128-byte Rx and Tx buffers with interrupt support
- Access FDL, Sa, or single/multiple DS0 channels
- DS0 access includes Nx64 or Nx56
- Compatible with polled or interrupt driven environments
- Bit-oriented code (BOC) support

Test and Diagnostics

- Programmable on-chip bit error-rate testing
- Pseudorandom patterns including QRSS
- User-defined repetitive patterns
- Daly pattern
- Error insertion single and continuous
- Total bit and errored bit counts
- Payload error insertion
- Error insertion in the payload portion of the T1 frame in the transmit path
- Errors can be inserted over the entire frame or selected channels
- Insertion options include continuous and absolute number with selectable insertion rates
- F-bit corruption for line testing

- Loopbacks: remote, local, analog, and per-channel loopback

Extended System Information Bus

- Host can read interrupt and alarm status on up to 8 ports with a single bus read

User-Programmable Output Pins

- Four user-defined output pins for controlling external logic

Control Port

- 8-bit parallel control port
- Multiplexed or nonmultiplexed buses
- Intel or Motorola formats
- Supports polled or interrupt environments
- Software access to device ID and silicon revision
- Software reset supported
  - Automatic clear on power-up
- Hardware reset pin

The DS2156 is compliant with the following standards:

ANSI:	T1.403-1995, T1.231–1993, T1.408
AT&T:	TR54016, TR62411
ITU:	G.703, G.704, G.706, G.736, G.775, G.823, G.932, I.431, O.151, Q.161
ITU-T:	Recommendation I.432–03/93 B-ISDN User-Network Interface—Physical Layer Specification
ETSI:	ETS 300 011, ETS 300 166, ETS 300 233, CTR12, CTR4
Japanese:	JTG.703, JTI.431, JJ-20.11 (CMI Coding Only)
ATM Forum:	“DS1 Physical Layer Specification,” af-phy-0016.000, September 1994
ATM Forum:	“E1 Physical Layer Specification,” af-phy-0064.000, September 1996
ATM Forum:	“UTOPIA Level 2 Specification,” Version 1.0, af-phy-0039.000, June 1995

2. DETAILED DESCRIPTION

The DS2156 is a software-selectable T1, E1, or J1 single-chip transceiver (SCT) for short-haul and long-haul applications. The backplane is user-configurable for a TDM or UTOPIA II bus interface. The DS2156 is composed of an LIU, framer, HDLC controllers, and a UTOPIA/TDM backplane interface, and is controlled by an 8-bit parallel port configured for Intel or Motorola bus operations. The DS2156 is pin and software compatible with the DS2155.

The LIU is composed of transmit and receive interfaces and a jitter attenuator. The transmit interface is responsible for generating the necessary waveshapes for driving the network and providing the correct source impedance depending on the type of media used. T1 waveform generation includes DSX-1 line buildouts as well as CSU line buildouts of -7.5dB, -15dB, and -22.5dB. E1 waveform generation includes G.703 waveshapes for both 75Ω coax and 120Ω twisted cables. The receive interface provides network termination and recovers clock and data from the network. The receive sensitivity adjusts automatically to the incoming signal and can be programmed for 0 to 43dB or 0 to 12dB for E1 applications and 0 to 30dB or 0 to 36dB for T1 applications. The jitter attenuator removes phase jitter from the transmitted or received signal. The crystal-less jitter attenuator requires only a 2.048MHz MCLK for both E1 and T1 applications (with the option of using a 1.544MHz MCLK in T1 applications) and can be placed in either transmit or receive data paths. An additional feature of the LIU is a CMI coder/decoder for interfacing to optical networks.

On the transmit side, clock, data, and frame-sync signals are provided to the framer by the backplane interface section. The framer inserts the appropriate synchronization framing patterns, alarm information, calculates and inserts the CRC codes, and provides the B8ZS/HDB3 (zero code suppression) and AMI line coding. The receive-side framer decodes AMI, B8ZS, and HDB3 line coding, synchronizes to the data stream, reports alarm information, counts framing/coding/CRC errors, and provides clock/data and frame-sync signals to the backplane interface section.

Both the transmit and receive path have two HDLC controllers. The HDLC controllers transmit and receive data through the framer block. The HDLC controllers can be assigned to any time slot, group of time slots, portion of a time slot or to FDL (T1) or Sa bits (E1). Each controller has 128-byte FIFOs, thus reducing the amount of processor overhead required to manage the flow of data. In addition, built-in support for reducing the processor time is required in SS7 applications.

The backplane interface provides a versatile method of sending and receiving data from the host system. Elastic stores provide a method for interfacing to asynchronous systems, converting from a T1/E1 network to a 2.048MHz, 4.096MHz, 8.192MHz, or N x 64kHz system backplane. The elastic stores also manage slip conditions (asynchronous interface). An interleave bus option (IBO) is provided to allow up to eight transceivers to share a high-speed backplane in TDM mode.

The parallel port provides access for control and configuration of the DS2156's features. The extended system information bus (ESIB) function allows up to eight transceivers to be accessed by a single read for interrupt status or other user-selectable alarm status information. Diagnostic capabilities include loopbacks, PRBS pattern generation/detection, and 16-bit loop-up and loop-down code generation and detection.

Reader's Note: This data sheet assumes a particular nomenclature of the T1 operating environment. In each 125µs frame there are 24 8-bit channels plus a framing bit. It is assumed that the framing bit is sent first followed by channel 1. Each channel is made up of eight bits that are numbered 1 to 8. Bit number 1 is the MSB and is transmitted first. Bit number 8 is the LSB and is transmitted last. The term "locked" is used to refer to two clock signals that are phase- or frequency-locked or derived from a common clock (i.e., a 1.544MHz clock can be locked to a 2.048MHz clock if they share the same 8kHz component). Throughout this data sheet, the following abbreviations are used:

B8ZS	Bipolar with 8 Zero Substitution
BOC	Bit-Oriented Code
CRC	Cyclical Redundancy Check
D4	Superframe (12 frames per multiframe) Multiframe Structure
ESF	Extended Superframe (24 frames per multiframe) Multiframe Structure
FDL	Facility Data Link
FPS	Framing Pattern Sequence in ESF
Fs	Signaling Framing Pattern in D4
Ft	Terminal Framing Pattern in D4
HDLC	High-Level Data Link Control
MF	Multiframe
SLC–96	Subscriber Loop Carrier—96 Channels

2.1 Block Diagram

Figure 2-1 shows a simplified block diagram featuring the major components of the DS2156. Details are shown in subsequent figures. About 30 device pins have dual functions depending on the selection of the backplane, UTOPIA, or TDM. Some of the block diagrams depict a configuration based on the state of the backplane selection. The block diagram is divided into three functional blocks: LIU, FRAMER, and BACKPLANE INTERFACE.

Figure 2-1. Block Diagram

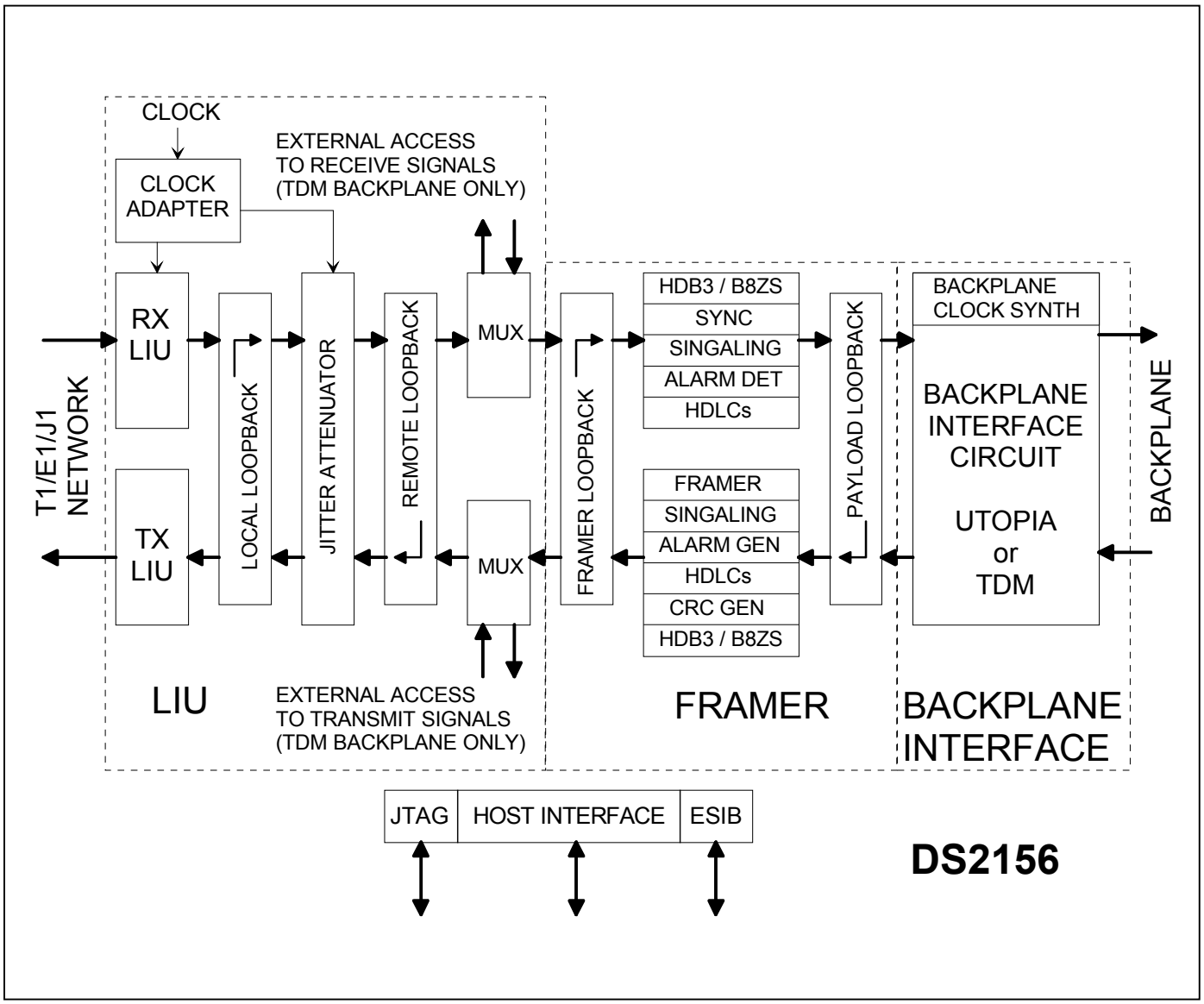


Figure 2-2. Receive and Transmit LIU (TDM Backplane Enabled)

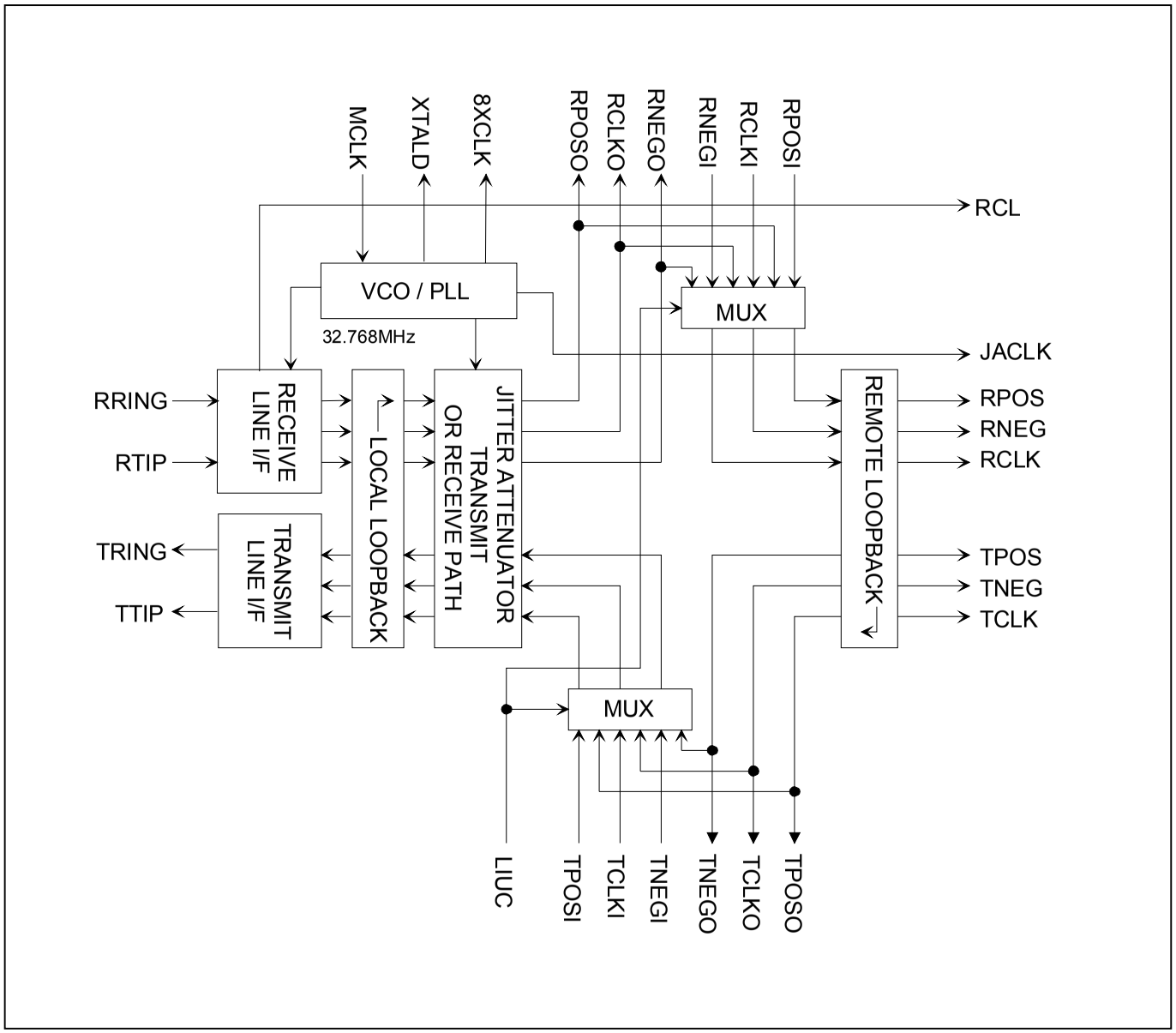


Figure 2-3. Receive and Transmit LIU (UTOPIA Backplane Enabled)

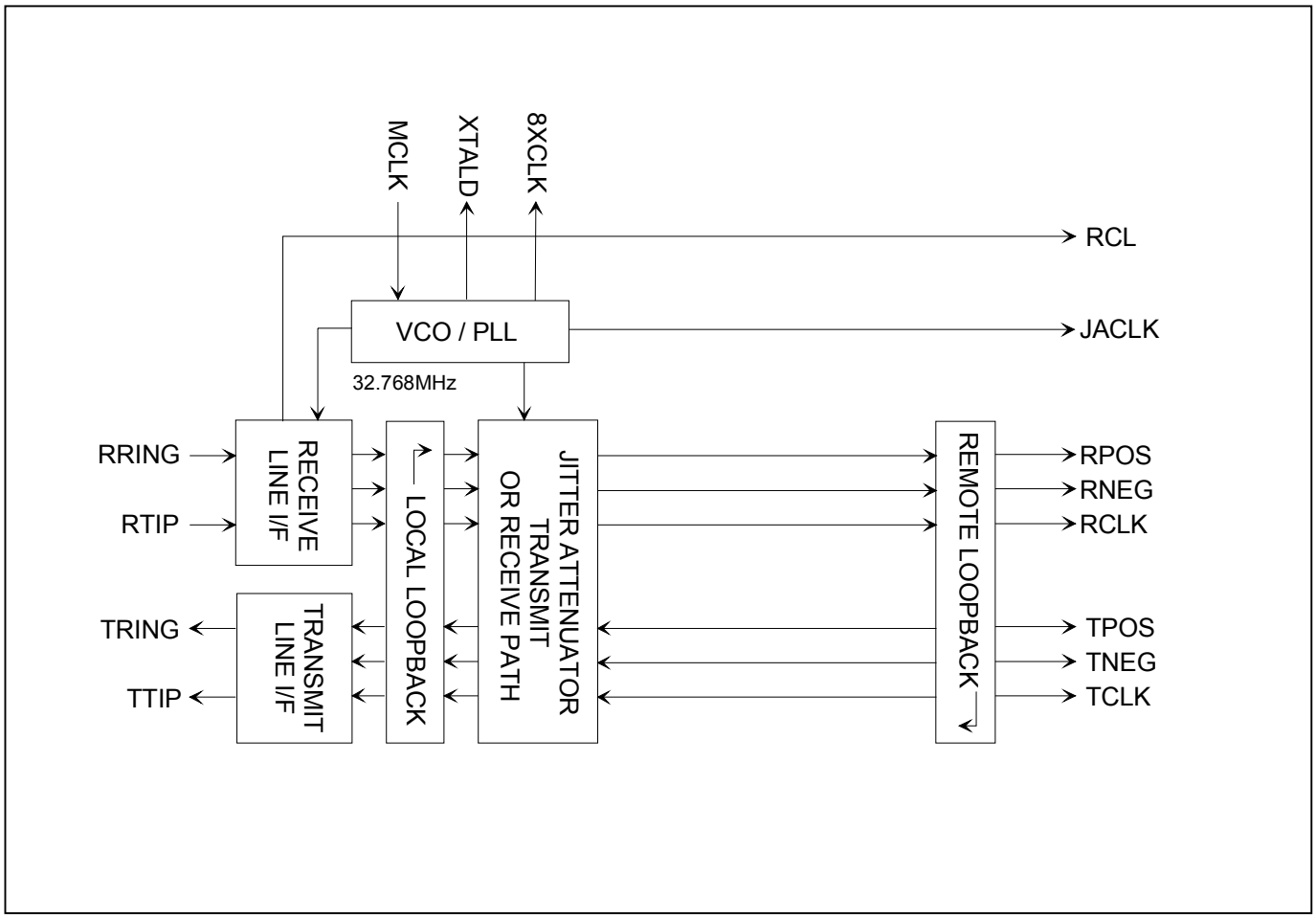


Figure 2-4. Receive and Transmit Framer/HDLC

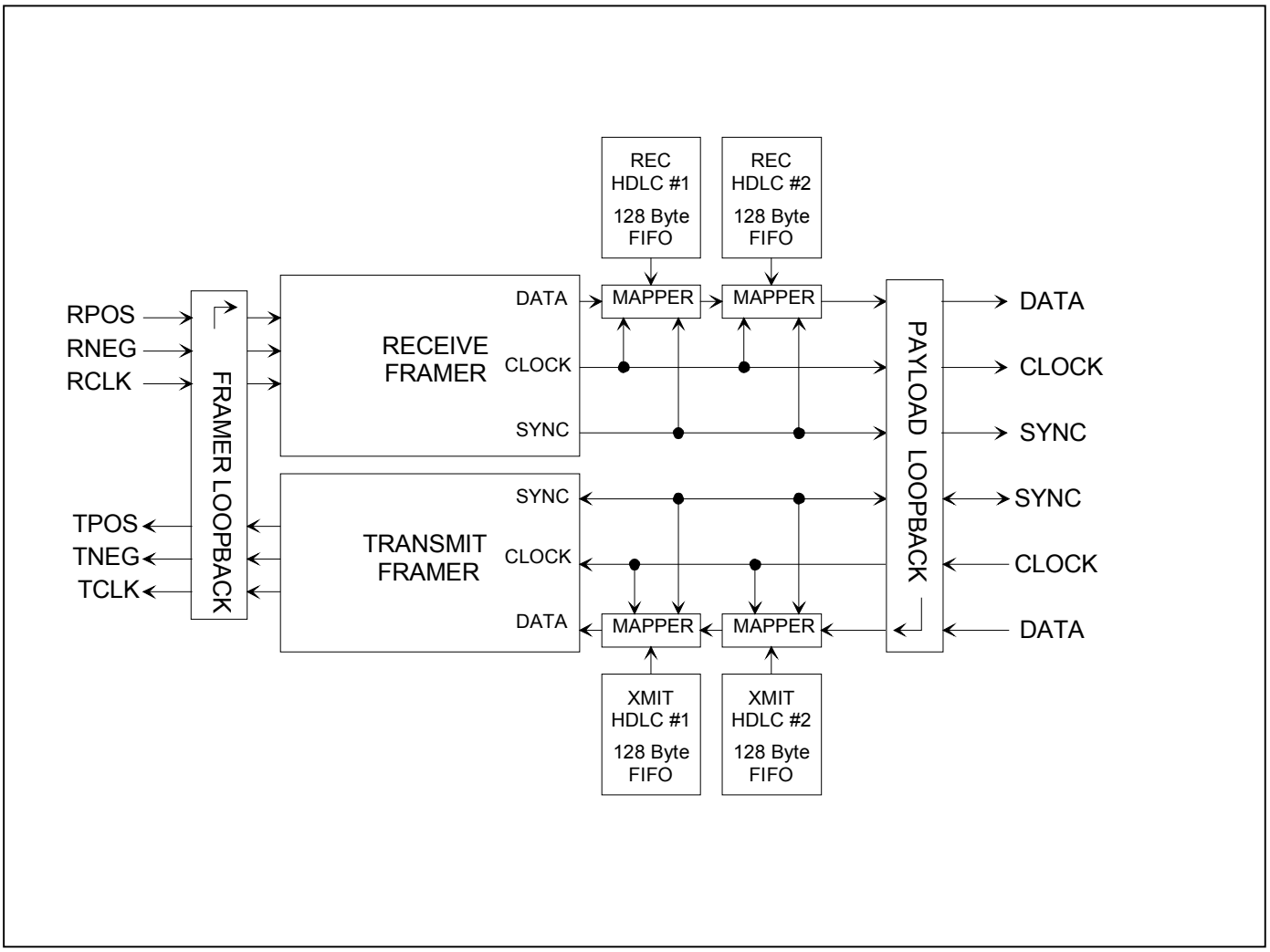


Figure 2-5. Backplane Interface (TDM Backplane Enabled)

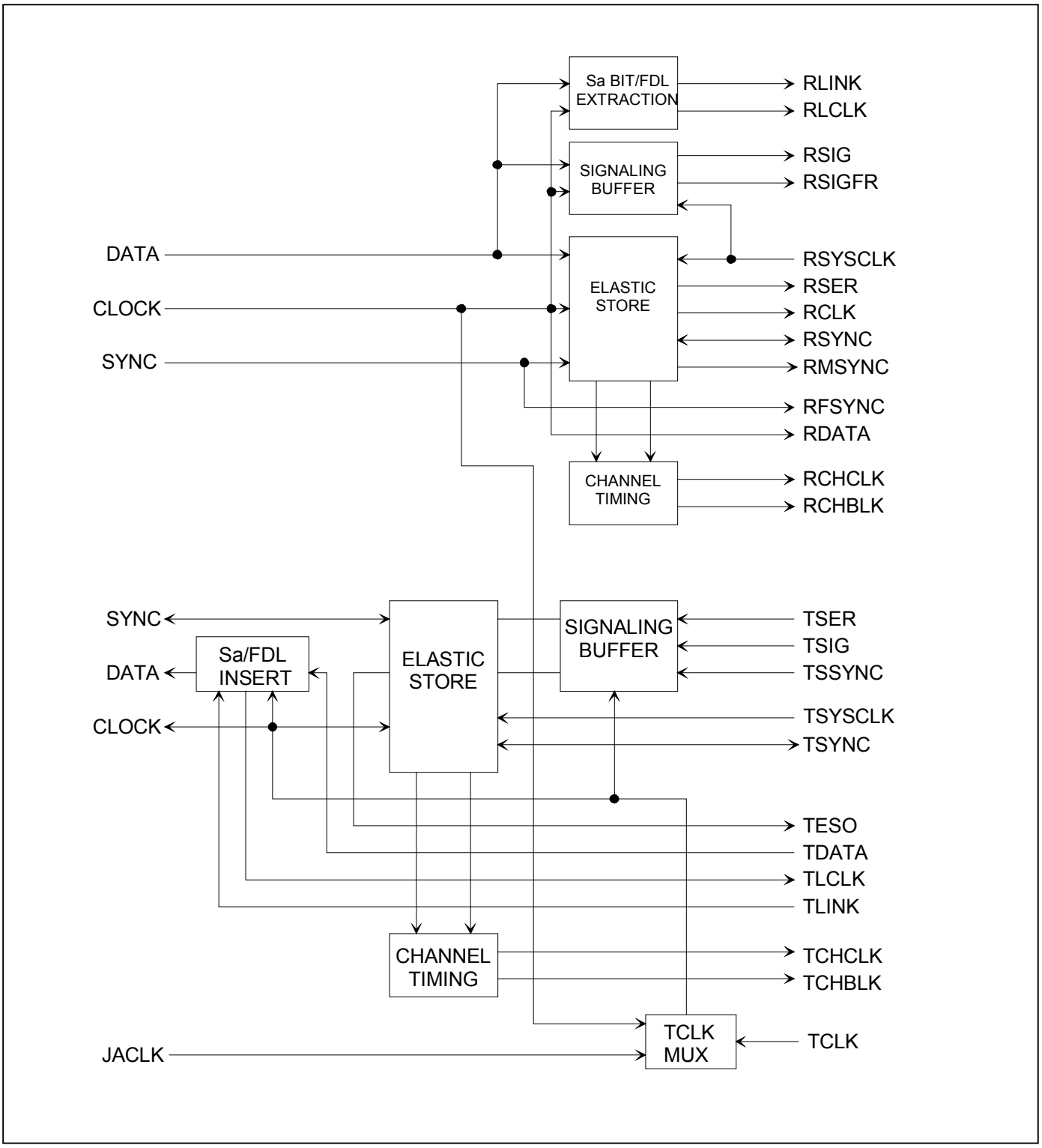
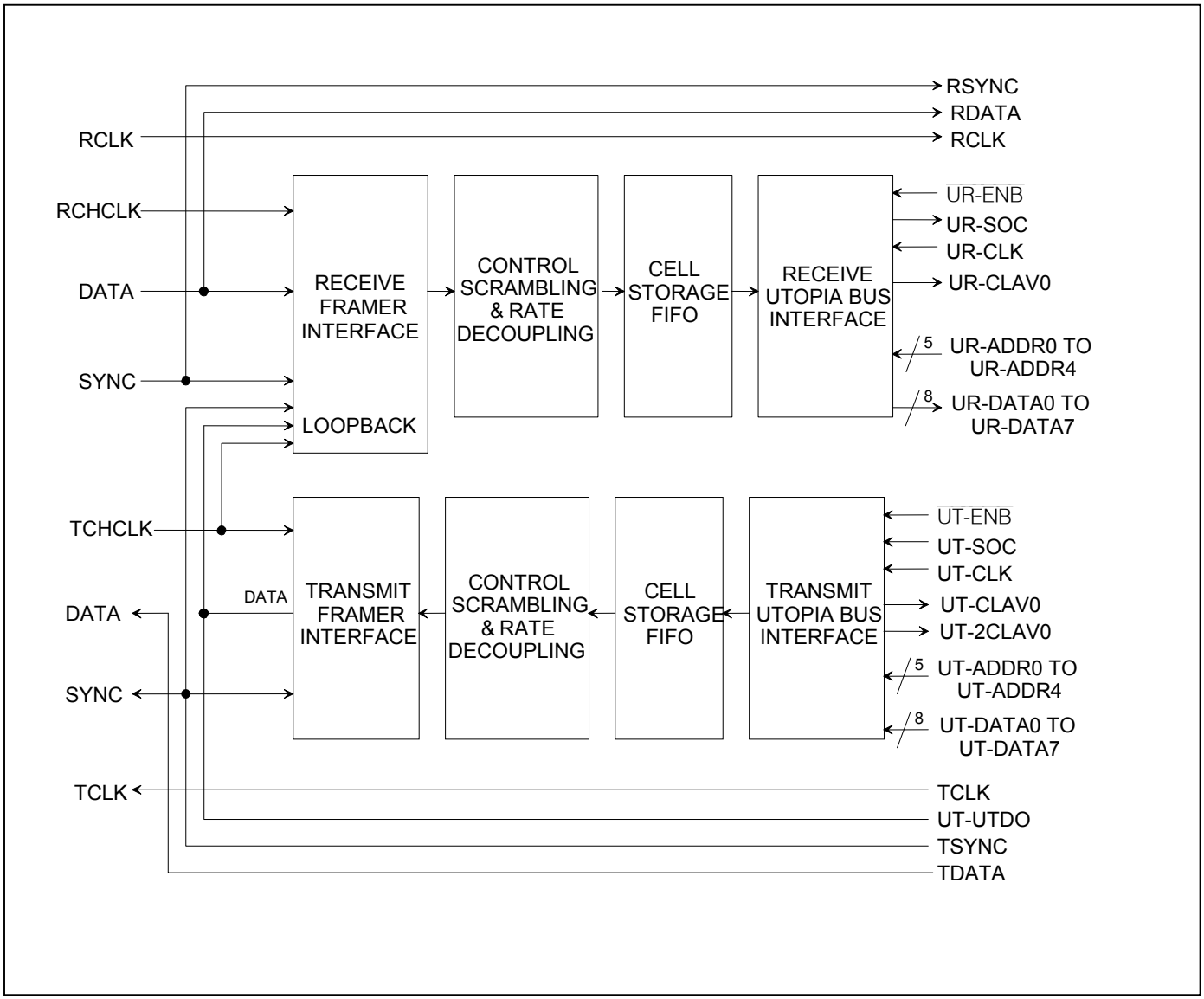


Figure 2-6. Backplane Interface (UTOPIA Bus Enabled)



3. PIN FUNCTION DESCRIPTION

The DS2156 has a user-selectable TDM or UTOPIA backplane. Table 3-A and Table 3-B indicate which pins have alternate functions depending on the backplane selected. Note that even when the UTOPIA backplane is selected, the basic TDM signals such as clock, data, and frame-sync are available for both the transmit and receive directions.

3.1 TDM Backplane

3.1.1 Transmit Side

Signal Name: **TCLK**
Signal Description: **Transmit Clock**
Signal Type: **Input**
A 1.544MHz (T1) or a 2.048MHz (E1) primary clock. Used to clock data through the transmit-side formatter. TCLK can be internally sourced from MCLK. This is the most flexible method and requires only a single clock signal for both T1 or E1. If internal sourcing is used, then the TCLK pin should be connected low.

Signal Name: **TSER**
Signal Description: **Transmit Serial Data**
Signal Type: **Input**
Transmit NRZ serial data. Sampled on the falling edge of TCLK when the transmit-side elastic store is disabled. Sampled on the falling edge of TSYSCLK when the transmit-side elastic store is enabled.

Signal Name: **TCHCLK**
Signal Description: **Transmit Channel Clock**
Signal Type: **Output**
A 192kHz (T1) or 256kHz (E1) clock that pulses high during the LSB of each channel. Can also be programmed to output a gated transmit bit clock on a per-channel basis. Synchronous with TCLK when the transmit-side elastic store is disabled. Synchronous with TSYSCLK when the transmit-side elastic store is enabled. Useful for parallel-to-serial conversion of channel data.

Signal Name: **TCHBLK**
Signal Description: **Transmit Channel Block**
Signal Type: **Output**
A user-programmable output that can be forced high or low during any of the channels. Synchronous with TCLK when the transmit-side elastic store is disabled. Synchronous with TSYSCLK when the transmit-side elastic store is enabled. Useful for blocking clocks to a serial UART or LAPD controller in applications where not all channels are used such as Fractional T1, Fractional E1, 384kbps (H0), 768kbps, or ISDN–PRI. Also useful for locating individual channels in drop-and-insert applications, for external per-channel loopback, and for per-channel conditioning.

Signal Name: **TSYSCLK**
Signal Description: **Transmit System Clock**
Signal Type: **Input**
1.544MHz, 2.048MHz, 4.096MHz, 8.192MHz, or 16.384MHz clock. Only used when the transmit-side elastic store function is enabled. Should be connected low in applications that do not use the transmit-side elastic store. See Section 28 for details on 4.096MHz, 8.192MHz, and 16.384MHz operation using the IBO.

Signal Name: **TLCLK**
Signal Description: **Transmit Link Clock**
Signal Type: **Output**
Demand clock for the transmit link data [TLINK] input.
T1 Mode: A 4kHz or 2kHz (ZBTSI) clock.
E1 Mode: A 4kHz to 20kHz clock.

Signal Name: **TLINK**
Signal Description: **Transmit Link Data**
Signal Type: **Input**
If enabled, this pin is sampled on the falling edge of TCLK for data insertion into either the FDL stream (ESF) or the Fs-bit position (D4), or the Z-bit position (ZBTSI) or any combination of the Sa-bit positions (E1).

Signal Name: **TSYNC**
Signal Description: **Transmit Sync**
Signal Type: **Input/Output**
A pulse at this pin establishes either frame or multiframe boundaries for the transmit side. Can be programmed to output either a frame or multiframe pulse. If this pin is set to output pulses at frame boundaries, it can also be set by IOCR1.3 to output double-wide pulses at signaling frames in T1 mode.

Signal Name: **TSSYNC**
Signal Description: **Transmit System Sync**
Signal Type: **Input**
Only used when the transmit-side elastic store is enabled. A pulse at this pin establishes either frame or multiframe boundaries for the transmit side. Should be connected low in applications that do not use the transmit-side elastic store.

Signal Name: **TSIG**
Signal Description: **Transmit Signaling Input**
Signal Type: **Input**
When enabled, this input samples signaling bits for insertion into outgoing PCM data stream. Sampled on the falling edge of TCLK when the transmit-side elastic store is disabled. Sampled on the falling edge of TSYSCLK when the transmit-side elastic store is enabled.

Signal Name: **TESO**
Signal Description: **Transmit Elastic Store Data Output**
Signal Type: **Output**
Updated on the rising edge of TCLK with data out of the transmit-side elastic store whether the elastic store is enabled or not. This pin is normally connected to TDATA.

Signal Name: **TDATA**
Signal Description: **Transmit Data**
Signal Type: **Input**
Sampled on the falling edge of TCLK with data to be clocked through the transmit-side formatter. This pin is normally connected to TESO.

Signal Name: **TPOSO**
Signal Description: **Transmit Positive-Data Output**
Signal Type: **Output**
Updated on the rising edge of TCLKO with the bipolar data out of the transmit-side formatter. Can be programmed to source NRZ data by the output data format (IOCR1.0) control bit. This pin is normally connected to TPOSI.

Signal Name: **TNEGO**
Signal Description: **Transmit Negative-Data Output**
Signal Type: **Output**
Updated on the rising edge of TCLKO with the bipolar data out of the transmit-side formatter. This pin is normally connected to TNEGI.

Signal Name: **TCLKO**
Signal Description: **Transmit Clock Output**
Signal Type: **Output**
Buffered clock that is used to clock data through the transmit-side formatter (i.e., either TCLK or RCLKI). This pin is normally connected to TCLKI.

Signal Name: **TPOSI**
Signal Description: **Transmit Positive-Data Input**
Signal Type: **Input**
Sampled on the falling edge of TCLKI for data to be transmitted out onto the T1 line. Can be internally connected to TPOSO by connecting the LIUC pin high. TPOSI and TNEGI can be connected together in NRZ applications.

Signal Name: **TNEGI**
Signal Description: **Transmit Negative-Data Input**
Signal Type: **Input**
Sampled on the falling edge of TCLKI for data to be transmitted out onto the T1 line. Can be internally connected to TNEGO by connecting the LIUC pin high. TPOSI and TNEGI can be connected together in NRZ applications.

Signal Name: **TCLKI**
Signal Description: **Transmit Clock Input**
Signal Type: **Input**
Line interface transmit clock. Can be internally connected to TCLKO by connecting the LIUC pin high.

3.1.2 Receive Side

Signal Name: **RLINK**
Signal Description: **Receive Link Data**
Signal Type: **Output**
T1 Mode: Updated with either FDL data (ESF) or Fs bits (D4) or Z bits (ZBTSI) one RCLK before the start of a frame.
E1 Mode: Updated with the full E1 data stream on the rising edge of RCLK.

Signal Name: **RLCLK**
Signal Description: **Receive Link Clock**
Signal Type: **Output**
T1 Mode: A 4kHz or 2kHz (ZBTSI) clock for the RLINK output.
E1 Mode: A 4kHz to 20kHz clock.

Signal Name: **RCLK**
Signal Description: **Receive Clock**
Signal Type: **Output**
1.544MHz (T1) or 2.048MHz (E1) clock that is used to clock data through the receive-side framer.

Signal Name: **RCHCLK**
Signal Description: **Receive Channel Clock**
Signal Type: **Output**
A 192kHz (T1) or 256kHz (E1) clock that pulses high during the LSB of each channel. Synchronous with RCLK when the receive-side elastic store is disabled. Synchronous with RSYSCLK when the receive-side elastic store is enabled. Useful for parallel-to-serial conversion of channel data.

Signal Name: **RCHBLK**
Signal Description: **Receive Channel Block**
Signal Type: **Output**
A user-programmable output that can be forced high or low during any of the 24 T1 or 32 E1 channels. Synchronous with RCLK when the receive-side elastic store is disabled. Synchronous with RSYSCLK when the receive-side elastic store is enabled. Useful for blocking clocks to a serial UART or LAPD controller in applications where not all channels are used such as fractional service, 384kbps service, 768kbps, or ISDN–PRI. Also useful for locating individual channels in drop-and-insert applications, for external per-channel loopback, and for per-channel conditioning. See Section 17 for details.

Signal Name: **RSER**
Signal Description: **Receive Serial Data**
Signal Type: **Output**
Received NRZ serial data. Updated on rising edges of RCLK when the receive-side elastic store is disabled. Updated on the rising edges of RSYSCLK when the receive-side elastic store is enabled.

Signal Name: **RSYNC**
Signal Description: **Receive Sync**
Signal Type: **Input/Output**
An extracted pulse, one RCLK wide, is output at this pin that identifies either frame (IOCR1.5 = 0) or multiframe (IOCR1.5 = 1) boundaries. If set to output frame boundaries, then through IOCR1.6, RSYNC can also be set to output double-wide pulses on signaling frames in T1 mode. If the receive-side elastic store is enabled, then this pin can be enabled to be an input through IOCR1.4, at which a frame or multiframe boundary pulse is applied.

Signal Name: **RFSYNC**
Signal Description: **Receive Frame Sync**
Signal Type: **Output**
An extracted 8kHz pulse, one RCLK wide, is output at this pin that identifies frame boundaries.

Signal Name: **RMSYNC**
Signal Description: **Receive Multiframe Sync**
Signal Type: **Output**
An extracted pulse, one RCLK wide (elastic store disabled) or one RSYSCLK wide (elastic store enabled), is output at this pin that identifies multiframe boundaries.

Signal Name: **RDATA**
Signal Description: **Receive Data**
Signal Type: **Output**
Updated on the rising edge of RCLK with the data out of the receive-side framer.

Signal Name: **RSYSCLK**
Signal Description: **Receive System Clock**
Signal Type: **Input**
1.544MHz, 2.048MHz, 4.096MHz, or 8.192MHz clock. Only used when the receive-side elastic store function is enabled. Should be connected low in applications that do not use the receive-side elastic store. See Section 28 for details on 4.096MHz and 8.192MHz operation using the IBO.

Signal Name: **RSIG**
Signal Description: **Receive Signaling Output**
Signal Type: **Output**
Outputs signaling bits in a PCM format. Updated on rising edges of RCLK when the receive-side elastic store is disabled. Updated on the rising edges of RSYSCLK when the receive-side elastic store is enabled.

Signal Name: **RLOS/LOTC**
Signal Description: **Receive Loss-of-Sync/Loss-of-Transmit Clock**
Signal Type: **Output**
A dual function output that is controlled by the CCR1.0 control bit. This pin can be programmed to either toggle high when the synchronizer is searching for the frame and multiframe or to toggle high if the TCLK pin has not been toggled for 5µs.

Signal Name: **RCL**
Signal Description: **Receive Carrier Loss**
Signal Type: **Output**
Set high when the line interface detects a carrier loss.

Signal Name: **RSIGF**
Signal Description: **Receive Signaling Freeze**
Signal Type: **Output**
Set high when the signaling data is frozen by either automatic or manual intervention. Used to alert downstream equipment of the condition.

Signal Name: **BPCLK**
Signal Description: **Backplane Clock**
Signal Type: **Output**
A user-selectable synthesized clock output that is referenced to the clock that is output at the RCLK pin.

Signal Name: **RPOSO**
Signal Description: **Receive Positive-Data Output**
Signal Type: **Output**
Updated on the rising edge of RCLKO with bipolar data out of the line interface. This pin is normally connected to RPOSI.

Signal Name: **RNEGO**
Signal Description: **Receive Negative-Data Output**
Signal Type: **Output**
Updated on the rising edge of RCLKO with the bipolar data out of the line interface. This pin is normally connected to RPOSI.

Signal Name: **RCLKO**
Signal Description: **Receive Clock Output**
Signal Type: **Output**
Buffered recovered clock from the network. This pin is normally connected to RCLKI.

Signal Name: **RPOSI**
Signal Description: **Receive Positive-Data Input**
Signal Type: **Input**
Sampled on the falling edge of RCLKI for data to be clocked through the receive-side framer. RPOSI and RNEGI can be connected together for an NRZ interface. Can be internally connected to RPOSO by connecting the LIUC pin high.

Signal Name: **RNEGI**
Signal Description: **Receive Negative-Data Input**
Signal Type: **Input**
Sampled on the falling edge of RCLKI for data to be clocked through the receive-side framer. RPOSI and RNEGI can be connected together for an NRZ interface. Can be internally connected to RNEGO by connecting the LIUC pin high.

Signal Name: **RCLKI**
Signal Description: **Receive Clock Input**
Signal Type: **Input**
Clock used to clock data through the receive-side framer. This pin is normally connected to RCLKO. Can be internally connected to RCLKO by connecting the LIUC pin high.