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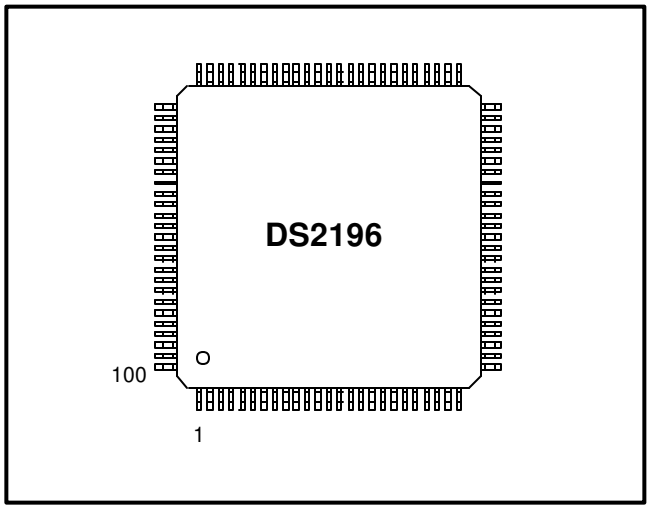
DS2196
T1 Dual Framer LIU

www.maxim-ic.com

GENERAL DESCRIPTION

The DS2196 T1 dual framer LIU is designed for T1 transmission equipment. The DS2196 combines dual optimized framers together with a LIU. This combination allows the users to extract and insert facility data-link (FDL) messages in the receive and transmit paths, collect line performance data, and perform basic channel conditioning and maintenance. The DS2196 contains all of the necessary functions for connection to T1 lines whether they are DS1 long haul or DSX–1 short haul. The clock recovery circuitry automatically adjusts to T1 lines from 0ft to over 6000ft in length. The device can generate both DSX–1 line buildouts as well as CSU line buildouts of -7.5dB, -15dB, and -22.5dB. The on-board jitter attenuator (selectable to either 32 bits or 128 bits) can be placed in either the transmit or receive data paths. The framer locates the frame and multiframe boundaries and monitors the data stream for alarms. The device contains a set of internal registers that the user can access and use to control the unit's operation of the unit. Quick access through the parallel control port allows a single controller to handle many T1 lines. The device fully meets all of the latest T1 specifications.

PACKAGE OUTLINE



FEATURES

- Two full-featured framers and a short/long-haul line interface unit (LIU) in one small package
- Based on Dallas Semiconductor's single-chip transceiver (SCT) family
- Two HDLC controllers with 64-byte buffers that can be used for the FDL or DS0 channels
- Supports NPRMs and SPRMs as per ANSI T1.403-1998
- Can be combined with a short/long-haul LIU or a HDSL modem chipset to create a low-cost office repeater/NIU/CSU, or a HDSL1/HDSL2 terminal unit with enhanced monitoring and data link control
- Supports fractional T1
- Can convert from D4 to ESF framing and ESF to D4 framing
- 32-bit or 128-bit crystal-less jitter attenuator
- Can generate and detect repeating in-band patterns from 1 to 8 bits or 16 bits in length
- Detects and generates RAI-CI and AIS-CI
- Generates DS1 idle codes
- On-chip programmable BERT generator and detector
- All key signals are routed to pins to support numerous hardware configurations
- Supports both NRZ and bipolar interfaces
- Can create errors in the F-bit position and BERT interface data paths
- 8-bit parallel control port that can be used directly on either multiplexed or nonmultiplexed buses (Intel or Motorola)
- IEEE 1149.1 JTAG Boundary Scan
- 3.3V supply with 5V tolerant inputs and outputs
- 100-pin LQFP (14 mm x 14 mm) package

ORDERING INFORMATION

PART	TEMP RANGE	PIN-PACKAGE
DS2196L	0ºC to +70ºC	100 LQFP
DS2196LN	-40ºC to +85ºC	100 LQFP

Note: *Some revisions of this device may incorporate deviations from published specifications known as errata. Multiple revisions of any device may be simultaneously available through various sales channels. For information about device errata, click here: www.maxim-ic.com/errata.*

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

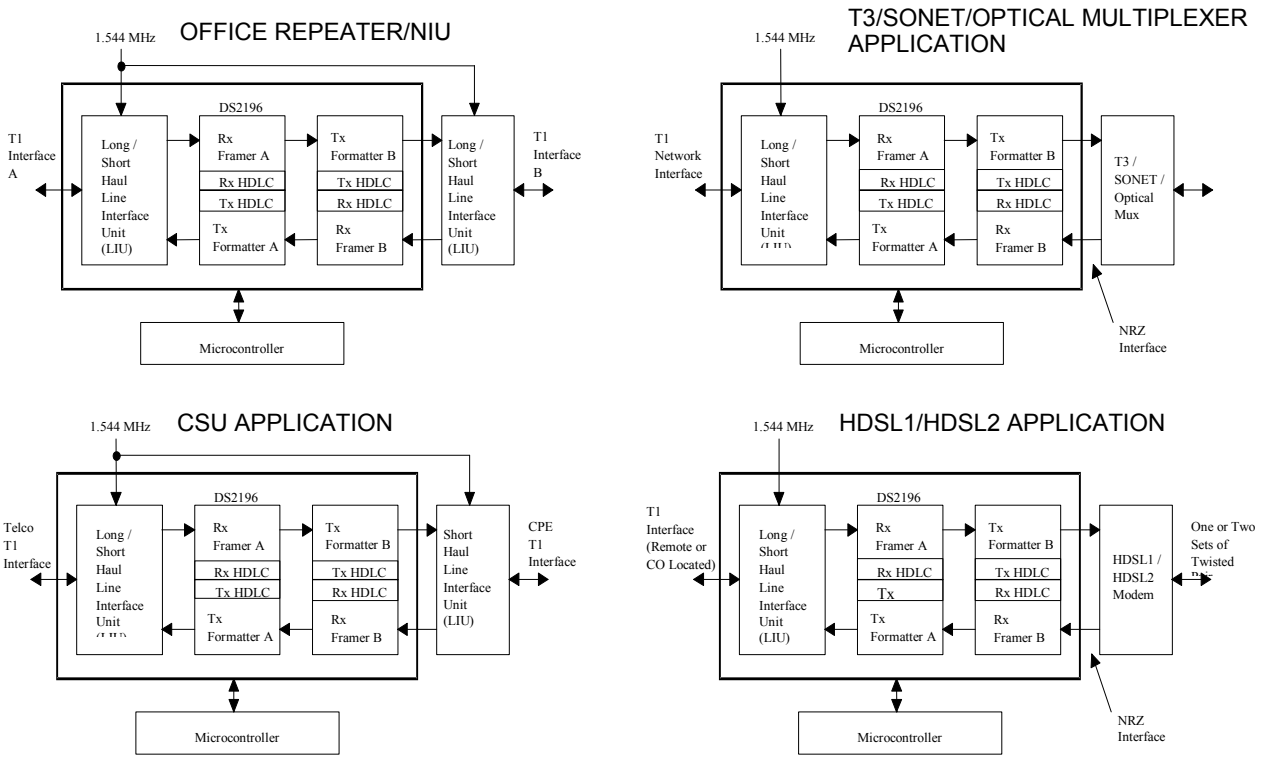
1. INTRODUCTION

The DS2196 is a derivative of the DS21352 T1 SCT. The feature set has been optimized for transport applications commonly found in T1 transmission equipment. The DS2196 register map and register bit definitions are compatible with the DS21352/DS21552, allowing for easy migration to the DS2196. Interface designs requiring per-channel code insertion, elastic stores, and ANSI 1's density monitoring should use the DS21352 or DS21552.

1.1 Feature Highlights

- Main features
  - Two full-featured independent framers
  - Short/long haul LIU
  - 100-pin LQFP small package
  - 3.3V operation with 5V tolerant I/O
- 8-bit parallel control port
  - Multiplexed or nonmultiplexed buses
  - Intel or Motorola formats
  - Polled or interrupt environments
- HDLC Support
  - Two independent HDLC controllers
  - 64-byte Rx and Tx buffers
  - Access FDL or single/multiple DS0 channels
- ANSI T1.403-1998 support
  - NPRMs
  - SPRMs
  - RAI-CI detection and generation
  - AIS-CI detection and generation
- Format Conversion
  - D4 to ESF framing
  - ESF to D4 framing
- LIU
  - Long and short-haul support
  - Receive sensitivity: 0dB to -36dB
  - 32-bit or 128-bit crystal-less jitter attenuator
  - DSX-1 and CSU line buildout options
  - Provisions for custom waveform generation
- DS1 Idle Code Generation
  - User-defined
  - Fixed 7F Hex
  - Digital milliwatt
- In-band repeating pattern generator and detector
  - Programmable pattern generator
  - Three programmable pattern detectors
  - Patterns from 1 to 8 bits or 16 bits in length
- Programmable on-chip bit error-rate testing
  - Pseudorandom patterns including QRSS
  - User-defined repetitive patterns
  - Daly pattern
  - Error insertion
  - Bit and error counts
- Payload Error Insertion
  - Error insertion in the payload portion of the T1 frame in the transmit path
  - Errors can be inserted over the entire frame or selected channels
  - Insertion options include continuous and absolute number with selectable insertion rates
- Function Isolation
  - All key signals are routed to pins
  - LIU, Framer A, and Framer B can be disconnected from each other
- Supports both NRZ and bipolar interfaces
- F-bit corruption for line testing
- Programmable output clocks for Fractional T1
- Fully independent transmit and receive functionality in each framer
- Large path and line error counters including BPV, CV, CRC6, and framing bit errors
- Ability to calculate and check CRC6 according to the Japanese standard
- Ability to generate Yellow Alarm according to the Japanese standard
- Per channel loopback
- RCL, RLOS, RRA, and RAIS alarms interrupt on change of state
- Hardware pins to indicate receive loss-of-sync and receive bipolar violations
- IEEE 1149.1 JTAG Boundary Scan

1.2 Typical Applications



1.3 Functional Description

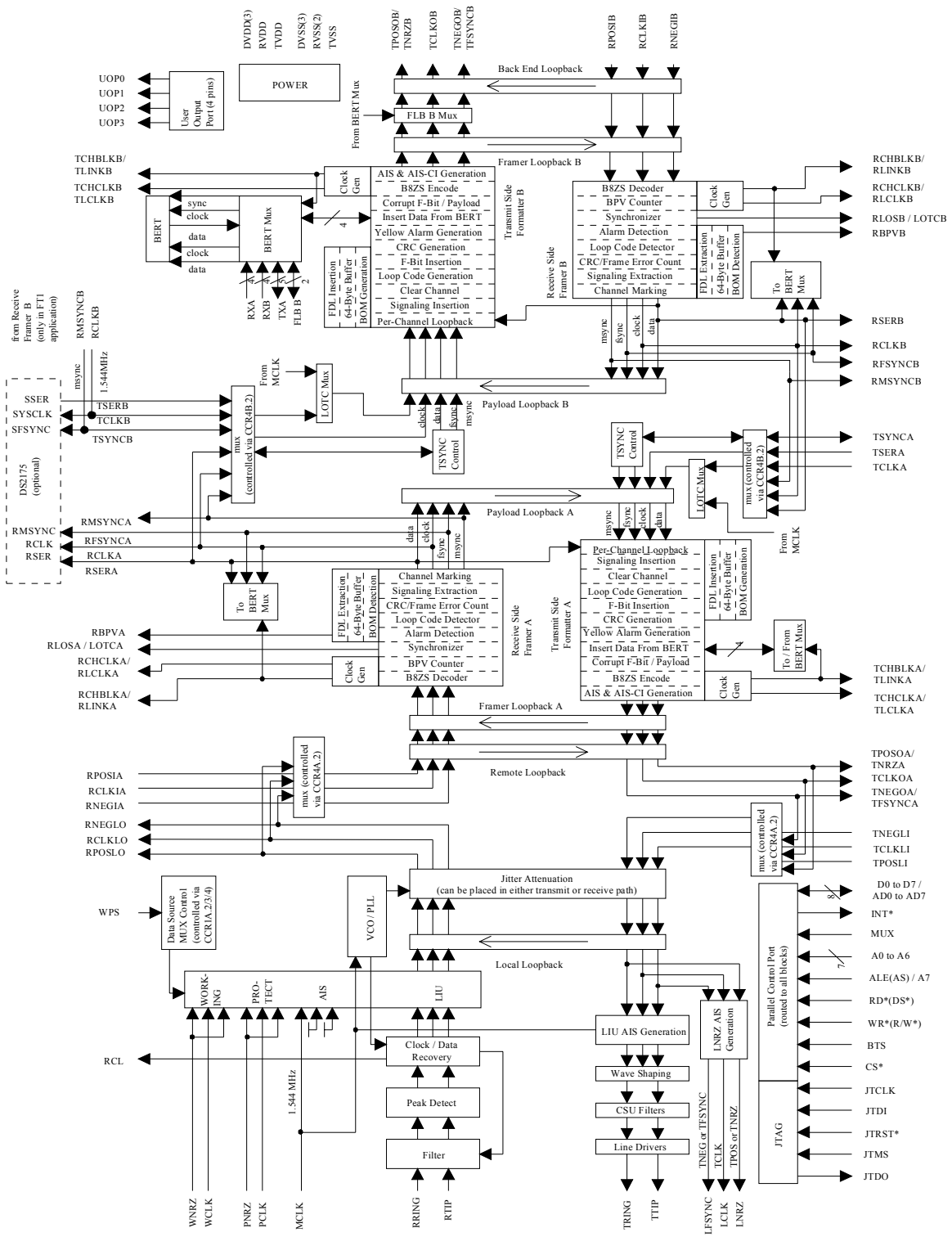
The analog AMI/B8ZS waveform off of the T1 line is transformer coupled into the RRING and RTIP pins of the DS2196. The device recovers clock and data from the analog signal and passes it through the optional jitter attenuator to the receive side framer where the digital serial stream is analyzed to locate the framing/multiframe pattern. The DS2196 contains an active filter that reconstructs the analog received signal for the nonlinear losses that occur in transmission. The device has a usable receive sensitivity of 0 dB to –36 dB, which allows the device to operate on cables up to 6000 feet in length. The receive side framer locates D4 (SLC–96) or ESF multiframe boundaries as well as detects incoming alarms including, carrier loss, loss of synchronization, blue (AIS) and yellow alarms.

The transmit side of the DS2196 is totally independent from the receive side in both the clock requirements and characteristics. The transmit formatter will provide the necessary frame/multiframe data overhead for T1 transmission. Once the data stream has been prepared for transmission, it is sent via the optional jitter attenuator to the wave shaping and line driver functions. The DS2196 will drive the T1 line from the TTIP and TRING pins via a coupling transformer. The line driver can handle both long haul (CSU) and short haul (DSX–1) lines.

Reader's Note: This data sheet assumes a particular nomenclature of the T1 operating environment. In each 125µs frame, there are 24 8-bit channels plus a framing bit. It is assumed that the framing bit is sent first followed by channel 1. Each channel is made up of 8 bits that are numbered 1 to 8. Bit number 1 is the MSB and is transmitted first. Bit number 8 is the LSB and is transmitted last. The following abbreviations are used throughout this data sheet:

BERT	Bit Error Rate Tester
D4	Superframe (12 frames per multiframe) Multiframe Structure
SLC–96	Subscriber Loop Carrier–96 Channels
ESF	Extended Superframe (24 frames per multiframe) Multiframe Structure
B8ZS	Bipolar with Eight Zero Substitution
CRC	Cyclical Redundancy Check
Ft	Terminal Framing Pattern in D4
Fs	Signaling Framing Pattern in D4
FPS	Framing Pattern in ESF
MF	Multiframe
BOC	Bit-Oriented Code
HDLC	High-Level Data-Link Control
FDL	Facility Data Link

Figure 1-1. T1 Dual Framer LIU



2. PIN DESCRIPTION

Table 2-1. Pin Description Sorted by Pin Number

PIN	SYMBOL	TYPE	FUNCTION
1	PCLK	I	Protect Clock Input.
2	PNRZ	I	Protect NRZ Data Input.
3	WCLK	I	Working Clock Input.
4	WNRZ	I	Working NRZ Data Input.
5	JTMS	I	IEEE 1149.1 Test Mode Select.
6	JTCLK	I	IEEE 1149.1 Test Clock Signal.
7	JTRST*	I	IEEE 1149.1 Test Reset.
8	JTDI	I	IEEE 1149.1 Test Data Input.
9	JTDO	O	IEEE 1149.1 Test Data Output.
10	RCL	O	Receive LIU Carrier Loss.
11	LNRZ	O	LIU NRZ & Positive Data Output.
12	LCLK	O	LIU Clock Output.
13	LFSYNC	O	LIU Frame Sync Pulse & Negative Data Output.
14	RPOSLO	O	Receive Positive & NRZ Data Output from the LIU.
15	RNEGLO	O	Receive Negative & NRZ Data Output from the LIU.
16	RCLKLO	O	Receive Clock Output from the LIU.
17	BTS	I	Bus Type Select. 0 = Intel / 1 = Motorola.
18	RTIP	I	Receive Analog Tip Input.
19	RRING	I	Receive Analog Ring Input.
20	RVDD	–	Receive Analog Positive Supply. 3.3V (±5%).
21	RVSS	–	Receive Analog Signal Ground.
22	INT*	O	Interrupt. Open Drain. Active Low Signal.
23	RVSS	–	Receive Analog Signal Ground.
24	MCLK	I	Master Clock Input. 1.544 MHz (±50 ppm).
25	UOP3	O	User Defined Output Port Bit 3.
26	UOP2	O	User Defined Output Port Bit 2.
27	UOP1	O	User Defined Output Port Bit 1.
28	UOP0	O	User Defined Output Port Bit 0.
29	TTIP	O	Transmit Analog Tip Output.
30	TVSS	–	Transmit Analog Signal Ground.
31	TVDD	–	Transmit Analog Positive Supply. 3.3V (±5%).
32	TRING	O	Transmit Analog Ring Output.
33	TPOSLI	I	Transmit Positive & NRZ Data for the LIU.
34	TNEGLI	I	Transmit Negative & NRZ Data for the LIU.
35	TCLKLI	I	Transmit Clock Input for the LIU.
36	TCHBLKB/ TLINKB	I/O	Transmit Channel Blocking Clock Output from Formatter B / Transmit FDL Link Data Input for Formatter B.
37	TCHCLKB/ TLCLKB	O	Transmit DS0 Channel Clock Output from Formatter B / Transmit FDL Link Clock Output from Formatter B.
38	TSYNCB	I/O	Transmit Frame & Multiframe Pulse for/from Formatter B.
39	TCLKB	I	Transmit Clock Input for Formatter B.
40	TSERB	I	Transmit Serial Data Input for Formatter B.
41	TPOSOB/ TNRZB	O	Transmit Positive Data Output from Formatter B / Transmit NRZ Data Output from Formatter B.
42	TNEGOB / TFSYNCB	O	Transmit Negative Data Output from Formatter B / Transmit Frame Sync Pulse Output from Formatter B.

PIN	SYMBOL	TYPE	FUNCTION
43	TCLKOB	O	Transmit Clock Output from Formatter B.
44	DVSS	–	Digital Signal Ground.
45	DVDD	–	Digital Positive Supply. 3.3V (±5%).
46	TCLKOA	O	Transmit Clock Output from Formatter A.
47	TNEGOA / TFSYNCA	O	Transmit Negative Data Output from Formatter A / Transmit Frame Sync Pulse Output from Formatter A.
48	TPOSOA / TNRZA	O	Transmit Positive Data Output / Transmit NRZ Data Output from Formatter A.
49	TSERA	I	Transmit Serial Data Input for Formatter A.
50	TCLKA	I	Transmit Clock Input for Formatter A.
51	TSYNCA	I/O	Transmit Frame & Multiframe Pulse for/from Formatter A.
52	TCHCLKA / TLCLKA	O	Transmit DS0 Channel Clock Output from Formatter A / Transmit FDL Link Clock Output from Formatter A.
53	TCHBLKA / TLINKA	I/O	Transmit Channel Blocking Clock Output from Formatter A / Transmit FDL Link Data Input for Formatter A.
54	MUX	I	Bus Operation. 0 = Non-Mux Bus / 1 = Mux Bus Operation.
55	D0 / AD0	I/O	Data Bus Bit 0 / Address/Data Bus Bit 0. LSB.
56	D1 / AD1	I/O	Data Bus Bit 1 / Address/Data Bus Bit 1.
57	D2 / AD2	I/O	Data Bus Bit 2 / Address/Data Bus Bit 2.
58	D3 / AD3	I/O	Data Bus Bit 3 / Address/Data Bus Bit 3.
59	D4 / AD4	I/O	Data Bus Bit 4 / Address/Data Bus Bit 4.
60	D5 / AD5	I/O	Data Bus Bit 5 / Address/Data Bus Bit 5.
61	D6 / AD6	I/O	Data Bus Bit 6 / Address/Data Bus Bit 6.
62	D7 / AD7	I/O	Data Bus Bit 7 / Address/Data Bus Bit 7. MSB.
63	DVSS	–	I/O Digital Signal Ground.
64	DVDD	–	I/O Digital Positive Supply. 3.3V (±5%).
65	A0	I	Address Bus Bit 0. LSB.
66	A1	I	Address Bus Bit 1
67	A2	I	Address Bus Bit 2
68	A3	I	Address Bus Bit 3
69	A4	I	Address Bus Bit 4
70	A5	I	Address Bus Bit 5
71	A6	I	Address Bus Bit 6
72	A7 / ALE(AS)	I	Address Bus Bit 7 / Address Latch Enable (Address Strobe). MSB.
73	RD*(DS*)	I	Read Input (Data Strobe).
74	CS*	I	Chip Select. Active Low Signal.
75	WR*(R/W*)	I	Write Input (Read/Write).
76	RCHBLKA / RLINKA	O	Receive Channel Blocking Clock Output from Framer A / Receive FDL Link Data Output from Framer A.
77	RCHCLKA / RLCLKA	O	Receive DS0 Channel Clock Output from Framer A / Receive FDL Link Clock Output from Framer A.
78	RCLKIA	I	Receive Clock Input for Framer A.
79	RPOSIA	I	Receive Positive & NRZ Data Input for Framer A.
80	RNEGIA	I	Receive Negative & NRZ Data Input for Framer A.
81	RCLKA	O	Receive Clock Output from Framer A.
82	RSERA	O	Receive Serial Data Output from Framer A.
83	RMSYNCA	O	Receive Multiframe Pulse from Framer A.
84	RFSYNCA	O	Receive Frame Pulse from Framer A.
85	RLOSA/ LOTCA	O	Receive Loss Of Synchronization from Framer A / Loss of Transmit Clock Framer A.

PIN	SYMBOL	TYPE	FUNCTION
86	RBPVA	O	Receive bipolar Violation (BPV) from Framer A.
87	DVSS	–	Digital Signal Ground.
88	DVDD	–	Digital Positive Supply. 3.3V (±5%).
89	RBPVB	O	Receive bipolar Violation (BPV) from Framer B.
90	RLOSB/ LOTCB	O	Receive Loss Of Synchronization from Framer B / Loss of Transmit Clock Framer B.
91	RFSYNCB	O	Receive Frame Pulse from Framer B.
92	RMSYNCB	O	Receive Multiframe Pulse from Framer B.
93	RSERB	O	Receive Serial Data Output from Framer B.
94	RCLKB	O	Receive Clock Output from Framer B.
95	RNEGIB	I	Receive Negative & NRZ Data Input for Framer B.
96	RPOSIB	I	Receive Positive & NRZ Data Input for Framer B.
97	RCLKIB	I	Receive Clock Input for Framer B.
98	RCHCLKB / RLCLKB	O	Receive DS0 Channel Clock Output from Framer B / Receive FDL Link Clock Output from Framer B.
99	RCHBLKB / RLINKB	O	Receive Channel Blocking Clock Output from Framer B / Receive FDL Link Data Output from Framer B.
100	WPS	I	Working/Protect Select.

3. PIN FUNCTION DESCRIPTION

Transmit Side Pins

Signal Name: **TCLKA/B**
Signal Description: **Transmit Clock**
Signal Type: **Input**
A 1.544 MHz primary clock is applied here. Used to clock data through the transmit side formatters. TCLKA/B can be internally connected to RCLKB/A via the CCR4B.2 control bit.

Signal Name: **TSERA/B**
Signal Description: **Transmit Serial Data**
Signal Type: **Input**
Transmit NRZ serial data. Sampled on the falling edge of TCLKA or TCLKB. TSERA/B can be internally connected to RSERB/A via the CCR4B.2 control bit.

Signal Name: **TSYNCA/B**
Signal Description: **Transmit Sync**
Signal Type: **Input / Output**
When programmed as an input, a pulse at this pin will establish either frame or multiframe boundaries for the transmit side. Via TCR2A.2 and TCR2B.2, the DS2196 can be programmed to output either a frame or multiframe pulse at this pin. If this pin is set to output pulses at frame boundaries, it can also be set via TCR2A.4 and TCR2B.4 to output double–wide pulses at signaling frames. See Section 21 for details. TSYNCA/B can be internally connected to RMSYNCB/A via the CCR4B.2 control bit.

Signal Name: **TCHCLKA/B / TLCLKA/B**
Signal Description: **Transmit Channel Clock / Transmit Link Clock**
Signal Type: **Output**
A dual function pin depending on the setting of the CCR4A.1 and CCR4B.1 control bits. If TCHCLK is selected, a 192-kHz clock, which pulses high during the LSB of each channel, will be output. If TLCLK is selected, either a 4 kHz or 2 kHz (ZBTSI) demand clock for the TLINK data is output. This output signal is always synchronous with TCLKA or TCLKB. See Section 21 for details.

Signal Name: **TCHBLKA/B / TLINKA/B**
Signal Description: **Transmit Channel Block / Transmit Link Data**
Signal Type: **Input / Output**
A dual function pin depending on the setting of the CCR4A.1 and CCR4B.1 control bits. If TCHBLK is selected, a user programmable output that can be forced high or low during any of the 24 T1 channels is output. Useful for blocking clocks to a serial UART or LAPD controller in applications where not all T1 channels are used such as Fractional T1, 384 kbps service, 768 kbps, or ISDN–PRI. Also useful for locating individual channels in drop–and–insert applications, for external per–channel loopback, and for per–channel conditioning. See Section 21 for details. If TLINK is selected, this pin will be sampled on the falling edge of TCLKA or TCLKB for data insertion into either the FDL stream (ESF) or the Fs–bit position (D4) or the Z–bit position (ZBTSI). See Section 21 for details. This signal is always synchronous with TCLKA or TCLKB.

Signal Name: **TPOSOA/B / TNRZA/B**
Signal Description: **Transmit Positive & NRZ Data Output**
Signal Type: **Output**
Updated on the rising edge of TCLKOA and rising or falling edge of TCLKOB with either bipolar data or NRZ data out of the transmit side formatter. This pin can be programmed to source NRZ data via the Output Data Format (CCR1A.6 and CCR1B.6) control bits.

Signal Name: **TNEGA/B / TFSYNCA/B**
Signal Description: **Transmit Negative Data & Frame Sync Pulse Output**
Signal Type: **Output**
Updated on the rising edge of TCLKA or TCLKB with either bipolar data or a frame sync pulse out of the transmit side formatter. This pin can be programmed to source the frame sync pulse via the Output Data Format (CCR1A.6 and CCR1B.6) control bits.

Receive Framer Pins

Signal Name: **RCHCLKA/B / RLCLKA/B**
Signal Description: **Receive Channel Clock / Receive Link Clock**
Signal Type: **Output**
A dual function pin depending on the setting of the CCR4A.1 and CCR4B.1 control bits. If RCHCLK is selected, a 192-kHz clock, which pulses high during the LSB of each channel, will be output. If RLCLK is selected, either a 4 kHz or 2 kHz (ZBTSI) clock for the RLINK data is output. This output signal is always synchronous with RCLKA or RCLKB.

Signal Name: **RCHBLKA/B / RLINKA/B**
Signal Description: **Receive Channel Block / Receive Link Data**
Signal Type: **Output**
A dual function pin depending on the setting of the CCR4A.1 and CCR4B.1 control bits. If RCHBLK is selected, a user programmable output that can be forced high or low during any of the 24 T1 channels. Useful for blocking clocks to a serial UART or LAPD controller in applications where not all T1 channels are used such as Fractional T1, 384 kbps service, 768 kbps, or ISDN–PRI. Also useful for locating individual channels in drop–and–insert applications, for external per–channel loopback, and for per–channel conditioning. See Section 21 for details. If RLINK is selected, then either FDL data (ESF) or Fs bits (D4) or Z bits (ZBTSI) one RCLKA before the start of a frame are output. See Section 21 for details. This signal is always synchronous with RCLKA or RCLKB.

Signal Name: **RSERA/B**
Signal Description: **Receive Serial Data**
Signal Type: **Output**
Received NRZ serial data. Updated on rising edges of RCLKA or RCLKB.

Signal Name: **RFSYNCA/B**
Signal Description: **Receive Frame Sync**
Signal Type: **Output**
An extracted pulse, one RCLKA or RCLKB wide, is output at this pin which identifies frame boundaries. Via RCR2A.5 and RCR2B.5, RFSYNC can also be set to output double–wide pulses on signaling frames. This signal is always synchronous with RCLKA or RCLKB.

Signal Name: **RMSYNCA/B**
Signal Description: **Receive Multiframe Sync**
Signal Type: **Output**
An extracted pulse, one RCLKA or RCLKB wide, is output at this pin which identifies multiframe boundaries. This signal is always synchronous with RCLKA or RCLKB.

Signal Name: **RLOSA/B / LOTCA/B**
Signal Description: **Receive Loss of Sync / Loss of Transmit Clock**
Signal Type: **Output**
A dual function output that is controlled by the CCR3.5 control bit. This pin can be programmed to either toggle high when the synchronizer is searching for the frame and multiframe or to toggle high if the TCLK pin has not been toggled for 5 μsec.

Signal Name: **RBPVA/B**
Signal Description: **Receive BPV**
Signal Type: **Output**
This pin will toggle high for one RCLKA or RCLKB clock cycle for each bipolar Violation (BPV) detected by the framer.

Signal Name: **RPOSIA/B**
Signal Description: **Receive Positive Data Input**
Signal Type: **Input**
Sampled on the falling edge of RCLKIA and either rising or falling edge of RCLKIB for data to be clocked through the receive side framer. RPOSIA/B and RNEGIA/B can be tied together for a NRZ interface. RPOSIA be internally connected to RPOSLO via the CCR4A.2 control bit.

Signal Name: **RNEGIA/B**
Signal Description: **Receive Negative Data Input**
Signal Type: **Input**
Sampled on the falling edge of RCLKI for data to be clocked through the receive side framer. RPOSIA/B and RNEGIA/B can be tied together for a NRZ interface. RNEGIA be internally connected to RNEGLO via the CCR4A.2 control bit.

Signal Name: **RCLKIA/B**
Signal Description: **Receive Clock Input**
Signal Type: **Input**
Signal used to clock data through the receive side framers. RCLKIA can be internally connected to RCLKLO via the CCR4A.2 control bit.

User Port Pins

Signal Name: **UOP0/1/2/3**
Signal Description: **User Output Port**
Signal Type: **Output**
These output port pins can be set low or high via the CCR7B.0 to CCR7B.3 control bits. The pins are forced low on power-up.

Parallel Control Port Pins

Signal Name: **INT***
Signal Description: **Interrupt**
Signal Type: **Output**
Flags host controller during conditions and change of states as defined in the Status Registers. Active low, open drain output.

Signal Name: **MUX**
Signal Description: **Bus Operation**
Signal Type: **Input**
Set low to select non-multiplexed bus operation. Set high to select multiplexed bus operation.

Signal Name: **D0 to D7 / AD0 to AD7**
Signal Description: **Data Bus or Address/Data Bus**
Signal Type: **Input / Output**
In non-multiplexed bus operation (MUX = 0), serves as the data bus. In multiplexed bus operation (MUX = 1), serves as a 8–bit multiplexed address / data bus.

Signal Name: **A0 to A6**
Signal Description: **Address Bus**
Signal Type: **Input**
In non-multiplexed bus operation (MUX = 0), serves as the address bus. In multiplexed bus operation (MUX = 1), these pins are not used and should be tied low.

Signal Name: **BTS**
Signal Description: **Bus Type Select**
Signal Type: **Input**
Strap high to select Motorola bus timing; strap low to select Intel bus timing. This pin controls the function of the RD*(DS*), ALE (AS), and WR*(R/W*) pins. If BTS = 1, then these pins assume the function listed in parenthesis ().

Signal Name: **RD* (DS*)**
Signal Description: **Read Input (Data Strobe)**
Signal Type: **Input**
RD* is an active low signal. DS* polarity is determined by the MUX pin setting. Refer to section 21 for details.

Signal Name: **CS***
Signal Description: **Chip Select**
Signal Type: **Input**
Must be low to read or write to the device. CS* is an active low signal.

Signal Name: **ALE(AS) / A7**
Signal Description: **A7 or Address Latch Enable (Address Strobe)**
Signal Type: **Input**
In non-multiplexed bus operation (MUX = 0), serves as the upper address bit. In multiplexed bus operation (MUX = 1), serves to demultiplex the bus on a positive–going edge.
Signal Name: **WR*(R/W*)**
Signal Description: **Write Input (Read/Write)**
Signal Type: **Input**
WR* is an active low signal.

Signal Name: **JTCLK**
Signal Description: **JTAG IEEE 1149.1 Test Serial Clock**
Signal Type: **Input**
This signal is used to shift data into JTDI on the rising edge and out of JTDO on the falling edge. If not used, this pin should be pulled high.

Signal Name: **JTDI**
Signal Description: **JTAG IEEE 1149.1 Test Serial Data Input**
Signal Type: **Input**
Test instructions and data are clocked into this signal on the rising edge of JTCLK. If not used, this pin should be pulled high. This pin has an internal pull-up.

Signal Name: **JTDO**
Signal Description: **JTAG IEEE 1149.1 Test Serial Data Output**
Signal Type: **Output**
Test instructions are clocked out of this signal on the falling edge of JTCLK. If not used, this pin should be left open circuited.

Signal Name: **JTRST***
Signal Description: **JTAG IEEE 1149.1 Test Reset**
Signal Type: **Input**
This signal is used to synchronously reset the test access port controller. At power up, JTRST must be set low and then high. This action will set the device into the boundary scan bypass mode allowing normal device operation. If boundary scan is not used, this pin should be held low. This pin has an internal pull-up.

Signal Name: **JTMS**
Signal Description: **JTAG IEEE 1149.1 Test Mode Select**
Signal Type: **Input**
This signal is sampled on the rising edge of JTCLK and is used to place the test port into the various defined IEEE 1149.1 states. If not used, this pin should be pulled high. This signal has an internal pull-up.

Line Interface Pins

Signal Name: **MCLK**
Signal Description: **Master Clock Input**
Signal Type: **Input**
A 1.544 MHz (±50 ppm) clock source with TTL levels is applied at this pin. This clock is used internally for both clock/data recovery and for jitter attenuation. This clock is also used to source AIS within the LIU.

Signal Name: **RTIP & RRING**
Signal Description: **Receive Tip and Ring**
Signal Type: **Input**
Analog inputs for clock recovery circuitry. These pins connect via a 1:1 transformer to the T1 line. See Section 19 for details.

Signal Name: **TTIP & TRING**
Signal Description: **Transmit Tip and Ring**
Signal Type: **Output**
Analog line driver outputs. These pins connect via a 1:2 step–up transformer to the T1 line. See Section 19 for details.

Signal Name: **LFSYNC**
Signal Description: **LIU Frame Sync**

Signal Type: **Output**
This digital output will provide either a frame synchronization pulse or the negative half of a bipolar data stream. The signal is based on what is provided at the TNEGLI input.

Signal Name: **LNRZ**
Signal Description: **LIU NRZ Data**
Signal Type: **Output**
This digital output will provide either a NRZ data stream or the positive half of a bipolar data stream. The signal is based on what is provided at the TPOSLI input.

Signal Name: **LCLK**
Signal Description: **LIU Clock**
Signal Type: **Output**
This digital output provides the 1.544 MHz transmit LIU clock. The signal is based on what is provided at the TCLKLI input.

Signal Name: **TNEGLI**
Signal Description: **Transmit Negative Data for the LIU**
Signal Type: **Input**
This digital input is used to pass either the negative half of a bipolar data stream or a frame synchronization pulse via the jitter attenuator block to the transmit line driver block and the LFSYNC output pin. Data input to this pin is sampled on the falling edge of TCLKLI. TNEGLI can be internally connected to TNEGOA/TFSYNCA via the CCR4A.2 control bit.

Signal Name: **TPOSLI**
Signal Description: **Transmit Positive Data for the LIU**
Signal Type: **Input**
This digital input is used to pass either the positive half of a bipolar data stream or a NRZ data stream via the jitter attenuator block to the transmit line driver block and the LNRZ output pin. Data input to this pin is sampled on the falling edge of TCLKLI. TPOSLI can be internally connected to TPOSOA/TNRZA via the CCR4A.2 control bit.

Signal Name: **TCLKLI**
Signal Description: **Transmit Clock for the LIU**
Signal Type: **Input**
This digital input is used to pass a 1.544 MHz clock via the jitter attenuator block to the transmit line driver block and the LCLK output pin. TCLKLI can be internally connected to TCLKOA via the CCR4A.2 control bit.

Signal Name: **WNRZ**
Signal Description: **Working NRZ Data**
Signal Type: **Input**
This digital input is used to pass a NRZ data stream via the Data Source Selection MUX and the jitter attenuator block to the RPOSLO and RNEGLO output pins. Data input to this pin is sampled on the falling or rising edge of WCLK.

Signal Name: **WCLK**
Signal Description: **Working Clock**
Signal Type: **Input**
This digital input is used to pass a 1.544 MHz clock via the Data Source Selection MUX and the jitter attenuator block to the RCLKLO output pin.

Signal Name: **PNRZ**
Signal Description: **Protect NRZ Data**
Signal Type: **Input**
This digital input is used to pass a NRZ data stream via the Data Source Selection MUX and the jitter attenuator block to the RPOSLO and RNEGLO output pins. Data input to this pin is sampled on the falling or rising edge of PCLK.

Signal Name: **PCLK**
Signal Description: **Protect Clock**
Signal Type: **Input**
This digital input is used to pass a 1.544 MHz clock via the Data Source Selection MUX and the jitter attenuator block to the RCLKLO output pin.

Signal Name: **RCL**
Signal Description: **Receive Carrier Loss**
Signal Type: **Output**
Set high when the line interface (LIU) detects a carrier loss.

Signal Name: **RPOSLO**
Signal Description: **Receive Positive Data Output from the LIU**
Signal Type: **Output**
Updated on the rising edge of RCLKLO with either bipolar data out of the LIU or NRZ data from the WNRZ or PNRZ inputs.

Signal Name: **RNEGLO**
Signal Description: **Receive Negative Data Output from the LIU**
Signal Type: **Output**
Updated on the rising edge of RCLKLO with either bipolar data out of the LIU or NRZ data from the WNRZ or PNRZ inputs.

Signal Name: **RCLKO**
Signal Description: **Receive Clock Output**
Signal Type: **Output**
Either a buffered recovered clock from the T1 line or the clock provided at the WCLK or PCLK inputs.

Signal Name: **WPS**
Signal Description: **Working or Protect Select**
Signal Type: **Input**
This digital input can be used to select between the WNRZ/WCLK (working) or PNRZ/PCLK (protect) data inputs. For this pin to be active the Data Source MUX must be properly configured via the CCR1A.2, CCR1A.3, and CCR1A.4 control bits.

Supply Pins

Signal Name: **DVDD**
Signal Description: **Digital Positive Supply**
Signal Type: **Supply**
3.3 volts ±5%. Should be tied to the RVDD and TVDD pins.

Signal Name: **RVDD**
Signal Description: **Receive Analog Positive Supply**
Signal Type: **Supply**
3.3 volts ±5%. Should be tied to the DVDD and TVDD pins.

Signal Name: **TVDD**
Signal Description: **Transmit Analog Positive Supply**
Signal Type: **Supply**
3.3 volts ±5%. Should be tied to the RVDD and DVDD pins.

Signal Name: **DVSS**
Signal Description: **Digital Signal Ground**
Signal Type: **Supply**
Should be tied to the RVSS and TVSS pins.

Signal Name: **RVSS**
Signal Description: **Receive Analog Signal Ground**
Signal Type: **Supply**
0.0 volts. Should be tied to the DVSS and TVSS pins.

Signal Name: **TVSS**
Signal Description: **Transmit Analog Ground**
Signal Type: **Supply**
0.0 volts. Should be tied to the DVSS and TVSS pins.

4. REGISTER MAP

Table 4-1. Register Map Sorted By Address

ADDRESS	R/W	REGISTER NAME	REGISTER ABBREVIATION
00	R/W	HDLC Control for Framer A	HCRA
01	R/W	HDLC Status from Framer A	HSRA
02	R/W	HDLC Interrupt Mask for Framer A	HIMRA
03	R/W	Receive HDLC Information for Framer A	RHIRA
04	R/W	Receive Bit Oriented Code for Framer A	RBOCA
05	R	Receive HDLC FIFO from Framer A	RHFA
06	R/W	Transmit HDLC Information for Formatter A	THIRA
07	R/W	Transmit Bit Oriented Code for Formatter A	TBOCA
08	W	Transmit HDLC FIFO for Formatter A	THFA
09	R/W	Test 2 for Framer A (Set to 00h on power-up)	—
0A	R/W	Common Control 7 for Framer A	CCR7A
0B	—	Reserved (Set to 00h on power-up)	—
0C	—	Reserved (Set to 00h on power-up)	—
0D	—	Reserved (Set to 00h on power-up)	—
0E	R	Interrupt Status Register	ISR
0F	R	Device ID	IDR
10	R/W	Receive Information 3 from Framer A	RIR3A
11	R/W	Common Control 4 for Framer A	CCR4A
12	R/W	In–Band Code Control for Framer A	IBCCA
13	R/W	Transmit Code Definition 1 for Framer A	TCD1A
14	R/W	Receive Up Code Definition 1 for Framer A	RUPCD1A
15	R/W	Receive Down Code Definition 1 for Framer A	RDNCD1A
16	R/W	Transmit Code Definition 2 for Framer A	TCD2A
17	R/W	Receive Up Code Definition 2 for Framer A	RUPCD2A
18	R/W	Receive Down Code Definition 2 for Framer A	RDNCD2A
19	R/W	Common Control 5 for Framer A	CCR5A
1A	R	Transmit DS0 Monitor for Framer A	TDS0MA
1B	R/W	Receive Spare Code Definition 1 for Framer A	RSCD1A
1C	R/W	Receive Spare Code Definition 2 for Framer A	RSCD2A
1D	R/w	Receive Spare Code Control for Framer A	RSCCA
1E	R/W	Common Control 6 for Framer A	CCR6A
1F	R	Receive DS0 Monitor from Framer A	RDS0MA
20	R/W	Status 1 from Framer A	SR1A
21	R/W	Status 2 from Framer A	SR2A
22	R/W	Receive Information 1 from Framer A	RIR1A
23	R	Line Code Violation Count 1 from Framer A	LCVCR1A
24	R	Line Code Violation Count 2 from Framer A	LCVCR2A
25	R	Path Code Violation Count 1 from Framer A Multiframe Out of Sync Count 1 from Framer A	PCVCR1A MOSCR1A
26	R	Path Code violation Count 2 from Framer A	PCVCR2A
27	R	Multiframe Out of Sync Count 2 from Framer A	MOSCR2A
28	R	Receive FDL Register from Framer A	RFDLA
29	R/W	Receive FDL Match 1 for Framer A	RMTCH1A
2A	R/W	Receive FDL Match 2 for Framer A	RMTCH2A
2B	R/W	Receive Control 1 for Framer A	RCR1A

ADDRESS	R/W	REGISTER NAME	REGISTER ABBREVIATION
2C	R/W	Receive Control 2 for Framer A	RCR2A
2D	R/W	Receive Mark 1 for Framer A	RMR1A
2E	R/W	Receive Mark 2 for Framer A	RMR2A
2F	R/W	Receive Mark 3 for Framer A	RMR3A
30	R/W	Common Control 3 for Framer A	CCR3A
31	R/W	Receive Information 2 for Framer A	RIR2A
32	R/W	Transmit Channel Blocking 1 for Formatter A	TCBR1A
33	R/W	Transmit Channel blocking 2 for Formatter A	TCBR2A
34	R/W	Transmit Channel Blocking 3 for Formatter A	TCBR3A
35	R/W	Transmit Control 1 for Formatter A	TCR1A
36	R/W	Transmit Control 2 for Formatter A	TCR2A
37	R/W	Common Control 1 for Framer A	CCR1A
38	R/W	Common Control 2 for Framer A	CCR2A
39	R/W	Transmit Transparency 1 for Formatter A	TTR1A
3A	R/W	Transmit Transparency 2 for Formatter A	TTR2A
3B	R/W	Transmit Transparency 3 for Formatter A	TTR3A
3C	R/W	Transmit Idle 1 for Formatter A	TIR1A
3D	R/W	Transmit Idle 2 for Formatter A	TIR2A
3E	R/W	Transmit Idle 3 for Formatter A	TIR3A
3F	R/W	Transmit Idle Definition for Formatter A	TIDRA
40	R/W	BERT Control Register 0	BC0
41	R/W	BERT Control Register 1	BC1
42	R/W	BERT Control Register 2	BC2
43	R	BERT Information Register	BIR
44	R/W	BERT Alternating Word Count	BAWC
45	R/W	BERT Repetitive Pattern Set Register 0	BRP0
46	R/W	BERT Repetitive Pattern Set Register 1	BRP1
47	R/W	BERT Repetitive Pattern Set Register 2	BRP2
48	R/W	BERT Repetitive Pattern Set Register 3	BRP3
49	R	BERT Bit Count Register 0	BBC0
4A	R	BERT Bit Count Register 1	BBC1
4B	R	BERT Bit Count Register 2	BBC2
4C	R	BERT Bit Count Register 3	BBC3
4D	R	BERT Bit Error Count Register 0	BEC0
4E	R	BERT Bit Error Count Register 1	BEC1
4F	R	BERT Bit Error Count Register 2	BEC2
50	R/W	BERT Interface Control	BIC
51	—	Reserved (Set to 00h on power-up)	—
52	—	Reserved (Set to 00h on power-up)	—
53	—	Reserved (Set to 00h on power-up)	—
54	—	Reserved (Set to 00h on power-up)	—
55	—	Reserved (Set to 00h on power-up)	—
56	—	Reserved (Set to 00h on power-up)	—
57	—	Reserved (Set to 00h on power-up)	—
58	—	Reserved (Set to 00h on power-up)	—
59	—	Reserved (Set to 00h on power-up)	—
5A	—	Reserved (Set to 00h on power-up)	—
5B	—	Reserved (Set to 00h on power-up)	—
5C	—	Reserved (Set to 00h on power-up)	—

ADDRESS	R/W	REGISTER NAME	REGISTER ABBREVIATION
5D	—	Reserved (Set to 00h on power-up)	—
5E	R/W	LIU Test Register 1 (Set to 00h on power-up)	—
5F	R/W	LIU Test Register 2 (Set to 00h on power-up)	—
60	R	Receive Signaling 1 from Framer A	RS1A
61	R	Receive Signaling 2 from Framer A	RS2A
62	R	Receive Signaling 3 from Framer A	RS3A
63	R	Receive Signaling 4 from Framer A	RS4A
64	R	Receive Signaling 5 from Framer A	RS5A
65	R	Receive Signaling 6 from Framer A	RS6A
66	R	Receive Signaling 7 from Framer A	RS7A
67	R	Receive Signaling 8 from Framer A	RS8A
68	R	Receive Signaling 9 from Framer A	RS9A
69	R	Receive Signaling 10 from Framer A	RS10A
6A	R	Receive Signaling 11 from Framer A	RS11A
6B	R	Receive Signaling 12A from Framer A	RS12A
6C	R/W	Receive Channel Blocking 1 for Framer A	RCBR1A
6D	R/W	Receive Channel Blocking 2 for Framer A	RCBR2A
6E	R/W	Receive Channel Blocking 3 for Framer A	RCBR3A
6F	R/W	Interrupt Mask 2 for Framer A.	IMR2A
70	R/W	Transmit Signaling 1 for Formatter A	TS1A
71	R/W	Transmit Signaling 2 for Formatter A	TS2A
72	R/W	Transmit Signaling 3 for Formatter A	TS3A
73	R/W	Transmit Signaling 4 for Formatter A	TS4A
74	R/W	Transmit Signaling 5 for Formatter A	TS5A
75	R/W	Transmit Signaling 6 for Formatter A	TS6A
76	R/W	Transmit Signaling 7 for Formatter A	TS7A
77	R/W	Transmit Signaling 8 for Formatter A	TS8A
78	R/W	Transmit Signaling 9 for Formatter A	TS9A
79	R/W	Transmit Signaling 10 for Formatter A	TS10A
7A	R/W	Transmit Signaling 11 for Formatter A	TS11A
7B	R/W	Transmit Signaling 12 for Formatter A	TS12A
7C	R/W	Line Interface Control	LICR
7D	R/W	Test 1 for Framer A (Set to 00h on power-up)	—
7E	R/W	Transmit FDL Register for Formatter A	TFDLA
7F	R/W	Interrupt Mask Register 1 for Framer A	IMR1A
80	R/W	Error Rate Control for Framer A	ERCA
81	W	Number of Errors 1 for Framer A	NOE1A
82	W	Number of Errors 2 for Framer A	NOE2A
83	R	Number of Errors Left 1 for Framer A	NOEL1A
84	R	Number of Errors Left 2 for Framer A	NOEL2A
85	R/W	Error Rate Control for Framer B	ERCB
86	W	Number of Errors 1 for Framer B	NOE1B
87	W	Number of Errors 2 for Framer B	NOE2B
88	R	Number of Errors Left 1 for Framer B	NOEL1B
89	R	Number of Errors Left 2 for Framer B	NOEL2B
8A	—	Reserved (Set to 00h on power-up)	—
8B	—	Reserved (Set to 00h on power-up)	—
8C	—	Reserved (Set to 00h on power-up)	—
8D	—	Reserved (Set to 00h on power-up)	—

ADDRESS	R/W	REGISTER NAME	REGISTER ABBREVIATION
8E	—	Reserved (Set to 00h on power-up)	—
8F	—	Reserved (Set to 00h on power-up)	—
90	R/W	Receive HDLC DS0 Control Register 1 for Framer A	RDC1A
91	R/W	Receive HDLC DS0 Control Register 2 for Framer A	RDC2A
92	R/W	Transmit HDLC DS0 Control Register 1 for Formatter A	TDC1A
93	R/W	Transmit HDLC DS0 Control Register 2 for Formatter A	TDC2A
94	R/W	Receive HDLC DS0 Control Register 1 for Framer B	RDC1B
95	R/W	Receive HDLC DS0 Control Register 2 for Framer B	RDC2B
96	R/W	Transmit HDLC DS0 Control Register 1 for Formatter B	TDC1B
97	R/W	Transmit HDLC DS0 Control Register 2 for Formatter B	TDC2B
98	—	Reserved (Set to 00h on power-up)	—
99	—	Reserved (Set to 00h on power-up)	—
9A	—	Reserved (Set to 00h on power-up)	—
9B	—	Reserved (Set to 00h on power-up)	—
9C	—	Reserved (Set to 00h on power-up)	—
9D	—	Reserved (Set to 00h on power-up)	—
9E	—	Reserved (Set to 00h on power-up)	—
A0	R/W	HDLC Control for Framer B	HCRB
A1	R/W	HDLC Status from Framer B	HSRB
A2	R/W	HDLC Interrupt Mask for Framer B	HIMRB
A3	R/W	Receive HDLC Information for Framer B	RHIRB
A4	R/W	Receive Bit Oriented Code for Framer B	RBOCB
A5	R	Receive HDLC FIFO from Framer B	RHFB
A6	R/W	Transmit HDLC Information for Formatter B	THIRB
A7	R/W	Transmit Bit Oriented Code for Formatter B	TBOCB
A8	W	Transmit HDLC FIFO for Formatter B	THFB
A9	R/W	Test 2 for Framer B (Set to 00h on power-up)	—
AA	R/W	Common Control 7 for Framer B	CCR7B
AB	—	Reserved (Set to 00h on power-up)	—
AC	—	Reserved (Set to 00h on power-up)	—
AD	—	Reserved (Set to 00h on power-up)	—
AE	—	Reserved (Set to 00h on power-up)	—
AF	—	Reserved (Set to 00h on power-up)	—
B0	R/W	Receive Information 3 from Framer B	RIR3B
B1	R/W	Common Control 4 for Framer B	CCR4B
B2	R/W	In–Band Code Control for Framer B	IBCCB
B3	R/W	Transmit Code Definition 1 for Framer B	TCD1B
B4	R/W	Receive Up Code Definition 1 for Framer B	RUPCD1B
B5	R/W	Receive Down Code Definition 1 for Framer B	RDNCD1B
B6	R/W	Transmit Code Definition 2 for Framer B	TCD2B
B7	R/W	Receive Up Code Definition 2 for Framer B	RUPCD2B
B8	R/W	Receive Down Code Definition 2 for Framer B	RDNCD2B

ADDRESS	R/W	REGISTER NAME	REGISTER ABBREVIATION
B9	R/W	Common Control 5 for Framer B	CCR5B
BA	R	Transmit DS0 Monitor from Formatter B	TDS0MB
BB	R/W	Receive Spare Code Definition 1 for Framer B	RSCD1B
BC	R/W	Receive Spare Code Definition 2 for Framer B	RSCD2B
BD	R/W	Receive Spare Code Control for Framer B	RSCCB
BE	R/W	Common Control 6 for Framer B	CCR6B
BF	R	Receive DS0 Monitor from Framer B	RDS0MB
C0	R/W	Status 1 from Framer B	SR1B
C1	R/W	Status 2 from Framer B	SR2B
C2	R/W	Receive Information 1 from Framer B	RIR1B
C3	R	Line Code Violation Count 1 from Framer B	LCVCR1B
C4	R	Line Code Violation Count 2 from Framer B	LCVCR2B
C5	R	Path Code Violation Count 1 from Framer B Multiframe Out of Sync Count 1 from Framer B	PCVCR1B MOSCR1B
C6	R	Path Code violation Count 2 from Framer B	PCVCR2B
C7	R	Multiframe Out of Sync Count 2 from Framer B	MOSCR2B
C8	R	Receive FDL Register from Framer B	RFDLB
C9	R/W	Receive FDL Match 1 for Framer B	RMTCH1B
CA	R/W	Receive FDL Match 2 for Framer B	RMTCH2B
CB	R/W	Receive Control 1 for Framer B	RCR1B
CC	R/W	Receive Control 2 for Framer B	RCR2B
CD	R/W	Receive Mark 1 for Framer B	RMR1B
CE	R/W	Receive Mark 2 for Framer B	RMR2B
CF	R/W	Receive Mark 3 for Framer B	RMR3B
D0	R/W	Common Control 3 for Framer B	CCR3B
D1	R/W	Receive Information 2 from Framer B	RIR2B
D2	R/W	Transmit Channel Blocking 1 for Formatter B	TCBR1B
D3	R/W	Transmit Channel blocking 2 for Formatter B	TCBR2B
D4	R/W	Transmit Channel Blocking 3 for Formatter B	TCBR3B
D5	R/W	Transmit Control 1 for Framer B	TCR1B
D6	R/W	Transmit Control 2 for Framer B	TCR2B
D7	R/W	Common Control 1 for Framer B	CCR1B
D8	R/W	Common Control 2 for Framer B	CCR2B
D9	R/W	Transmit Transparency 1 for Formatter B	TTR1B
DA	R/W	Transmit Transparency 2 for Formatter B	TTR2B
DB	R/W	Transmit Transparency 3 for Formatter B	TTR3B
DC	R/W	Transmit Idle 1 for Formatter B	TIR1B
DD	R/W	Transmit Idle 2 for Formatter B	TIR2B
DE	R/W	Transmit Idle 3 for Formatter B	TIR3B
DF	R/W	Transmit Idle Definition for Formatter B	TIDRB
E0	R	Receive Signaling 1 from Framer B	RS1B
E1	R	Receive Signaling 2 from Framer B	RS2B
E2	R	Receive Signaling 3 from Framer B	RS3B
E3	R	Receive Signaling 4 from Framer B	RS4B
E4	R	Receive Signaling 5 from Framer B	RS5B
E5	R	Receive Signaling 6 from Framer B	RS6B
E6	R	Receive Signaling 7 from Framer B	RS7B
E7	R	Receive Signaling 8 from Framer B	RS8B
E8	R	Receive Signaling 9 from Framer B	RS9B