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DS21FT42/DS21FF42
4 x 3 12-Channel T1 Framer
4 x 4 16-Channel T1 Framer

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FEATURES

- 16 or 12 completely independent T1 framers in one small 27mm x 27mm, 1.27mm pitch BGA package
- Each multichip module (MCM) contains four (FF) or three (FT) DS21Q42 die
- Each quad framer can be concatenated into a single 8.192MHz backplane data stream
- IEEE 1149.1 JTAG-Boundary Scan Architecture
- DS21FF42 and DS21FT42 are pin compatible with DS21FF44 and DS21FT44, respectively, to allow the same footprint to support T1 and E1 applications
- 300-pin MCM 1.27mm pitch BGA package (27mm x 27mm)
- Low-power 3.3V CMOS with 5V tolerant input and outputs

APPLICATIONS

- DSLAMs
- Multiplexers/Demultiplexers
- Switches
- High-Density Line Cards

ORDERING INFORMATION

PART	CHANNEL	PIN-PACKAGE	TEMP RANGE
DS21FT42	12	300 BGA, 27mm x 27mm	0°C to +70°C
DS21FT42N	12	300 BGA, 27mm x 27mm	-40°C to +85°C
DS21FF42	16	300 BGA, 27mm x27mm	0°C to +70°C
DS21FF42N	16	300 BGA, 27mm x 27mm	-40°C to +85°C

1. MULTICHIP MODULE DESCRIPTION

The 4 x 4 and 4 x 3 multichip modules (MCM) offer a high-density packaging arrangement for the DS21Q42 T1 Enhanced Quad Framer. Either three (DS21FT42) or four (DS21FF42) silicon die of these devices is packaged in an MCM with the electrical connections as shown in Figure 1-1.

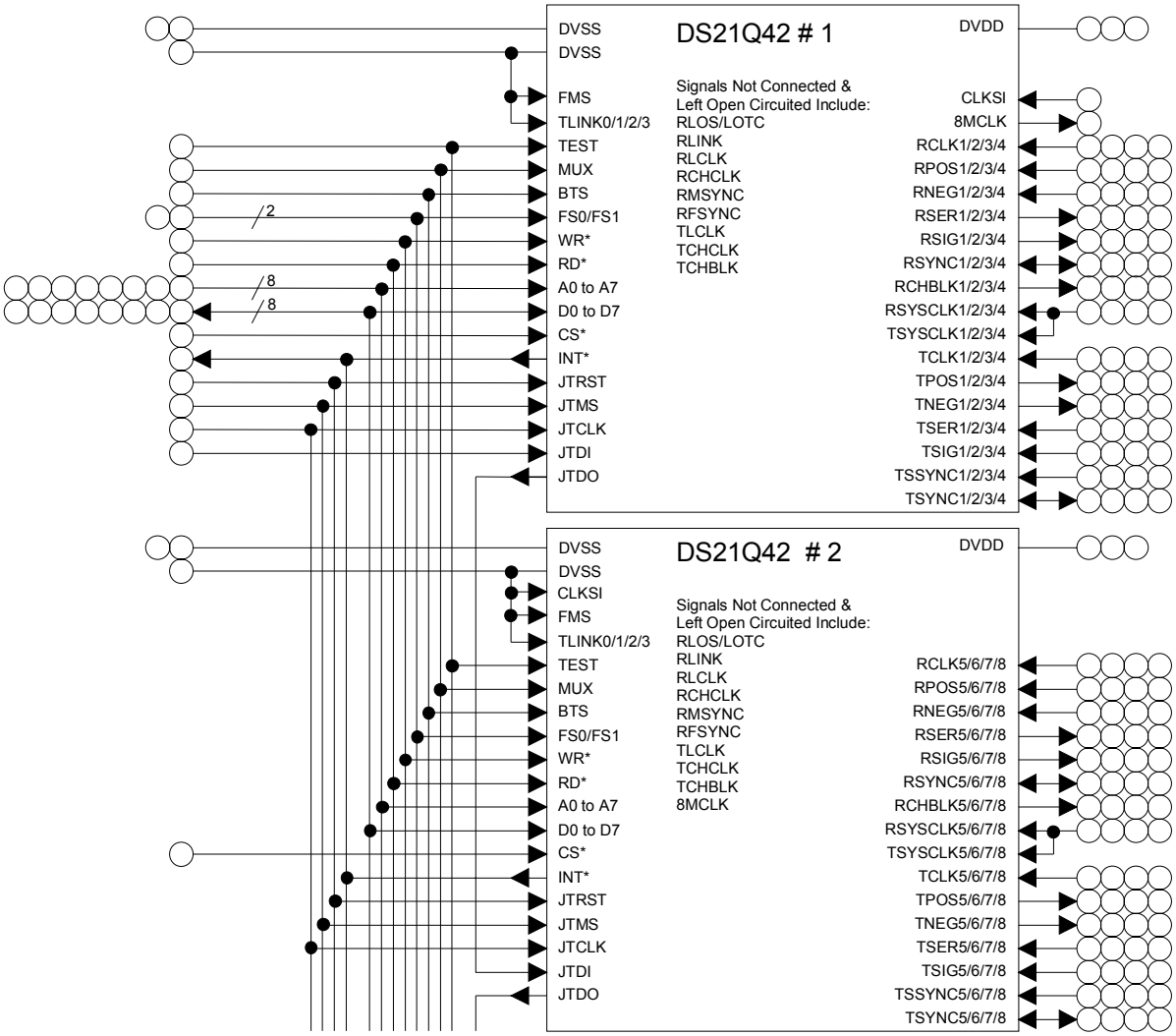
All of the functions available on the DS21Q42 are also available in the MCM packaged version. However, in order to minimize package size, some signals have been deleted or combined. These differences are detailed in Table 1-1. In the 4 x 3 (FT) version, the fourth quad framer is not populated and hence all of the signals to and from this fourth framer are absent and should be treated as No Connects (NC). Table 2-1 lists all of the signals on the MCM and it also lists the absent signals for the 4 x 3.

The availability of both a 12-channel and a 16-channel version allow the maximum framer density with the lowest cost. For example, in a T3 application, two devices (one DS21FF42 and one DS21FT42) provide 28 framers without the additional cost and power consumption of any unused framers that appear in an octal approach.

CHANGES FROM NORMAL DS21Q42 CONFIGURATION Table 1-1

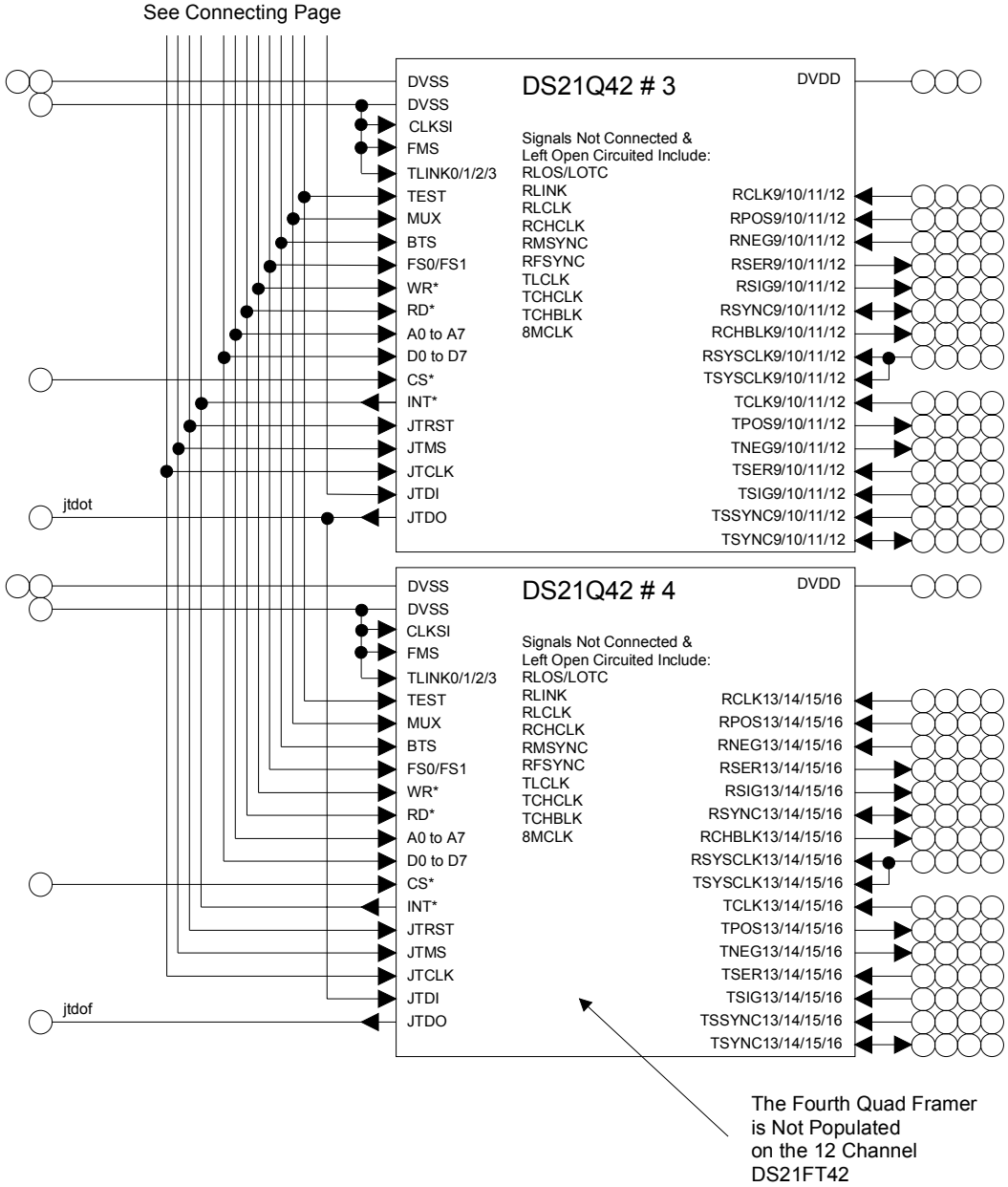
1) TSYSCLK and RSYSCLK are tied together.
2) The following signals are not available:
   RFSYNC/RLCLK/RLINK/RCHCLK/RMSYNC/RLOS/LOTC/TCHBLK/TLCLK/TLINK/TCHCLK

DS21FF42/DS21FT42 SCHEMATIC Figure 1-1



See Connecting Page

DS21FF42/DS21FT42 SCHEMATIC Figure 1-1 (continued)



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MCM PIN DESCRIPTION

PIN DESCRIPTION SORTED BY SYMBOL Table 2-1

PIN	SYMBOL	I/O	DESCRIPTION
B7	8MCLK	O	8.192 MHz Clock Based on CLKSI.
G20	A0	I	Address Bus Bit 0 (lsb).
H20	A1	I	Address Bus Bit 1.
G19	A2	I	Address Bus Bit 2.
H19	A3	I	Address Bus Bit 3.
G18	A4	I	Address Bus Bit 4.
H18	A5	I	Address Bus Bit 5.
G17	A6	I	Address Bus Bit 6.
H17	A7	I	Address Bus Bit 7 (msb).
W15	BTS	I	Bus Timing Select. 0 = Intel / 1 = Motorola.
B6	CLKSI	I	Reference clock for the 8.192 MHz clock synthesizer.
T8	CS1*	I	Chip Select for Quad Framer 1.
Y4	CS2*	I	Chip Select for Quad Framer 2.
Y15	CS3*	I	Chip Select for Quad Framer 3.
E19	CS4*/NC	I	Chip Select for Quad Framer 4. NC on Four x Three.
L20	D0	I/O	Data Bus Bit 0 (lsb).
M20	D1	I/O	Data Bus Bit 1.
L19	D2	I/O	Data Bus Bit 2.
M19	D3	I/O	Data Bus Bit 3.
L18	D4	I/O	Data Bus Bit 4.
M18	D5	I/O	Data Bus Bit 5.
L17	D6	I/O	Data Bus Bit 6.
M17	D7	I/O	Data Bus Bit 7 (msb).
C7	DVDD1	–	Digital Positive Supply for Framer 1.
E4	DVDD1	–	Digital Positive Supply for Framer 1.
D2	DVDD1	–	Digital Positive Supply for Framer 1.
K3	DVDD2	–	Digital Positive Supply for Framer 2.
U7	DVDD2	–	Digital Positive Supply for Framer 2.
P2	DVDD2	–	Digital Positive Supply for Framer 2.
V19	DVDD3	–	Digital Positive Supply for Framer 3.
T12	DVDD3	–	Digital Positive Supply for Framer 3.
L16	DVDD3	–	Digital Positive Supply for Framer 3.
D17	DVDD4/NC	–	Digital Positive Supply for Framer 4. NC on Four x Three.
F16	DVDD4/NC	–	Digital Positive Supply for Framer 4. NC on Four x Three.
B11	DVDD4/NC	–	Digital Positive Supply for Framer 4. NC on Four x Three.
E9	DVSS1	–	Digital Signal Ground for Framer 1.
A6	DVSS1	–	Digital Signal Ground for Framer 1.
D5	DVSS1	–	Digital Signal Ground for Framer 1.
U3	DVSS2	–	Digital Signal Ground for Framer 2.
K4	DVSS2	–	Digital Signal Ground for Framer 2.
U8	DVSS2	–	Digital Signal Ground for Framer 2.
U4	DVSS3	–	Digital Signal Ground for Framer 3.

PIN	SYMBOL	I/O	DESCRIPTION
R16	DVSS3	–	Digital Signal Ground for Framer 3.
Y20	DVSS3	–	Digital Signal Ground for Framer 3.
J20	DVSS4/NC	–	Digital Signal Ground for Framer 4. NC on Four x Three.
A11	DVSS4/NC	–	Digital Signal Ground for Framer 4. NC on Four x Three.
D19	DVSS4/NC	–	Digital Signal Ground for Framer 4. NC on Four x Three.
Y14	FS0	I	Framer Select 0 for the Parallel Control Port.
W14	FS1	I	Framer Select 1 for the Parallel Control Port.
G16	INT*	O	Interrupt for all four Quad Framers.
V14	JTCLK	I	JTAG Clock.
E10	JTDI	I	JTAG Data Input.
A19	JTDOF/NC	O	JTAG Data Output for Four x Four Version. NC on Four x Three.
T17	JTDOT	O	JTAG Data Output for Four x Three Version.
H16	JTMS	I	JTAG Test Mode Select.
K17	JTRST*	I	JTAG Reset.
A13	TEST	I	Tri-State. 0 = do not tri-state / 1 = tri-state all outputs & I/O signals
P17	MUX	I	Bus Operation Select. 0 = non-multiplexed bus / 1 = multiplexed bus
C2	RCHBLK1	O	Receive Channel Blocking Clock.
G3	RCHBLK2	O	Receive Channel Blocking Clock.
E6	RCHBLK3	O	Receive Channel Blocking Clock.
A8	RCHBLK4	O	Receive Channel Blocking Clock.
N1	RCHBLK5	O	Receive Channel Blocking Clock.
Y1	RCHBLK6	O	Receive Channel Blocking Clock.
U6	RCHBLK7	O	Receive Channel Blocking Clock.
N5	RCHBLK8	O	Receive Channel Blocking Clock.
Y8	RCHBLK9	O	Receive Channel Blocking Clock.
W12	RCHBLK10	O	Receive Channel Blocking Clock.
V17	RCHBLK11	O	Receive Channel Blocking Clock.
U17	RCHBLK12	O	Receive Channel Blocking Clock.
D16	RCHBLK13/NC	O	Receive Channel Blocking Clock. NC on Four x Three.
K20	RCHBLK14/NC	O	Receive Channel Blocking Clock. NC on Four x Three.
B18	RCHBLK15/NC	O	Receive Channel Blocking Clock. NC on Four x Three.
B16	RCHBLK16/NC	O	Receive Channel Blocking Clock. NC on Four x Three.
A2	RCLK1	I	Receive Clock for Framer 1
K1	RCLK2	I	Receive Clock for Framer 2.
D10	RCLK3	I	Receive Clock for Framer 3.
B9	RCLK4	I	Receive Clock for Framer 4.
M3	RCLK5	I	Receive Clock for Framer 5.
V1	RCLK6	I	Receive Clock for Framer 6.
W6	RCLK7	I	Receive Clock for Framer 7.
J3	RCLK8	I	Receive Clock for Framer 8.
T9	RCLK9	I	Receive Clock for Framer 9.
W10	RCLK10	I	Receive Clock for Framer 10.

PIN	SYMBOL	I/O	DESCRIPTION
Y18	RCLK11	I	Receive Clock for Framer 11.
N17	RCLK12	I	Receive Clock for Framer 12.
D14	RCLK13/NC	I	Receive Clock for Framer 13. NC on Four x Three.
P20	RCLK14/NC	I	Receive Clock for Framer 14. NC on Four x Three.
C18	RCLK15/NC	I	Receive Clock for Framer 15. NC on Four x Three.
C12	RCLK16/NC	I	Receive Clock for Framer 16. NC on Four x Three.
E18	RD*	I	Read Input.
B2	RNEG1	I	Receive Negative Data for Framer 1.
H2	RNEG2	I	Receive Negative Data for Framer 2.
D9	RNEG3	I	Receive Negative Data for Framer 3.
A9	RNEG4	I	Receive Negative Data for Framer 4.
M2	RNEG5	I	Receive Negative Data for Framer 5.
V3	RNEG6	I	Receive Negative Data for Framer 6.
V7	RNEG7	I	Receive Negative Data for Framer 7.
P3	RNEG8	I	Receive Negative Data for Framer 8.
U9	RNEG9	I	Receive Negative Data for Framer 9.
W11	RNEG10	I	Receive Negative Data for Framer 10.
W17	RNEG11	I	Receive Negative Data for Framer 11.
T20	RNEG12	I	Receive Negative Data for Framer 12.
E14	RNEG13/NC	I	Receive Negative Data for Framer 13. NC on Four x Three.
N20	RNEG14/NC	I	Receive Negative Data for Framer 14. NC on Four x Three.
C20	RNEG15/NC	I	Receive Negative Data for Framer 15. NC on Four x Three.
B13	RNEG16/NC	I	Receive Negative Data for Framer 16. NC on Four x Three.
A1	RPOS1	I	Receive Positive Data for Framer 1.
H1	RPOS2	I	Receive Positive Data for Framer 2.
H4	RPOS3	I	Receive Positive Data for Framer 3.
C9	RPOS4	I	Receive Positive Data for Framer 4.
M1	RPOS5	I	Receive Positive Data for Framer 5.
W2	RPOS6	I	Receive Positive Data for Framer 6.
V5	RPOS7	I	Receive Positive Data for Framer 7.
P4	RPOS8	I	Receive Positive Data for Framer 8.
T10	RPOS9	I	Receive Positive Data for Framer 9.
V11	RPOS10	I	Receive Positive Data for Framer 10.
Y19	RPOS11	I	Receive Positive Data for Framer 11.
R19	RPOS12	I	Receive Positive Data for Framer 12.
D15	RPOS13/NC	I	Receive Positive Data for Framer 13. NC on Four x Three.
J18	RPOS14/NC	I	Receive Positive Data for Framer 14. NC on Four x Three.
A20	RPOS15/NC	I	Receive Positive Data for Framer 15. NC on Four x Three.
A14	RPOS16/NC	I	Receive Positive Data for Framer 16. NC on Four x Three.
C1	RSER1	O	Receive Serial Data from Framer 1.
H3	RSER2	O	Receive Serial Data from Framer 2.
C6	RSER3	O	Receive Serial Data from Framer 3.
C8	RSER4	O	Receive Serial Data from Framer 4.
P1	RSER5	O	Receive Serial Data from Framer 5.
W4	RSER6	O	Receive Serial Data from Framer 6.

PIN	SYMBOL	I/O	DESCRIPTION
T7	RSER7	O	Receive Serial Data from Framer 7.
N4	RSER8	O	Receive Serial Data from Framer 8.
U11	RSER9	O	Receive Serial Data from Framer 9.
Y12	RSER10	O	Receive Serial Data from Framer 10.
V16	RSER11	O	Receive Serial Data from Framer 11.
T16	RSER12	O	Receive Serial Data from Framer 12.
E16	RSER13/NC	O	Receive Serial Data from Framer 13. NC on Four x Three.
F20	RSER14/NC	O	Receive Serial Data from Framer 14. NC on Four x Three.
C16	RSER15/NC	O	Receive Serial Data from Framer 15. NC on Four x Three.
A12	RSER16/NC	O	Receive Serial Data from Framer 16. NC on Four x Three.
D3	RSIG1	O	Receive Signaling Output from Framer 1.
G2	RSIG2	O	Receive Signaling Output from Framer 2.
D4	RSIG3	O	Receive Signaling Output from Framer 3.
D8	RSIG4	O	Receive Signaling Output from Framer 4.
N2	RSIG5	O	Receive Signaling Output from Framer 5.
V4	RSIG6	O	Receive Signaling Output from Framer 6.
V6	RSIG7	O	Receive Signaling Output from Framer 7.
K5	RSIG8	O	Receive Signaling Output from Framer 8.
U10	RSIG9	O	Receive Signaling Output from Framer 9.
Y11	RSIG10	O	Receive Signaling Output from Framer 10.
W19	RSIG11	O	Receive Signaling Output from Framer 11.
U20	RSIG12	O	Receive Signaling Output from Framer 12.
E15	RSIG13/NC	O	Receive Signaling Output from Framer 13. NC on Four x Three.
K19	RSIG14/NC	O	Receive Signaling Output from Framer 14. NC on Four x Three.
C17	RSIG15/NC	O	Receive Signaling Output from Framer 15. NC on Four x Three.
A15	RSIG16/NC	O	Receive Signaling Output from Framer 16. NC on Four x Three.
B1	RSYNC1	I/O	Receive Frame/Multiframe Sync for Framer 1.
G1	RSYNC2	I/O	Receive Frame/Multiframe Sync for Framer 2.
D6	RSYNC3	I/O	Receive Frame/Multiframe Sync for Framer 3.
A7	RSYNC4	I/O	Receive Frame/Multiframe Sync for Framer 4.
N3	RSYNC5	I/O	Receive Frame/Multiframe Sync for Framer 5.
Y2	RSYNC6	I/O	Receive Frame/Multiframe Sync for Framer 6.
U5	RSYNC7	I/O	Receive Frame/Multiframe Sync for Framer 7.
J4	RSYNC8	I/O	Receive Frame/Multiframe Sync for Framer 8.
T11	RSYNC9	I/O	Receive Frame/Multiframe Sync for Framer 9.
V13	RSYNC10	I/O	Receive Frame/Multiframe Sync for Framer 10.
V15	RSYNC11	I/O	Receive Frame/Multiframe Sync for Framer 11.
P18	RSYNC12	I/O	Receive Frame/Multiframe Sync for Framer 12.
J17	RSYNC13/NC	I/O	Receive Frame/Multiframe Sync for Framer 13. NC on Four x Three.
J19	RSYNC14/NC	I/O	Receive Frame/Multiframe Sync for Framer 14. NC on Four x

PIN	SYMBOL	I/O	DESCRIPTION
			Three.
B17	RSYNC15/NC	I/O	Receive Frame/Multiframe Sync for Framer 15. NC on Four x Three.
B12	RSYNC16/NC	I/O	Receive Frame/Multiframe Sync for Framer 16. NC on Four x Three.
B5	SYSCLK1	I	System Clock for Framer 1.
E2	SYSCLK2	I	System Clock for Framer 2.
E5	SYSCLK3	I	System Clock for Framer 3.
B8	SYSCLK4	I	System Clock for Framer 4.
M4	SYSCLK5	I	System Clock for Framer 5.
T2	SYSCLK6	I	System Clock for Framer 6.
Y5	SYSCLK7	I	System Clock for Framer 7.
W3	SYSCLK8	I	System Clock for Framer 8.
T4	SYSCLK9	I	System Clock for Framer 9.
Y9	SYSCLK10	I	System Clock for Framer 10.
U12	SYSCLK11	I	System Clock for Framer 11.
R17	SYSCLK12	I	System Clock for Framer 12.
E13	SYSCLK13/NC	I	System Clock for Framer 13. NC on Four x Three.
N18	SYSCLK14/NC	I	System Clock for Framer 14. NC on Four x Three.
E20	SYSCLK15/NC	I	System Clock for Framer 15. NC on Four x Three.
C14	SYSCLK16/NC	I	System Clock for Framer 16. NC on Four x Three.
D1	TCLK1	I	Transmit Clock for Framer 1.
H5	TCLK2	I	Transmit Clock for Framer 2.
C5	TCLK3	I	Transmit Clock for Framer 3.
A5	TCLK4	I	Transmit Clock for Framer 4.
R1	TCLK5	I	Transmit Clock for Framer 5.
Y3	TCLK6	I	Transmit Clock for Framer 6.
T6	TCLK7	I	Transmit Clock for Framer 7.
K2	TCLK8	I	Transmit Clock for Framer 8.
U13	TCLK9	I	Transmit Clock for Framer 9.
Y13	TCLK10	I	Transmit Clock for Framer 10.
T18	TCLK11	I	Transmit Clock for Framer 11.
P16	TCLK12	I	Transmit Clock for Framer 12.
K16	TCLK13/NC	I	Transmit Clock for Framer 13. NC on Four x Three.
F19	TCLK14/NC	I	Transmit Clock for Framer 14. NC on Four x Three.
E17	TCLK15/NC	I	Transmit Clock for Framer 15. NC on Four x Three.
C11	TCLK16/NC	I	Transmit Clock for Framer 16. NC on Four x Three.
C3	TNEG1	O	Transmit Negative Data from Framer 1.
J1	TNEG2	O	Transmit Negative Data from Framer 2.
F5	TNEG3	O	Transmit Negative Data from Framer 3.
A10	TNEG4	O	Transmit Negative Data from Framer 4.
L1	TNEG5	O	Transmit Negative Data from Framer 5.
V2	TNEG6	O	Transmit Negative Data from Framer 6.
V8	TNEG7	O	Transmit Negative Data from Framer 7.
P5	TNEG8	O	Transmit Negative Data from Framer 8.

PIN	SYMBOL	I/O	DESCRIPTION
U14	TNEG9	O	Transmit Negative Data from Framer 9.
V12	TNEG10	O	Transmit Negative Data from Framer 10.
W18	TNEG11	O	Transmit Negative Data from Framer 11.
T19	TNEG12	O	Transmit Negative Data from Framer 12.
D11	TNEG13/NC	O	Transmit Negative Data from Framer 13. NC on Four x Three.
K18	TNEG14/NC	O	Transmit Negative Data from Framer 14. NC on Four x Three.
C19	TNEG15/NC	O	Transmit Negative Data from Framer 15. NC on Four x Three.
B15	TNEG16/NC	O	Transmit Negative Data from Framer 16. NC on Four x Three.
B3	TPOS1	O	Transmit Positive Data from Framer 1.
J2	TPOS2	O	Transmit Positive Data from Framer 2.
J5	TPOS3	O	Transmit Positive Data from Framer 3.
B10	TPOS4	O	Transmit Positive Data from Framer 4.
L2	TPOS5	O	Transmit Positive Data from Framer 5.
W1	TPOS6	O	Transmit Positive Data from Framer 6.
W7	TPOS7	O	Transmit Positive Data from Framer 7.
R3	TPOS8	O	Transmit Positive Data from Framer 8.
T14	TPOS9	O	Transmit Positive Data from Framer 9.
Y10	TPOS10	O	Transmit Positive Data from Framer 10.
V18	TPOS11	O	Transmit Positive Data from Framer 11.
V20	TPOS12	O	Transmit Positive Data from Framer 12.
E12	TPOS13/NC	O	Transmit Positive Data from Framer 13. NC on Four x Three.
N19	TPOS14/NC	O	Transmit Positive Data from Framer 14. NC on Four x Three.
B19	TPOS15/NC	O	Transmit Positive Data from Framer 15. NC on Four x Three.
B14	TPOS16/NC	O	Transmit Positive Data from Framer 16. NC on Four x Three.
B4	TSER1	I	Transmit Serial Data for Framer 1.
E1	TSER2	I	Transmit Serial Data for Framer 2.
F3	TSER3	I	Transmit Serial Data for Framer 3.
D7	TSER4	I	Transmit Serial Data for Framer 4.
L5	TSER5	I	Transmit Serial Data for Framer 5.
T1	TSER6	I	Transmit Serial Data for Framer 6.
Y6	TSER7	I	Transmit Serial Data for Framer 7.
T3	TSER8	I	Transmit Serial Data for Framer 8.
M16	TSER9	I	Transmit Serial Data for Framer 9.
W9	TSER10	I	Transmit Serial Data for Framer 10.
W16	TSER11	I	Transmit Serial Data for Framer 11.
W20	TSER12	I	Transmit Serial Data for Framer 12.
D13	TSER13/NC	I	Transmit Serial Data for Framer 13. NC on Four x Three.
F17	TSER14/NC	I	Transmit Serial Data for Framer 14. NC on Four x Three.
D18	TSER15/NC	I	Transmit Serial Data for Framer 15. NC on Four x Three.
A18	TSER16/NC	I	Transmit Serial Data for Framer 16. NC on Four x Three.
C4	TSIG1	I	Transmit Signaling Input for Framer 1.
F1	TSIG2	I	Transmit Signaling Input for Framer 2.
G4	TSIG3	I	Transmit Signaling Input for Framer 3.
C10	TSIG4	I	Transmit Signaling Input for Framer 4.
L3	TSIG5	I	Transmit Signaling Input for Framer 5.

PIN	SYMBOL	I/O	DESCRIPTION
U2	TSIG6	I	Transmit Signaling Input for Framer 6.
V9	TSIG7	I	Transmit Signaling Input for Framer 7.
R5	TSIG8	I	Transmit Signaling Input for Framer 8.
U15	TSIG9	I	Transmit Signaling Input for Framer 9.
V10	TSIG10	I	Transmit Signaling Input for Framer 10.
U18	TSIG11	I	Transmit Signaling Input for Framer 11.
R18	TSIG12	I	Transmit Signaling Input for Framer 12.
E11	TSIG13/NC	I	Transmit Signaling Input for Framer 13. NC on Four x Three.
P19	TSIG14/NC	I	Transmit Signaling Input for Framer 14. NC on Four x Three.
B20	TSIG15/NC	I	Transmit Signaling Input for Framer 15. NC on Four x Three.
A16	TSIG16/NC	I	Transmit Signaling Input for Framer 16. NC on Four x Three.
A3	TSSYNC1	I	Transmit System Sync for Framer 1.
F2	TSSYNC2	I	Transmit System Sync for Framer 2.
G5	TSSYNC3	I	Transmit System Sync for Framer 3.
E8	TSSYNC4	I	Transmit System Sync for Framer 4.
L4	TSSYNC5	I	Transmit System Sync for Framer 5.
U1	TSSYNC6	I	Transmit System Sync for Framer 6.
Y7	TSSYNC7	I	Transmit System Sync for Framer 7.
R4	TSSYNC8	I	Transmit System Sync for Framer 8.
T15	TSSYNC9	I	Transmit System Sync for Framer 9.
W8	TSSYNC10	I	Transmit System Sync for Framer 10.
Y17	TSSYNC11	I	Transmit System Sync for Framer 11.
U19	TSSYNC12	I	Transmit System Sync for Framer 12.
C13	TSSYNC13/NC	I	Transmit System Sync for Framer 13. NC on Four x Three.
R20	TSSYNC14/NC	I	Transmit System Sync for Framer 14. NC on Four x Three.
D20	TSSYNC15/NC	I	Transmit System Sync for Framer 15. NC on Four x Three.
A17	TSSYNC16/NC	I	Transmit System Sync for Framer 16. NC on Four x Three.
E3	TSYNC1	I/O	Transmit Sync for Framer 1.
F4	TSYNC2	I/O	Transmit Sync for Framer 2.
E7	TSYNC3	I/O	Transmit Sync for Framer 3.
A4	TSYNC4	I/O	Transmit Sync for Framer 4.
R2	TSYNC5	I/O	Transmit Sync for Framer 5.
W5	TSYNC6	I/O	Transmit Sync for Framer 6.
T5	TSYNC7	I/O	Transmit Sync for Framer 7.
M5	TSYNC8	I/O	Transmit Sync for Framer 8.
T13	TSYNC9	I/O	Transmit Sync for Framer 9.
W13	TSYNC10	I/O	Transmit Sync for Framer 10.
U16	TSYNC11	I/O	Transmit Sync for Framer 11.
N16	TSYNC12	I/O	Transmit Sync for Framer 12.
J16	TSYNC13/NC	I/O	Transmit Sync for Framer 13. NC on Four x Three.
F18	TSYNC14/NC	I/O	Transmit Sync for Framer 14. NC on Four x Three.
C15	TSYNC15/NC	I/O	Transmit Sync for Framer 15. NC on Four x Three.
D12	TSYNC16/NC	I/O	Transmit Sync for Framer 16. NC on Four x Three.
Y16	WR*	I	Write Input.

2. DS21FF42 (4 X 4) PCB LAND PATTERN Figure 3-1

The diagram shown below is the pin pattern that will be placed on the target PCB. This is the same pattern that would be seen as viewed through the MCM from the top.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
A	rpos 1	rclk 1	ts sync1	tsync 4	tclk 4	dvss 1	rsync 4	rch blk 4	rneg 4	tneg 4	dvss 4	rser 16	test	rpos 16	rsig 16	tsig 16	ts sync 16	tser 16	jtdof	rpos 15
B	rsync 1	rneg 1	tpos 1	tser 1	sys clk 1	clksi	8 mclk	sys clk 4	rclk 4	tpos 4	dvdd 4	rsync 16	rneg 16	tpos 16	tneg 16	rch blk 16	rsync 15	rch blk 15	tpos 15	tsig 15
C	rser 1	rch blk 1	tneg 1	tsig 1	tclk 3	rser 3	dvdd 1	rser4	rpos 4	tsig 4	tclk 16	rclk 16	ts sync 13	sys clk 16	tsync 15	rser 15	rsig 15	rclk 15	tneg 15	rneg 15
D	tclk 1	dvdd 1	rsig 1	rsig 3	dvss 1	rsync 3	tser 4	rsig4	rneg 3	rclk 3	tneg 13	tsync 16	tser 13	rclk 13	rpos 13	rch blk 13	dvdd 4	tser 15	dvss 4	ts sync 15
E	tser 2	sys clk 2	tsync 1	dvdd 1	sys clk 3	rch blk 3	tsync 3	ts sync 4	dvss 1	jtdi	tsig 13	tpos 13	sys clk 13	rneg 13	rsig 13	rser 13	tclk 15	rd*	cs4*	sys clk 15
F	tsig 2	ts sync 2	tser 3	tsync 2	tneg 3											dvdd 4	tser 14	tsync 14	tclk 14	rser 14
G	rsync 2	rsig 2	rch blk 2	tsig 3	ts sync 3											int*	A6	A4	A2	A0
H	rpos 2	rneg 2	rser 2	rpos 3	tclk 2											jtms	A7	A5	A3	A1
J	tneg 2	tpos 2	rclk 8	rsync 8	tpos 3											tsync 13	rsync 13	rpos 14	rsync 14	dvss 4
K	rclk 2	tclk 8	dvdd 2	dvss 2	rsig 8											tclk 13	jtrst*	tneg 14	rsig 14	rch blk 14
L	tneg 5	tpos 5	tsig 5	ts sync 5	tser 5											dvdd 3	D6	D4	D2	D0
M	rpos 5	rneg 5	rclk 5	sys clk 5	tsync 8											tser 9	D7	D5	D3	D1
N	rch blk 5	rsig 5	rsync 5	rser 8	rch blk 8											tsync 12	rclk 12	sys clk 14	tpos 14	rneg 14
P	rser 5	dvdd 2	rneg 8	rpos 8	tneg 8											tclk 12	mux	rsync 12	tsig 14	rclk 14
R	tclk 5	tsync 5	tpos 8	ts sync 8	tsig 8											dvss 3	sys clk 12	tsig 12	rpos 12	ts sync 14
T	tser 6	sys clk 6	tser 8	sys clk 9	tsync 7	tclk 7	rser 7	cs1*	rclk 9	rpos 9	rsync 9	dvdd 3	tsync 9	tpos 9	ts sync 9	rser 12	jtdot	tclk 11	tneg 12	rneg 12
U	ts sync 6	tsig 6	dvss 2	dvss 3	rsync 7	rch blk 7	dvdd 2	dvss 2	rneg 9	rsig 9	rser 9	sys clk 11	tclk 9	tneg 9	tsig 9	tsync 11	rch blk 12	tsig 11	tssync 12	rsig 12
V	rclk 6	tneg 6	rneg 6	rsig 6	rpos 7	rsig 7	rneg 7	tneg 7	tsig 7	tsig 10	rpos 10	tneg 10	rsync 10	jtclk	rsync 11	rser 11	rch blk 11	tpos 11	dvdd 3	tpos 12
W	tpos 6	rpos 6	sys clk 8	rser 6	tsync 6	rclk 7	tpos 7	ts sync 10	tser 10	rclk 10	rneg 10	rch blk 10	tsync 10	fs1	bts	tser 11	rneg 11	tneg 11	rsig 11	tser 12
Y	rch blk 6	rsync 6	tclk 6	cs2*	sys clk 7	tser 7	ts sync 7	rch blk 9	sys clk 10	tpos 10	rsig 10	rser 10	tclk 10	fs0	cs3*	wr*	ts sync 11	rclk 11	rpos 11	dvss 3

3. DS21FT42 (4 X 3) PCB LAND PATTERN Figure 4-1

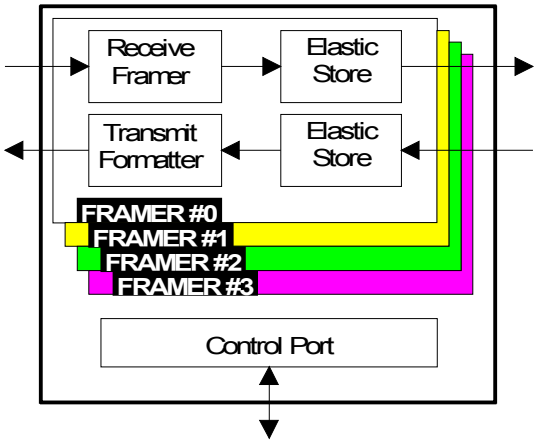
The diagram shown below is the lead pattern that will be placed on the target PCB. This is the same pattern that would be seen as viewed through the MCM from the top.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
A	rpos 1	rclk 1	ts sync1	tsync 4	tclk 4	dvss 1	rsync 4	rch blk 4	rneg 4	tneg 4	nc	nc	test	ns	ns	nc	nc	nc	nc	nc
B	rsync 1	rneg 1	tpos 1	tser 1	sys clk 1	clksi	8 mclk	sys clk 4	rclk 4	tpos 4	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc
C	rser 1	rch blk 1	tneg 1	tsig 1	tclk 3	rser 3	dvdd 1	rser4	rpos 4	tsig 4	nc	nc	nc	nc	ns	nc	nc	nc	nc	nc
D	tclk 1	dvdd 1	rsig 1	rsig 3	dvss 1	rsync 3	tser 4	rsig4	rneg 3	rclk 3	nc	nc	nc	nc	nc	nc	nc	nc	nc	nc
E	tser 2	sys clk 2	tsync 1	dvdd 1	sys clk 3	rch blk 3	tsync 3	ts sync 4	dvss 1	jtdi	nc	nc	nc	nc	nc	nc	nc	rd*	nc	nc
F	tsig 2	ts sync 2	tser 3	tsync 2	tneg 3											nc	nc	nc	nc	nc
G	rsync 2	rsig 2	rch blk 2	tsig 3	ts sync 3											int*	A6	A4	A2	A0
H	rpos 2	rneg 2	rser 2	rpos 3	tclk 2											jtms	A7	A5	A3	A1
J	tneg 2	tpos 2	rclk 8	rsync 8	tpos 3											nc	nc	nc	nc	nc
K	rclk 2	tclk 8	dvdd 2	dvss 2	rsig 8											nc	jtrst*	nc	nc	nc
L	tneg 5	tpos 5	tsig 5	ts sync 5	tser 5											dvdd 3	D6	D4	D2	D0
M	rpos 5	rneg 5	rclk 5	sys clk 5	tsync 8											tser 9	D7	D5	D3	D1
N	rch blk 5	rsig 5	rsync 5	rser 8	rch blk 8											tsync 12	rclk 12	nc	nc	nc
P	rser 5	dvdd 2	rneg 8	rpos 8	tneg 8											tclk 12	mux	rsync 12	nc	nc
R	tclk 5	tsync 5	tpos 8	ts sync 8	tsig 8											dvss 3	sys clk 12	tsig 12	rpos 12	nc
T	tser 6	sys clk 6	tser 8	sys clk 9	tsync 7	tclk 7	rser 7	cs1*	rclk 9	rpos 9	rsync 9	dvdd 3	tsync 9	tpos 9	ts sync 9	rser 12	jtdot	tclk 11	tneg 12	rneg 12
U	ts sync 6	tsig 6	dvss 2	dvss 3	rsync 7	rch blk 7	dvdd 2	dvss 2	rneg 9	rsig 9	rser 9	sys clk 11	tclk 9	tneg 9	tsig 9	tsync 11	rch blk 12	tsig 11	tssync 12	rsig 12
V	rclk 6	tneg 6	rneg 6	rsig 6	rpos 7	rsig 7	rneg 7	tneg 7	tsig 7	tsig 10	rpos 10	tneg 10	rsync 10	jtclk	rsync 11	rser 11	rch blk 11	tpos 11	dvdd 3	tpos 12
W	tpos 6	rpos 6	sys clk 8	rser 6	tsync 6	rclk 7	tpos 7	ts sync 10	tser 10	rclk 10	rneg 10	rch blk 10	tsync 10	fs1	bts	tser 11	rneg 11	tneg 11	rsig 11	tser 12
Y	rch blk 6	rsync 6	tclk 6	cs2*	sys clk 7	tser 7	ts sync 7	rch blk 9	sys clk 10	tpos 10	rsig 10	rser 10	tclk 10	fs0	cs3*	wr*	ts sync 11	rclk 11	rpos 11	dvss 3

4. DS21Q42 FEATURES

- Four T1 DS1/ISDN–PRI/J1 framing transceivers
- All four framers are fully independent
- Each of the four framers contain dual two-frame elastic store slip buffers that can connect to asynchronous backplanes up to 8.192 MHz
- 8-bit parallel control port that can be used directly on either multiplexed or nonmultiplexed buses (Intel or Motorola)
- Programmable output clocks for Fractional T1
- Fully independent transmit and receive functionality
- Integral HDLC controller with 64-byte buffers. Configurable for FDL or DS0 operation
- Generates and detects in-band loop codes from 1 to 8 bits in length including CSU loop codes
- Pin compatible with DS21Q44 E1 Enhanced Quad E1 Framer
- 3.3V supply with 5V tolerant I/O; low power CMOS
- Available in 128--pin TQFP package
- IEEE 1149.1 support

FUNCTIONAL DIAGRAM



DESCRIPTION

The DS21Q42 is an enhanced version of the DS21Q41B Quad T1 Framer. The DS21Q42 contains four framers that are configured and read through a common microprocessor compatible parallel port. Each framer consists of a receive framer, receive elastic store, transmit formatter and transmit elastic store. All four framers in the DS21Q42 are totally independent, they do not share a common framing synchronizer. Also the transmit and receive sides of each framer are totally independent. The dual two-frame elastic stores contained in each of the four framers can be independently enabled and disabled as required. The device fully meets all of the latest T1 specifications including ANSI T1.403–1995, ANSI T1.231–1993, AT&T TR 62411 (12–90), AT&T TR54016, and ITU G.704 and G.706.

5. DS21Q42 INTRODUCTION

The DS21Q42 is a superset version of the popular DS21Q41 Quad T1 framer offering the new features listed below. All of the original features of the DS21Q41 have been retained and software created for the original device is transferable to the DS21Q42.

NEW FEATURES

- Additional hardware signaling capability including:
  - Receive signaling re-insertion to a backplane multiframe sync
  - Availability of signaling in a separate PCM data stream
  - Signaling freezing
  - Interrupt generated on change of signaling data
- Full HDLC controller with 64–byte buffers in both transmit and receive paths. Configurable for FDL or DS0 access
- Per–channel code insertion in both transmit and receive paths
- Ability to monitor one DS0 channel in both the transmit and receive paths
- RCL, RLOS, RRA, and RAIS alarms now interrupt on change of state
- Detects AIS-CI
- 8.192 MHz clock synthesizer
- Per–channel loopback
- Ability to calculate and check CRC6 according to the Japanese standard
- Ability to pass the F–Bit position through the elastic stores in the 2.048 MHz backplane mode
- IEEE 1149.1 support

FEATURES

- Four T1 DS1/ISDN–PRI/J1 framing transceivers
- All four framers are fully independent
- Frames to D4, ESF, and SLC–96 R formats
- Each of the four framers contain dual two–frame elastic store slip buffers that can connect to asynchronous backplanes up to 8.192 MHz
- 8–bit parallel control port that can be used directly on either multiplexed or non–multiplexed buses (Intel or Motorola)
- Extracts and inserts robbed bit signaling
- Detects and generates yellow (RAI) and blue (AIS) alarms
- Programmable output clocks for Fractional T1
- Fully independent transmit and receive functionality
- Generates and detects in–band loop codes from 1 to 8 bits in length including CSU loop codes
- Contains ANSI one’s density monitor and enforcer
- Large path and line error counters including BPV, CV, CRC6, and framing bit errors
- Pin compatible with DS21Q44 E1 Enhanced Quad E1 Framer
- 3.3V supply with 5V tolerant I/O; low power CMOS
- Available in 128–pin TQFP package

FUNCTIONAL DESCRIPTION

The receive side framer locates D4 (SLC–96) or ESF multiframe boundaries as well as detects incoming alarms including, carrier loss, loss of synchronization, blue (AIS) and yellow alarms. If needed, the receive side elastic store can be enabled in order to absorb the phase and frequency differences between the recovered T1 data stream and an asynchronous backplane clock which is provided at the RSYSCLK input. The clock applied at the RSYSCLK input can be either a 2.048 MHz clock or a 1.544 MHz clock. The RSYSCLK can be a burst clock with speeds up to 8.192 MHz.

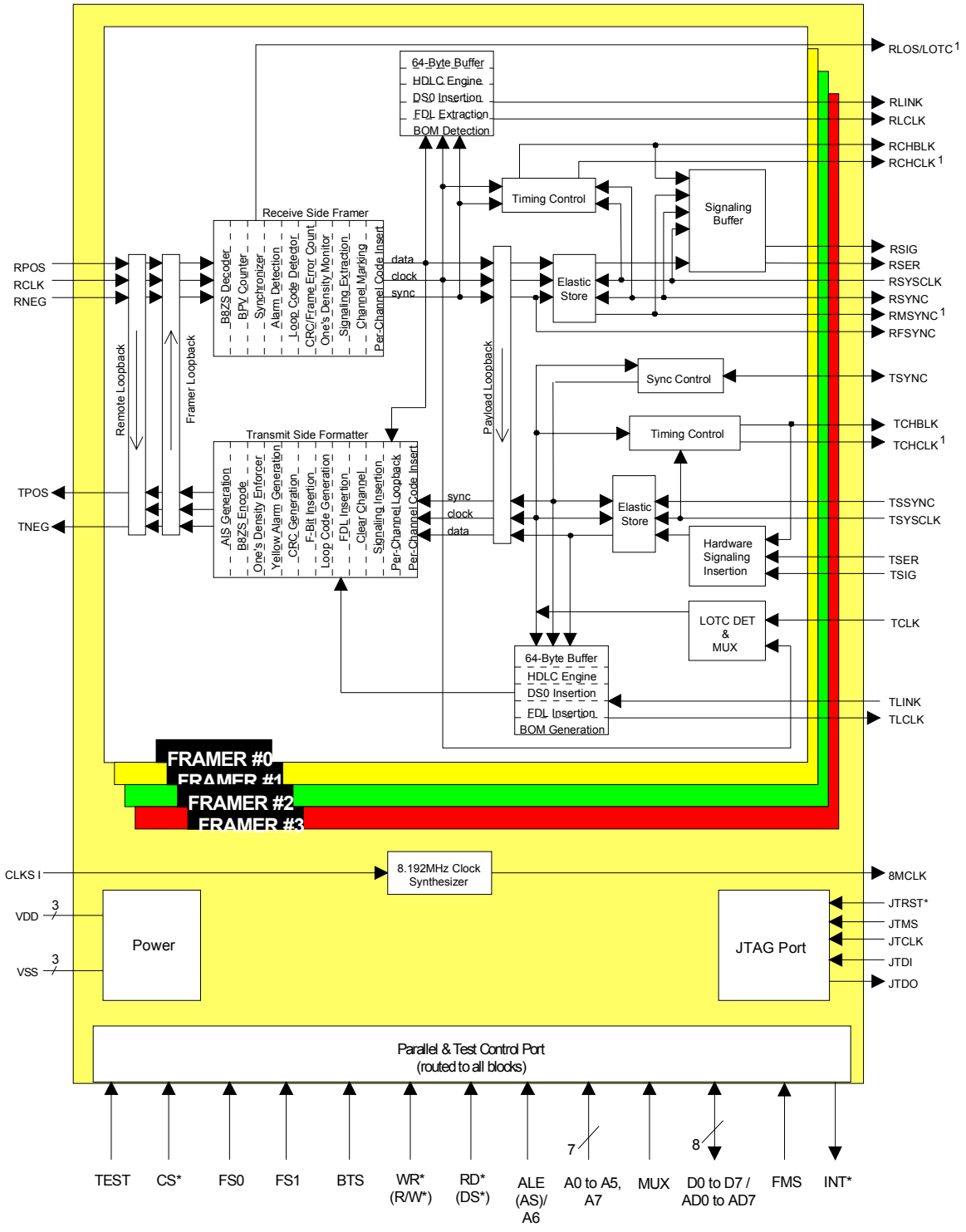
The transmit side of the DS21Q42 is totally independent from the receive side in both the clock requirements and characteristics. Data off of a backplane can be passed through a transmit side elastic store if necessary. The transmit formatter will provide the necessary frame/multiframe data overhead for T1 transmission.

READER'S NOTE:

This data sheet assumes a particular nomenclature of the T1 operating environment. In each 125 us frame, there are 24 8–bit channels plus a framing bit. It is assumed that the framing bit is sent first followed by channel 1. Each channel is made up of 8 bits which are numbered 1 to 8. Bit number 1 is the MSB and is transmitted first. Bit number 8 is the LSB and is transmitted last. Throughout this data sheet, the following abbreviations will be used:

D4	Superframe (12 frames per multiframe) Multiframe Structure
SLC–96	Subscriber Loop Carrier – 96 Channels (SLC–96 is an AT&T registered trademark)
ESF	Extended Superframe (24 frames per multiframe) Multiframe Structure
B8ZS	Bipolar with 8 Zero Substitution
CRC	Cyclical Redundancy Check
Ft	Terminal Framing Pattern in D4
Fs	Signaling Framing Pattern in D4
FPS	Framing Pattern in ESF
MF	Multiframe
BOC	Bit Oriented Code
HDLC	High Level Data Link Control
FDL	Facility Data Link

DS21Q42 ENHANCED QUAD T1 FRAMER Figure 5-1



Note:
1. Alternate pin functions. Consult data sheet for restrictions.

6. DS21Q42 PIN FUNCTION DESCRIPTION

This section describes the signals on the DS21Q42 die. Signals that are not bonded out or have limited functionality in the DS21FT42 and DS21FF42 are noted in italics.

TRANSMIT SIDE PINS

Signal Name: **TCLK**
Signal Description: **Transmit Clock**
Signal Type: **Input**
A 1.544 MHz primary clock. Used to clock data through the transmit side formatter.

Signal Name: **TSER**
Signal Description: **Transmit Serial Data**
Signal Type: **Input**
Transmit NRZ serial data. Sampled on the falling edge of TCLK when the transmit side elastic store is disabled. Sampled on the falling edge of TSYSCLK when the transmit side elastic store is enabled.

Signal Name: **TCHCLK**
Signal Description: **Transmit Channel Clock**
Signal Type: **Output**
A 192 kHz clock which pulses high during the LSB of each channel. Synchronous with TCLK when the transmit side elastic store is disabled. Synchronous with TSYSCLK when the transmit side elastic store is enabled. Useful for parallel to serial conversion of channel data. This function is available when FMS = 1 (DS21Q41 emulation). *This signal is not bonded out in the DS21FF42/DS21FT42.*

Signal Name: **TCHBLK**
Signal Description: **Transmit Channel Block**
Signal Type: **Output**
A user programmable output that can be forced high or low during any of the 24 T1 channels. Synchronous with TCLK when the transmit side elastic store is disabled. Synchronous with TSYSCLK when the transmit side elastic store is enabled. Useful for blocking clocks to a serial UART or LAPD controller in applications where not all T1 channels are used such as Fractional T1, 384 Kbps service, 768 Kbps or ISDN–PRI . Also useful for locating individual channels in drop–and–insert applications, for external per–channel loopback, and for per–channel conditioning. See Section 16 for details. *This signal is not bonded out in the DS21FF42/DS21FT42.*

Signal Name: **TSYSCLK**
Signal Description: **Transmit System Clock**
Signal Type: **Input**
1.544 MHz or 2.048 MHz clock. Only used when the transmit side elastic store function is enabled. Should be tied low in applications that do not use the transmit side elastic store. Can be burst at rates up to 8.192 MHz. *This pin is tied to the RSYSCLK signal in the DS21FF42/DS21FT42.*

Signal Name: **TLCLK**
Signal Description: **Transmit Link Clock**
Signal Type: **Output**
4 kHz or 2 kHz (ZBTSI) demand clock for the TLINK input. See Section 19 for details. *This signal is not bonded out in the DS21FF42/DS21FT42.*

Signal Name: **TLINK**
Signal Description: **Transmit Link Data**
Signal Type: **Input**
If enabled via TCR1.2, this pin will be sampled on the falling edge of TCLK for data insertion into either the FDL stream (ESF) or the Fs–bit position (D4) or the Z–bit position (ZBTSI). See Section 19 for details. *This signal is not bonded out in the DS21FF42/DS21FT42.*

Signal Name: **TSYNC**
Signal Description: **Transmit Sync**
Signal Type: **Input /Output**
A pulse at this pin will establish either frame or multiframe boundaries for the transmit side. Via TCR2.2, the DS21Q42 can be programmed to output either a frame or multiframe pulse at this pin. If this pin is set to output pulses at frame boundaries, it can also be set via TCR2.4 to output double–wide pulses at signaling frames. See Section 24 for details.

Signal Name: **TSSYNC**
Signal Description: **Transmit System Sync**
Signal Type: **Input**
Only used when the transmit side elastic store is enabled. A pulse at this pin will establish either frame or multiframe boundaries for the transmit side. Should be tied low in applications that do not use the transmit side elastic store.

Signal Name: **TSIG**
Signal Description: **Transmit Signaling Input**
Signal Type: **Input**
When enabled, this input will sample signaling bits for insertion into outgoing PCM T1 data stream. Sampled on the falling edge of TCLK when the transmit side elastic store is disabled. Sampled on the falling edge of TSYSCLK when the transmit side elastic store is enabled. This function is available when FMS = 0. *FMS is tied to ground for the DS21FF42/DS21FT42.*

Signal Name: **TPOS**
Signal Description: **Transmit Positive Data Output**
Signal Type: **Output**
Updated on the rising edge of TCLK with the bipolar data out of the transmit side formatter. Can be programmed to source NRZ data via the Output Data Format (CCR1.6) control bit.

Signal Name: **TNEG**
Signal Description: **Transmit Negative Data Output**
Signal Type: **Output**
Updated on the rising edge of TCLK with the bipolar data out of the transmit side formatter.

RECEIVE SIDE PINS

Signal Name: **RLINK**
Signal Description: **Receive Link Data**
Signal Type: **Output**
Updated with either FDL data (ESF) or Fs bits (D4) or Z bits (ZBTSI) one RCLK before the start of a frame. See Section 24 for details. *This signal is not bonded out in the DS21FF42/DS21FT42.*

Signal Name: **RLCLK**
Signal Description: **Receive Link Clock**
Signal Type: **Output**
A 4 kHz or 2 kHz (ZBTSI) clock for the RLINK output. This signal is not bonded out in the DS21FF42/DS21FT42.

Signal Name: **RCHCLK**
Signal Description: **Receive Channel Clock**
Signal Type: **Output**
A 192 kHz clock which pulses high during the LSB of each channel. Synchronous with RCLK when the receive side elastic store is disabled. Synchronous with RSYSCLK when the receive side elastic store is enabled. Useful for parallel to serial conversion of channel data. This function is available when FMS = 1 (DS21Q41 emulation). *This signal is not bonded out in the DS21FF42/DS21FT42.*

Signal Name: **RCHBLK**
Signal Description: **Receive Channel Block**
Signal Type: **Output**
A user programmable output that can be forced high or low during any of the 24 T1 channels. Synchronous with RCLK when the receive side elastic store is disabled. Synchronous with RSYSCLK when the receive side elastic store is enabled. Useful for blocking clocks to a serial UART or LAPD controller in applications where not all T1 channels are used such as Fractional T1, 384K bps service, 768K bps, or ISDN–PRI. Also useful for locating individual channels in drop–and–insert applications, for external per–channel loopback, and for per–channel conditioning. See Section 16 for details.

Signal Name: **RSER**
Signal Description: **Receive Serial Data**
Signal Type: **Output**
Received NRZ serial data. Updated on rising edges of RCLK when the receive side elastic store is disabled. Updated on the rising edges of RSYSCLK when the receive side elastic store is enabled.

Signal Name: **RSYNC**
Signal Description: **Receive Sync**
Signal Type: **Input /Output**
An extracted pulse, one RCLK wide, is output at this pin which identifies either frame (RCR2.4 = 0) or multiframe (RCR2.4 = 1) boundaries. If set to output frame boundaries then via RCR2.5, RSYNC can also be set to output double–wide pulses on signaling frames. If the receive side elastic store is enabled via CCR1.2, then this pin can be enabled to be an input via RCR2.3 at which a frame or multiframe boundary pulse is applied. See Section 24 for details.

Signal Name: **RFSYNC**
Signal Description: **Receive Frame Sync**
Signal Type: **Output**
An extracted 8 kHz pulse, one RCLK wide, is output at this pin which identifies frame boundaries. *This signal is not bonded out in the DS21FF42/DS21FT42.*

Signal Name: **RMSYNC**
Signal Description: **Receive Multiframe Sync**
Signal Type: **Output**
An extracted pulse, one RSYSCLK wide, is output at this pin which identifies multiframe boundaries. If the receive side elastic store is disabled, then this output will output multiframe boundaries associated with RCLK. This function is available when FMS = 1 (DS21Q41 emulation). *This signal is not bonded out in the DS21FF42/DS21FT42.*

Signal Name: **RSYSCLK**
Signal Description: **Receive System Clock**
Signal Type: **Input**
1.544 MHz or 2.048 MHz clock. Only used when the elastic store function is enabled. Should be tied low in applications that do not use the elastic store. Can be burst at rates up to 8.192 MHz. *This pin is tied to the TSYSCLK signal in the DS21FF42/DS21FT42.*

Signal Name: **RSIG**
Signal Description: **Receive Signaling Output**
Signal Type: **Output**
Outputs signaling bits in a PCM format. Updated on rising edges of RCLK when the receive side elastic store is disabled. Updated on the rising edges of RSYSCLK when the receive side elastic store is enabled. This function is available when FMS = 0. *FMS is tied to ground for the DS21FF42/DS21FT42.*

Signal Name: **RLOS/LOTC**
Signal Description: **Receive Loss of Sync / Loss of Transmit Clock**
Signal Type: **Output**
A dual function output that is controlled by the CCR3.5 control bit. This pin can be programmed to either toggle high when the synchronizer is searching for the frame and multiframe or to toggle high if the TCLK pin has not been toggled for 5 usec. This function is available when FMS = 1 (DS21Q41 emulation). *This signal is not bonded out in the DS21FF42/DS21FT42.*

Signal Name: **CLKSI**
Signal Description: **8 MHz Clock Reference**
Signal Type: **Input**
A 1.544 MHz reference clock used in the generation of 8MCLK. This function is available when FMS = 0. *FMS is tied to ground for the DS21FF42/DS21FT42.*

Signal Name: **8MCLK**
Signal Description: **8 MHz Clock**
Signal Type: **Output**
A 8.192 MHz output clock that is referenced to the clock that is input at the CLKSI pin. This function is available when FMS = 0. *FMS is tied to ground for the DS21FF42/DS21FT42.*

Signal Name: **RPOS**
Signal Description: **Receive Positive Data Input**
Signal Type: **Input**
Sampled on the falling edge of RCLK for data to be clocked through the receive side framer. RPOS and RNEG can be tied together for an NRZ interface. Connecting RPOS to RNEG disables the bipolar violation monitoring circuitry.

Signal Name: **RNEG**
Signal Description: **Receive Negative Data Input**
Signal Type: **Input**
Sampled on the falling edge of RCLK for data to be clocked through the receive side framer. RPOS and RNEG can be tied together for an NRZ interface. Connecting RPOS to RNEG disables the bipolar violation monitoring circuitry.

Signal Name: **RCLK**
Signal Description: **Receive Clock Input**
Signal Type: **Input**
Clock used to clock data through the receive side framer.

PARALLEL CONTROL PORT PINS

Signal Name: **INT***
Signal Description: **Interrupt**
Signal Type: **Output**
Flags host controller during conditions and change of conditions defined in the Status Registers 1 and 2 and the HDLC Status Register. Active low, open drain output.

Signal Name: **FMS**
Signal Description: **Framer Mode Select**
Signal Type: **Input**
Set low to select DS21Q42 feature set. Set high to select DS21Q41 emulation. *FMS is tied to ground for the DS21FF42/DS21FT42.*

Signal Name: **MUX**
Signal Description: **Bus Operation**
Signal Type: **Input**
Set low to select non–multiplexed bus operation. Set high to select multiplexed bus operation.

Signal Name: **D0 to D7/ AD0 to AD7**
Signal Description: **Data Bus or Address/Data Bus**
Signal Type: **Input /Output**
In non–multiplexed bus operation (MUX = 0), serves as the data bus. In multiplexed bus operation (MUX = 1), serves as a 8–bit multiplexed address / data bus.

Signal Name: **A0 to A5, A7**
Signal Description: **Address Bus**
Signal Type: **Input**
In non–multiplexed bus operation (MUX = 0), serves as the address bus. In multiplexed bus operation (MUX = 1), these pins are not used and should be tied low.

Signal Name: **ALE(AS)/A6**
Signal Description: **A6 or Address Latch Enable (Address Strobe)**
Signal Type: **Input**
In non–multiplexed bus operation (MUX = 0), serves as address Bit 6. In multiplexed bus operation (MUX = 1), serves to demultiplex the bus on a positive–going edge.

Signal Name: **BTS**
Signal Description: **Bus Type Select**
Signal Type: **Input**
Strap high to select Motorola bus timing; strap low to select Intel bus timing. This pin controls the function of the RD*(DS*), ALE(AS), and WR*(R/W*) pins. If BTS = 1, then these pins assume the function listed in parenthesis ().

Signal Name: **RD*(DS*)**
Signal Description: **Read Input (Data Strobe)**
Signal Type: **Input**
RD* and DS* are active low signals. Note: DS is active high when MUX=1. Refer to bus timing diagrams in section 25.

Signal Name: **FS0 AND FS1**
Signal Description: **Framer Selects**
Signal Type: **Input**
Selects which of the four framers to be accessed.

Signal Name: **CS***
Signal Description: **Chip Select**
Signal Type: **Input**
Must be low to read or write to the device. CS* is an active low signal.

Signal Name: **WR*(R/W*)**
Signal Description: **Write Input(Read/Write)**
Signal Type: **Input**
WR* is an active low signal.

TEST ACCESS PORT PINS

Signal Name: **TEST**
Signal Description: **3–State Control**
Signal Type: **Input**
Set high to 3–state all output and I/O pins (including the parallel control port) when FMS = 1 or when FMS = 0 and JTRST* is tied low. Set low for normal operation. Ignored when FMS = 0 and JTRST* = 1. Useful in board level testing. *FMS is tied to ground for the DS21FF42/DS21FT42.*

Signal Name: **JTRST***
Signal Description: **IEEE 1149.1 Test Reset**
Signal Type: **Input**
This signal is used to asynchronously reset the test access port controller. At power up, JTRST* must be set low and then high. This action will set the device into the DEVICE ID mode allowing normal device operation. If boundary scan is not used and FMS = 0, this pin should be held low. This function is available when FMS = 0. When FMS=1, this pin is held LOW internally. This pin is pulled up internally by a 10K ohm resistor. *FMS is tied to ground for the DS21FF42/DS21FT42.*

Signal Name: **JTMS**
Signal Description: **IEEE 1149.1 Test Mode Select**
Signal Type: **Input**
This pin is sampled on the rising edge of JTCLK and is used to place the test port into the various defined IEEE 1149.1 states. This pin is pulled up internally by a 10K ohm resistor. If not used, this pin should be left unconnected. This function is available when FMS = 0. *FMS is tied to ground for the DS21FF42/DS21FT42.*

Signal Name: **JTCLK**
Signal Description: **IEEE 1149.1 Test Clock Signal**
Signal Type: **Input**
This signal is used to shift data into JTDI pin on the rising edge and out of JTDO pin on the falling edge. If not used, this pin should be connected to VSS. This function is available when FMS = 0. *FMS is tied to ground for the DS21FF42/DS21FT42.*

Signal Name: **JTDI**
Signal Description: **IEEE 1149.1 Test Data Input**
Signal Type: **Input**
Test instructions and data are clocked into this pin on the rising edge of JTCLK. This pin is pulled up internally by a 10K ohm resistor. If not used, this pin should be left unconnected. This function is available when FMS = 0. *FMS is tied to ground for the DS21FF42/DS21FT42.*

Signal Name: **JTDO**
Signal Description: **IEEE 1149.1 Test Data Output**
Signal Type: **Output**
Test instructions and data are clocked out of this pin on the falling edge of JTCLK. If not used, this pin should be left unconnected. This function is available when FMS = 0. *FMS is tied to ground for the DS21FF42/DS21FT42.*

SUPPLY PINS

Signal Name: VDD
Signal Description: **Positive Supply**
Signal Type: **Supply**
2.97 to 3.63 volts.